

1-Bit Full Adder Cell Implemented Using Nanostructures Field-Effect Transistors (nano-FETs)

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ABSTRACT

This paper aims at designing a 1-bit full adder circuits using high-mobility nanostructures n-channel spatial wave-function switching (SWS) FETs which provide a significant reduction of cell area (52% smaller in size) and power dissipation. Unlike conventional FETs, SWS-FETs are comprised of two or more vertically stacked coupled quantum dot or quantum well channels, and the spatial location of carriers within these channels is used to encode the logic states (00), (01), (10) and (11). The device is models based on integration of the Berkeley Short-channel IGFET Model (BSIM4.6) and the Analog Behavioral Model (ABM), the model are used to design and develop SWS-FET logic gates (NOT, NAND, NOR and XOR) using 20 nm FETs model. The SWS-FET gates are adjusted for a 1 bit fulladder circuits. The one-bit full addercan be implemented with two XOR and three NANDcomplementary metal-oxide-semiconductor (CMOS) logic gates, the proposed SWS 1-bit full adder circuitis successfully designed and simulatedwith less number of transistors (61% less than CMOS1-bit full adder circuit counterpart).In addition, simulation of the proposed SWS1-bit full adder is presented including the operation speed (delay). The accuracy of the circuit is verified in Cadence OrCAD simulator.

Keywords

SWS-FETS; FULL ADDER MULTI-CHANNEL FETS; VLSI.

INTRODUCTION

The semiconductor industry follows Moore's Law, which predicts the size of Metal-Oxide-Semiconductor (MOS) devices to shrink by 50% every 18-24 months [1, 2]. When the devices sizes have started to approach sub-20 nm regime, several issues have begun to make further miniaturization difficult [3]. The MOS scaling will be not satisfying the requirements of the full adder circuit which is one of the major components in a VLSI. In order to reduce the transistors count of and increase the performance of VLSI circuits, the nanostructures n-FETs to be introduced to implement the full adder circuit.

One of the nanostructures n-FETs device is quantum well channels spatial wave-function switched field effect transistor (SWS-FET) as shown in Fig. 1, the SWS-FET device consists of multiple Quantum Well/Dot channels that allow the electron wave-function s switching from one channel to the other as a function of gate voltage. The spatial location of carriers in multiple channels is used to enable the switch between the channels and encode the logic states (00), (01), (10) and (11) [1]. Since each channel is connected to different sources and drains, the current in a SWS-FET is routed between multiple channel drains according to the voltage on a single gate transistor. SWS-FETs can be fabricated in same way as CMOS-FETs with few modifications in process, the fabrication process of SWS-FET is explained in detail by Jain et al. [4].

Fig. 1 shows Structures of n- and p- SWS-FET with two Si Quantum Well (2-QW) channel, the device has upper Si well (W1) and lower Si well (W2) sandwiched between SiGe barriers. Fig. 2 presents quantum simulations showing the transfer of electron Wave-function from the lower well (W2) to the upper well (W1) as the gate voltage is changed from 0.4V to 1.2V for then-SWS-FET device. While, Fig. 3 shows transfer of holes in a similar manner for the gate voltage changed -0.2V to -0.8V for the p-SWS-FET device. Fig. 4 shows the fabricated SiO_x-cladded Si quantum dot n-SWS-FET structure [5]. This device has four QD layers with

single source and two drains (D1 and D2). However, Fig.5 presents the drain-to- source characteristics (I_{DS} vs V_{DS}) for gate voltage in the range of 1.8-2.0V [5].

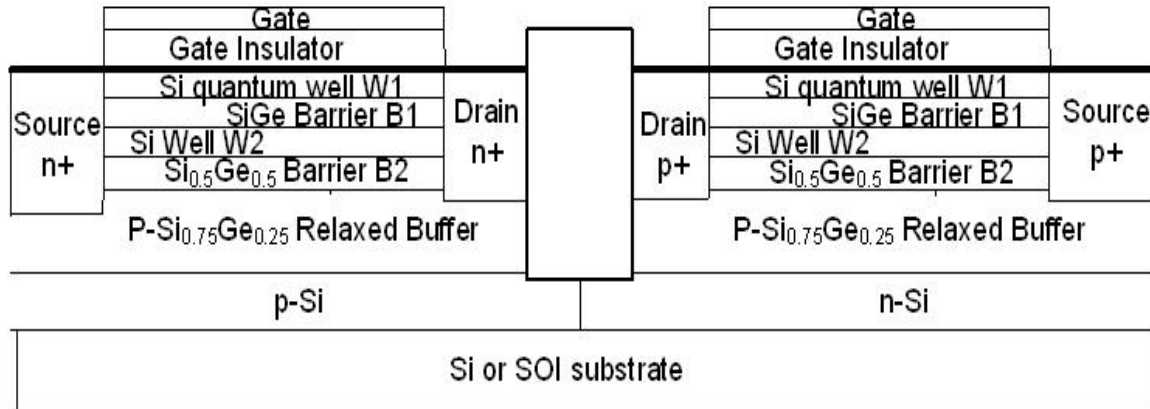


Fig 1: Two QW n-SWS-FET (left) and p-SWS-FET (right).

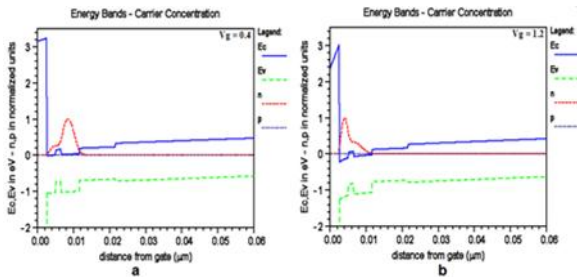


Fig 2: Electron Wave-function at $V_G=0.4V$ (a) & $1.2V$ (b).

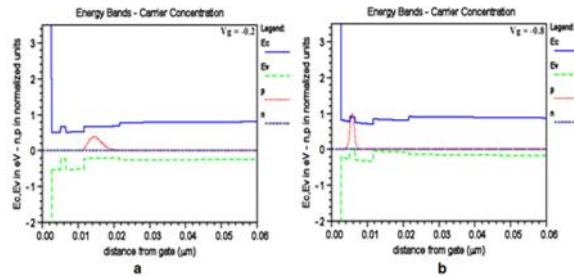


Fig 3: Hole Wave-function at $V_G=-0.2V$ (a) & $-0.8V$ (b).

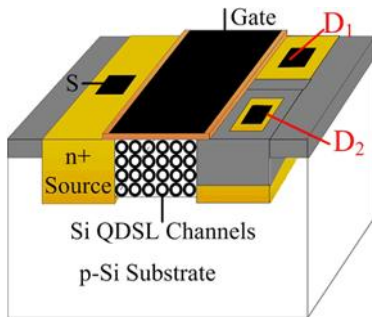


Fig 4: The fabricated two QD n-SWS-FET.

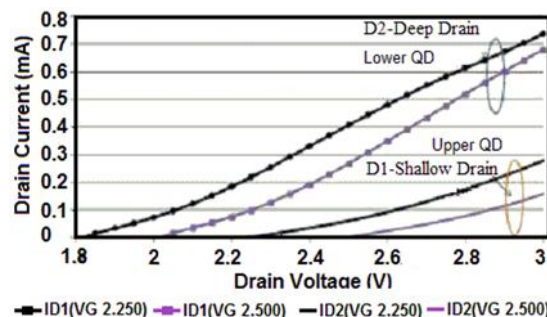


Fig 5: The Experimental I_{DS} - V_{DS} Four QD n-SWS-FET.

In terms of circuits design, the device provides opportunity to process 2-bits simultaneously. We have reported circuits of logic gates, analog to digital convertor (ADC), D-latches and static random access memory (SRAM) cells using SWS-FETs with an area saving as shown in Table 1 [6, 7, 8]. In these circuits, the SWS-FETs have utilized multiple source/drain configurations of n-channel SWS-FETs.

Table 1. The number of transistors between CMOS and SWSFET technology

Circuit	Reeducation %	CMOS			SWS-FET		
		n-type	p-type	Total	n-type	p-type	Total
3-bit ADC	1-32/74=56%	37	37	74	30	2	32
D-latches	1-12/16=25%	8	8	16	12	0	12
1-bit SRAM (6T)	1-2/6=66.7%	3	3	6	2	0	2

SWSFET CIRCUIT MODEL

The two QW-SWS-FET has more number of states in its transfer characteristic based on the switching of charge carriers from one channel to other channel of the device [6], the follow of current in each channel/well is related to the gate voltage (V_G) and two threshold voltages (V_{TH2} for the lower well W2 and V_{TH1} for the upper well W1). Once $V_G > V_{TH2}$, the electrons appear in W2 and current flows in W2. If V_G is increased more as $> V_{TH1}$, the carrier (or their wave-function) start transferring to W1 and the current flows in both wells. Finally, V_G is further increased ($V_G \gg V_{TH2}$), carrier completely transfer from W2 to W1 and the current flows only in W1.

The self-consistent solution to Poisson and Schrödinger equations give 2D charge density and distribution in two QW[4]. The solution also helps to compute the drains current in each wells I_{DS-W1} and I_{DS-W2} . In a simpler model, I_{DS-W1} and I_{DS-W2} can be expressed by adapting the classical MOS-FET equations. Equations (1) and (2) represent I_{DS-W1} and I_{DS-W2} , respectively. Equation (3) expresses the developed threshold voltage for the lower well (V_{th-W2}) [9].

$$I_{DS-W1} = \frac{W_1}{L} C_{OX} \mu_n \left((V_{GS1} - V_{th1}) V_{DS1} - \frac{V_{DS1}^2}{2} \right) \quad (1)$$

$$I_{DS-W2} = \frac{W_2}{L} C_{OX} \mu_n \left((V_{GS2} - V_{th-W2}) V_{DS2} - \frac{V_{DS2}^2}{2} \right) \quad (2)$$

$$V_{th-W2} = \begin{cases} V_{th2} & V_{GS2} < V_{UL} \\ V_{th2} + \frac{(V_{GS2} - V_{UL})^2}{V_{th1} - V_{UL}} & V_{GS2} \geq V_{UL} \end{cases} \quad (3)$$

Where

- L the channel length of the device.
- W_1, W_2 the width of the upper well and the lower well, respectively.
- C_{OX} the gate capacitance per unit area.
- μ_n the channel mobility.
- V_{GS1}, V_{GS2} the gate to source voltage of the upper well and the lower well, respectively.
- V_{DS1}, V_{DS2} the drain to source voltage of the upper well and the lower well, respectively.
- V_{th1}, V_{th2} the threshold voltage of the upper well and the lower well, respectively.
- V_{UL} the transition voltage
- V_{th-W2} the developed threshold voltage of well 2

A circuit model for a SWS-FET has already been introduced based on the equation above [9]. The circuit model is an integration between the Berkeley Short-channel IGFET Model (BSIM4.6) and the Analog Behavioral Model (ABM). This model is set in hierarchical block and it ready to be used in Cadence-OrCAD CIS. Fig. 6 shows a simulation $I_{DS}-V_{GS}$ characteristic of 2 QW n-SWS-FET with twin-drain and single-source. The twin-drain n-SWS-FET model have 230-parameters obtained using modeled BSIM4.6.0 level 7 Third Generation Model. The major parameters are ($V_{DD}=1V$, $L=20nm$, $W1=40nm$, $W2=100nm$, $V_{TH1}=0.3V$, $5V$, $V_{TH2}=0.2V$, and $V_{UL}=0.2V$). The simulation result show excellent performance on switching and output currents.

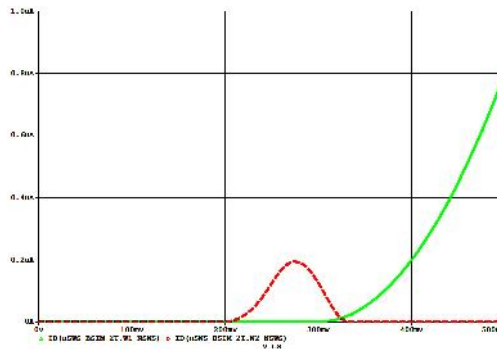


Fig6: The simulation of twin-drain 20nm n-SWS-FET modeled $I_{DS-w2}(-)$ & $I_{DS-w1}()$.

LOGIC GATES CIRCUITS USING N-SWS-FET

The complementary MOS (CMOS) uses PMOS and NMOS transistors to implement any Boolean functions [14]. This section shows the design possibilities of logic gates using only n-SWS-FETs. The truth table for the various logic gates is presented in Table 2. Fig. 7 shows the circuit designs of logic gates (NOT/Inverter, NAND, NOR and XNOR) gates using SWS-FETs, where the circuits of SWS-FET gate are established by Jain et al. [1, 9].

Table 2. The truth table for the implemented logic gates.

A	B	NOT (A) \bar{A}	NAND $\overline{A \cdot B}$	NOR $\overline{A + B}$	XOR $A \oplus B = \bar{A}B + A\bar{B}$	XNOR $A \odot B = \overline{\bar{A} + B}$
0	0	1	1	1	0	1
0	1	1	1	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	0	1
# CMOS transistors		1-PMOS 1-NMOS	2-PMOS 2-NMOS	2-PMOS 2-NMOS	16 (by 4-NAND)	16 (by 4-NOR)
					8 (by Transmission Gate [10,11])	
# n-SWS-FET transistors		2	3	3	4	4

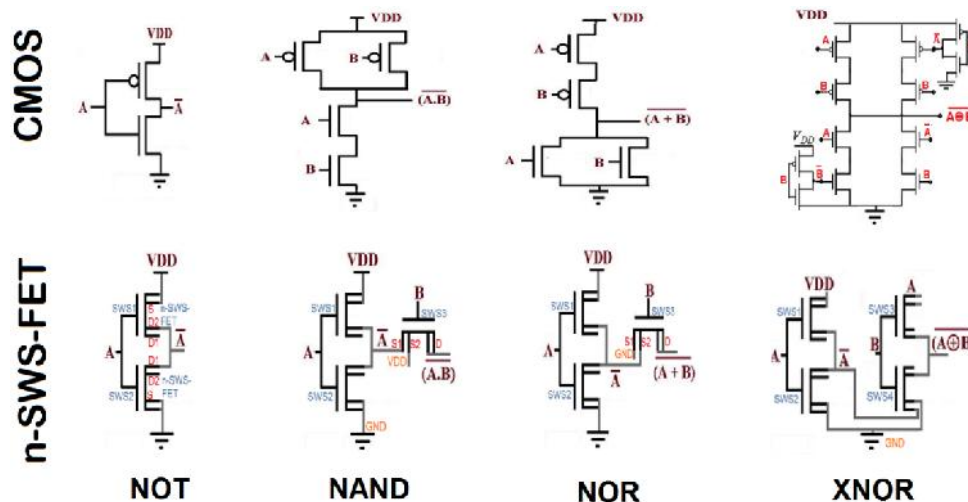


Fig7: The circuits of NOT, NAND and NOR (CMOS and n-SWS-FET)

The accuracy of the CMOS and SWS gates are verified as shown in Fig 8. The outputs of SWS-FET and CMOS are identical and responding in the same time.

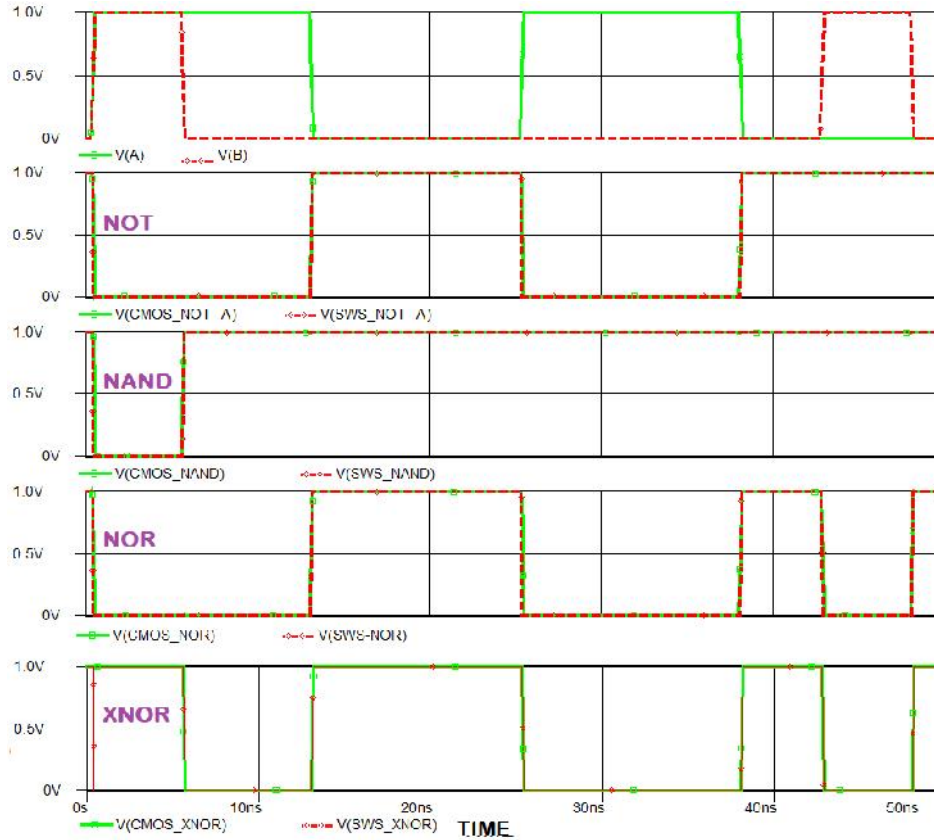


Fig8: The simulation of CMOS and n-SWS logic gates

ONE-BIT FULL ADDER CIRCUITS USING N-SWS-FET

The 1-bit full adder can be performed by 3 NAND and 2 XOR gates as circuit shown in Fig. 9 (a), Table 3 shows Truth Table of the 1-bit full adder [12]. The 1-bit full adder adds three one-bit numbers A, B, and C. where, A and B are the operands and C is a bit carried in from the previous stage. The circuit has a two-bit output carry (C_{out}) and Sum.

The conventional CMOS 1-bit full adder circuit has 44 transistors (12 FETs NANDs and 32 FETs for XORs) as shown in Fig. 9. However, this high number of transistors may result in large power consumption and introduces more delay. If the XOR is designed by using CMOS transmission gate, the number of transistors is reduced to 28 transistors (12 FETs for NANDs + 16 FETs for XORs). Based on pull-up and pull-down CMOS network, the 1-bit full adder can be also done by 28 CMOS transistors as shown in Fig. 9 (b) [13]. Also, many 1-bit full adder circuits are designed with the transistor counts varies from 28 to 6 [13]. In this paper, 17 n-SWS-FETs are used to build the 1-bit full adder circuit (9 SWS-FETs for SWS-NANDs and 8 SWS-FETs for SWS-XORs).

Fig 10 shows the simulation of conventional CMOS 44 transistors (--) and the SWS-FET () 1-bit full adder circuit. The simulations have been done at 20nm channel length transistors, the major simulation parameters are ($V_{DD}=1V$, $L=20nm$, $W1=40nm$, $W2=100nm$, $V_{TH1}=0.3V$, $5V$, $V_{TH2}=0.2V$, and $V_{UL}=0.2V$). The binary inputs are $V(A)$, $V(B)$, and $V(C)$. A sum of the binary input data is denoted by $V(SUM)$ and a carry bit is indicated as $V(Cout)$. In the simulation, the sum is the XOR of the three inputs (A, B, C). The simulation

results show excellent performance for CMOS and SWS-FET and their outputs are typically as of the 1-bit full adder Truth Table.

The simulation analysis is carried out with three inputs (A, B, C) and two outputs (Sum and C_{out}) of full Adder. The simulation waveform of delay is shown in Fig.11 and Table 4, the comparison shows that the SWS-FETs adder circuit has less number of transistors and less delay compare with the conventional CMOS adder circuit. As a result, the SWS-FET 1-bit full adder circuit takes lesser area and consumes lesser power, while maintaining the fast speed of operation.

1-bit full adder circuit

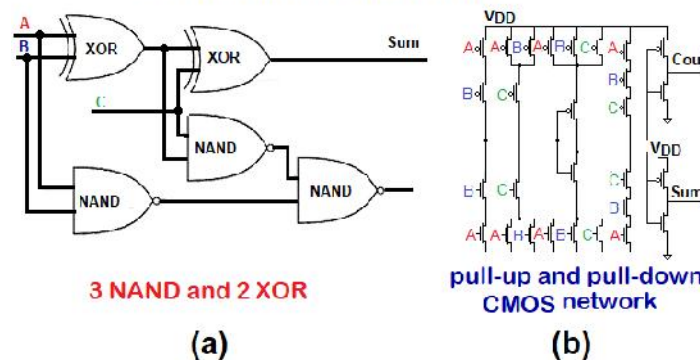


Fig9: The 1-bit full Adder Circuit.

Table 3: Truth Table of 1-bit full adder

A	B	C	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1

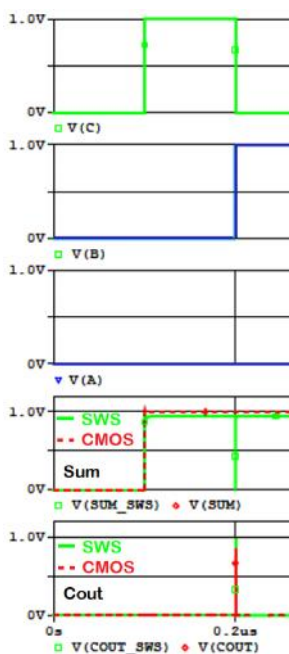


Fig10: The simulation of CMOS & SWS-FET Full Adder.

Table 4: The delay Simulation Result 1-bit full adder circuits

Circuit	# Transistors	Delay Sum	Delay C_{out}
CMOS	44	60picosecond	40picosecond
SWSFET	21	<10picosecond	<10picosecond

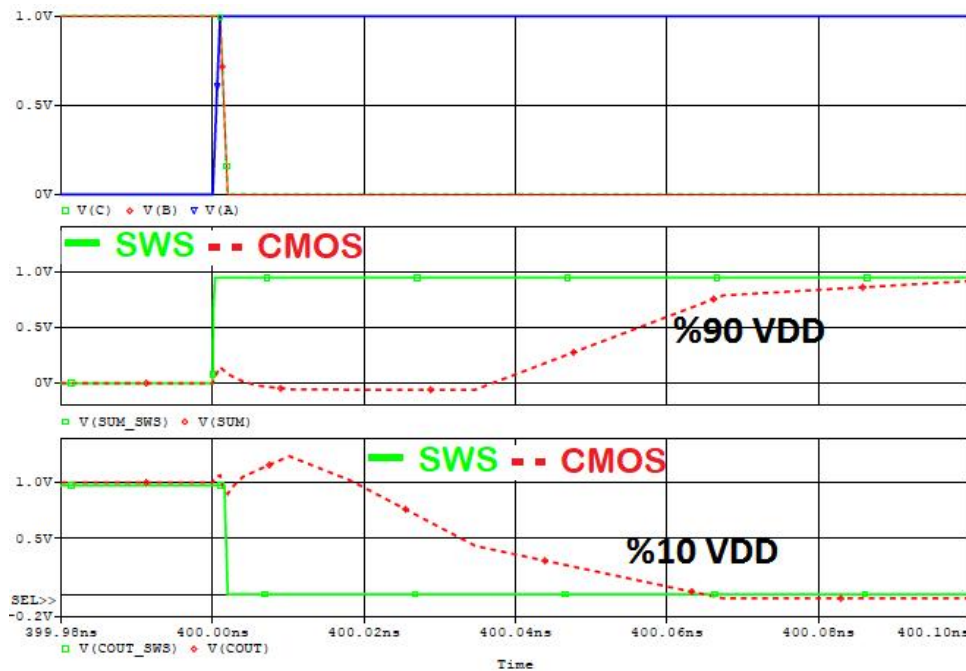


Fig11: The delay simulation of the conventional CMOS & SWS-FET 1-bit Full Adder.

CONCLUSION

This paper presents the modeling of logic circuits based on spatial wave-function-switched field-effect transistors (SWS-FETs). The circuits of SWS-FET logic gates, 1-bit Full Adder circuits are been designed in a Cadence Or CAD using 20nm technology, with a voltage supply of 1V.

In summary, we have successfully demonstrated conventional CMOS and SWS-FET 1-bit full adder circuits. The simulation of the two circuits are presented, the comparison and results are tabulated. The number of the FETs is reduced from 44 in conventional CMOS architecture to 17 using n channel SWS-FETs. This reduces cell area and power dissipation, then the delay is reduced from 60 ps conventional CMOS to <10 ps using SWS-FETs. This is making SWS-FET a promising technology for analog applications.

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