

10 THINGS TO KNOW ABOUT PCIe

eBOOK



PCIe Overview

PCI Express (PCIe) is a high performance, general purpose I/O interconnect used in a wide variety of computing and communications products. There is a high degree of convergence on PCIe as a high speed serial bus standard because of its low level latency and significantly higher bandwidth capabilities. PCIe has become especially popular for NVMe Express SSD applications.

PCIe has both Serial Communications and Storage interfaces unlike SAS and SATA leading to additional industry scalability. It is projected by 2018 PCIe will be the leading SSD interface in Data Communications after overtaking SAS in 2017 and SATA in 2018.

- PCIe is based upon a point-to-point bus topology between a root-complex (system/host) and an end-point (add-in card) that supports full-duplex communications.
- Specifications are developed and maintained by the PCI-SIG, a consortium of >900 companies.
- The PCIe physical layer consists of:
 - Differential low-voltage 100 MHz Refclk
 - Scalable lane widths: x1, x2, x4, x8, x12, x16, x32
 - Scalable speeds: 2.5GT/s (Gen1), 5GT/s (Gen2), 8GT/s (Gen3), and 16GT/s (Gen4)
 - Uses different connectors for compliance level testing, e.g., CEM, U.2 (SFF-8639), M.2 or soldered directly to PCB

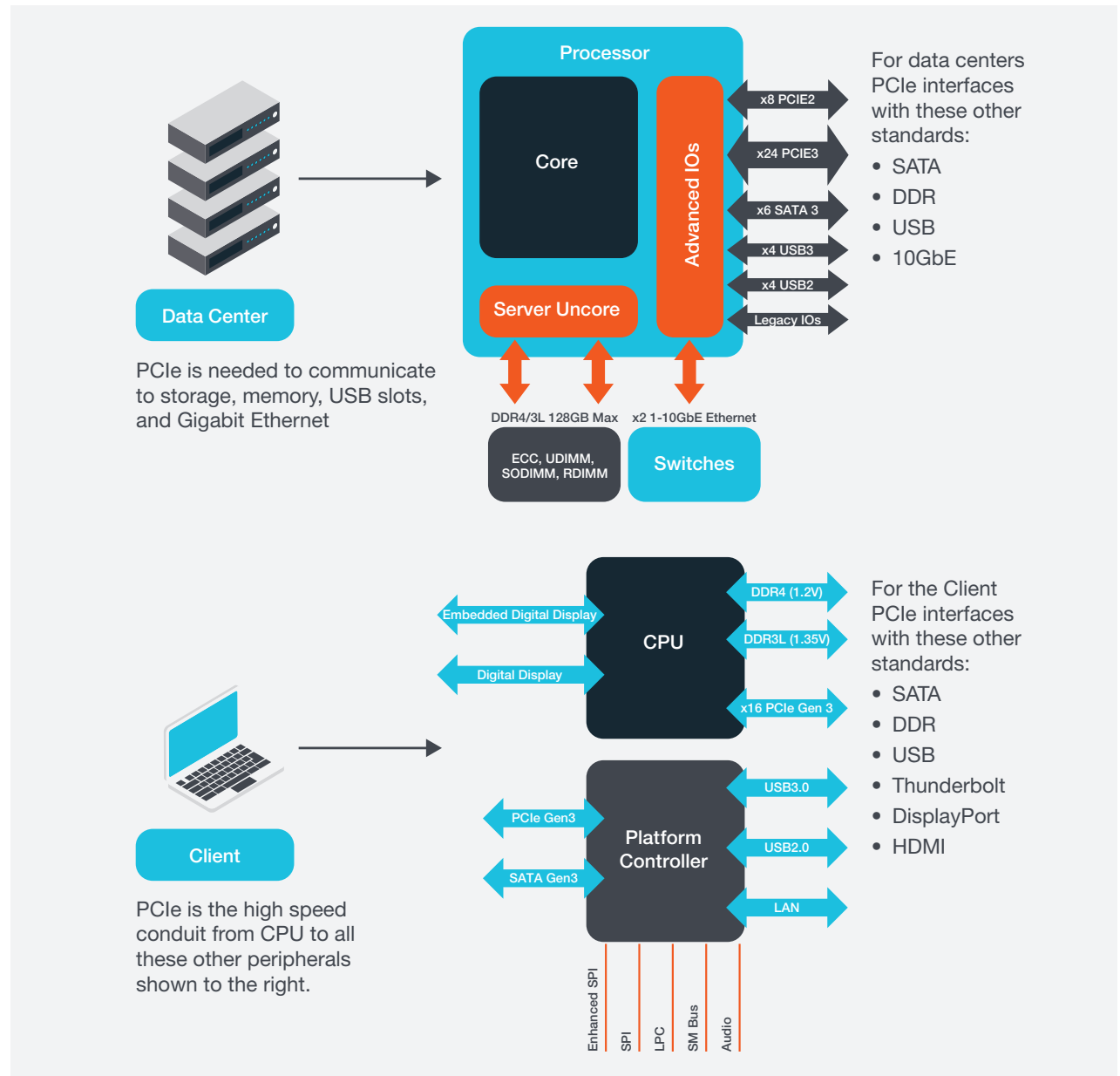
CONTENT

01. PCI Express—Where is it Used?	4
02. PCIe Gen4 Update	5
03. PCIe RefClk Architectures	6
04. PCI Express Form Factors	7
05. Compliance Presets	8
06. Basics of Transmitter (Tx) Testing.....	9
07. Base Spec Transmitter (Tx) Testing	10
08. CEM & U.2 Spec Transmitter (Tx) Testing	11
09. Basics of Receiver (Rx) Testing	12
10. Key Considerations in Setting up PCIe Test and Debug.....	13

01. PCI Express— Where is it Used?

PCIe is emerging as the primary, high-performance storage and serial bus for data center and client side applications. PCIe enables data communication among peripherals.

Both Data Center and Client Applications have a core processor which provides the raw processing power for the architecture on the host system. Both applications also must interface with a variety of endpoint peripheral devices such as SATA drives, USB devices and others. Between the root-complex host and the end-point devices there are usually numerous lanes of long, lossy channels and connectors that impose noise, crosstalk, timing irregularities, and other impairments. Therefore it is imperative that PCIe devices on both the Client and Data Center side is able to reliably demonstrate PCI specified compliance, compensate for impairments, and interoperate with other PCIe devices.



02. PCIe Gen4 Update

What You Need to Know

With the need for increased data and bandwidth throughput, PCIe data rates must increase to keep up with the demand. Therefore, one of the biggest changes in Gen4 is that the data rate has increased by 2x from 8GT/s for Gen3 to 16GT/s for Gen4.

Outlined here are the key enhancements the new Gen4 standard brings to the marketplace.

Key Enhancements with PCIe 4.0

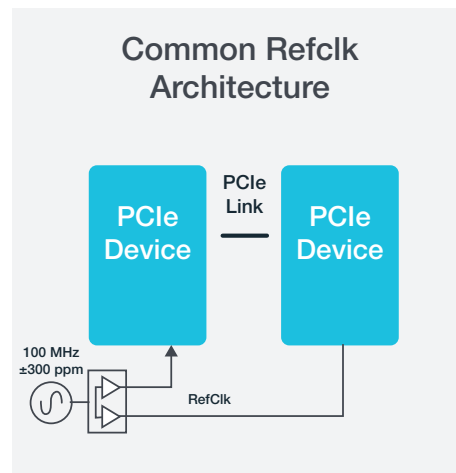
- 16 GT/s, using scrambling, same as 8 GT/s, no encoding change from Gen3 (128b/130b)
- Reduction in RJ (random jitter) from 3 ps (PCIe3) to ~1 ps (PCIe4) for stressed Rx eye parameters
- Gen4 connector backwards-compatible with Gen1/2/3
- Behavioral Rx EQ data rate dependent
- Limited channel: requires use of repeater (both redriver & retimer) for longer channels and/or 2nd connector
- Test channel is around 12" long and has a total of -28 dB loss
- When testing for both Gen3 and Gen4 on the same device the number of individual presets to be tested will double to a total of 22. Gen3 has 11 presets (P0 to P10) and Gen4 has 11 presets (P0 to P10).
- New SRIS independent RefClk modes
 - SRNS – Separate RefClk Independent with No SSC Architecture
 - SRIS – Separate RefClk Independent with SSC Architecture
- New Rx Lane Margining feature measures Eye Height (EH)/Eye Width (EW) margin at the end of the channel
- The minimum eye height for Gen4 has been reduced to 15mVpp
- Rev 0.9 Base spec draft expected to be finalized in Q2 2017
- Gen4 CEM spec released rev 0.5, draft 0.7 in process as of Q2 2017

03. PCIe Refclk Architectures

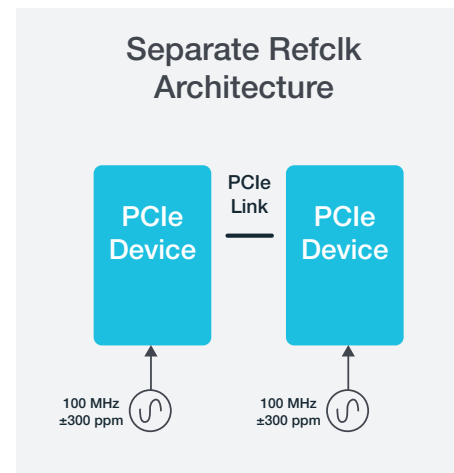
To facilitate reliable data transmission for both transmitting and receiving devices, PCI-SIG has very stringent specification requirements for the reference clock. The standard specifies the use of a 100 MHz clock (Refclk) with greater than ± 300 ppm frequency stability at both the transmitting and receiving devices and supports for three distinct clocking architectures to enable synchronous coordination of both root complex and end point silicon.

Traditionally PCIe has used a common clock architecture. This allows for both the root complex and silicon to run off the same clock configuration rather than running at different intervals which is more challenging to test. Common Clock is a more precise architecture but is less flexible to integrate into a system. With the adoption of the Gen4 standard, it's likely that systems will increasingly use the the separate/independent clock architecture.

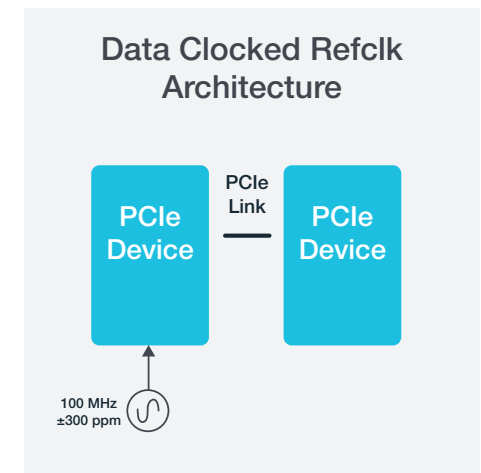
Frequency stability is imperative with support for three distinct clocking architectures.



Common – Most popular, supports SSC (Spread Spectrum Clocking); same clock must be connected to all devices while maintaining skew ≤ 12 ns between devices



Separate/Independent – Primarily used for cabled applications; ref clock between transmitting and receiving devices and allows for increased scalability and interoperability with SATA and SAS devices

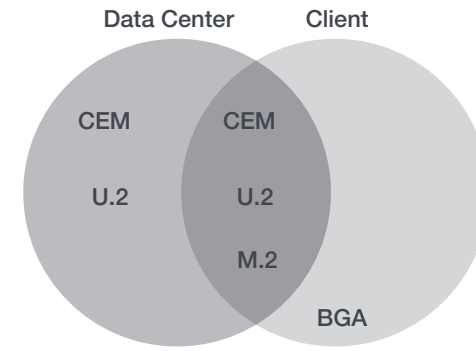


Data Clocked – Simplest to implement, is not commonly implemented in PCIe architectures

“Selecting the Optimum PCI Express Clock Source”, Figure 3 page 3, Silicon Laboratories, Inc.

04. PCI Express Form Factors

PCI-SIG defines specific mechanical form factors and associated test fixtures that all devices must comply with for PCIe testing. All the current form factors are shown below along with typical applications.



PCI Express Form Factors		
CEM Add-In-Card (AIC)		CEM Add-In-Card is the most commonly used form factor. An example of this is the SSD device pictured.
U.2 (SFF-8639)	 <p style="text-align: center;">U.2-to-CEM Adapter</p>	<p>U.2 is a newer and smaller form factor which is currently in FYI testing, as of April 2017, at compliance workshops using U.2 fixtures.</p> <p>Also, U.2 devices can be officially added to the PCI-SIG Integrator's List if they are tested as if they were CEM devices using the adapter fixtures shown.</p>
M.2	 <p style="text-align: center;">M.2-to-CEM Adapter</p>	<p>M.2 form factor is coming and is even smaller than U.2, but as of April 2017 has not yet begun FYI compliance testing.</p> <p>Also, M.2 devices can be officially added to the PCI-SIG Integrator's List if they are tested as if they were CEM devices using the adapter fixtures shown.</p>
BGA (Embedded)		BGA or Embedded SOC devices are not currently supported by compliance testing but can be validated by using high-speed probing or custom fixturing.

Fixtures and adapters are available through PCI-SIG - pcisig.com

05. Compliance Presets

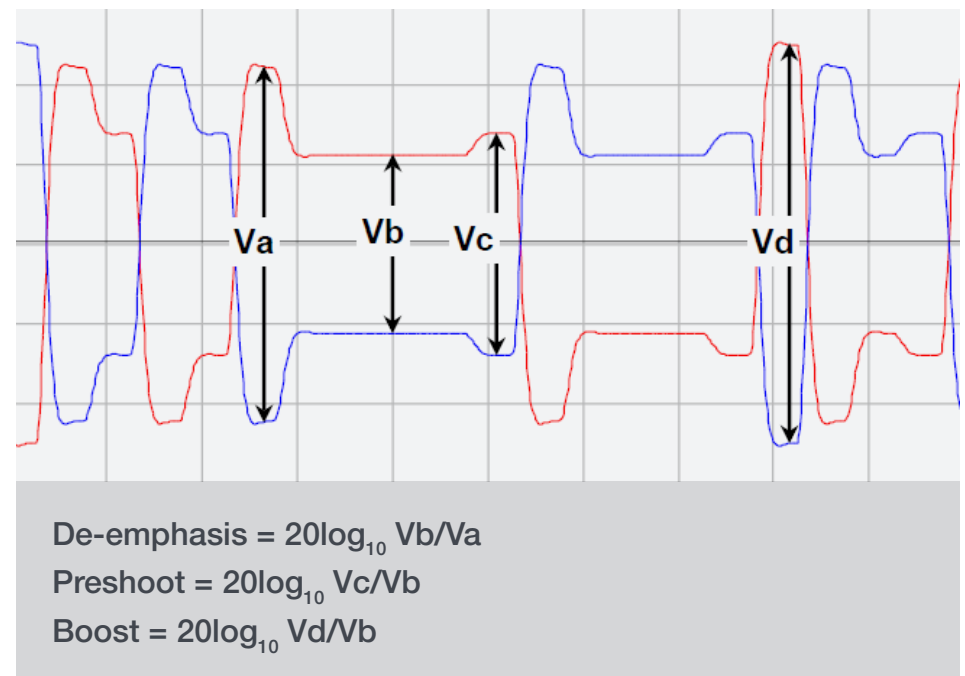
Every device PCI-SIG certifies is required to go through compliance testing for interoperability based on a list of preset or transmitter equalization settings, ranging from a low data rate of 2.5 gigabits per second (Gb/s) up to a new high data rate of 16 Gb/s. These presets are used to equalize channel loss and optimize signal integrity on the link. Each of these presets is a specific combination of preshoot and de-emphasis applied by the host system to the endpoint. The table below details the 11 presets for Gen3 and Gen4. All preset values must be supported by the DUT.

In order to decrease test time and increase the speed of automation, it's recommended to use a 100MHz clock burst as an input to the compliance test fixture to quickly toggle through these presets. If you can automate preset testing using 100MHz pulse toggling, you can save valuable test time by automatically acquiring and analyzing metrics such as jitter, voltage, and timing.

The present values below are applicable to both transmitter and receiver testing.

Preset #	Preshoot (dB)	De-emphasis (dB)
P4	0	0
P1	0	-3.5 ± 1 dB
P0	0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0
P6	2.5 ± 1 dB	0
P3	0	-2.5 ± 1 dB
P2	0	-4.4 ± 1.5 dB
P10	0	Variable ¹

1. P10 levels are not fixed; its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used to test the boost level of the Tx during full swing.

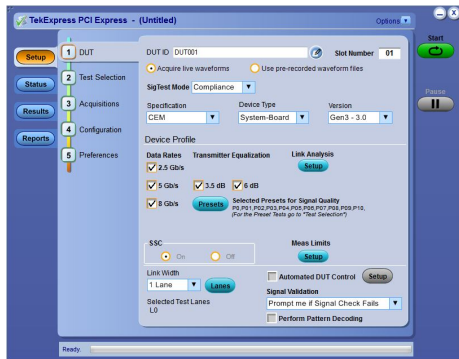


06. Basics of Transmitter (Tx) Testing

Outlined below are the steps for automated compliance testing of a PCIe transmitter. Automated software is vital because it allows for automatic toggling through preset test modes using the 100 MHz ref clock and decreases test time by more than 2x over having to manually push buttons for toggling.

Many early implementors for PCI-SIG testing are electing to use tools like Tektronix's DPOJET and SDLA software to complete early Gen4 characterization and debug.

Setup



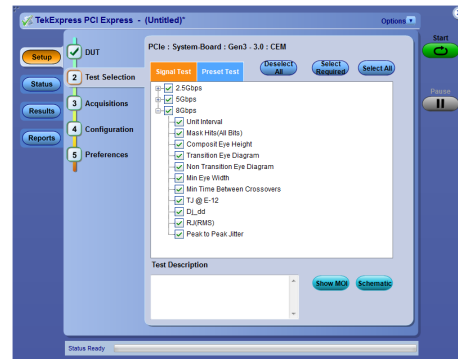
Run Analysis on Live or Pre-Recorded Data

Type of Test/Device Selection

Test Selection

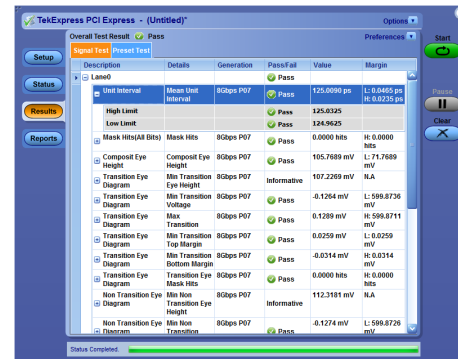
Automate DUT Control

Test



Run Test Selection

Report



Generate Standards Compliant Pass/Fail Reports



Tektronix's complete, automated test and debug solution for transmitter testing using the DPO70000SX Series High Performance Oscilloscopes and the AFG3252. Tek solutions, in addition to Gen3 and Gen4 solutions, are backwards compatible for Gen1 and Gen2 as well.

07. Base Spec Transmitter (Tx) Testing

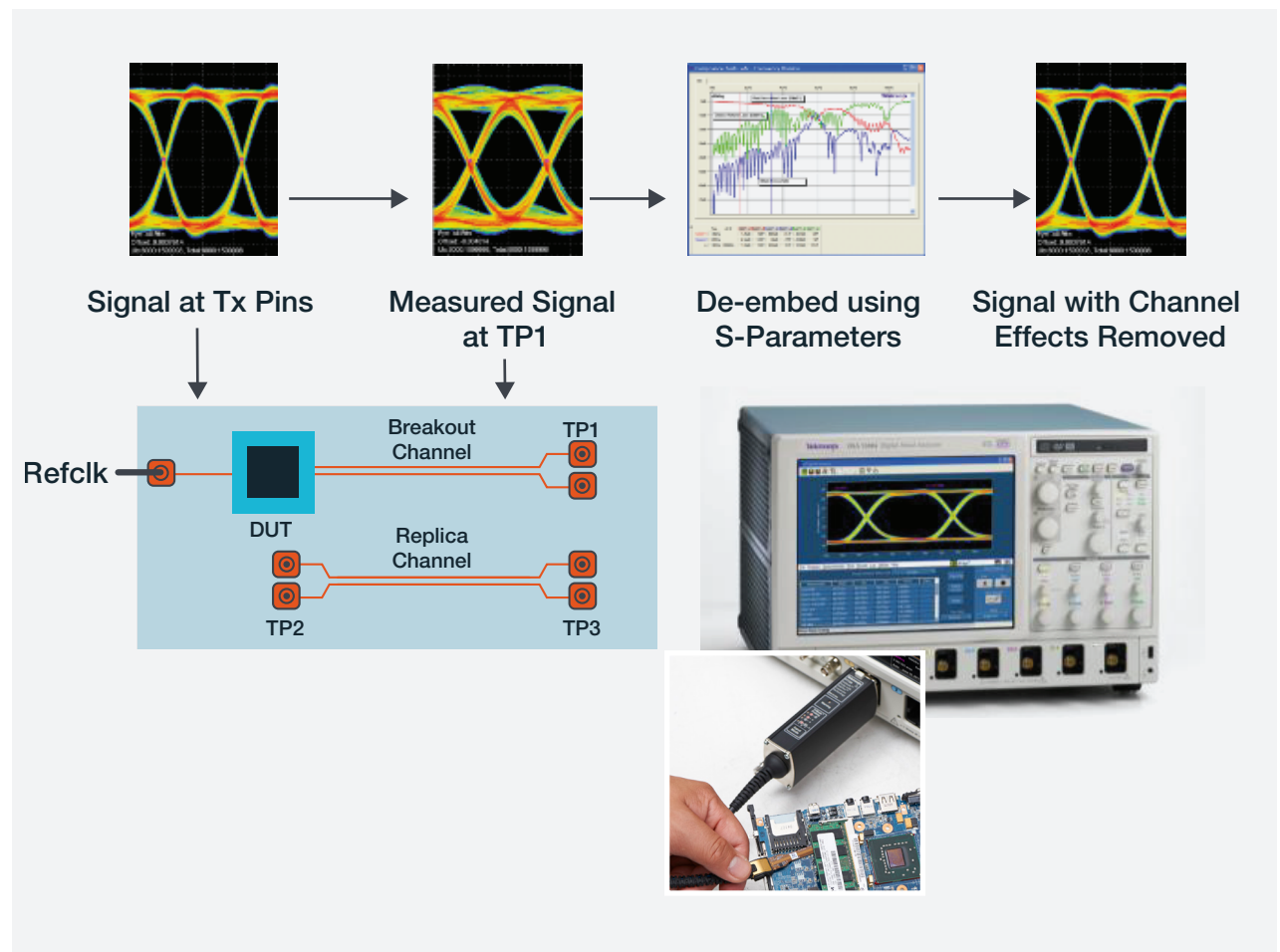
In Base transmitter testing of silicon devices, measurements are specified directly at the pins of the transmitter. Since direct access to the pins is sometimes impossible, measurements should be taken as close as possible to this reference point.

There are several ways to do this at the Silicon Level:

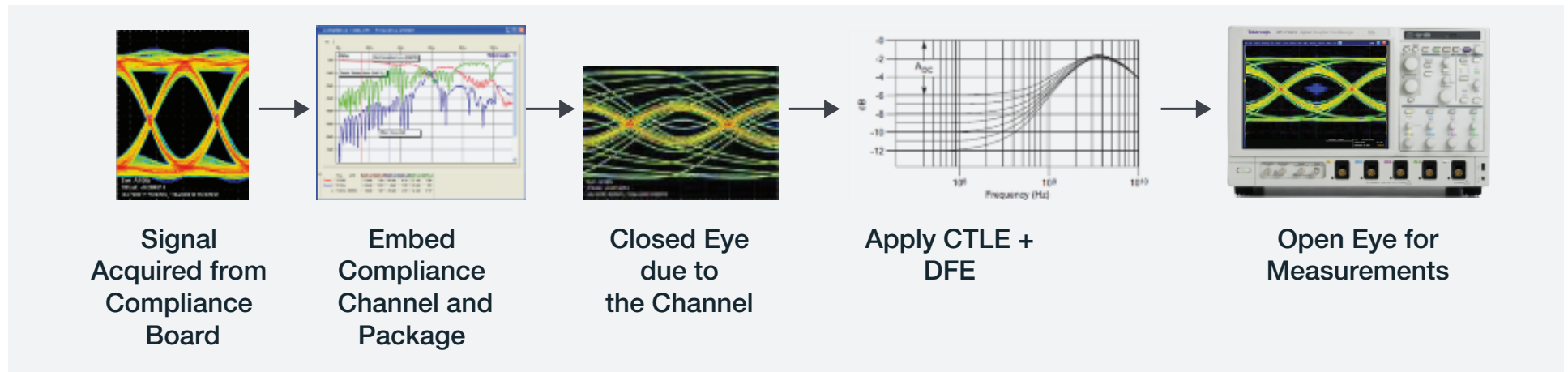
1. De-embed the loss of the breakout channel if you have a good understanding of the S-parameters of a similar replica channel. This allows you to see what the signal looks like at the pins of the transmitter without the added effects of the channel.
2. Use equalization or CTLE on an oscilloscope to equalize out channel loss.
3. Use a high-bandwidth probe to probe as close as possible to the transmitter pin (for example the Tektronix P7700 probe).

Software tools like SDLA, Seasim, and SigTest can be used by an oscilloscope to perform embedding/de-embedding, equalization, and eye analysis. This software-level analysis allows designers to optimize and debug their silicon's performance before tape-out, saving time, money, and extensive debug.

Make sure you employ a measurement system that is flexible enough to test and debug the specific capabilities of the device under test.



08. CEM & U.2 Spec Transmitter (Tx) Testing



System and Add-In Card

In CEM level transmitter testing the transmitter's signal integrity is measured as seen by the slicer of the receiver, but because of the form factor and fixtures used during testing direct signal access is impossible. To ensure measurement accuracy implement the two important components described here.

1. Embed the performance characteristics of the compliance channel back into the signal you're measuring. This requires a solid understanding of the channel's insertion loss and S-parameters. For this reason, the PCI-SIG offers compliance test fixtures for CEM testing with known s-parameter parameters.
2. Apply channel equalization using software tools to measure and analyze an open eye at the end of the channel. PCI-SIG provides a software tool known as SIG-Test to apply the behavioral equalizer specific to PCI-SIG features and provide Pass/Fail results. Custom oscilloscope software, like Tektronix's DPOJET and SDLA, can fully characterize and debug an equalized signal from a closed eye to an open eye.

09. Basics of Receiver (Rx) Testing

1. Putting device into loopback (i.e., self test mode)
2. Performing link equalization to overcome channel loss

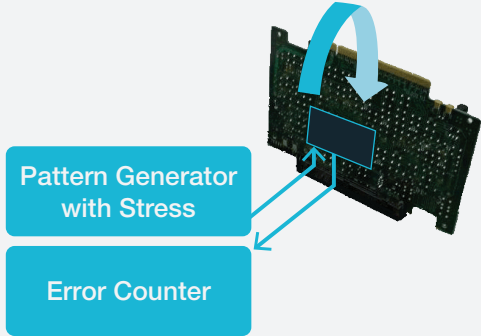
Requires Protocol Awareness

3. Easy setup of impaired signal
4. Auto calibration of stress impairments
5. Making accurate and repeatable BER measurements

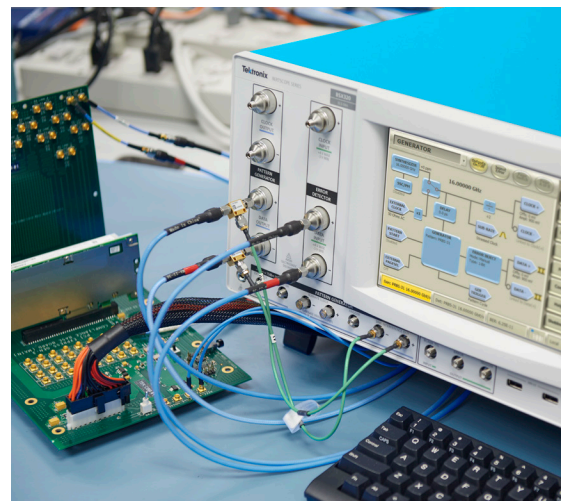
Need Automated Solutions for Gen3 and Gen4 Standards

6. Root-causing factors leading to bit-error or link training problems

Go Beyond Compliance



ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	



— Tektronix offers the new BSX series BERTScope for PCIe Gen1-4 receiver calibration, automated compliance, and debug. The BSX instrument enables users to put PCIe devices into loopback using a customizable protocol sequencer, perform link equalization to overcome channel loss, and perform calibrated impairment testing.

10. Key Considerations in Setting up PCIe Test and Debug

As PCIe becomes faster and more complex with the emergence of the Gen 4 standard, engineers are faced with new design challenges, shorter time-to-market windows, new standards specifications to understand and apply, and new compliance testing requirements.

Before you tackle testing and debug of your Gen 3 or Gen 4 PCIe device, here are some key questions to ask:

- How will you verify protocol compliance on your device?
- How will you verify that actual transmitter margin meets design goals?
- How will you debug and perform interoperability testing when repeaters/re-timers are present?
- How will you verify that actual receiver margin meets design goals?
- How will you test your custom interface and verify operation to design goals?
- How will you establish loopback mode on your device to enable testing?
- Do you have a plan for verifying and debugging link training on your device and putting your device into loopback?
- Can you automatically optimize Tx and Rx equalizer settings?
- Do you understand how much margin your receiver has against the test standard?
- Do you have the tools to automatically and quickly perform compliance testing at various corner conditions?
- Do you have the tools and expertise to configure, optimize and calibrate your entire test set up?

—
Don't waste your time.

Make sure your device passes the first time.

Historically, when a new generation of PCIe devices enters compliance testing, a significant percentage of them fail their first plugfest for PHY and link training compliance. Thus, it is vital to have a comprehensive test equipment and software solution in place prior to workshop testing. Tektronix's PCIe test and debug solution can easily guide you through compliance testing and debug before a plugfest to ensure your design meets the standards requirements with a high degree of confidence.

Need help in answering these questions?

Your Tektronix Account Manager will be happy to help, just give them a call.

To contact any of our worldwide offices for assistance please refer to the telephone numbers on the next page.

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