1200 A, 3300 V IGBT Power Module exhibiting Very Low Internal Stray Inductance

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Abstract

The ABB **F**lat **L**ow **I**nductance **P**ackage (FLIP®) technology enables the production of High Power IGBT Modules from 1800 A, 1800 V to 1200 A, 3300 V with an internal inductance as low as 3 nH . This represents an improvement of a factor of 2 compared to conventional modules at this power level. Because of a novel terminal arrangement inside the module, the internal terminal and bond wire arrangement contributes only 0.2 nH to the total module inductance. All other parasitic inductance originates from the screw type terminal contacts to the outer power circuit. The new terminal arrangement enables an improved high power inverter construction which results in a total parasitic inductance of only 40 nH for an inverter in the MW range. This paper describes the internal module and the inverter construction, the test method to measure the module inductance, and the actual test results for different module configurations. Switching and short circuit test wave forms underline the relevance of the achievements for the application.

Introduction

High current, high voltage power modules require the paralleling of many IGBT and diode chips inside one package. A typical 1200 A, 3300 V module contains 20 IGBT and 12 diode chips. For fast switching operation, all internal package inductances must be kept small to minimise voltage overshoots during turn-on and turn-off. To enable equal current sharing between the chips the parasitic inductances should be of the same value to each chip.
Today's high power modules (800 A and higher) /1,2/ are constructed as follows:

1. A few (4 to 8) IGBT and diode chips are soldered to a metallized ceramic substrate. The metal pattern on the ceramic is such that it provides space for the chips and for the pad areas of terminals and bond wires.
2. Emitter (anode) and gate connections between chip surface and pad areas are established by multiple wire bonds.
3. The substrates are attached to a common base plate (typically soldered) and load terminals are attached (e.g. soldered, welded, pressed) to these substrates to provide connections to the power circuit. In today's advanced designs, these terminals are arranged in parallel /3,4/ to minimize inductance.
4. Auxiliary and gate connections are provided either by wire harnesses between substrates and terminals and / or PCB board (s).

This construction has some drawbacks with respect to inductance:

1. Substrate:

The pattern on the ceramic substrate should be wide and short to give minimum inductance. On the other hand, the ceramic real estate should be as small as possible for cost and reliability reasons. Chips and pad areas require finite space and the overall module construction may press further geometrical restrictions. Therefore, very often, the design for minimum inductance has to be

compromised: Long and narrow copper patterns are not uncommon in today's modules. Chips have to be placed in a row relative to the terminal pad position which leads to unequal inductance. One approach to resolve this conflicting situation has been the use of double layer ceramics /3,5/. However, this approach was not adopted for wide-spread use. Recently, lower power modules (with considerable smaller footprints) have been introduced to the market where the terminals are not longer attached directly to the ceramic substrate. In these constructions /6,7/ the terminals are molded-in into the plastic housing and the connection to the ceramic substrates is provided by multiple wire bonds. This enables better usage of ceramic real estate and leads to substrate designs with lower inductance.

2. **Bond Wires**: The IGBT chip layout and the substrate layout typically restrict the optimization of the bonding pattern from an inductance point of view: Gate connections have to be accommodated and the number of bond wires to run in parallel is restricted by the bond pad area on the chip.

3. **Auxiliary terminals**: The auxiliary terminals are located on top of the module with considerable space between them to fulfil creepage and air distance requirements. With the load terminals protruding from the centre of the module, it becomes necessary to route quite long wires from the substrates to these terminals, leading to parasitic inductance. Inductance implications can be minimized by using twisted pair wires or a horizontal PCB board which collects the substrate's auxiliaries and routes them to the auxiliary terminals.

FLIP® Module Construction

The construction of a FLIP® Module is shown in Fig. 1. The main difference to conventional concepts lies in the arrangement of the main terminals as sheets parallel to the base plate /8/. The construction is now described more in detail to explain how issues regarding inductance were solved:

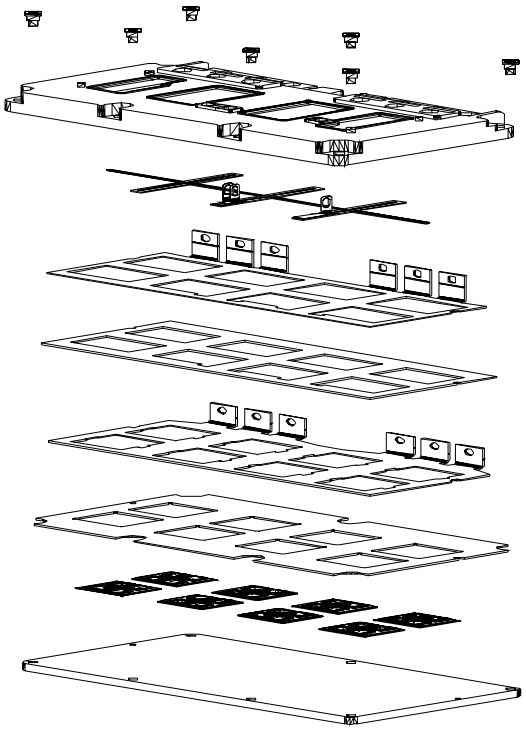

Fig. 1: FLIP® Module construction (5SNA 12F3300D).
The basic assembly process flow is similar to that of a conventional module. The construction starts with a substrate which is shown in Fig. 2a and 2b.

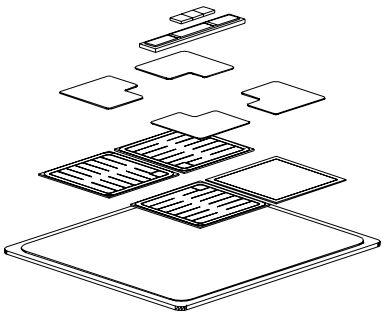

Fig. 2a: Substrate with 3 IGBT and 1 diode chips

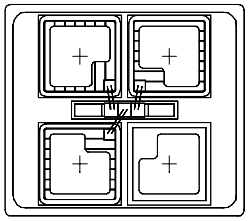

Fig. 2b: Substrate with 3 IGBT and 1 diode chips as it is used in FLIP® modules

The substrate has an unpatterned metallization which provides lowest possible inductance for any given geometry. Three IGBTs and one diode chip are soldered to the substrate together with a very small DCB substrate in the middle which provides space for the discrete silicon gate resistors. Gate resistor and gate pad on the chip are connected by two parallel 8 mil Al wires.

After mechanical tests (i.e. solder void inspection) and electrical tests (i.e. static and dynamic test, including short circuit type I and type II), these substrates are soldered to a common base plate and checked for mechanical integrity (i.e. solder voids).

The main terminals are attached by stacking insulating and conductive layers on top of each other, followed by a printed circuit board which holds all auxiliary connections (see Fig. 2). All layers are glued together using an adhesive which enables excellent temperature cycling. The process has to be carried out carefully to avoid trapped air between the layers which would result in poor partial discharge capability.

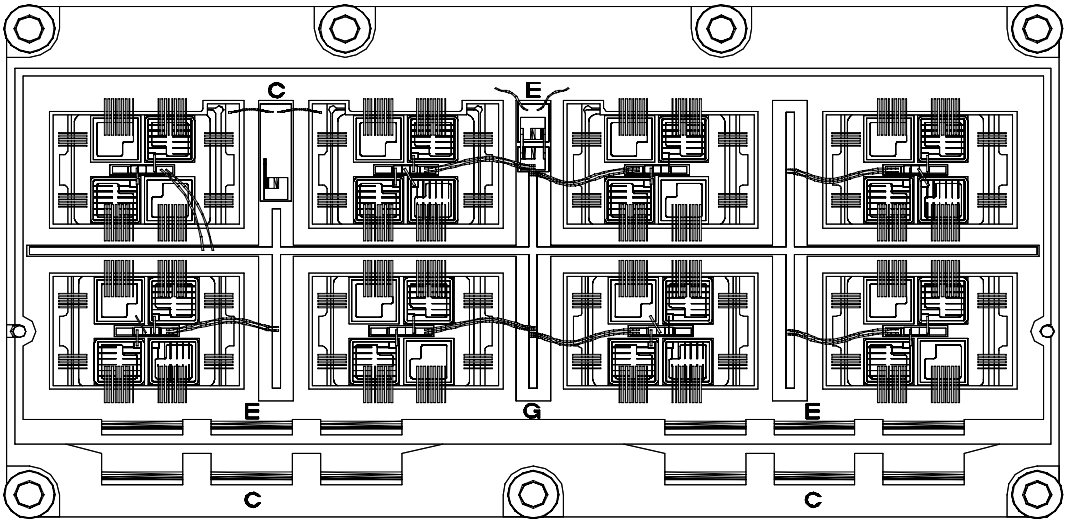

Fig.3: Bond wire schematic of a FLIP® module.

The electrical connection between terminals and chips is established by bonding parallel wires (15 mil thickness) directly from the emitter terminal to the emitter (anode) chip electrode and from the collector terminal to the ceramic substrate pad area. Gate and auxiliary connections are made using wire bonding between the PCB board and gate runners on the substrate subassemblies. Fig. 3 shows the bonding diagram of a finished module.

Fig. 4 shows the photo of a FLIP® module for 1200 A, 3300 V. The predominant visible feature is the power terminal arrangement at the side of the module which extends over it's entire length. The lids on top of the module have been removed to provide a view inside the module.

Fig.4: Photo of a 1200 Amp, 3300 V IGBT FLIP® Module
(Part No. 5SNB 12F3300D). The lids on top of the module have been removed to provide a view inside the module.

From an inductance point of view, the following remarkable advantages have been achieved by this construction:

1. Emitter and collector terminal are arranged as parallel sheets which are wide and short. Thickness of the insulating and conductive layers are optimized for inductance, following known design rules for bus bars /9/. Geometrical electrical design constraints are minimal because of the simple form and function requirements.
2. The terminal sheets virtually extend down to the chips by multiple bond wires which can be, as a group, considered to be wide and short. It is very important to note that the bond wires to one terminal are all of equal length. The current path is such that no single chip position in the whole module is preferred or discriminated from an inductance point of view.
3. All chips are equipped with a soldered metal disc on top which gives maximum freedom to lay out the bond pattern for minimum inductance.
4. As the main terminals are arranged as a stack, glued to the solid base of the module, no provisions have to be made for mechanical stress compensation (i.e. "S-shape" bend) which would lead to increased inductance.
5. Since the terminals are not attached to the ceramic substrates, the geometry of the substrates as well as the geometry of the terminals can be optimised for low inductance.

6. Connection between the auxiliary terminals and the substrates is established by wire bond connections from the substrates to a common PCB board which hold also the auxiliary terminals (though with an S-shaped bend) and which is glued to the main terminal stack.

Inverter construction

To achieve lowest inductance in the inverter, the module design has to take the whole inverter construction into consideration.
The primary goal is to minimize the inductance from DC capacitor to the three phase output of the inverter. The internal inductance of the DC capacitor bank can be minimized by selection of the capacitor type and the series / parallel arrangement to achieve a specific capacitance value. For the particular power level under consideration in this paper, the DC capacitor is of considerable size and has to be connected to large power modules (typically six single pack devices) which are bolted down to a big heatsink. Therefore a low inductance connection is not simple to achieve, if the power module has not been designed for that purpose.
Fig. 5 shows schematically the construction of an inverter using FLIP® modules as it has been implemented in traction applications.

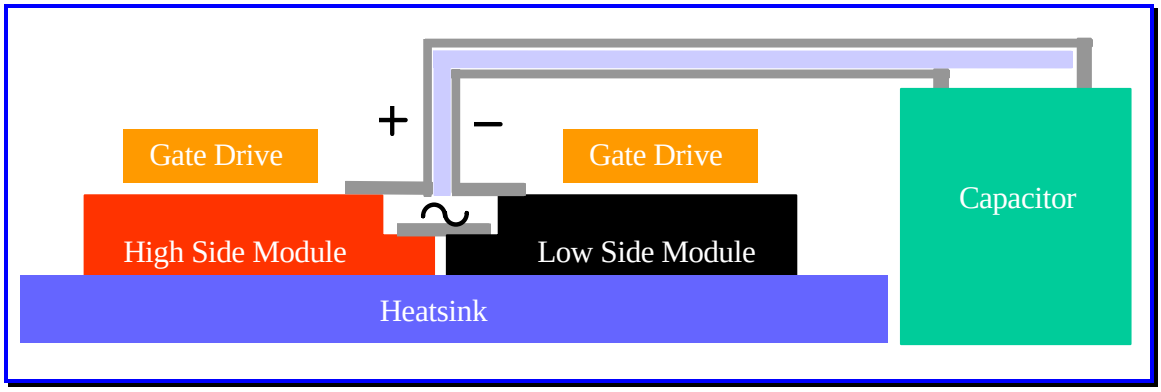

Fig. 5: Construction of an inverter using FLIP® modules.

In the FLIP® module, the power terminals are located at the side of the module and (because of the internal laminated busbar construction) reach out at different heights. The power terminals extend over the entire length of the module.
By designing two types of modules, one with the emitter layer on top (low-side module, black) and another one with the collector terminal on top (high-side module, red) a favourable bus bar arrangement can now be achieved when placing the modules face to face on the common heat sink: The DC bus is designed as two parallel short and wide metal sheets reaching from the DC capacitor bank to the module. The phase output does not obstruct or restrict the DC side geometrically because it leaves the arrangement at the lower level perpendicular to the DC side.
In fast switching devices, it is not only important to achieve minimum inductance for the power connection, but also to achieve low inductance for the gate and auxiliary connections.
In the construction shown in Fig. 5, a favourable solution can be provided because the main terminals are at the side of the module:
This provides space on top of the module to locate the gate drive unit there and to achieve shortest possible connections between gate drive and gate and auxiliary terminals. No additional wires are necessary to be routed between power terminals and gate units which would otherwise be situated far away.

Test Method

Different test methods to measure the internal inductance of power modules are used. Most frequently, the inductance is calculated from the collector - emitter voltage drop at turn-on /10/ or the voltage overshoot at turn-off at known dI/dt /3/. The test accuracy is limited by the fact that one has to measure the potential at the main terminals with reference to the potential at the auxiliary terminals and has therefore to subtract two large numbers from each other.
Fig. 6 explains the test setup used in this experiment.

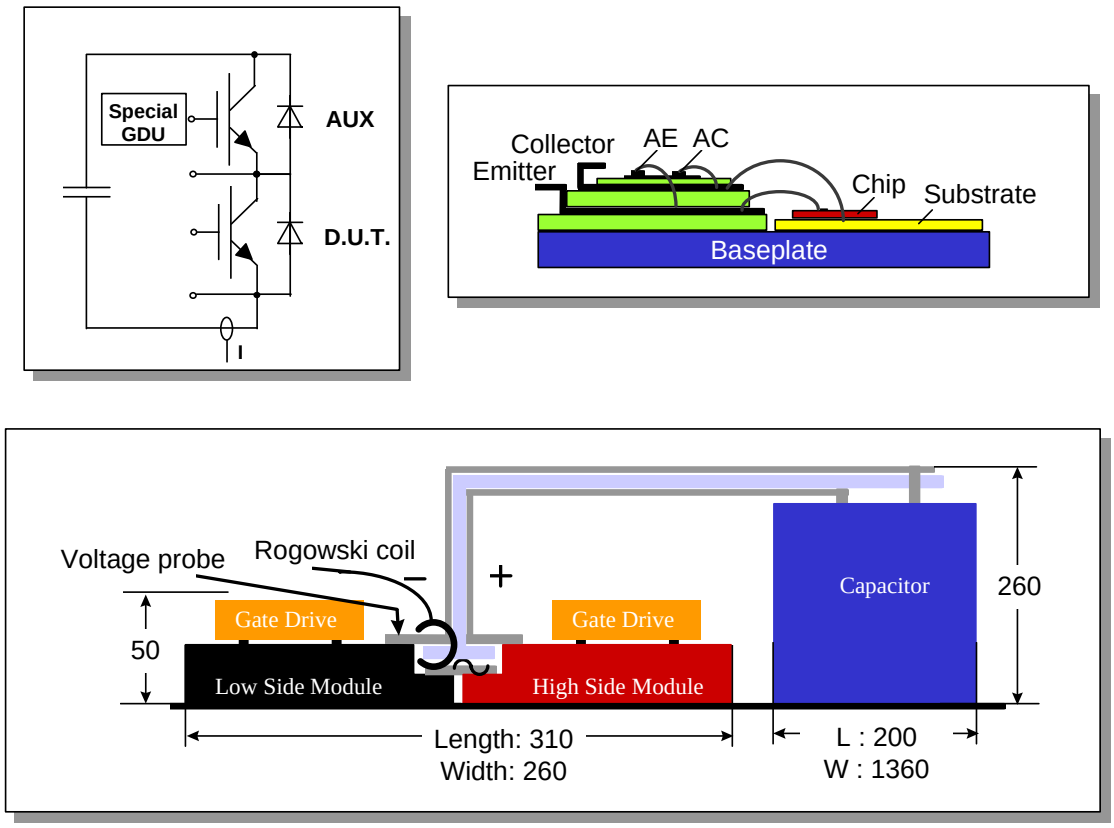

Fig. 6: Measurement set - up for inductance measurement
(all dimensions in mm).

In the upper left insert in Fig. 6 the circuit diagram of the test setup is shown. The device under test (D.U.T.) is connected in series with a second module (AUX) which is equipped with a special gate unit. In the test sequence, the capacitor is charged to 50 V with the D.U.T. turned on. Next, the auxiliary IGBT is turned-on into short circuit causing the current to rise to the desaturation level of the D.U.T. which is at about 6000 Amp for this particular device.
After 40 μs, the auxiliary device is turned off with constant dI/dt controlled by the gate unit and the voltage drop between two terminals is recorded. The inductance between the terminals is given by the linear dI/dt and the respective voltage drop:

$$L = U / (dI/dt)$$

The best results are achieved with a dI/dt of - 3 kA/μs. With such a current slope the signal voltage is 3 V per nH and the current slope can be measured with appropriate accuracy. The forward voltage drop of the device is subtracted from the measured voltage arrive at the voltage caused by the inductance only.

The lower insert in Fig. 6 shows the mechanical arrangement in a schematic drawing: The DC capacitor bank is build from 24 electrolytic capacitors (400 V, 8.9 mF, 3 in series, 8 in parallel). The total inductance of the DC capacitor bank and the bus bar arrangement is about 40 nH. For the current measurements we use a Rogowski coil /11/, type CWT 60 from Power Electronic Measurement Ltd. The voltage is measured using standard 1:1 probes.
The upper right insert of Fig. 6 shows a schematic cross section of a high side module to explain the physical location of the terminals which were accessed in the measurements.
Because of the two module configurations (high side and low side) and in order to test IGBT and diode part, four different test circuits were used. Fig. 7a to 7d shows the electrical diagram of the test circuits together with all the measured parasitic inductances which are relevant to the application engineer.

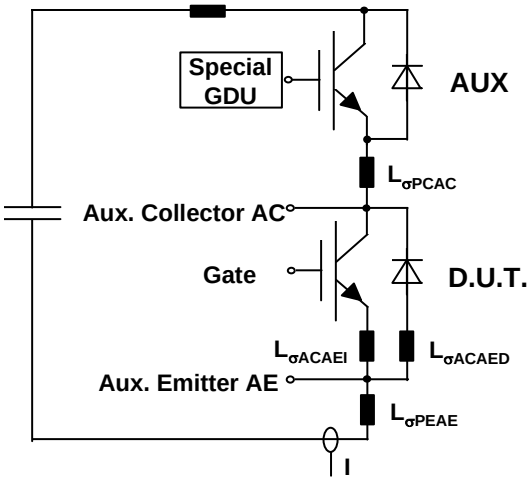

Fig. 7a: Inductance low side IGBT

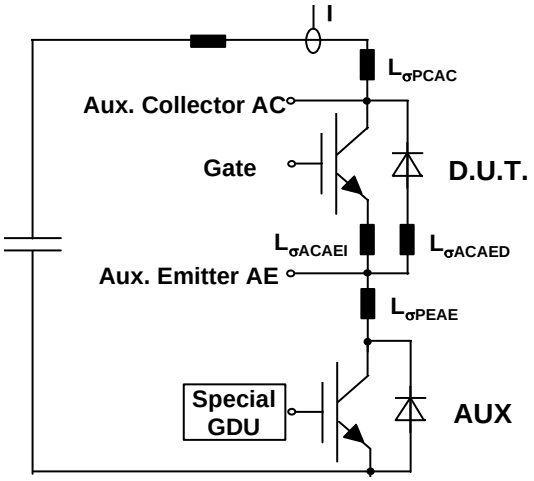

Fig 7b: Inductance of high side IGBT

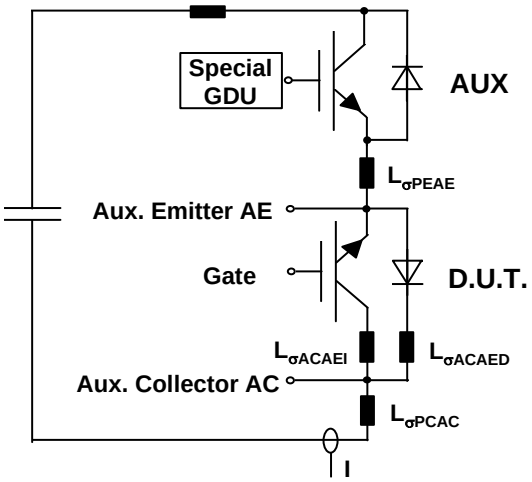

Fig. 7c: Inductance high side Diode

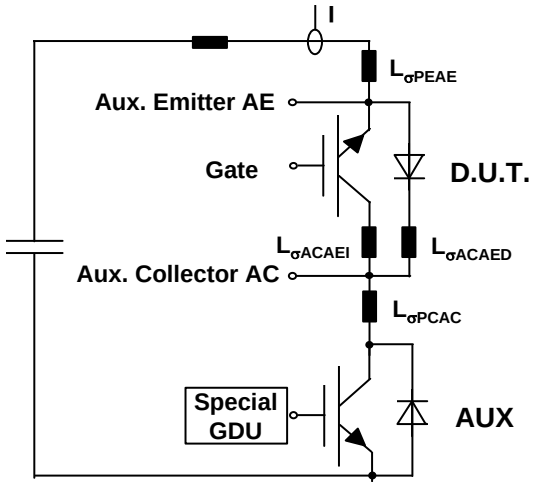

Fig. 7d: Inductance low side Diode

Results

The measured wave form of the test sequence is shown in Fig. 8. It can be seen how the capacitor is charged, the auxiliary device being turned-on into short circuit, and being turned-off again with a linear dI/dt . Fig. 9 shows the turn-off of the device under test in an extended time scale. The voltage between different terminal locations at the module is plotted versus time, as well as the collector current.

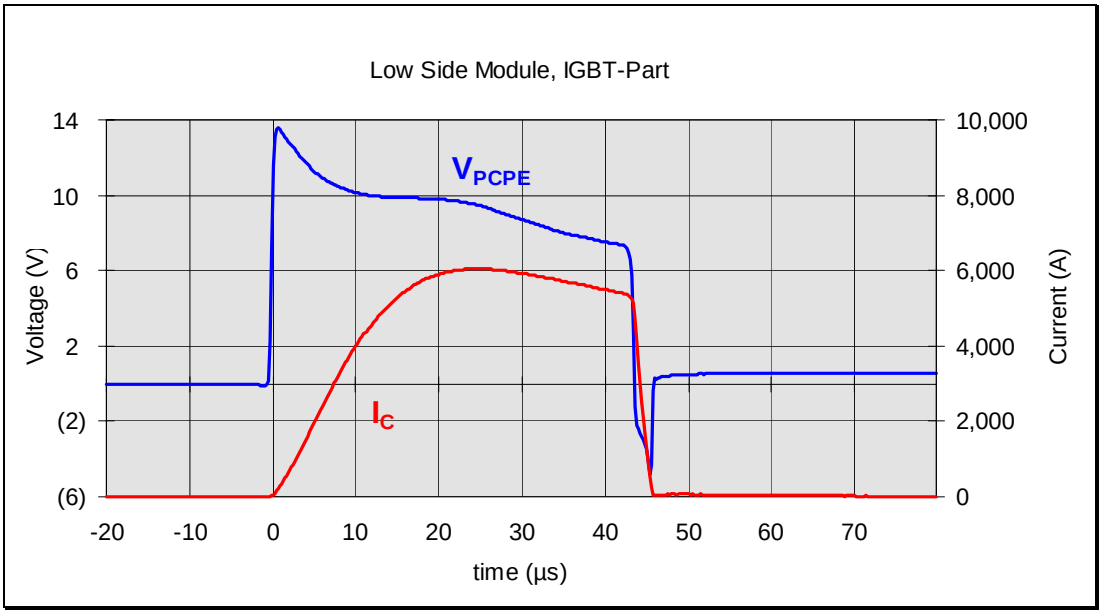

Fig. 8: Current and voltage waveforms during turn-off from short circuit with controlled dI/dt for a high side module.

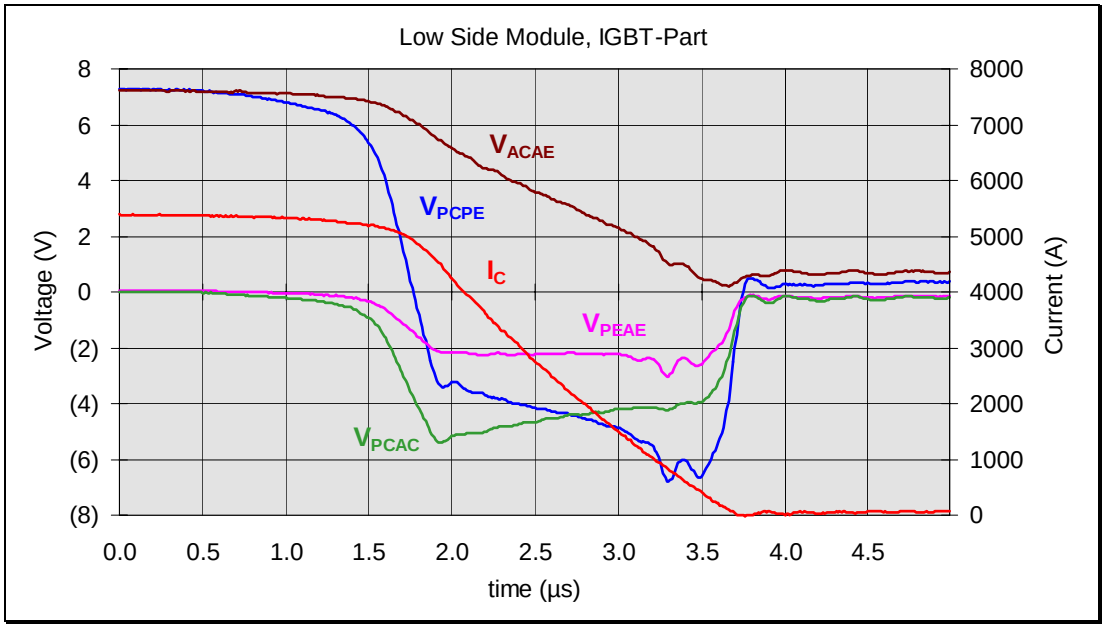

Fig. 9: Current and voltage waveforms during turn-off from short circuit with controlled dI/dt for a high side module in an expanded view.

Table 1 summarizes the measured inductances.

Inductance in nH	IGBT part, low side module	IGBT part, high side module	Diode part, low side module	Diode part, high side module
Collector to emitter	**2.9**	**3.3**	**3.0**	**3.1**
Aux. collector to collector	**1.9**	**1.1**	**2.0**	**1.0**
Aux. emitter to emitter	**0.8**	**2.0**	**0.8**	**1.9**
Aux. emitter to aux. coll.	**0.2**	**0.2**	**0.2**	**0.2**

Tab.1: Measured inductance between different terminals in a high power FLIP® module.

If one compares the results shown in Tab. 1 with the upper right schematic in Fig. 6, it becomes obvious which construction elements cause how much parasitic inductance.

- The upper terminal connector contributes 0.8 to 1.0 nH
- The mulitple bondwire arrangement contributes only 0.2 nH
- The lower terminal connector contributes 2.0 nH.

Therefore further improvement in parasitic inductance will not come from improving the internal layout but from better construction of the connectors to the outer power circuit. Any bending of the terminals to accommodate screw type contacts should be avoided carefully.

Although the measured inductances are already very small, the level of improvement can only be seen, when comparing the FLIP® module with a conventional module of equal power rating:

Using the same test circuit as described above, a conventional power module (1600 V, 1800 Amp) was tested. The results of this test are listed in Table 2:

Inductance (nH)	**IGBT Part**	**Diode Part**
Collector to emitter	**7.0**	**7.0**
Aux. collector to collector	**4.3**	**4.9**
Aux. emitter to emitter	**1.9**	**0.9**
Aux. emitter to aux. coll.	**0.7**	**1.1**

Tab.2: Measured inductance between the different terminals in a conventional high power module (1600 V,1800 A).

A conventional exhibits a parasitic inductance which is about a factor of 2 higher than the FLIP® module. However, the same conclusion as above is valid: The main contributor to inductance is the terminal connection to the power circuit and a novel contacting scheme could improve the situation dramatically.

Fig. 10 and 11 show the turn-on and turn-off waveforms as well as the shortcircuit test waveforms of a 1200 A, 3300 V FLIP® module. The max. DC voltage was set to 2600 V, the max. collector current to 1200 Amp.

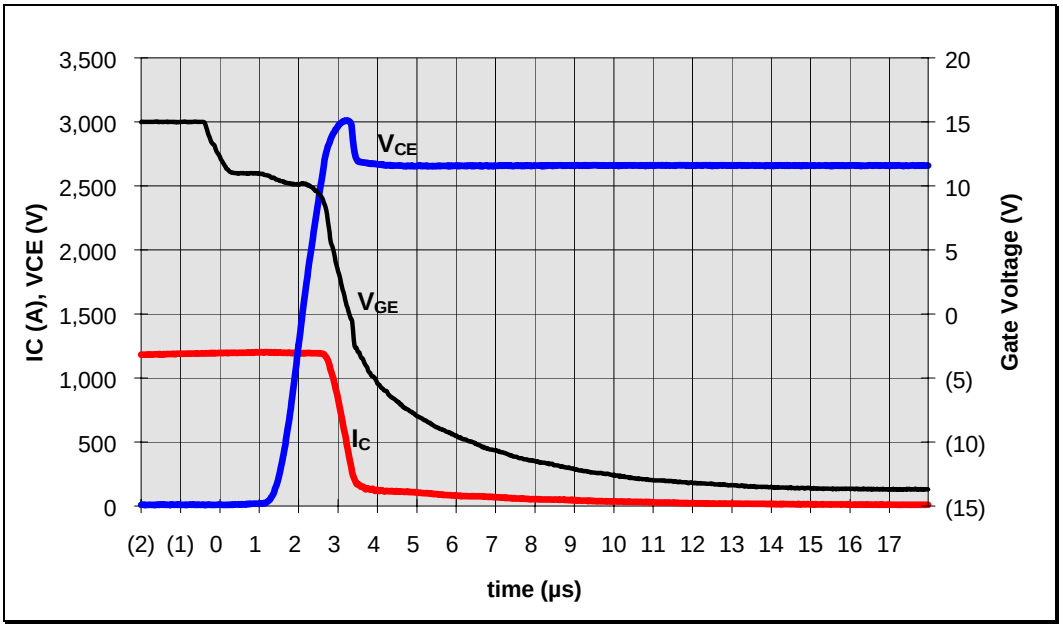

Fig. 10a: Current and voltage waveforms at turn-off in a double pulse test of a 1200 A, 3300 V FLIP® module. Conditions: V_{DC} =2600 V, I_C = 1200 A

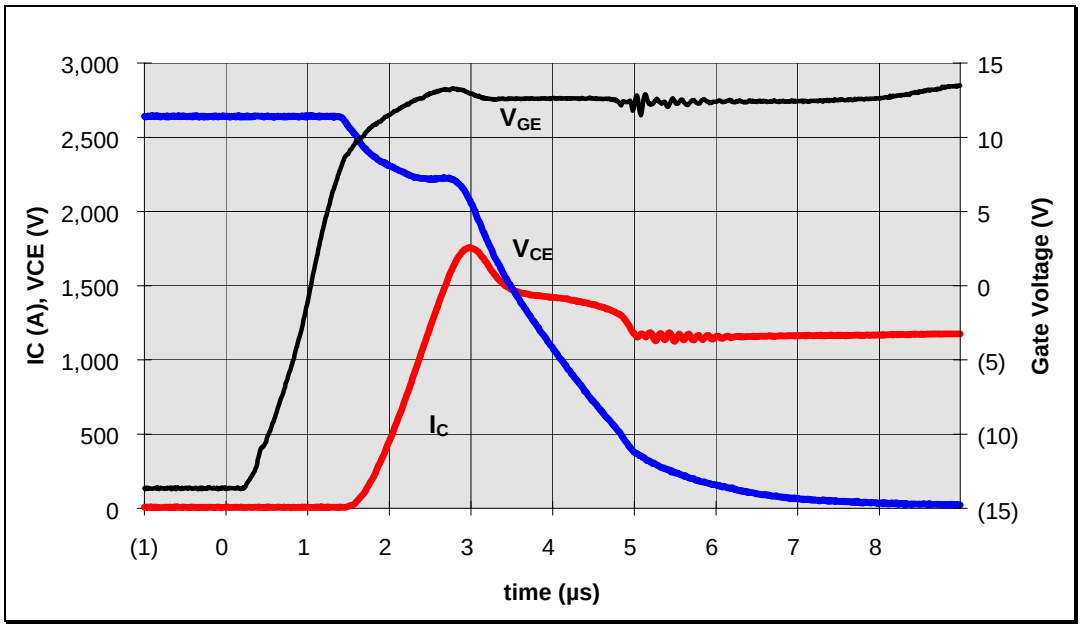

Fig. 10b: Current and voltage waveforms at turn-on in a double pulse test of a 1200 A, 3300 V FLIP® module. Conditions: V_{DC} =2600 V, I_C = 1200 A

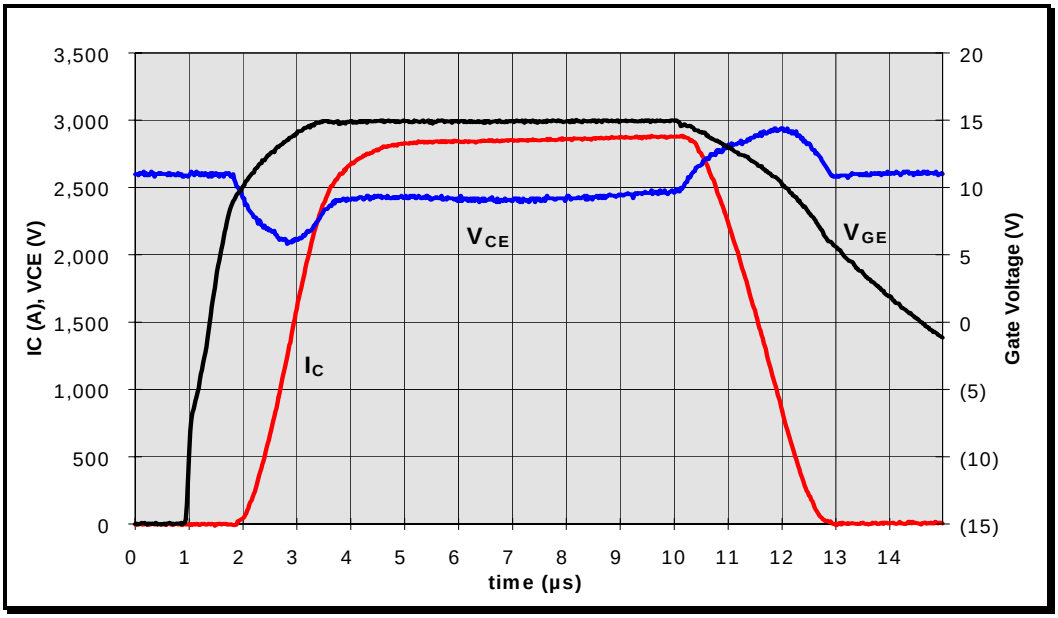

Fig. 11: Shortcircuit test waveforms for a 1200 A, 3300 V FLIP® module.
Conditions: V_{DC} = 2600 V, t_p = 10 µsec.

Conclusions

For the emerging use of fast switching IGBT devices at very high power levels the optimization of inverter and module inductances becomes an ever more important task. In this paper we showed how a different internal module construction and a new terminal arrangement can lead to drastically reduced parasitic inductances, resulting in reduced voltage overshoots at any switching event.
All relevant parts and processes (substrate, terminals, bond wiring) could be optimized for inductance because the usual design constraints were eliminated by a new terminal arrangement concept.
The internal terminal construction and bond wire scheme yielded only 0.2 nH which is very favourable for parallel connection of multiple, fast switching devices. However, the terminal arrangement which contributes about 1.0 nH for the upper terminal and 2.0 nH from the lower terminal should be improved using a different type of connection to the power circuit.
The test method applied here proved to be useful to determine even very low inductances in a reliable fashion. The set-up is easy to use and doesn't require any special mechanical constructions or precautions.
The new FLIP® module exhibits a collector to emitter inductance of only 2.9 to 3.3 nH, depending on the module configuration which is an improvement of a factor of 2 over today's conventional high power modules.

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