Agenda At-a-Glance

	Monday July 10th	Tuesday July 11th	Wednesday July 12th
09:00		Opening	Keynote Speech Prof. Seiji Kajihara, KyuTech, Japan "Right Power Testing for Scan-Based BIST and Its Evaluation with TEG Chips" Chair: Prof. Shyue-Kung Lu, NTUST
09:10		Keynote Speech Prof. Seiji Kajihara, KyuTech, Japan "Right Power Testing for Scan-Based BIST and Its Evaluation with TEG Chips" Chair: Prof. Shyue-Kung Lu, NTUST	
09:50			Break
10:00			
10:10		Invited Talk Director C.F. Wu, RealTek, Taiwan "Decision Making for Complex SoCs" Chair: Prof. Chih-Tsun Huang, NTHU	Academic-Industrial Panel Chair: Charles H.-P. Wen, NCTU "The Trends and Challenges of Automotive Test and Reliability"
10:50			
11:10		Break	
11:30	Registration & Reception (Hostel) Lunch (Oriental, Lalu)	Paper Session 1 Clock Test/Synthesis and Debug/Verification Chair: Prof. Ching-Hwa Cheng, FCU	Best Paper Award Program Chair: Prof. S.-M. Li, NSYSU
11:40			
12:00			Lunch Box & Farewell
12:10		Lunch (Oriental, Lalu)	
13:30		Paper Session 2 Memory Test and Repair Chair: Prof. Jing-Jia Liou, NTHU	
14:00			
14:15	Tutorial 1 Chair: Prof. S.-M. Li, NSYSU Lecturer: Prof. Gang Qu, UMD, US "Challenges about Hardware Security" / The 3rd VTTF 2017 Technical Session Chair: Prof. T.-C. Huang		
14:20		Paper Session 3 Error Detection and Correction Chair: Prof. Chun-Lung Hsu, ITRI	
15:20			
15:30	Break & Check-in	Poster Session & Break Chair: Prof. Yingchieh Ho, NDHU	
16:00		Paper Session 4 Scan Test and FPGA Formatter Chair: Prof. Jwu-E Chen, NCU	
16:45			
16:50	Tutorial 2 Chair: Prof. S.-M. Li, NSYSU Lecturer: Prof. Charles H.-P. Wen "Study on Soft Error Rate (SER): Past, Present, and Future" / The 3rd VTTF 2017 Discussions Chair: Prof. T.-C. Huang		
17:30		Paper Session 5 Mixed-Signal Chair: Prof. Soon-Jyh Chang	
17:50	Break & Check-in		
18:00			
20:00	Reception (Lake-view, Lalu)	Banquet (Hostel)	
21:30		Review Meeting Chair: Prof. Meng-Leih Sheu	

Local Area Map

Conference Venue

Sun Moon Lake Teachers' Hostel
南投縣魚池鄉日月潭教師會館
Address:水社村中興路 136 號
Tel: (049) 2855991#3502
VTTW2017 Website: http://TestLab.NCUE.edu.tw/VTTW2017

Emergency Contact

General Co-chair Prof. Tsung-Chu Huang (黃宗柱) 0939-039500
Assistant Miss Shih (施少婷) (04)7232105#8305
Assistant Mr. Lin (林毓乾) 0921-736896

The 11th VLSI Test Technology Workshop
(VTTW2017)

Sun Moon Lake Teachers' Hostel
July 10-12, 2017

Final PROGRAM

Sponsored by

National Changhau University of Educaiton
Taiwan IC Design Society
Industrial Technology Research Institute

台灣積體電路設計學會主辦
工業技術研究院資通所協辦
國立暨南國際大學協辦
國立中山大學協辦
國立彰化師範大學電子系承辦

Contents

Paper Session 5

Mixed-Signal
Chair: Prof. Soon-Jyh Chang
16:50-17:50 Assembly Hall

S5-1 *A Resistor-String Digital-to-Analog Converter Based Waveform Generator*
Hsin-Wen Ting, Jian-Zhou Yan, Hsin-Ying Wu and Zi-Tao Wu

S5-2 *Co-Placement Optimization of Cyber-Physical Digital Microfluidic Biochips for Testing*
Jian-De Li and Sying-Jyan Wang

S5-3 *Lifetime Estimation of NBTI Effects for Manufactured Circuits*
Hau Hsu, Jing-Jia Liou, Zih Huan Gao and Ting-Shuo Hsu

S5-4 *Process-Compensated Track-and-Hold Circuit with Leakage Suppression in Low-voltage SAR Analog-to-Digital Converters*
Yingchieh Ho and Yan-Ze Lin

Poster Session

SP-1 *Multiple-TSV Schemes for Lagging-Defect Tolerant Clock-Delivery in 3D ICs*
Yu-Chien Lin and Tsung-Chu Huang

SP-2 *A Defect-Tolerant Multi-TSV Structure and Placement for Power-Grids in 3D ICs*
Kun-Yuan Li, Mong-Lin Li and Tsung-Chu Huang

SP-3*The Rainbow Transformed from a Set of Uniform-defect Wafer Maps*
Chen Jwu-E, Liang Hsing-Chung, Lin Ching-Ju and Wu Ya-Syuan

SP-4 *Detection for Stealthy Combinational Hardware Trojans*
Sying-Jyan Wang, Jhih-Yu Wei, Shih-Heng Huang, Katherine Shu-Min Li

SP-5 *Digital Rights Management for Paper-Based Microfluidic Biochips*
Jian-De Li, Sying-Jyan Wang, Katherine Shu-Min Li and Tsung-Yi Ho

SP-6 *The Image Stitching Performance and Quality Improve Techniques*
Nguyen Van Thang and Ching-Hwa Cheng

Paper Session 3

Error Detection and Correction
Chair: Prof. Chun-Lung Hsu
14:20-15:20 Assembly Hall

S3-1 *Radiation-Hardened Designs for Soft-Error-Rate Reduction by Delay-Adjustable D-Flip-Flops*
Dave Y.-W. Lin and Charles H.-P. Wen

S3-2 *Low-Latency Multiple-Cluster Error Correction for Critical Interconnect Arrays*
Yi-Shan Li, Sing-Ni Huang and Tsung-Chu Huang

S3-3 *A Hybrid Concurrent Error Detection Scheme for Simultaneous Improvement on Probability of Detection and Diagnosability*
Chih-Hao Wang and Tong-Yu Hsieh

S3-4 *An Image Error-Tolerability Test Method for Face Detection Applications*
Tong-Yu Hsieh, Chao-Ru Chen and Tai-Ang Cheng

Paper Session 4

Scan-Test and FPGA Formatter
Chair: Prof. Jwu-E Chen
16:00-16:45 Assembly Hall

S4-1 *Design and Implementation of an EG-Pool Based FPGA Formatter with Temperature Compensation*
Yang-Kai Huang, Kuan-Te Li, Chih-Lung Hsiao, Chia-An Lee, Jiun-Lang Huang and Terry Kuo

S4-2 *DR-scan: Dual-rail Asynchronous Scan DfT and ATPG*
Shih-An Hsieh, Ying-Hsu Wang, Ting-Yu Shen, Kuan-Yen Huang, Chien-Mo Li and Chia-Cheng Pai

S4-3 *The Interconnection Evaluation and Reconfiguration Mechanisms for 3D-Stacking System*
Ching-Hwa Cheng

Welcome Remarks

Ten years was a milestone and the 11th year should be a new start. Starting next decade, we wish to welcome all ladies and gentlemen to this VLSI Test Technology Workshop held on July 10-12, 2017.

Following the tradition, the technical program has a wide coverage - including 2 tutorials, 16 regular paper in oral presentations, 6 poster presentations, 2 keynote speeches 1 invited talk, and 1 academic-industrial panel discussion. In the first day Prof. Gang Qu from UMD and Prof. Charles Wen from NCTU will give us smart lectures.

In the plenary sessions, the first keynote speech will be given by Prof. Seiji Kajihara from Kyushu Institutue of Technology with the title of “Right Power Testing for Scan-Based BIST and Its Evaluation with TEG Chips.” The second keynote speech will be given by Prof. Shi-Yu Huang from National Tsing-Hua University with the title of “Eye in the Sky--Health Condition Monitoring for IoT Devices in the Field.” The invited talks will be given by Dr. Chi-Feng Wu from RealTek with a topic on “Decision Making for Complex SoC.”

In the panel, Six expert panelists from both academia and industry will share their opinions on “The Trends and Challenges of Automotive Test and Reliability.”

Not mentioned that a workshop cannot be successful without active participation from the audience. Through active interaction, we sincerely hope that all of us will find this event not only rewarding but also memorable.

Welcome to Sun-Moon Lake, Taiwan.
Happy 11th Anniversary to VTTW!

General Chair Prof. Meng-Lieh Sheu, NCNU
TPC Chair Prof. Shu-Min Li, NSYSU
General/PC Co-chair Prof. Tsung-Chu Huang, NCUE

Organizing Committee

General Co-chair

Prof. Meng-Lieh Sheu, NCNU

General Co-chair

Program Co-chair

Prof. Tsung-Chu Huang, NCUE

Program Chair

Prof. Shu-Min Li, NSYSU

Finance Chair

Prof.Ming-Der Shieh, NCKU

Registration Chair Prof. Ying-Chieh Ho, NDHU

Paper Session 1

Clock Test/Synthesis and Debug/Verification

Chair: Prof. Ching-Hwa Cheng

11:10-12:10 Assembly Hall

S1-1 *DLL-Assisted Clock Synchronization Method for Multi-Die ICs*

Chia-Yuan Cheng, Shi-Yu Huang, Ding-Ming Kwai and Yung-Fa Chou

S1-2 *A Silicon Debug Technique for Multiple Clock Domain Systems*

Shuo-Lian Hong and Kuen-Jong Lee

S1-3 *Exploring Domain Equivalence for Accelerating UPF-based Power Verification of RTL Designs*

Chia Hao Hsu and Charles H.-P. Wen

S1-4 *Testing Clock Distribution Networks*

Sying-Jyan Wang, Hsiang-Hsueh Chen, Chin-Hung Lien and Katherine Shu-Min Li

Paper Session 2

Memory Test and Repair

Chair: Prof. Jing-Jia Liou

13:30-14:15 Assembly Hall

S2-1 *Fault Models and Test Algorithms for Multi-Level Cell (MLC) Crossbar RRAM*

Kuan-Wei Hou and Cheng-Wen Wu

S2-2 *Efficient Built-In Self-Test Scheme for Multi-Channel DRAMs*

Kuan-Te Wu, Jin-Fu Li, Chih-Yen Lo, Jenn-Shiang Lai, Ding-Ming Kwai and Yung-Fa Chou

S2-3 *Fault-Aware Page Address Remapping Techniques for Enhancing Yield and Reliability of Flash Memories*

Shyue-Kung Lu

Panel Discussion

The Trends and Challenges of Automotive Test and Reliability

10:10-11:30 Assembly Hall

Chair: Charles H.-P. Wen, NCTU

Panelists:

Dr. Cheng-Foo Chen, Cubelec

Dr. Harry Chen, Mediatek

Dr. Ying-Yen Chen, Realtek

Prof. Jing-Jou Tang, STUST

Dr. Ting-Pu Tai, Mentor

Prof. Syng-Jyan Wang, NCHU

(*arphabetics ordered*)

Local Arrangement Chair

Prof. Ching-Hwa Cheng, FCU

Tutorial Chair

Prof. Shu-Min Li, NSYSU

Panel Chair

Prof. Hung-Pin Wen, NCTU

Publicity Chair

Prof. Chia-Tso Chao, NCTU

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Professor Ching-Hwa Cheng, FCU
Professor Yingchieh Ho, NDHU
Professor Hao-Chiao Hong, NCTU
Professor Tong-Yu Hsieh, NSYSU
Professor Chun-Lung Hsu, ITRI
Professor Chih-Tsun Huang, NTHU
Professor Jiun-Lang Huang, NTUST
Professor Tsung-Chu Huang, NCUE
Professor Shi-Yu Huang, NTHU
Professor Kuen-Jong Lee, NCKU
Professor Katherine Shu-Min Li, NSYSU
Professor Jin-Fu Li, NCUE
Professor Shyue-Kung Lu, NTUST
Professor Jiaann-Chyi Rau, TKU
Professor Meng-Lieh Sheu, NCNU
Professor Ming-Der Shieh, NCKU
Professor Sying-Jyan Wang, NCHU
Professor Wei-Lun Wang, CSU

Tutorial II

Study on Soft Error Rate (SER): Past, Present, and Future

Chair: Prof. S.-M. Li, NSYSU
Lecturer: Prof. Charles H.-P. Wen, NCTU

Charles H.-P. Wen received the Ph.D. degree in very-large-scale integration (VLSI) verification and test from the University of California, Santa Barbara, Santa Barbara, CA, USA, 2007. He is currently an Associate Professor with National Chiao Tung University, Hsinchu, Taiwan, and is a specialist in computer engineering. Over the past five years, his research has been focused on data mining/machine learning techniques to VLSI designs (especially on statistical soft error rates), software-defined networking and network function virtualization (SDN/NFV).
Prof. Wen was also a recipient of the best paper awards from the 17th Asia and South Pacific Design Automation Conference (ASP-DAC 2012), the 18th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2015), the 30th and the 31th International Conference on Information Networking (ICOIN 2016 & ICOIN 2017), and the Distinguished Young Scholar Award of Taiwan IC Design Society in 2015.

Abstract

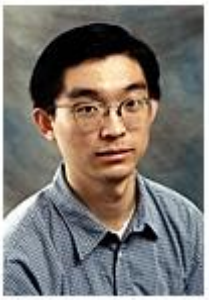
In this tutorial, we re-examine the soft-error effect caused by radiation-induced particles beyond the deep submicron regime. Considering the impact of process variations, voltage pulse widths of transient faults are found no longer monotonically diminishing after propagation, as they were formerly. As a result, the soft error rates in scaled electronic designs escape traditional static analysis and are seriously underestimated. A new concept of statistical soft error rate (SSER) is presented with analysis frameworks for coping with the aforementioned concerns. More advanced issues like aging will be covered if time permits.

Tutorial I

Challenges about Hardware Security

Chair: Prof. S.-M. Li, NSYSU

Lecturer: Prof. Gang Qu, UMD, US



Dr. Qu received his M.S. and Ph.D. degrees from UCLA, both in Computer Science. Previously, he had studied Mathematics in the Univerisy of Science and Technology of China (USTC) and the University of Oklahoma.

Dr. Qu is the co-director of the Embedded System Research Laboratory and the Wireless Sensor Laboratory. His primary research interests are in the area of embedded systems and VLSI (Very Large Scale Integration) CAD (Computer Aided Design) with focus on low power system design and hardware related security and trust. He studies optimization and combinatorial problems and applies his theoretical discovery to applications in VLSI CAD, wireless sensor network, bioinformatics, and cybersecurity.

Dr. Qu and his research group are sponsored by AFOSR, ARO, DARPA, NSA-LTS, NSF, ONR, USDA; Cisco, Fujitsu Research, and Microsoft Research.

Abstract

In this tutorial, we will study security and trust from the hardware perspective. Upon completing the course, students will understand the vulnerabilities in current digital system design flow and the physical attacks to these systems. They will learn that security starts from hardware design and be familiar with the tools and skills to build secure and trusted hardware.

Right Power Testing for Scan-Based BIST and Its Evaluation with TEG Chips

Chair: Prof. Shyue-Kung Lu, NTUST

Speaker: Prof. Seiji Kajihara, KyuTech, Japan

Seiji Kajihara received the B.S. and M.S. degrees from Hiroshima University, Japan, and the Ph.D. degree from Osaka University, Japan, in 1987, 1989, and 1992, respectively. From 1992 to 1995, he worked with Osaka University, as an Assistant Professor. In 1996, he joined the School of Computer Science and Systems Engineering of Kyushu Institute of Technology, Japan, where he is a Dean and Professor currently. His research interest includes logic testing and dependable systems. He received the Young Engineer Award from IEICE in 1997, the IEEE ITC2005 Most Significant Paper Award, and several Best Paper Awards from IEICE, IEEE WRTLT 2007, IEEE ATS 2016. Dr. Kajihara is a member of the IEEE and the IPSJ, and a fellow of the IEICE.

Abstract

High power dissipation during scan-based logic BIST (LBIST) is a crucial issue that may lead to chip damage, cost increase, reliability degradation, or over-testing. Although many sophisticated low-power approaches were proposed in the past, it is still difficult to control the test power of LBIST to an appropriate level which is different depending on applications. This talk discusses a power-controlling method for LBIST that controls the toggle rate during scan-shift operation to an arbitrary level by modifying pseudo-random patterns. Furthermore the method maintains high fault coverage without increasing test time. Simulation-based experiments clearly demonstrate that the proposed method can flexibly control toggle rate, and evaluations on TEG chips show the effect on circuit delay by test power controlling.

Keynote Speech II

Eye in the Sky - Health Condition Monitoring for IoT Devices in the Field

Chair: Prof. Jin-Fu Li, NCU

Speaker: Prof. S.-Y. Huang, NTHU, Taiwan

Dr. Shi-Yu Huang received his B.S. and M.S. degrees in Electrical Engineering from National Taiwan University in 1988 and 1992, respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of California, Santa Barbara, in 1997. He joined the faculty of Electrical Engineering Department, National Tsing Hua University, Taiwan, in 1999, where he is currently Professor.

His research interests broadly cover VLSI design, automation, and testing, with prior experiences on formal verification, power estimation, fault diagnosis, and resilient nanometer SRAM Design. More recently, his research concentrates on cell-based timing circuit designs and their compiler techniques, including Phase-Locked Loop (PLL), Delay-Locked Loop (DLL), Time-to-Digital Converter (TDC), and Programmable Phase-Shifter (PPS), and the applications of these timing circuits to the parametric fault testing and reliability enhancement for 3D-ICs or multi-die integrated ICs. He has published more than 140 refereed technical papers.

Dr. Huang ever co-founded a company, TinnoTek Inc. (2007-2012), specializing a cell-based PLL compiler and system-level power estimation tools. He is a recipient of the Best-Presentation Award from VLSI-DAT in 2006, the Best-Paper Awards from VLSI-DAT in 2013, and ATS in 2014, respectively. Dr. Huang has actively served in the IEEE community, as Program Chair or Co-Chair for 5 IEEE conferences. He is a senior member of IEEE and has been serving in the Editorial Board of IEEE Trans. on Computers as an Associate Editor since 2015.

Absttract

Internet of Things (IoT) devices have found their ways into various applications in smart homes, offices, automobiles, factories, and cities. These new types of devices not only demand new design and manufacturing methodologies, but also bring numerous challenges from the general testing point of view - such as zero-defect quality, high reliability, and long lifetime, etc. To satisfy all these objectives, not only the offline test methods are needed, but also the online monitoring schemes, so that the health condition of an IoT device can be monitored continually throughout its lifetime. By doing so, a run-time failure threat can be detected, diagnosed, and then averted just-in-time via some reconfiguration or replacement procedure to minimize the chance of sudden collapse. In this talk, we will first overview a number of online health condition monitoring schemes and then present a prototype system with some fabricated Design-for-Health-Monitoring circuitry. We will demonstrate how the dynamic supply voltage of an IoT device in the field can be monitored from the cloud, by riding the free wireless communication function provided by the device itself.

Invited Talk

Decision Making for Complex SoCs

Chair: Prof. Chih-Tsun Huang, NTHU

Speaker: Chi-Feng Wu, RealTek, Taiwan

Chi-Feng Wu received the B.S. degree in 1996, the M.S. degree in 1998, and the Ph.D. degree in 2001, all in electrical engineering, from National Tsing Hua University (NTHU), Hsinchu, Taiwan. His research interests include the design and test of VLSI cores and systems. He is currently the Senior Director of R&D Center at Realtek Semiconductor Corp., Hsinchu, Taiwan, where he is responsible for design technology of processor and system-on-chip platform and IP outsourcing strategy. He has published more than 20 research papers in these areas and is an inventor of 6 US patents. He received the Outstanding Award in the IC/CAD Contest of Ministry of Education in 1999, the Best Paper Award in Professor Wen-Zen Shen Memorial Award of Taiwan IC Design Society in 2003, the Outstanding Employee Award of Hsinchu Science Park in 2013, and the Outstanding I.T. Elite Award in 2015.

Abstract

A series of significant mergers and acquisitions indicates the mature of semiconductor industry. Fabless companies, as part of the whole semiconductor industry, also face challenges to maintain continuous growth. In this talk, we review the decision making of each and every stage of complex SoC design, from silicon to system, to find out opportunities for innovation.