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2-BIT COMPARATOR WITH 8-TRANSISTOR 1-BIT FULL ADDER WITH CAPACITOR

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Abstract **— In modern technology comparator is most widely used circuit to convert the analog to digital signals and to compare a digital signal with the corresponding reference signal. But the circuit complexity is high as per existed system and also the delay produced by the existed comparator produces same delay in the final response. So we present a new 2-Bit comparator system in which 1-Bit full adder and 1-Transistor AND gate are present. The 1-Bit full adder is constructed using 8-Transistor with capacitor to decrease the delay, power dissipation, no of transistor's, circuit complexity and average power consumption.**

Keywords— comparator ,no of transistor count,1-bit full adder.

I. INTRODUCTION

Digital comparators are nothing but binary comparators or logical comparators. By using combinational circuit we can test and obtain '>','<' and '=' values in digital form. Applications of comparator are CPU and MCUs as CMOS 4063 and 4585 and the TTL 7485 and 74682'89.A simple basic comparator circuit is an XOR gate. Digital comparators as shown in Fig.1 are most widely used.

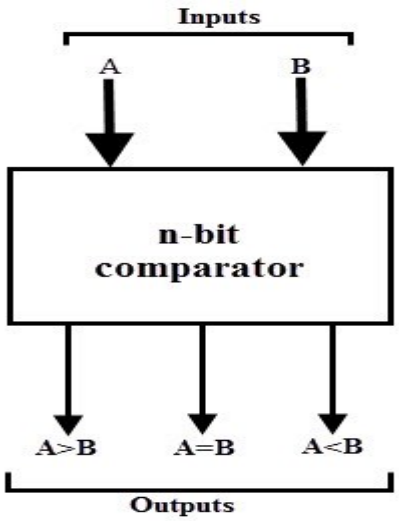

Fig.1 Block Diagram of Digital Comparator

For example, If we need to add and subtract binary numbers comparison should be done among the numbers and to determine whether the value of input A is '<','>' or '=' to the value at input B etc. Several logic gates are used to construct digital comparator on the basis of Boolean Algebra. Digital Comparator's are classified into 2-types.

- EQUALITY COMPARATOR: As the name equality indicates comparator produces output high when both the inputs are equal.
- MAGNITUDE COMPARATOR**:** The magnitude comparator contains three output terminals, one for A=B, A>B and other for A<B.

a) EQUALITY COMPARATOR

In this circuit we use four XNOR gates connected to a single AND gate and the inputs of XNOR gates are A(A_0...A_3) and B(B_0...B_3) as shown in Fig.2 .An XNOR gate produces output logic-'1' when both the inputs are same.

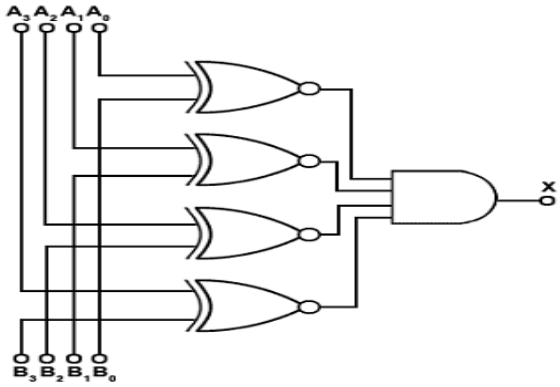

Fig.2 Four Bit Equality Comparator

Similarly all the four XNOR gates are connected to an AND gate in which if any one of the XNOR gate is logic-'0'.Then output of AND gate is forced to logic-'0'.

b) MAGNITUDE COMPARATOR

Magnitude comparator is constructed using 2-and gates 2-inverters and an XNOR gate as shown in Fig.3. And the circuit provides 3-outputs.

i. A > B (A greater than B).
ii. A = B (A equal to B).
iii. A < B (A less than B).

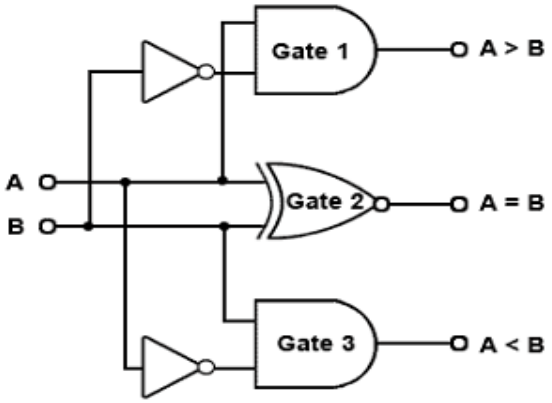

Fig.3 One Bit Magnitude Comparator

The magnitude comparator circuit contains an equality comparator which provides output A equal to B when both the inputs are equal. When the input-A is greater than input-B gate 1 is activated and provides output. similarly input-A is less than input-B gate 3 is activated and provides output.

APPLICATIONS OF COMPARATORS

- These are the devices used in computers and microprocessors for address decoding circuitry.
- These are used in control applications such as temperature, position and so on and they are also used to drive the actuators.
- Process controllers
- Servo-motor control

II. EXISTING DESIGN

Existing design consist of

a) Single transistor AND gate using MOSFET
b) 3-Transistor XOR gate
c) 2-Transistor MUX design
d) Full adder design using 2-XOR and 1-MUX
e) 1-bit full adder
   I. 8 Transistors Full Adder
   II. 9 Transistors Full Adder
   III. 8-T 1-bit Full Adder with Capacitor

a) SINGLE TRANSISTOR AND GATE USING MOSFET

The following and gate is constructed using MOSFET as shown in Fig.4 in which input A is given at Vdd and input B is connected to gate terminal. When input A (Vdd) is zero then the output is forced to zero. When input A is '1'

case1:Input B is '0' then output is '0'.

When gate terminal is supplied with '0V' the MOSFET enters in to cut-off region and then output is '0'.

case 2:input B is '1' then output is '1'.

when gate terminal is supplied with '1V' the MOSFET exceeds the threshold voltage and enters into saturation in which the device is operated for linear application so output is '1'.

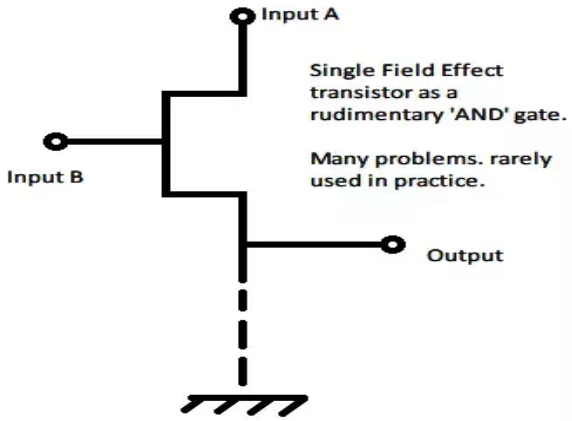

Fig.4 AND Gate Implementation Using Single MOSFET

b) 3-TRANSISTOR XOR GATE

3-transistor XOR gate as shown in Fig.5 using in this 8T full adder circuit. This a combination of CMOS inverter & one pass transistor. By using this full adder circuit we can minimize the delay of circuit & power dissipation .The XOR [14] gate is constructed using a CMOS inverter and a pass transistor when input B='1' the output of XOR gate is inversion to input A. Another condition when B='0' CMOS inverter output goes to high. The pass transistor is turned ON, output is same as the input A .Which works as XOR gate, when A=logic-1 and B=logic-0. Both the transistor PMOS-2 & NMOS trying to switched ON because of the W/L ratio PMOS-2 threshold voltage is minimum comparative NMOS that the reason PMOS-2 is conducted first & the output is same as the A input.

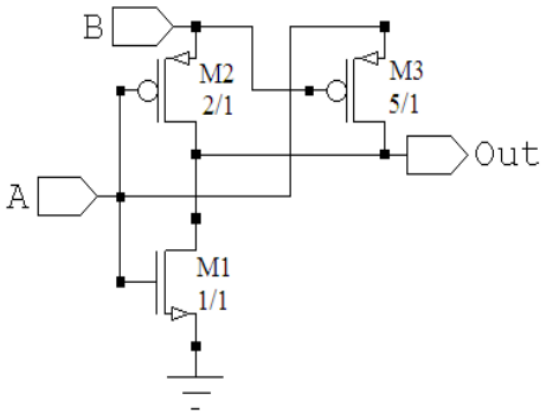

Fig.5 XOR Gate Using 3 Transistor

Table1. 3T-XOR Gate Truth Table

A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

c) 2-Transistor MUX design

Let us see 2 input lines having signals as X and Y for selecting one of the 2 inputs signals .We require addresses which can be a one bit word and the address line are designated as C.

Table 2. Truth Table for 2×1 Multiplexer

C	Z
0	X
1	Y

This truth table can be expressed by the following Boolean expression.

Output = C' X + C Y

Multiplexer circuit also works as select line C. When C='0' the PMOS transistor is activated and it produces X input at output terminal. When C='1' NMOS transistor is activated and it produces Y input

at output terminal. NMOS W/L ratio is 1/1 and PMOS W/L ratio 2/1. MUX output is satisfied full adder carry output. 2×1 Multiplexer shown in Fig.6.

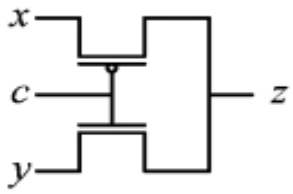

Fig.6 2×1 Multiplexer

d) Full adder design using 2-XOR and 1-MUX

The full adder [12] as shown in Fig.7 is constructed using 2-XOR gates and 1-MUX. The output of first XOR gate becomes the selection lines for MUX and A and Cin are given as inputs for second XOR gate and the output sum is produced based on the selection line given by MUX.

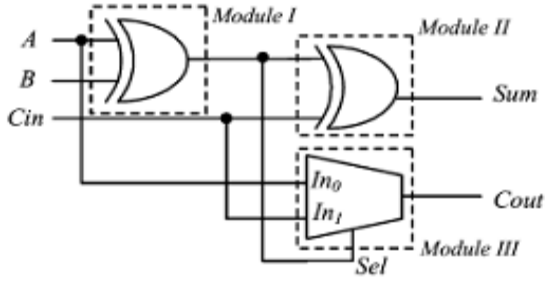

Fig.7 Full Adder Using 2-XOR and 1-MUX

I. 8 Transistors Full Adder

The combination of first 3 transistors becomes an XOR gate[7,8] and the combination of second 3 transistors becomes an another XOR gate which is driven by previous XOR gate output. Now the output of second XOR gate is connected to a 2-transistor combinational circuit which forms a multiplexer. The dimensions of the transistors PM_0,PM_1 are constructed to W/L ratio equal to 2u:1u and PM_2,PM_4 W/L = 5u:1u and NM_0,NM_1,NM_2,PM_3 W/L=1u:1u. The whole circuit works as a1-Bit full adder [17] which is constructed using 8 transistors [8] as shown in Fig.8.

When cin is low problem of threshold loss occurs at second XOR gate as NOMS (NM_1) turns ON. So that current is shorted to ground and due to this attenuation takes place at output. When the first XOR gate becomes high the NMOS transistor (NM_2) turns ON and due to threshold loss [9] complete output cannot be obtained.

For example when we take input "011" the first XOR gate become ON. So that NMOS transistor NM_2 gets activated and due to this complete output will not be produced as we discussed in earlier section.

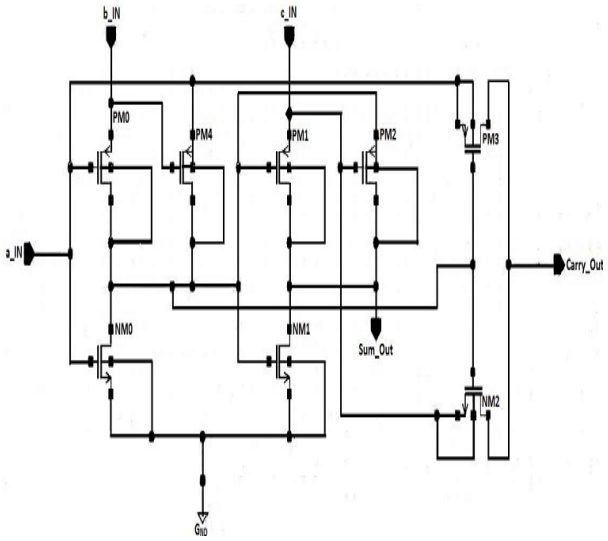

Fig.8 Schematic of 8T 1-Bit full adder

II. 9 Transistors Full Adder

A problem of threshold loss [4] as mentioned earlier in case of 8T adder has been eliminated by the approach as proposed in [5]. Fig. 9 represents the circuit of adder using 9 transistors. An additional N-channel metal-oxide semiconductor (NMOS) transistor (NM1) has been added in the 8T [6] design to achieve full swing at the output. With the input combinations of ABC (i.e. Input Vector) = "000", "010" and "110",two transistors turn on simultaneously in 8T based full adder. Thus, a

combined parallel resistance effect reduces the output voltage as discussed earlier. With the insertion of an additional transistor (NM1 in Fig.9), this problem has been removed. Now for these input combinations, it gives a complete 1 at the first stage of XOR gate, giving a complete 0 for carry input c_IN=0. Thus, the problem for full swing at the output gets eliminated.

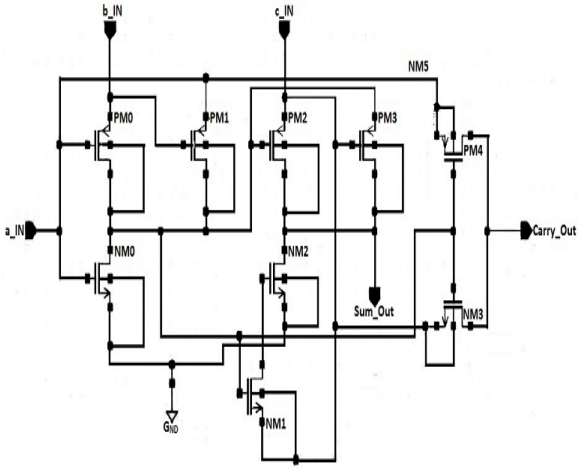

Fig.9 Schematic of 9T 1-Bit full adder

In 9-Transistor 1-Bit full adder similarly as 8-Transistor when we take input "011" the first XOR gate become ON. So that NMOS transistor NM_3 gets activated and due to this complete output will not be produced as we discussed in earlier section.

III. 8T 1-Bit Full Adder with Capacitor

The 1-Bit full adder [1,2] constructed using 9-Transistor[3,5,9] in which the NMOS (NM_1) is replaced by a capacitor in the order of few pf value in order to produce full output swing and to reduce the fabrication process. The dimensions of transistors using 8T 1-bit full adder with capacitor are PM_0,PM_2 ratios are W/L=2u:1u,PM_1,PM_3 ratios are W/L=5u:1u,NM_0,NM_1,NM_2,PM_4 ratios are W/L=1u:1u as shown in Fig.10.

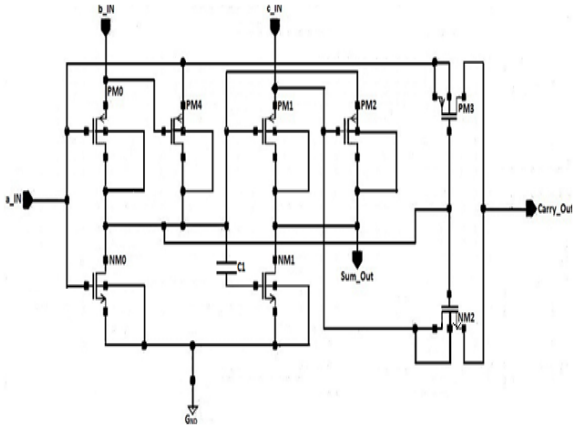

Fig.10 8-Transistor with Capacitor 1-Bit Full Adder

OUTPUT WAVEFORM :

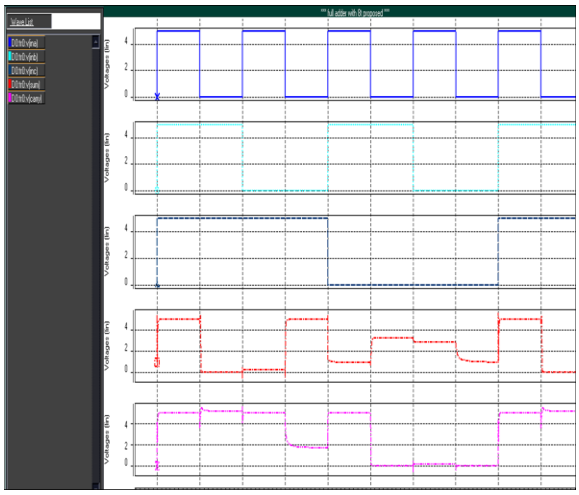

Fig.11 Input and output waveforms of 8-T 1-bit Full Adder with Capacitor

III. PROPOSED DESIGN

a) 2-BIT COMPARATOR USING FULL ADDERS:

In digital systems Comparator is basic and useful arithmetic component. The comparison between the pair of input signals is done and output is produced according to the requirement.

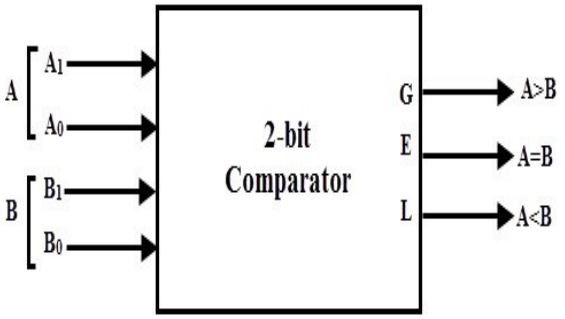

Fig.12 2-Bit Comparator

The comparison between 2-Bits $A_{0,}A_1$ and $B_{0,}B_1$ is done by using 2-Bit Magnitude Comparator [11]. The comparison of A0,A1 with B0,B1 binary bit's. To produce the output binary bit's as A>B,A=B and A<B. The truth table combination is shown in Table-1.

b) COMPARISONS AND CALCULATIONS:

COMPARISONS:

Table 3. Truth Table of 2-Bit Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

CALCULATIONS:

Boolean equations derived from k-map by using truth table

$A>B = A_1B_1'+A_0B_0'A_1'B_1'+A_0B_0'A_1B_1$

$= A_1B_1'+[A_1'B_1'+A_1B_1]A_0B_0'$

$= A_1B_1'+X_1A_0B_0'$.....

.....Assume $A_1'B_1'+A_1B_1 = X_1$

$A=B = A_1'A_0'B_1'B_0'+A_1'A_0B_1'B_0+A_1A_0'B_{10}' + A_{-1}A_0B_1B_0$

$= [A_1'B_1'+A_1B_1]\ [A_0'B_0'+A_0B_0]$

$=X_1X_0$.....

..... Assume $X_0 = A_0'B_0'+A_0B_0$

$A<B = A_1'B_1+A_0'B_0A_1'B_1'+A_0'B_0A_1B_1$

$= A_1'B_1+A_0'B_0[A_1'B_1'+A_1B_1]$

$= A_1'B_1+A_0'B_0X_1$

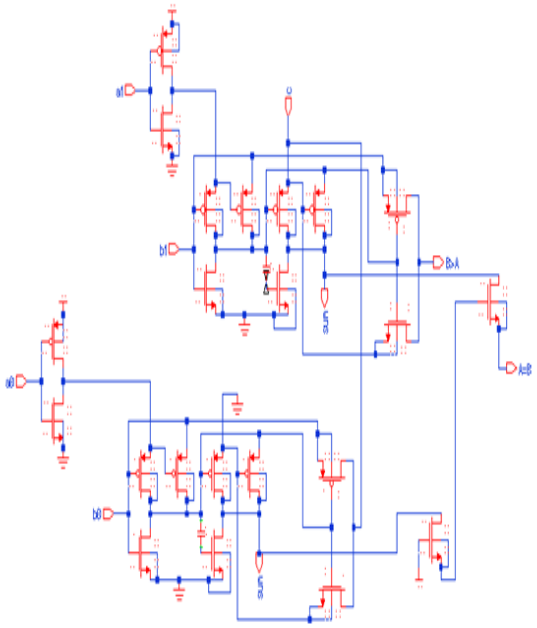

Fig.13 Schematic for 2-bit comparator by using 8T with capacitor 1-bit full adder

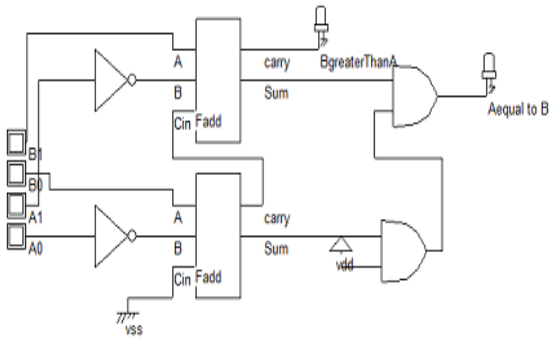

Fig.14 2-Bit Comparator Using 1-Bit Full Adder

The 2-Bit comparator is constructed using 2-full adders [10], 2-inverters and 2-AND gates as shown in Fig.14. There are three outputs. One shows A=B and another shows B>A.

By using 8-transistor with capacitor 1-bit full adder's are used to reduce the total no of transistors compare to conventional CMOS [13]. Here using NOT-gate as conventional CMOS logic [15,16] and here by using 1-transistor AND gate is implemented based on 3-T XOR gate. This AND gate is constructed using N-channel MOS transistor. Still if we need to produce the output A>B then we need to XNOR both A=B and B>A inputs.

c) ADVANTAGES :

i. No of transistor count decrease

ii. Circuit complexity decreases

IV. RESULTS

a) SIMULATION WAVEFORM

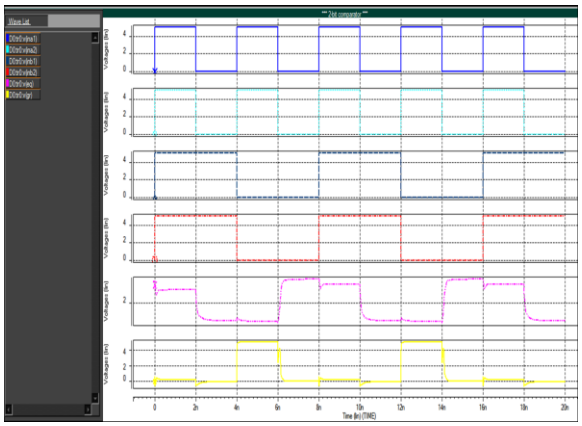

Fig.15 2-Bit Comparator Output Waveform

b) PARAMETERS:

Power Dissipation = 691.7142pwatts

Total Delay = 6.1236E-09

Avg Power Consumption = 1.1875E-01

Number of Transistor = 22

V. CONCLUSION

In proposed design 2-bit comparator implementation by using full adder design style. Here 2-T MUX, two 3-T XOR are used to implement 8-T 1-Bit full adder with capacitor. Here we chosen capacitor as 10 pF . So that the power consumption, delay ,number of transistor count and circuit complexity decreases. By using 8-T 1-Bit full adder and 1-Bit AND gate in 2-Bit comparator the beneficial parameters are listed above.

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