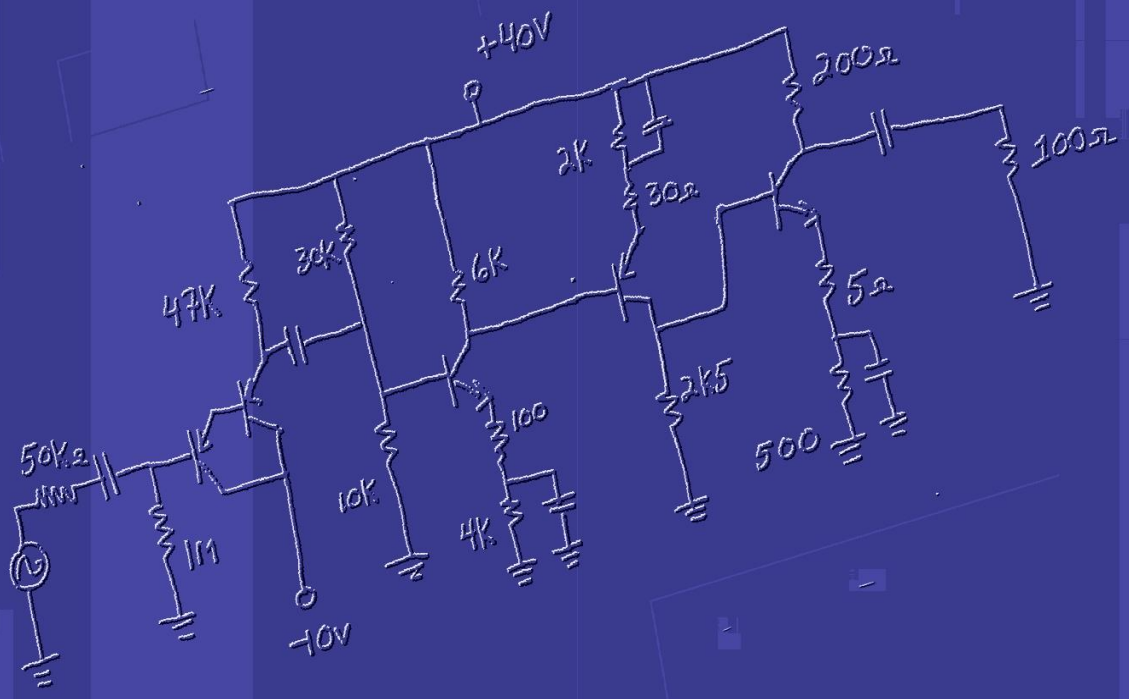
Linear Electronics

Laboratory Manual



James M. Fiore

Laboratory Manual

for

Linear Electronics

by

James M. Fiore

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Cover art by the author

Introduction

This manual is intended for use in a linear semiconductor devices course and is appropriate for two and four year electrical engineering technology curriculums. The manual contains sufficient exercises for a typical 15 week course using a two to three hour practicum period. The topics cover basic diodes through DC biasing and AC analysis of small signal bipolar and FET amplifiers along with class A and B large signal analysis. For equipment, each lab station should include a dual adjustable DC power supply, a dual trace oscilloscope, a function generator and a quality DMM. Some exercises also make use of a distortion analyzer and a low distortion generator (generally, THD below 0.01%), although these portions may be bypassed. For components, a selection of standard value ¼ watt carbon film resistors ranging from a few ohms to a few megohms is required along with an array of typical capacitor values (film types recommended below 1 µF and aluminum electrolytics above). A decade resistance box and a 10 kΩ potentiometer may also be useful. Active devices include small signal diodes such as the 1N914 or 1N4148, the NZX5V1B or 1N751 zener, standard single LEDs, 2N3904 or 2N2222 NPN transistor, 2N3906 PNP transistor, and MPF102 N channel JFET.

Each exercise begins with an Objective and a Theory Overview. The Equipment List follows with space provided for serial numbers and measured values of components. Schematics are presented next along with the step-by-step procedure. Many exercises include sections on troubleshooting and design. Simulations with Multisim are often presented as well, although any quality simulation package such as PSpice can be used instead. All data tables are grouped together, typically with columns for the theoretical and experimental results, along with a column for the percent deviations between them. Finally, a group of appropriate questions are presented.

Other manuals in this series include DC and AC Electrical Circuits, Computer Programming with Python, and Embedded Controllers Using C and Arduino.

A Note from the Author

This manual is used at Mohawk Valley Community College in Utica, NY, for our ABET accredited AAS program in Electrical Engineering Technology. It was created out of a desire to offer an affordable lab manual for our students which covered the requisite material and made optimal use of our laboratory facilities. I am indebted to my students, co-workers and the MVCC family for their support and encouragement of this project. While it would have been possible to seek a traditional publisher for this work, as a long-time supporter and contributor to freeware and shareware computer software, I have decided instead to release this using a Creative Commons non-commercial, share-alike license. I encourage others to make use of this manual for their own work and to build upon it. If you do add to this effort, I would appreciate a notification.

"It doesn't matter how beautiful your theory is, it doesn't matter how smart you are. If it doesn't agree with experiment, it's wrong."

- Richard Feynman

Table of Contents

1

Diode Curves

Objective

The objective of this exercise is to examine the operation of the basic switching diode and to plot its characteristic curve.

Theory Overview

The basic diode is an asymmetric non-linear device. That is, its current-voltage characteristic is not a straight line and it is sensitive to the polarity of an applied voltage or current. When placed in forward bias (i.e. positive polarity from anode to cathode), the diode will behave much like a shorted switch and allow current flow. When reversed biased the diode will behave much like an open switch, allowing little current flow. Unlike switch, a silicon diode will exhibit an approximate .7 volt drop when forward biased. The precise voltage value will depend on the semiconductor material used. This volt drop is sometimes referred to as the *knee voltage* as the resulting I-V curve looks something like a bent knee.

The effective instantaneous resistance of the diode above the turn-on threshold is very small, perhaps a few ohms or less, and is often ignored. Analysis of diode circuits typically proceeds by determining if the diode is forward or reversed biased, substituting the appropriate approximation for the device, and then solving for desired circuit parameters using typical analysis techniques. For example, when forward biased, a silicon diode can be thought of as a fixed .7 volt drop, and then KVL and KCL can be applied as needed.

Equipment

(1) Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(2) Signal diodes (1N4148, 1N914)	
(1) 1 k Ω resistor ¼ watt	actual: _____
(1) 10 k Ω resistor ¼ watt	actual: _____
(1) 4.7 k Ω resistor ¼ watt	actual: _____

1N4148 Datasheet: http://www.fairchildsemi.com/ds/1N/1N4148.pdf

1N914 Datasheet: http://www.fairchildsemi.com/ds/1N/1N914.pdf

Schematics

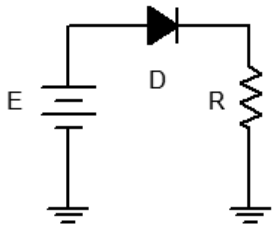

Figure 1.1

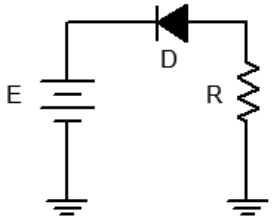

Figure 1.2

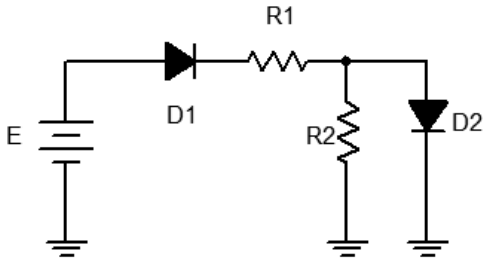

Figure 1.3

Procedure

Forward Curve

1. Consider the circuit of Figure 1.1 using R = 1 kΩ. For any positive value of E, the diode should be forward biased. Once E exceeds the knee voltage, all of E (minus approximately .7 volts) drops across R. Thus, as E increases, so does the diode current.

2. Build the circuit of Figure 1.1 using R = 1 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 1.1. Repeat this process for the remaining source voltages listed.

3. From the data collected in Table 1.1, plot the current versus voltage characteristic of the forward biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

Reverse Curve

4. Consider the circuit of Figure 1.2 using R = 1 kΩ. For any positive value of E, the diode should be reversed biased. In this case, the diode should always behave like an open switch and thus no current should flow. If no current flows, the voltage across R should be zero, and thus the diode voltage should be equal to the applied source voltage. Note that the diode's voltage polarity is negative with respect to that of Figure 1.1.

5. Build the circuit of Figure 1.2 using R = 1 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 1.2. Repeat this process for the remaining source voltages listed.

6. From the data collected in Table 1.2, plot the current versus voltage characteristic of the reverse biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

Practical Analysis

7. Consider the circuit of Figure 1.3 using E = 12 volts, R1 = 10 kΩ and R2 = 4.7 kΩ. Analyze the circuit using the ideal .7 volt forward drop approximation and determine the voltages across the two resistors. Record the results in the first two columns of the first row (Variation 1) of Table 1.3.

8. Build the circuit of Figure 1.3 using E = 12 volts, R1 = 10 kΩ and R2 = 4.7 kΩ. Measure the voltages across the two resistors. Record the results in columns three and four of the first row (Variation 1) of Table 1.3. Also compute and record the percent deviations in columns four and five.

9. Reverse the direction of D1 and repeat steps 7 and 8 as Variation 2 in Table 1.3.

10. Return D1 to the original orientation and reverse the direction of D2. Repeat steps 7 and 8 as Variation 3 in Table 1.3.

11. Reverse the direction of both D1 and D2, and repeat steps 7 and 8 as Variation 4 in Table 1.3.

Multisim

12. Repeat steps 7 through 11 using Multisim, recording the results in Table 1.4.

Data Tables

E (volts)	V_D	I_D
0		
.5		
1		
2		
4		
6		
8		
10		

Table 1.1

E (volts)	V_D	I_D
0		
1		
2		
5		
10		
15		

Table 1.2

Variation	$V_{R1\ Theory}$	$V_{R2\ Theory}$	$V_{R1\ Exp}$	$V_{R2\ Exp}$	% Dev V_{R1}	% Dev V_{R2}
1						
2						
3						
4						

Table 1.3

Variation	$V_{R1\ Multisim}$	$V_{R2\ Multisim}$
1		
2		
3		
4		

Table 1.4

Questions

1. Is .7 volts a reasonable approximation for a forward bias potential? Is an open circuit a reasonable approximation for a reverse biased diode? Support your arguments with experimental data.

2. The "average" resistance of a forward biased diode can be computed by simply dividing the diode's voltage by its current. Using Table 1.1, determine the smallest average diode resistance (show work).

3. The instantaneous resistance (also known as AC resistance) of a diode may be approximated by taking the differences between adjacent current-voltage readings. That is, $r_{diode} = \Delta V_{diode}/\Delta I_{diode}$. What are the smallest and largest resistances using Table 1.1 (show work)? Based on this, what would a plot of instantaneous diode resistance versus diode current look like?

4. If the circuit of Figure 1.3 had been constructed with LEDs in place of switching diodes, would there be any changes to the values measured in Table 1.3? Why/why not?

2

The Zener Diode

Objective

The objective of this exercise is to examine the operation of the zener diode and to plot its characteristic curve.

Theory Overview

When forward biased, the zener diode behaves similarly to an ordinary switching diode, that is, it incurs a .7 volt drop for silicon devices. Unlike a switching diode, the zener is normally placed in reverse bias. If the circuit potential is high enough, the zener will exhibit a fixed voltage drop. This is called the zener potential or V_Z. Manufacturer's specify this voltage with respect to the zener test current, or $I_{ZT;}$ a point past the knee of the voltage-current curve. That is, if the zener's current is at least equal to I_{ZT}, then its voltage is approximately equal to the rated V_Z. Above this current, even very large increases in current will produce only very modest changes in voltage. Therefore, for basic circuit analysis, the zener can be replaced mathematically by a fixed voltage source equal to V_Z.

Equipment

(1) Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(1) Zener diode around 5.1 volts (NZX5V1B, 1N751)
(1) 2.2 k Ω resistor ¼ watt actual: _____
(1) 4.7 k Ω resistor ¼ watt actual: _____

NZX5V1B Datasheet: http://www.nxp.com/documents/data_sheet/NZX_SER.pdf
1N751 Datasheet: http://www.fairchildsemi.com/ds/1N/1N751A.pdf

Schematics

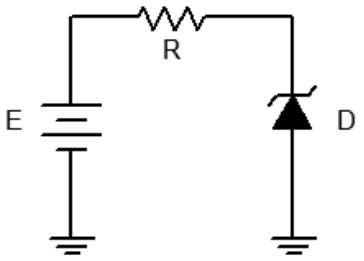

Figure 2.1

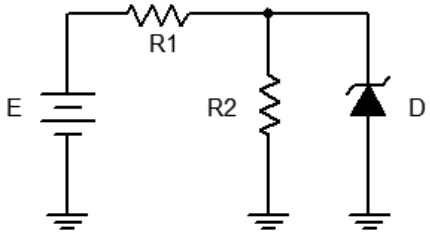

Figure 2.2

Procedure

Forward Curve

1. Consider the circuit of Figure 2.1 using R = 2.2 kΩ. For any positive value of E the zener is reverse biased. Until the zener potential is reached, the diode resistance is effectively infinite and thus no current flows. In this case the voltage across R is zero due to Ohm's Law. Consequently, all of E should appear across the zener. Once the source exceeds the zener voltage, the remainder of E (i.e. E minus the zener potential) drops across R. Thus, as E increases, the circulating current increases but the voltage across the zener remains steady.

2. Build the circuit of Figure 2.1 using R = 2.2 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 2.1. Repeat this process for the remaining source voltages listed.

3. From the data collected in Table 2.1, plot the current versus voltage characteristic of the forward biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

Practical Analysis

4. Consider the circuit of Figure 2.2 using R1 = 2.2 kΩ and R2 = 4.7 kΩ. In general, to analyze circuits like this, first assume that the zener is out of the circuit and then compute the voltage across R2 using the voltage divider rule. If the resulting voltage is less than the zener potential then the zener is

inactive (high resistance) and does not affect the circuit. If, on the other hand, the resulting voltage is greater than the zener potential then the zener is active and will limit the voltage across R2 to V_Z. Via KVL, the remainder of the voltage drops across R1 and from this the supply current may be determined. This current will then split between R2 and the zener. The R2 current is found using Ohm's Law. The zener current is then found via KCL. Note that for higher and higher values of E, the voltage across (and therefore the current through) R2 does not change. Instead, all of the "excess" current from the source passes through the zener.

5. Build the circuit of Figure 2.2 using R1 = 2.2 kΩ and R2 = 4.7 kΩ. Set E to 2 volts. Compute the theoretical diode voltage and current, and record them in the first row of Table 2.2. Then measure the diode current and voltage and record in Table 2.2. Finally, compute and record the deviations.

6. Repeat step 5 for the remaining source voltages in Table 2.2.

Multisim

7. Repeat steps 5 and 6 using Multisim, recording the results in Table 2.3.

Data Tables

E (volts)	V_D	I_D
0		
1		
2		
5		
10		
15		
20		

Table 2.1

E (volts)	$V_{D\ Theory}$	$I_{D\ Theory}$	$V_{D\ Exp}$	$I_{D\ Exp}$	% Dev V_D	% Dev I_D
2						
5						
10						
15						
20						

Table 2.2

E (volts)	$V_{D\ Multsim}$	$I_{D\ Multisim}$
2		
5		
10		
15		
20		

Table 2.3

Questions

1. Is it safe to assume that the voltage across a zener is always equal to the rated V_Z? Why/why not?

2. The instantaneous resistance (also known as AC resistance) of a diode may be approximated by taking the differences between adjacent current-voltage readings. That is, $r_{diode} = \Delta V_{diode}/\Delta I_{diode}$. What is the smallest effective resistance of the zener using Table 2.1 (show work)?

3. If the circuit of Figure 2.1 had been constructed with the zener reversed, how would this effect the results recorded in Table 2.1?

4. Assume that a diode with a much higher I_{ZT} rating (say, 100 mA) was used in this exercise. In general, what would the likely outcome be for the circuit of Figure 2.2?

3

Base Bias: CE Configuration

Objective

The objective of this exercise is to explore the operation of a basic common emitter biasing configuration for bipolar junction transistors, namely fixed base bias. Along with the general operation of the transistor and the circuit itself, circuit stability with changes in beta is also examined.

Theory Overview

For a bipolar junction transistor to operate properly, the base-emitter junction must be forward biased while the collector-base junction must be reverse biased. This will place V_{BE} at approximately .7 volts and the collector current I_C will be equal to the base current I_B times the current gain β. For small signal devices, the current gain is greater than 100 typically. Thus, $I_C >> I_B$ and $I_C \approx I_E$.

The common emitter configuration places the emitter terminal at ground. The base terminal is seen as the input and the collector as the output. Using a fixed base supply, the base current is dependent on the value of the base resistor via Ohm's law. Consequently, any variation in current gain across a batch of transistors will show up as an equivalent variation in collector current, and by extension, a variation in collector-emitter voltage V_{CE}.

Equipment

(1) Dual Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(3) Small signal NPN transistors (2N3904)
(1) 1.2 k Ω resistor ¼ watt actual: _____
(1) 330 k Ω resistor ¼ watt actual: _____

2N3904 Datasheet: http://www.fairchildsemi.com/ds/2N/2N3904.pdf

Schematics

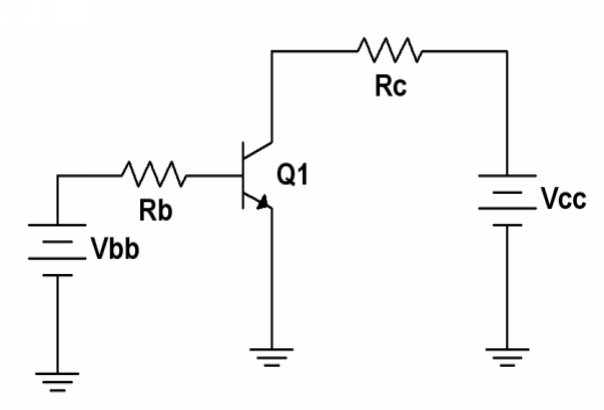

Figure 3.1

Procedure

A Quick Check

1. A quick and easy way to determine if a transistor is damaged is through the use of the resistance (or diode) function of a multimeter. The multimeter will produce a small current in order to determine the connected resistance value. This current is sufficient to partially forward or reverse bias a PN junction. Thus, for an NPN device, placing the red lead on the base and the black lead on the emitter and collector in turn will produce forward bias on the junctions and the meter will show a low resistance. Reversing the leads will create reverse bias and a high resistance will be indicated. If the leads are connected from collector to emitter, one of the two junctions will be reverse biased regardless of lead polarity, and thus, a high resistance is always indicated. Before proceeding to the next step, check the three transistors using this method to ensure that they are functioning. (Note: some multimeters include a "beta checker" function. This may also be used to determine if the devices are good but the beta value produced should not be considered precise as the measurement current and voltage are most likely different from the circuit in which the transistor will be used.)

Base Bias

2. Consider the circuit of Figure 3.1 with Vbb = 11V, Vcc = 15V, Rb = 330 k and Rc = 1.2 k. Assume V_{BE} = .7 volts. Further, assume that beta is 150 (a typical value for this device in this application). Calculate the expected values of I_B, I_C and I_E, and record them in the "Theory" columns of Table 3.1. Note that the theoretical values will be the same for all three transistors.

3. Based on the expected value of I_C, determine the theoretical value of V_{CE} and record it in Table 3.2. Also, fill in Table 3.2 with the typical (theoretical) beta value of 150.

4. Build the circuit of Figure 3.1 with Vbb = 11V, Vcc = 15V, Rb = 330 k and Rc = 1.2 k. Measure and record the base, collector and emitter currents, and record them in the first row of Table 3.1. Determine the deviations between the theoretical and experimental currents, and record these in Table 3.1.

5. Measure the base-emitter and collector-emitter voltages and record in the first row of Table 3.2. Based on the measured values of base and collector current from Table 3.1, calculate and record the experimental betas in Table 3.2. Finally, compute and record the deviations for the voltages and for the current gain in Table 3.2.

6. Remove the first transistor and replace it with the second unit. Repeat steps four and five using the second row of Tables 3.1 and 3.2.

7. Remove the second transistor and replace it with the third unit. Repeat steps four and five using the third row of Tables 3.1 and 3.2.

Design

8. One way of improving the circuit of Figure 3.1 is to redesign it so that a single power supply may be used. As noted previously, the base current is largely dependent on the value of V_{BB} and R_B. If the supply is changed, the resistance can be changed by a similar factor in order to keep the base current constant. This is just an application of Ohm's law. Based on this, determine a new value for R_B that will produce the original I_B if V_{BB} is increased to the V_{CC} value (i.e., a single power supply is used). Record this value in Table 3.3.

9. Rewire the circuit so that the original R_B is replaced by the new calculated value (the nearest standard value will suffice). Also, the V_{BB} supply should be removed and the left side of R_B connected to the V_{CC} supply. Measure the new base current and record it in Table 3.3. Also determine and record the deviation between the measured and target base current values.

Multisim

10. Build the original circuit in Multisim. Run a single simulation and record the I_B, I_C, I_E and V_{CE} values in Table 3.4.

Data Tables

Transistor	$I_{B\ Theory}$	$I_{B\ Exp}$	%D I_B	$I_{C\ Theory}$	$I_{C\ Exp}$	%D I_C	$I_{E\ Theory}$	$I_{E\ Exp}$	%D I_E
1									
2									
3									

Table 3.1

Transistor	$V_{BE\ Thry}$	$V_{BE\ Exp}$	%D V_{BE}	$V_{CE\ Thry}$	$V_{CE\ Exp}$	%D V_{CE}	$\beta_{\ Theory}$	$\beta_{\ Exp}$	%D β
1									
2									
3									

Table 3.2

Calculated R_B	Actual R_B Used	I_B Measured	% Deviation I_B

Table 3.3

$I_{B\ Multisim}$	$I_{C\ Multisim}$	$I_{E\ Multisim}$	$V_{CE\ Multisim}$

Table 3.4

Questions

1. Are the basic transistor parameters borne out in this exercise? That is, are the approximations of V_{BE}=.7 and I_C=I_E valid?

2. Is the typical beta value of 150 highly accurate and repeatable?

3. Which circuit parameters are affected by beta changes? Which parameters appear to be immune to changes in beta?

4. Comparing Tables 3.1 and 3.2, is there a notable pattern between the deviations for beta and collector current? Why/why not?

5. In the circuit of Figure 3.1, what must R_B be set to if V_{BB} = 5V and the desired base current is 10 µA?

4

LED Driver Circuits

Objective

The objective of this exercise is to examine two methods of driving LEDs with a constant current. Method one involves a saturating switch while method two utilizes a non-saturating circuit.

Theory Overview

LEDs behave similarly to switching diodes in that they conduct current easily in forward bias and appear as an approximate open circuit when reverse biased. Unlike standard silicon switching diodes, however, the forward bias potential is *not* approximately .7 volts. Instead, this potential will vary depending on the design of the LED but typically will be in the neighborhood of 2 volts for everyday devices. The brightness of the LED is directly controlled by its current: the higher the current, the brighter the LED. Consequently, it is important to drive LEDs with constant current sources to ensure consistent brightness.

Many circuits cannot drive LEDs directly so an intervening circuit is used (a *driver*) to boost the current up to the value the LED requires for a given brightness. The driving signal is attached to the base while the LED is situated in the collector, thus the transistor's current gain, beta, is exploited. Unfortunately, beta is not a particularly stable and consistent parameter so methods are required to alleviate this shortcoming. A saturating switch works by operating at the extreme ends of the DC load line; that is, either cutoff or saturation. If no signal is applied to the base, both base and collector currents will be zero, and thus, the LED is off. When a base signal is applied, it is designed to be large enough to force the transistor into saturation even with very modest betas. Therefore, the LED will always see the saturation current, regardless of the normal beta value. In contrast, the non-saturating circuit works by placing a resistor in the emitter. This establishes a constant emitter current (and thus, constant collector and LED current) in spite of beta changes. That is, if beta changes, the effect is seen in the base current, not the collector current. The non-saturating circuit has the advantage of using one less resistor, however, the saturating switch has the greater advantage of using the same collector and base voltages (the non-saturating circuit requires a collector source potential at least a few volts greater than the base voltage).

Equipment

(1) Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(3) Small signal transistors (2N3904)
(1) LED
(1) 220 Ω resistor ¼ watt actual: _____
(1) 470 Ω resistor ¼ watt actual: _____

(1) 4.7 k Ω resistor ¼ watt actual: _____

Schematics

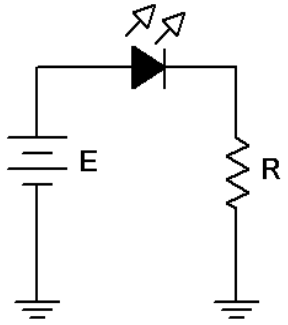

Figure 4.1

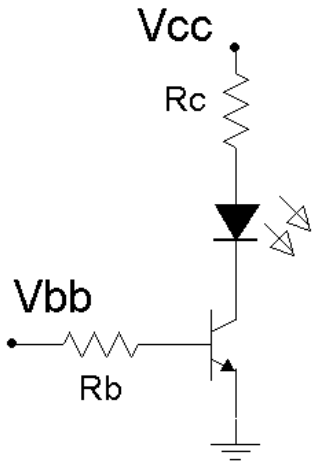

Figure 4.2

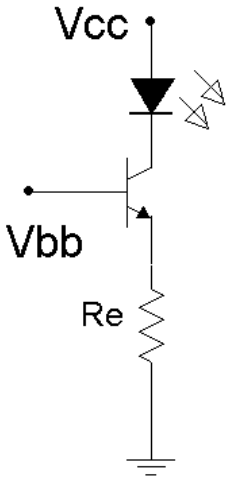

Figure 4.3

Procedure

Determining V_{LED}

1. The forward potential of an LED depends on its design and the current flowing through it. The other two circuits in this exercise are designed to produce LED currents of approximately 10 mA so a determination of the forward potential of this particular diode at 10 mA is desired. Assemble the circuit of Figure 4.1 using R = 470 Ω, and E = 5 volts. Insert an ammeter in line with the LED. Increase E until 10 mA is reached (the LED should be reasonably bright). Record the resulting LED voltage in Table 4.1.

Saturating Switch

2. Consider the saturating switch of Figure 4.2 using Vcc = Vbb = 5 volts, Rb = 4.7 k and Rc = 220. Calculate the base and collector currents and record them in the first row of Table 4.2 (theory). As the circuit is in saturation, the theoretical V_{CE} is close to zero and may be found on the transistor data sheet via the V_{CE}/I_C saturation graph. Record this value in the first row of Table 4.2 as well.

3. Build the saturating switch of Figure 4.2 using Vcc = Vbb = 5 volts, Rb = 4.7 k and Rc = 220. Measure and record the base and collector currents, and record the collector-emitter voltage in the first row of Table 4.2 (experimental). Also compute and record the deviations between theory and experimental results.

4. Remove the base resistor from Vbb and connect it to ground. Without a base source potential, the circuit will be in cutoff. Determine the theoretical base and collector currents along with the collector-emitter voltage and record them in the second row of Table 4.2. Measure these parameters, record them in Table 4.2, and also compute and record the resulting deviations.

5. Reconnect the base resistor to the Vbb supply and swap in the second transistor. Repeat steps 3 and 4 using the next two rows of Table 4.2.

6. Reconnect the base resistor to the Vbb supply and swap in the third transistor. Repeat steps 3 and 4 using the final two rows of Table 4.2.

Non-saturating Current Source

7. Consider the non-saturating current source of Figure 4.3 using Vcc = 10 volts, Vbb = 5 volts and Re = 470. Using a typical beta of 150, calculate the base and collector currents, and the collector-emitter voltage and record them in the first row of Table 4.3 (theory).

8. Build the non-saturating current source of Figure 4.3 using Vcc = 10 volts, Vbb = 5 volts and Re = 470. Measure and record the base and collector currents, and record the collector-emitter voltage in the first row of Table 4.3 (experimental). Also compute and record the deviations between theory and experimental results.

9. Remove the base resistor from Vbb and connect it to ground. Without a base source potential, the base current will be zero. Determine the theoretical base and collector currents along with the collector-emitter voltage and record them in the second row of Table 4.3. Measure these parameters, record them in Table 4.3, and also compute and record the resulting deviations.

10. Reconnect the base resistor to the Vbb supply and swap in the second transistor. Repeat steps 8 and 9 using the next two rows of Table 4.3.

11. Reconnect the base resistor to the Vbb supply and swap in the third transistor. Repeat steps 8 and 9 using the final two rows of Table 4.3.

Design

12. As seen in steps 7 through 11, the LED current of Figure 4.3 is a function of the base supply and the emitter resistor. Determine a new value for the emitter resistance that will yield an LED current of 15 mA. Record this value in Table 4.4. Obtain a new resistor close in value to the calculated result and swap it into the circuit. Measure the resulting LED current and record in Table 4.4.

Multisim

13. Simulate the circuit of Figure 4.2 and record the currents and voltage in Table 4.5.

14. Simulate the circuit of Figure 4.3 and record the currents and voltage in Table 4.6.

Data Tables

V_{LED}	

Table 4.1

Vbb	$I_{B\ Theory}$	$I_{C\ Theory}$	$V_{CE\ Theory}$	$I_{B\ Exp}$	$I_{C\ Exp}$	$V_{CE\ Exp}$	% D I_B	% D I_C	% D V_{CE}
5									
0									
5									
0									
5									
0									

Table 4.2

Vbb	$I_{B\ Theory}$	$I_{C\ Theory}$	$V_{CE\ Theory}$	$I_{B\ Exp}$	$I_{C\ Exp}$	$V_{CE\ Exp}$	% D I_B	% D I_C	% D V_{CE}
5									
0									
5									
0									
5									
0									

Table 4.3

Vbb	$R_{E\ Theory}$	$R_{E\ exp}$	$I_{C\ exp}$
5			

Table 4.4

Vbb	$I_{B\ Multisim}$	$I_{C\ Multisim}$	$V_{CE\ Multisim}$
5			
0			

Table 4.5

Vbb	$I_{B\ Multisim}$	$I_{C\ Multisim}$	$V_{CE\ Multisim}$
5			
0			

Table 4.6

Questions

1. Do the two driver circuits produce a stable and predictable LED current in spite of changes in beta?

2. The circuit of Figure 4.2 is stated to be a saturating switch. How do the data of Table 4.2 confirm this statement?

3. The circuit of Figure 4.3 is stated to be a non-saturating current source. How do the data of Table 4.3 confirm this statement?

5

Voltage Divider Bias

Objective

The objective of this exercise is to examine the voltage divider bias topology and determine whether or not it produces a stable Q point. Various potential troubleshooting issues are also explored.

Theory Overview

One of the problems with simpler biasing schemes such as the base bias is that the Q point (I_C and V_{CE}) will fluctuate with changes in beta. This will result in inconsistent circuit performance. A possible solution is to attempt to place a fixed voltage across an emitter resistor. This will result in a stable emitter current, and by extension, stable collector current and collector-emitter voltage. As beta varies, this change will be reflected in a change in base current. With proper design, this change in base current will have little overall impact on circuit performance. One method of obtaining a stable voltage across the emitter resistor is to apply a stiff voltage divider to the base. "Stiff", in this case, means that the current through the divider resistors should be much higher than the current tapped off of the divider (the current being tapped off is the base current). By doing so, variations in base current will not excessively load the divider and this will lead to a very stable base voltage. The emitter voltage is one base-emitter drop less, and is the potential across the emitter resistor. Hence, the emitter resistor's voltage will be kept stable.

When troubleshooting, circuit faults often result in either shorted or open components. Typically this will alter the circuit radically and push the Q point into either cutoff or saturation. The fault may also alter the DC load line itself. Once the transistor goes into either cutoff or saturation, normal linear operation will be lost.

Equipment

(1) Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(3) Small signal transistors (2N3904)	
(1) 3.3 k Ω resistor ¼ watt	actual: _____
(1) 4.7 k Ω resistor ¼ watt	actual: _____
(1) 5.6 k Ω resistor ¼ watt	actual: _____
(1) 10 k Ω resistor ¼ watt	actual: _____

Schematic

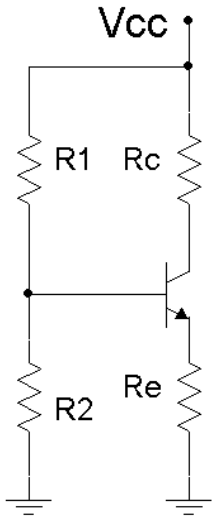

Figure 5.1

Procedure

DC Load Line

1. Consider the circuit of Figure 5.1 using Vcc = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Using the approximation of a lightly loaded "stiff" voltage divider, determine the ideal end points of the DC load line and the Q point, and record these in Table 5.1.

Circuit Voltages and Beta

2. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 5.2 (Theory).

3. Build the circuit of Figure 5.1 using Vcc = 10 volts, R1 = 10 k, R2 = 3.3 k, Re = 4.7 k and Rc = 5.6 k. Measure the base, emitter and collector voltages and record them in the first row of Table 5.2 (Experimental). Compute the deviations between theoretical and experimental and record these in the first row of Table 5.2 (% Deviation).

4. Measure the base and collector currents and record these in the first row of Table 5.3. Based on these, compute and record the experimental beta as well.

5. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

6. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

Design

7. The collector current of the circuit can be altered by a variety of means including changing the emitter resistance. If the base voltage is held constant, the collector current is determined by the emitter resistance via Ohm's Law. Redesign the circuit to achieve half of the quiescent collector current recorded in Table 5.1. Obtain a resistor close to this value, swap out the original emitter resistor and measure the resulting current. Record the appropriate values in Table 5.4.

Troubleshooting

8. Return the original emitter resistor to the circuit. Consider each of the individual faults listed in Table 5.5 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 5.5.

Multisim

9. Build the circuit of Figure 5.1 in Multisim. Run a DC simulation and record the resulting transistor voltages in Table 5.6.

Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 5.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	%D V_B	%D V_E	%D V_C
1									
2									
3									

Table 5.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 5.3

$R_{E\ Theory}$	$R_{E\ Actual}$	$I_{C\ Measured}$

Table 5.4

Issue	V_B	V_E	V_C
R_2 Short			
R_E Open			
R_C Short			
R_C Open			
V_{CE} Short			
V_{CE} Open			

Table 5.5

V_B Multisim	
V_E Multisim	
V_C Multisim	

Table 5.6

Questions

1. Based on the results of Table 5.1, is the transistor operating in saturation, cutoff or in the linear region?

2. Based on the results of Tables 5.2 and 5.3, does the circuit achieve a stable operating point when compared to beta?

3. Based on the measurements of Table 5.5, is it possible for different circuit problems to produce similar or even identical voltages in the circuit, or is every fault unique in its outcome?

4. What is the required design condition for the voltage divider bias to achieve high Q point stability in spite of changes in beta?

5. Using the original circuit, determine a new value for the collector resistance that will yield a collector voltage of approximately half of the power supply value.

6

Emitter Bias

Objective

The objective of this exercise is to examine the two supply emitter bias topology and determine whether or not it produces a stable Q point. Various potential troubleshooting issues are also explored.

Theory Overview

A method of obtaining a stable Q point is to attempt to place a fixed voltage across an emitter resistor. In the Voltage Divider bias this is achieved by applying a stiff voltage divider to the base. Alternately, a negative supply may be attached to the low side of the emitter resistor instead of grounding it. The base is then simply connected back to ground via a single resistor. If this base resistance is relatively small, the base voltage will be close to zero as only the base current flows through it. Consequently, almost all of the negative emitter supply will drop across the emitter resistor, with the exception of the single base-emitter potential. As in the Voltage Divider circuit, this will result in a stable emitter current, and by extension, stable collector current and collector-emitter voltage. As beta varies, this change will be reflected in a change in base current. This can result in large percentage changes in base voltage; however, the magnitude of the base potential will remain small, and thus, inconsequential.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(3) Small signal transistors (2N3904)	
(1) 15 k Ω resistor ¼ watt	actual: _____
(1) 22 k Ω resistor ¼ watt	actual: _____
(1) 33 k Ω resistor ¼ watt	actual: _____

Schematic

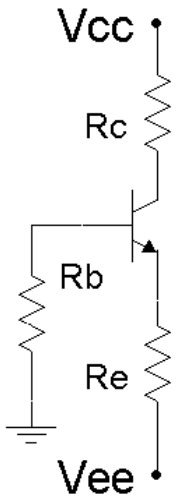

Figure 6.1

Procedure

DC Load Line

1. Consider the circuit of Figure 6.1 using Vcc = 15 volts, Vee = -12 volts, Rb = 33 kΩ, Re = 22 kΩ and Rc = 15 kΩ. Using the approximation of a negligible base voltage, determine the ideal end points of the DC load line and the Q point, and record these in Table 6.1.

Circuit Voltages and Beta

2. Continuing with the component values indicated in step one, compute the theoretical emitter and collector voltages, and record them in Table 6.2 (Theory). For the theoretical base voltage entry, assume a beta of approximately 150 and determine the base current and voltage from the theoretical collector current recorded in the Table 6.1.

3. Build the circuit of Figure 6.1 using Vcc = 15 volts, Vee = -12 volts, Rb = 33 kΩ, Re = 22 kΩ and Rc = 15 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 6.2 (Experimental). Compute the deviations between theoretical and experimental and record these in the first row of Table 6.2 (% Deviation).

4. Measure the base and collector currents and record these in the first row of Table 6.3. Based on these, compute and record the experimental beta as well.

5. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

6. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

Design

7. The collector voltage of the circuit can be altered by a variety of means including changing the collector resistance. If the emitter supply and resistance are held constant, the collector voltage is determined by the collector resistance and the collector supply. Redesign the circuit to achieve a collector voltage of approximately 10 volts. Obtain a resistor close to this value, swap out the original collector resistor and measure the resulting voltage. Record the appropriate values in Table 6.4.

Troubleshooting

8. Return the original collector resistor to the circuit. Consider each of the individual faults listed in Table 6.5 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 6.5.

Multisim

9. Build the circuit of Figure 6.1 in Multisim. Run a DC simulation and record the resulting transistor voltages in Table 6.6.

Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 6.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	%D V_B	%D V_E	%D V_C
1									
2									
3									

Table 6.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 6.3

$R_{C\ Theory}$	$R_{C\ Actual}$	$V_{C\ Measured}$

Table 6.4

Issue	V_B	V_E	V_C
R_B Short			
R_B Open			
R_C Short			
R_C Open			
R_E Open			
V_{CE} Open			

Table 6.5

V_B Multisim	
V_E Multisim	
V_C Multisim	

Table 6.6

Questions

1. Based on the results of Table 6.1, is the transistor operating in saturation, cutoff or in the linear region?

2. Based on the results of Tables 6.2 and 6.3, does the circuit achieve a stable operating point when compared to beta?

3. How does the Emitter Bias circuit compare to Base Bias and Voltage Divider Bias in terms of Q point stability and complexity?

4. Using the original circuit, determine a new value for the emitter resistance that will yield half of the quiescent collector current recorded in Table 6.1.

7

Feedback Biasing

Objective

The objective of this exercise is to examine two kinds of feedback biasing: collector feedback and emitter feedback. Both forms potentially are more stable than simple base bias in terms of the impact of beta on collector current.

Theory Overview

By inserting a resistor in either the emitter or collector portions of the transistor circuit, it is possible to partially control the base current in such a way that an increase in beta will cause a decrease in base current which in turn helps to mitigate the tendency of collector current to increase. This will result in circuits that have greater Q point stability than simple base bias circuits although for certain practical reasons they might not be as stable as voltage divider or dual supply emitter bias schemes.

In the collector feedback arrangement, the base resistor is connected from the collector to the base. Therefore, its voltage is one base-emitter drop less than the collector voltage. The collector voltage, in turn, is simply the supply potential minus the collector resistor's drop. Therefore, as the collector current rises, the collector resistor's drop increases, forcing the collector voltage down and thus reducing the base resistor's voltage. By Ohm's Law, this means that the base current must decrease. This decrease helps to limit the overall increase in collector current.

The emitter feedback situation is similar. In this instance, as collector current increases the drop across the emitter resistor rises. This will result in an increase in base voltage as it is locked to one base-emitter drop above the emitter. Consequently, as the collector current increases, the voltage across the base resistor decreases which helps to compensate for the original increase in collector current.

Equipment

(1) Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(3) Small signal transistors (2N3904)	
(1) 330 Ω resistor ¼ watt	actual: _____
(1) 470 Ω resistor ¼ watt	actual: _____
(1) 1 k Ω resistor ¼ watt	actual: _____
(1) 220 k Ω resistor ¼ watt	actual: _____

Schematics

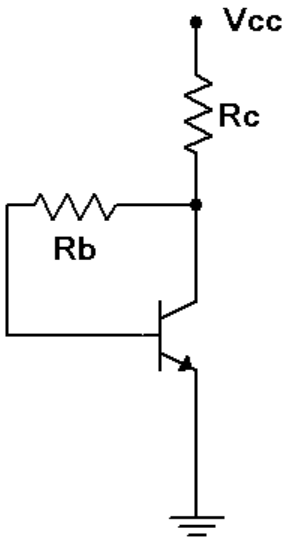

Figure 7.1

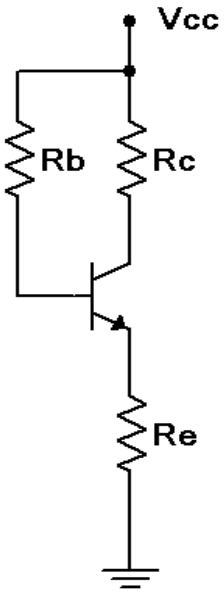

Figure 7.2

Procedure

Collector Feedback - DC Load Line

1. Consider the circuit of Figure 7.1 using Vcc = 12 volts, Rb = 220 kΩ and Rc = 1 kΩ. Determine the ideal end points of the DC load line and the Q point, and record these in Table 7.1.

Circuit Voltages and Beta

2. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 7.2 (Theory).

3. Build the circuit of Figure 7.1 using Vcc = 12 volts, Rb = 220 kΩ and Rc = 1 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 7.2 (Experimental).

4. Measure the base and collector currents and record these in the first row of Table 7.3. Based on these, compute and record the experimental beta as well.

5. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

6. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

Stability

7. Based on the measurements of Table 7.3, determine the maximum percent change of collector current and record in Table 7.4. Also determine the maximum percent change of beta and record in Table 7.4.

Emitter Feedback - DC Load Line

8. Consider the circuit of Figure 7.2 using Vcc = 12 volts, Rb = 220 kΩ, Re = 470 Ω and Rc = 330 Ω. Determine the ideal end points of the DC load line and the Q point, and record these in Table 7.5.

Circuit Voltages and Beta

9. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 7.6 (Theory).

10. Build the circuit of Figure 7.2 using Vcc = 12 volts, Rb = 220 kΩ, Re = 470 Ω and Rc = 330 Ω. Measure the base, emitter and collector voltages and record them in the first row of Table 7.6 (Experimental).

11. Measure the base and collector currents and record these in the first row of Table 7.7. Based on these, compute and record the experimental beta as well.

12. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

13. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

Stability

14. Based on the measurements of Table 7.7, determine the maximum percent change of collector current and record in Table 7.8. Also determine the maximum percent change of beta and record in Table 7.8.

Troubleshooting

15. For the emitter feedback bias circuit, consider each of the individual faults listed in Table 7.9 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 7.9.

Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 7.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 7.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 7.3

% Δ β	
% Δ I_C	

Table 7.4

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 7.5

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 7.6

Transistor	I_B	I_C	β
1			
2			
3			

Table 7.7

% Δ β	
% Δ I_C	

Table 7.8

Issue	V_B	V_E	V_C
R_B Open			
R_E Open			
R_E Short			
R_C Open			
R_C Short			
V_{CE} Open			

Table 7.9

Questions

1. Based on the results of Tables 7.4 and 7.8, do these circuits achieve a stable operating point when compared to beta?

2. Which circuit is more stable in this exercise; the emitter feedback bias or the collector feedback bias? Is it safe to say that this will always be the case for any emitter feedback bias circuit versus any collector feedback bias circuit?

3. Are the transistor voltages always as stable as the collector current or can they be more or less stable?

4. Based on the collector current equation derivations for the two circuits, derive the collector current equation for a combination circuit which consists of a collector feedback bias circuit with an emitter resistor added.

8

PNP Transistors

Objective

The objective of this exercise is to investigate the practical differences between circuits implemented with PNP transistors versus NPN transistors. PNP versiosn of basic biasing and LED driver circuits will be used.

Theory Overview

On a practical level, PNP transistors may be thought of as a mirror image of their NPN counterparts. That is, all of the device's voltage polarities and current directions will be opposite of those found with NPNs. In fact, a simple way to turn an NPN circuit into an equivalent PNP circuit is to swap out the transistor and then flip the polarity of the power supply (or supplies, as the case may be). The resulting circuit will produce essentially the same voltages and currents as the original but with reversed polarities. By no means are negative power supplies a requirement to use PNPs, though. Commonly, the circuit is "flipped top to bottom" and implemented with a positive supply. In this case the emitter will be found toward the top and the collector toward the bottom. In some instances this orientation may also reverse the operational logic of the circuit. For example, the "flipped" PNP LED driver becomes an inverting driver. That is, a logic low will light the LED instead of a logic high.

Equipment

(1) Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(3) Small signal PNP transistors (2N3906)
(1) LED
(1) 220 Ω resistor ¼ watt actual: _____
(1) 3.3 k Ω resistor ¼ watt actual: _____
(1) 4.7 k Ω resistor ¼ watt actual: _____
(1) 5.6 k Ω resistor ¼ watt actual: _____
(1) 10 k Ω resistor ¼ watt actual: _____

2N306 Datasheet: http://www.fairchildsemi.com/ds/2N/2N3906.pdf

Schematics

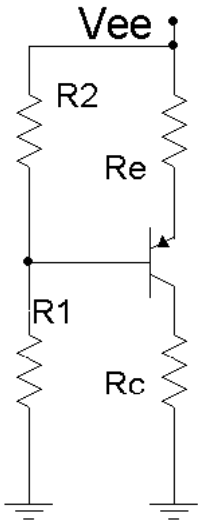

Figure 8.1

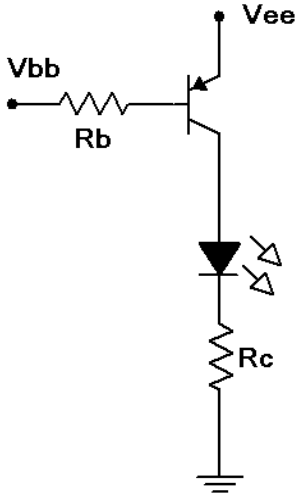

Figure 8.2

Procedure

PNP Voltage Divider

1. Consider the circuit of Figure 8.1 using Vcc = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Using the approximation of a lightly loaded "stiff" voltage divider, determine the theoretical base, emitter and collector voltages, and record them in Table 8.1 (Theory).

2. Build the circuit of Figure 8.1 using Vcc = 10 volts, R1 = 10 k, R2 = 3.3 k, Re = 4.7 k and Rc = 5.6 k. Measure the base, emitter and collector voltages and record them in the first row of Table 8.1 (Experimental).

3. Swap the transistor with the second transistor and repeat steps 1 and 2 using the second row of the table.

4. Swap the transistor with the third transistor and repeat steps 1 and 2 using the third row of the table.

Troubleshooting

5. Consider each of the individual faults listed in Table 8.2 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 8.2.

PNP LED Driver

6. Consider the PNP saturating switch of Figure 8.2 using Vcc = Vbb = 5 volts, Rb = 4.7 k and Rc = 220. Calculate the base and collector currents and record them in the first row of Table 8.3 (Theory). As the circuit is in saturation, the theoretical V_{CE} is close to zero and may be found on the transistor data sheet via the V_{CE}/I_C saturation graph. Record this value in the first row of Table 8.3 as well.

7. Build the saturating switch of Figure 8.2 using Vcc = Vbb = 5 volts, Rb = 4.7 k and Rc = 220. Measure and record the base and collector currents, and record the collector-emitter voltage in the first row of Table 8.3 (Experimental). Also compute and record the deviations between theory and experimental results.

8. Remove the base resistor from Vbb and connect it to ground. Without a base source potential, the circuit will be in cutoff. Determine the theoretical base and collector currents along with the collector-emitter voltage and record them in the second row of Table 8.3. Measure these parameters, record them in Table 8.3, and also compute and record the resulting deviations.

9. Reconnect the base resistor to the Vbb supply and swap in the second transistor. Repeat steps 3 and 4 using the next two rows of Table 8.3.

10. Reconnect the base resistor to the Vbb supply and swap in the third transistor. Repeat steps 3 and 4 using the final two rows of Table 8.3.

Design

11. A simple way to program the LED current in the driver is by altering the collector resistor. First, measure the LED potential while it is lit. Assuming that the collector-emitter saturation voltage is neglible, all of the power supply voltage will drop across the collector resistor when the LED is lit, with the exception of the LED voltage. Ohm's Law can then be used to determine a resistance value for a desired target current. Compute the required value of resistance to achieve an LED current of 8 mA. Replace the collector resistor with the nearest value available and measure the resulting current. Record the appropriate values in Table 8.4.

Data Tables

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 8.1

Issue	V_B	V_E	V_C
R_2 Short			
R_E Open			
R_C Short			
R_C Open			
V_{CE} Short			
V_{CE} Open			

Table 8.2

Vbb	$I_{B\ Theory}$	$I_{C\ Theory}$	$V_{CE\ Theory}$	$I_{B\ Exp}$	$I_{C\ Exp}$	$V_{CE\ Exp}$
5						
0						
5						
0						
5						
0						

Table 8.3

$R_{C\ Theory}$	$R_{C\ Actual}$	$I_{C\ Measured}$

Table 8.4

Questions

1. Is the PNP voltage divider circuit as stable as its NPN counterpart studied earlier?

2. Compare the NPN voltage divider lab results to this PNP version. If the various transistor voltages are added together (e.g., NPN base voltage plus PNP base voltage), a constant results. What is the significance of this value and will it always work out in this fashion? Why/why not?

3. Do the troubleshooting faults presented in the PNP circuit produce similar transistor voltages compared to the same faults in the NPN version of the circuit? Why/why not?

4. How does the operational logic of the PNP LED driver compare to the NPN version of the same circuit?

5. Are the LED current design considerations the same as those of the NPN version?

9

Common Emitter Amplifier

Objective

The objective of this exercise is to examine the characteristics of a common emitter amplifier, specifically voltage gain, input impedance and output impedance. A method for experimentally determining input and output impedance is investigated along with various potential troubleshooting issues.

Theory Overview

An ideal common emitter amplifier simply multiples the input function by a constant value while also inverting the signal. The voltage amplification factor, A_v, is largely a function of the AC load resistance at the collector and the internal emitter resistance, r'_e. This internal resistance is, in turn, inversely proportional to the DC emitter current. Therefore, if the underlying bias is stable with changes in beta, the voltage gain will also be stable. The circuit will appear as an impedance to the signal source, Z_{in}. This impedance is approximately equal to the base biasing resistor(s) in parallel with the impedance seen looking into the base ($Z_{in(base)}$) which is approximately equal to $\beta\, r'_e$. Consequently, the amplifier's input impedance may experience some variation with beta. In contrast, the circuit's output impedance as seen by the load is approximately equal to the DC collector biasing resistor.

From a practical standpoint, input and output impedance cannot be measured directly with an ohmmeter. This is because ohmmeters measure resistance by sending out a small "sensing" current. The DC bias and AC signal currents will interact with this current and produce an unreliable result. Instead, impedances can be measured indirectly through a voltage divider effect. That is, if the voltages of both legs of a voltage divider can be measured and the resistance of one of the legs is known, the remaining resistance may be determined using Ohm's Law or the voltage divider rule.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(1) Dual Channel Oscilloscope	model:_____ srn:_____
(1) Function Generator	model:_____ srn:_____
(3) Small signal transistors (2N3904)	
(1) 10 k Ω resistor ¼ watt	actual: _____
(1) 15 k Ω resistor ¼ watt	actual: _____
(1) 20 k Ω resistor ¼ watt	actual: _____
(1) 22 k Ω resistor ¼ watt	actual: _____
(1) 33 k Ω resistor ¼ watt	actual: _____

(2) 10 µF capacitors actual: _____

(1) 470 µF capacitor actual: _____

Schematics

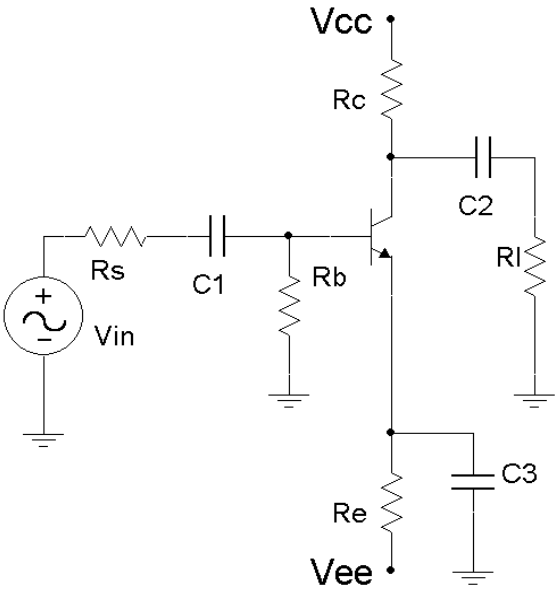

Figure 9.1

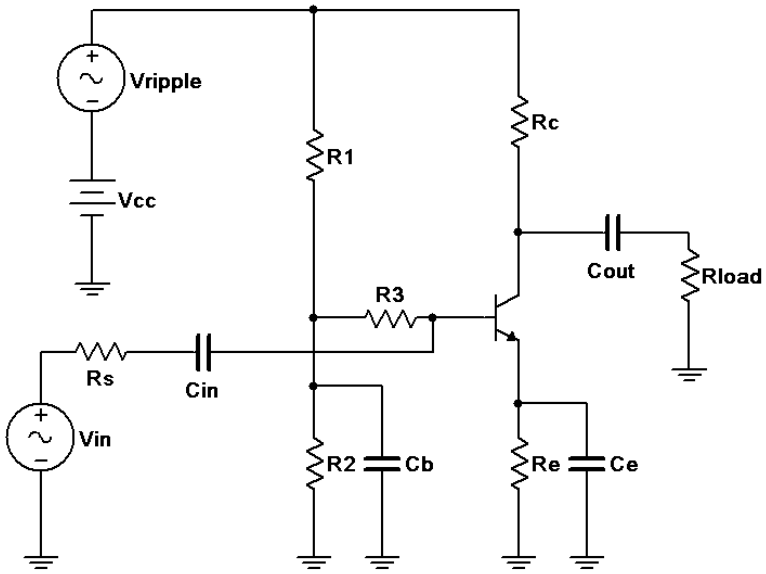

Figure 9.2

Procedure

DC Circuit Voltages

1. Consider the circuit of Figure 9.1 using Vcc = 15 volts, Vee = -12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re = 22 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, C1 = C2 = 10 μF and C3 = 470 μF. Using the approximation of a negligible base voltage, determine the DC voltages at the base, emitter, and collector along with the collector current, and record these in Table 9.1.

2. Build the circuit of Figure 9.1 using Vcc = 15 volts, Vee = -12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re = 22 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, C1 = C2 = 10 μF and C3 = 470 μF. Make sure that the AC source is turned off or disconnected. Measure the DC voltages at the base, emitter, and collector along with the collector current, and record these in Table 9.1. Note, you may wish to use a transistor curve tracer or beta checker to get approximate values of beta for each of the three transistors to be used.

AC Circuit Voltages

3. Based on the calculated collector current, determine the resulting theoretical r'_e, A_v, Z_{in} and Z_{out}, and record these in Table 9.2. Assume a beta of approximately 150 for the Z_{in} calculation.

4. Continuing with the values in Table 9.2 and using an AC source voltage of a 40 mV peak-peak 1 kHz sine wave, compute the theoretical AC base, emitter and load voltages, and record them in Table 9.3 (Theory). Note that R_s will create a voltage divider effect with Z_{in}, thus reducing the signal that reaches the base. This reduced signal is then multiplied by the voltage gain and appears at the collector.

5. Set the source to a 40 mV peak-peak 1 kHz sine wave and apply to the circuit. Using the oscilloscope, place one probe at the base and the second at the emitter. Record the resulting peak-peak voltages in the first row of Table 9.3 (Experimental). The oscilloscope inputs should be set for AC coupling with the bandwidth limit engaged. Capture an image of the oscilloscope display.

6. Move the second probe to the load and record its peak-peak value in the first row of Table 9.3. Also include whether the signal is in phase or out of phase with the base signal. Capture an image of the oscilloscope display.

7. Unhook the load resistor from the output capacitor and measure the resulting collector voltage (do not connect the output capacitor to ground-simply leave it dangling). Record this value in the final column of Table 9.3.

8. Reattach the load resistor. Swap the transistor with the second transistor and repeat steps 5 through 7 using the second row of Table 9.3.

9. Reattach the load resistor. Swap the transistor with the third transistor and repeat steps 5 through 7 using the third row of Table 9.3.

10. Using the measured base and collector voltages from Table 9.3, determine the experimental gain for each transistor. From these gains determine the experimental r'_e. Using the source voltage, the measured base voltages and the source resistance, determine the effective input impedances via Ohm's Law or the voltage divider rule. Finally, in similar manner and using the loaded and unloaded collector voltages along with the load resistor value, determine the experimental output impedances. Record these values in Table 9.4. Also determine and record the percent deviations.

Troubleshooting

11. Return the load resistor to the circuit. Consider each of the individual faults listed in Table 9.5 and estimate the resulting AC load voltage. Introduce each of the individual faults in turn and measure and record the load voltage in Table 9.5.

Multisim

12. One issue with amplifiers is noise and ripple on the power supply. This will be directly coupled to output of the circuit via the collector resistor. Worse, this noise or ripple may be coupled into the base and then amplified along with the desired input signal. This can be an issue with amplifiers that use a voltage divider bias. One way to reduce this effect is to decouple the voltage divider from the base. This modification is shown in the circuit of Figure 9.2. Cb effectively shorts R2, sending power supply noise and ripple to ground instead of into the base. By itself this would also short the desired input signal so an extra resistor, R3 is added between the capacitor and the base. The input impedance of the circuit is approximately equal to R3 in parallel with $\beta r'_e$. To show the effectiveness of this technique, build the circuit of Figure 9.2 in Multisim. Use Vin = 20 mV peak at 1 kHz, Vripple = 20 mV peak at 120 Hz, Vcc = 12 volts, Rs = 1 kΩ, R1 = 10 kΩ, R2 = 3.3 kΩ, R3 = 22 kΩ, Re = 4.7 kΩ, Rc = 3.3 kΩ, Rload = 1 kΩ, Cin = Cout = 10 μF, Cb= 100 μF and Ce = 470 10 μF. Run a Transient simulation and look at the load voltage. A very small low frequency variation should be noted. This is the 120 Hz ripple coupled in through the collector resistor. Alter the circuit by removing Cb and R3 to produce the basic voltage divider circuit (or more simply, set Cb and R3 to extremely small values such as pF and mΩ). Rerun the simulation. The load voltage should now show a much more obvious ripple contribution, thus showing how effective the power supply decoupling components can be.

Data Tables

$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$I_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	$I_{C\ Exp}$

Table 9.1

r'_e	A_v	Z_{in}	Z_{out}

Table 9.2

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{L\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{L\ Exp}$	Phase V_L	$V_{L\ No\ Load}$
1								
2								
3								

Table 9.3

Transistor	$A_{v\ Exp}$	$r'_{e\ Exp}$	$Z_{in\ Exp}$	$Z_{out\ Exp}$	%D A_v	%D r'_e	%D Z_{in}	%D Z_{out}
1								
2								
3								

Table 9.4

Issue	V_{Load}
R_B Short	
C_1 Open	
R_C Short	
R_C Open	
R_E Open	
C_2 Open	
C_3 Open	
V_{CE} Open	

Table 9.5

Questions

1. Does the common emitter amplifier produce a considerable amplification effect and if so, are the results consistent across transistors?

2. Does the common emitter amplifier produce a phase shift at the output and if so, is it affected by the transistor beta?

3. If the collector and base voltages had been measured with the oscilloscope DC coupled, how would the measurements of Table 9.3 have changed?

4. Does the value of the transistor beta play any role in setting the input impedance? Was a considerable variation in input impedance apparent?

10

Swamped CE Amplifier

Objective

The objective of this exercise is to examine the characteristics of a swamped common emitter amplifier, specifically the effects of swamping on voltage gain, input impedance and distortion.

Theory Overview

As the signal current changes in a transistor, the total current flowing through the emitter changes along with it. As a result, these changes produce small changes in r'_e which in turn changes the voltage gain. In other words, the gain changes throughout the signal producing slightly more or less gain at some points along the signal than others. These changes show up as a squashing or elongating of the positive and negative peaks of the output signal. Generally, these forms of waveform distortion are to be avoided. Also, they tend to worsen as the output signal amplitude increases. A method of mitigating this distortion is to add AC resistance to the emitter portion of the circuit. This added resistance tends to buffer or "swamp out" the changes in r'_e and therefore reduces the distortion. A side bonus is that $Z_{in(base)}$ will also be increased which will result in an increased Z_{in} to the circuit. On the downside, the added resistance will lower the voltage gain. Consequently the swamped amplifier exhibits a lower gain but one of higher quality. In general, the larger the swamping resistance is compared to r'_e, the greater the effects on distortion, gain and input impedance.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(1) Dual Channel Oscilloscope	model:_____ srn:_____
(1) Low Distortion Function Generator	model:_____ srn:_____
(1) Distortion Analyzer	model:_____ srn:_____
(1) Small signal transistor (2N3904)	
(1) 220 Ω resistor ¼ watt	actual: _____
(1) 1 k Ω resistor ¼ watt	actual: _____
(1) 10 k Ω resistor ¼ watt	actual: _____
(1) 15 k Ω resistor ¼ watt	actual: _____
(1) 20 k Ω resistor ¼ watt	actual: _____
(1) 22 k Ω resistor ¼ watt	actual: _____
(1) 33 k Ω resistor ¼ watt	actual: _____
(2) 10 µF capacitors	actual: _____

(1) 470 µF capacitor actual: _____

Schematic

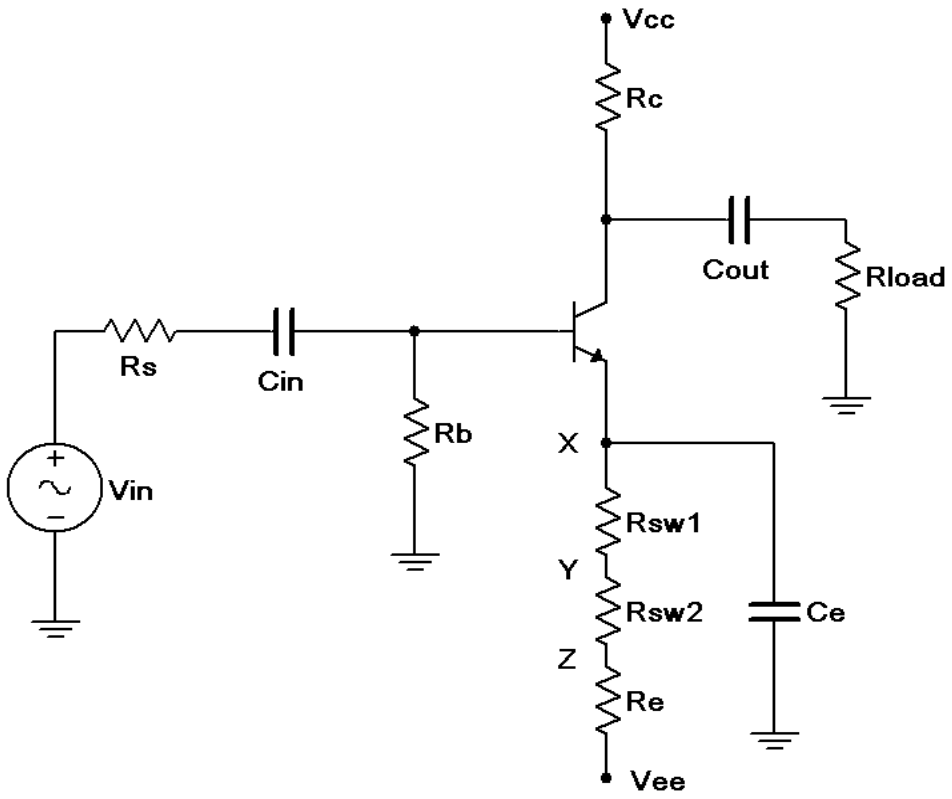

Figure 10.1

Procedure

AC Circuit Voltages

1. Consider the circuit of Figure 10.1 using Vcc = 15 volts, Vee = -12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re = 22 kΩ, Rsw1 = 220 Ω, Rsw2 = 1 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, Cin = Cout = 10 µF and Ce=470 µF. Using the approximation of a negligible DC base voltage, determine the DC collector current and r'_e, and record these in Table 10.1. Using the r'_e, calculate the expected Z_{in}, $Z_{in(base)}$, and A_v for the X, Y and Z connection points for Ce (shown at position X in the schematic). Record these in Table 10.2. If a transistor curve tracer or beta checker is not available to get an approximate value of beta for the transistor, estimate it at 150.

2. Build the circuit of Figure 10.1 using Vcc = 15 volts, Vee = -12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re=22 kΩ, Rsw1 = 220 Ω, Rsw2 = 1 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, Cout = Cout = 10 µF and

Ce=470μF. Connect Ce to postion X. Disconnect the signal source and check the DC transistor voltages to ensure that the circuit is biased correctly. (Note, the DC equivalent circuit is very similar to the ones used in Exercises 6 and 9, and should exhibit similar DC voltage readings.)

3. Using a 1 kHz sine wave setting, apply the signal source to the amplifier and adjust it to achieve a **load voltage** of 2 volts peak-peak.

4. Measure the AC peak-peak voltages at the source, the base, and the load, and record these in Table 10.3. The load waveforms may exhibit some asymmetry due to distortion so be sure to record the peak-peak voltage not the peak. If asymmetry is observed between the positive and negative peaks, make a note of it. Also, capture images of the oscilloscope displays (V_s with V_b and V_b with V_{load}).

5. Set the distortion analyzer to 1 kHz and % total harmonic distortion (% THD). Apply it across the load and record the resulting reading in the final column of Table 10.3.

6. Remove the distortion analyzer and connect Ce to position Y instead of X. Repeat steps 3, 4 and 5.

7. Remove the distortion analyzer and connect Ce to point Z instead of Y. Repeat steps 3, 4 and 5.

8. Using the measured base and load voltages from Table 10.3, determine the experimental gain for the transistor. Using the measured source and base voltages along with the source resistance, determine the effective input impedances via Ohm's Law or the voltage divider rule. Record these values in Table 10.4. Also determine and record the percent deviations.

Multisim

9. Build the circuit in Multisim and run three sets of simulations, one for each of the three Ce positions. For each trial, set the AC source voltage to the value measured in Table 10.3 ($V_{S\,Exp}$). Run a Transient Analysis and inspect the voltages at the base and load. The AC source voltage may have to be adjusted slightly to achieve the desired the desired 2 volt peak-peak load voltage. Record these values in Table 10.5. Add the Distortion Analyzer instrument at the load and record the resulting value.

Data Tables

I_C	
r'_e	

Table 10.1

Position	A_v Theory	$Z_{in(Base)}$ Theory	Z_{in} Theory
X			
Y			
Z			

Table 10.2

Position	$V_{S\ Exp}$	$V_{B\ Exp}$	$V_{L\ Exp}$	% THD
X				
Y				
Z				

Table 10.3

Position	A_v Exp	Z_{in} Exp	%Dev A_v	%Dev Z_{in}
X				
Y				
Z				

Table 10.4

Position	$V_{S\ Multisim}$	$V_{B\ Multisim}$	$V_{L\ Multisim}$	% Distortion
X				
Y				
Z				

Table 10.5

Questions

1. In summary, what are the effects of swamping?

2. Is the change in voltage gain directly proportional to the amount of swamping?

3. Is the change in input impedance directly proportional to the amount of swamping?

4. Is the change in distortion directly proportional to the amount of swamping?

5. Are THD levels below 1% easily discerned on a simple oscilloscope display?

6. Why is it important that the load voltage be set to the same value in each of the three trials instead of setting the source to the same value?

11

Voltage Follower

Objective

The objective of this exercise is to examine the characteristics of a voltage follower, specifically an emitter follower using a Darlington pair. Voltage gain, input impedance and distortion will all be examined.

Theory Overview

The function of a voltage follower is to present a high input impedance and a low output impedance with a non-inverting gain of one. This allows the load voltage to accurately track or follow the source voltage in spite of a large source/load impedance mismatch. Ordinarily this mismatch would result in a large voltage divider loss. Consequently, followers are often used to drive a low impedance load or to match a high impedance source. While typical laboratory sources exhibit low internal impedances, some circuits and passive transducers can exhibit quite high internal impedances. For example, electric guitar pickups can exhibit in excess of 10 k Ω at certain frequencies. Although the voltage gain may be approximately one, current gain and power gain can be quite high, especially if a Darlington pair is used. Besides unity voltage gain and a high Z_{in} and low Z_{out}, followers also tend to exhibit low levels of distortion.

The Darlington pair effectively produces a "beta times beta" effect by feeding the emitter current of one device into the base of a second transistor. This also produces the effect of doubling both the effective V_{BE} and r'_e.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(1) Dual Channel Oscilloscope	model:_____ srn:_____
(1) Low Distortion Function Generator	model:_____ srn:_____
(1) Distortion Analyzer	model:_____ srn:_____
(2) Small signal transistors (2N3904)	
(1) 220 Ω resistor ¼ watt	actual: _____
(1) 1 k Ω resistor ¼ watt	actual: _____
(1) 22 k Ω resistor ¼ watt	actual: _____
(1) 470 k Ω resistor ¼ watt	actual: _____
(1) 10 µF capacitor	actual: _____
(1) 470 µF capacitor	actual: _____

Schematic

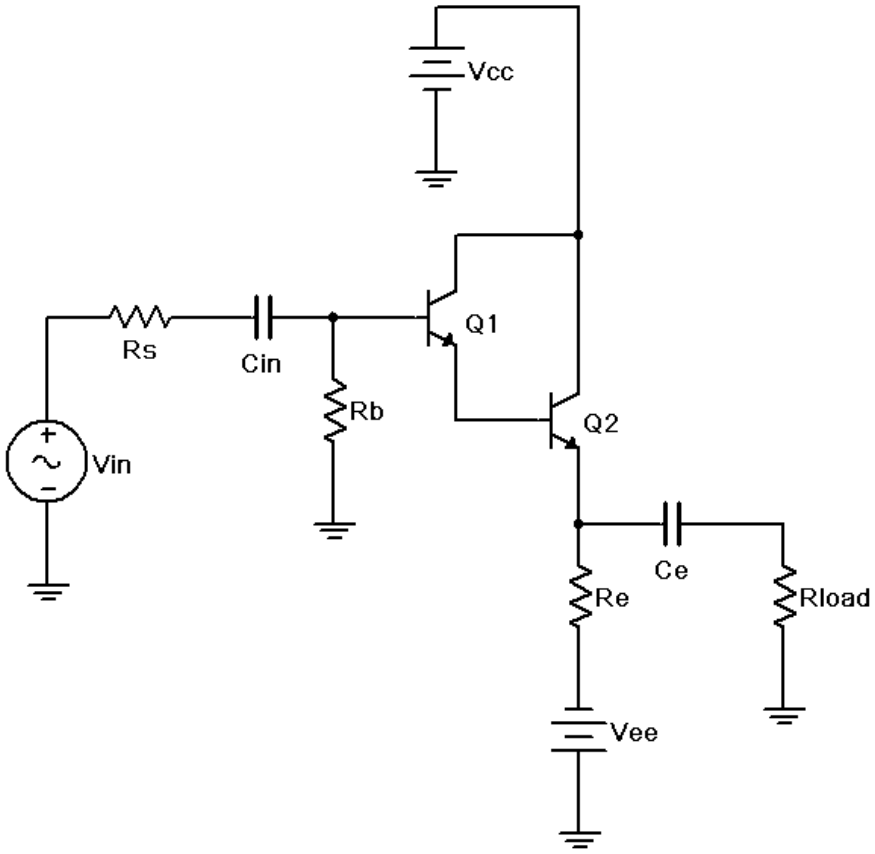

Figure 11.1

Procedure

1. Consider the circuit of Figure 11.1 using Vcc = 5 volts, Vee = -12 volts, Rs = 22 kΩ, Rb = 470 kΩ, Re = 1 kΩ, Rload = 220 Ω, Cin = Ce = 10 µF and Ce = 470 µF. Using the approximation of a negligible DC base voltage, determine the DC collector current and r'_e, and record these in Table 11.1. Using the r'_e, calculate the expected Z_{in}, $Z_{in(base)}$, Z_{out} and A_v. Record these in Table 11.2. If a transistor curve tracer or beta checker is not available to get an approximate value of beta for the transistors, estimate the pair at 10,000.

2. Build the circuit of Figure 11.1 using Vcc = 5 volts, Vee = -12 volts, Rs = 22 kΩ, Rb = 470 kΩ, Re=1kΩ, Rload = 220 Ω, Cin = Ce = 10 µF and Ce = 470 µF. Disconnect the signal source and check the DC transistor voltages to ensure that the circuit is biased correctly. (Note: The base should be close to zero while the emitter will be two V_{BE} drops less, or about -1.4VDC.)

3. Using a 1 kHz sine wave setting, apply the signal source to the amplifier and adjust it to achieve a **source voltage** of 2 volts peak-peak (i.e., to the left of Rs).

4. Measure the AC peak-peak voltages at the source, the base, and the load, and record these in Table 11.3. Also note the phase of the load voltage compared to the source. If distortion asymmetry is observed between the positive and negative peaks, make a note of it. Also, capture images of the oscilloscope displays (V_s with V_b and V_b with V_{load}).

5. Set the distortion analyzer to 1 kHz and % total harmonic distortion (% THD). Apply it across the load and record the resulting reading in Table 11.3.

6. Finally, unhook (i.e., open) the load and measure the resulting load voltage. Record this in the final column of Table 11.3.

7. Using the measured base and load voltages from Table 11.3, determine the experimental gain for the circuit. Using the measured source and base voltages along with the source resistance, determine the effective input impedance via Ohm's Law or the voltage divider rule. In similar fashion, using the loaded and unloaded load voltages along with the load resistance, determine the effective output impedance. Record these values in Table 11.4. Also determine and record the percent deviations.

Troubleshooting

8. Return the load resistor to the circuit. Consider each of the individual faults listed in Table 9.5 and estimate the resulting AC load voltage. Introduce each of the individual faults in turn and measure and record the load voltage in Table 9.5.

Multisim

9. Build the circuit in Multisim and run a Transient Analysis. Use a 1 kHz 1 volt peak sine for the source. Inspect the voltages at the source, base and load. Record these values in Table 11.6. Add the Distortion Analyzer instrument at the load and record the resulting value.

Data Tables

I_C	
r'_e	

Table 11.1

A_v Theory	$Z_{in(Base)}$ Theory	Z_{in} Theory	Z_{out} Theory

Table 11.2

$V_{S\ Exp}$	$V_{B\ Exp}$	$V_{L\ Exp}$	*Phase* V_L	% THD	$V_{L\ No\ Load}$

Table 11.3

A_v Exp	Z_{in} Exp	Z_{out} Exp	%Dev A_v	%Dev Z_{in}	%Dev Z_{out}

Table 11.4

Issue	V_{Load}
R_b Short	
C_{in} Open	
R_e Open	
C_e Open	
R_{Load} Short	
V_{CE} Open	
V_{CC} Open	

Table 11.5

$V_{S\ Multisim}$	$V_{B\ Multisim}$	$V_{L\ Multisim}$	% Distortion

Table 11.6

Questions

1. Would the results of this exercise have been considerably different if the load had been ten times larger? What does that say about the performance of the circuit?

2. If the 22 k source had been directly connected to the 220 load without the follower in between, what would be the load voltage?

3. How do the THD levels of the follower compare to those of the swamped common emitter amplifier?

4. How would the circuit parameters change if a Darlington pair had not been used?

12

Class A Power Analysis

Objective

The objective of this exercise is to examine large signal class A operation. A voltage follower will be investigated by plotting the AC load line and determining output compliance, maximum load power, supplied DC power and efficiency. The effects of clipping will be noted.

Theory Overview

The maximum output signal, or compliance, of a class A amplifier is determined by its AC load line. The maximum peak level is determined by the smaller of V_{CEQ} and $I_{CQ} \bullet r_{Load}$. If either of these levels is hit, the output signal will begin to clip causing greatly increased distortion. Knowing this voltage and the load resistance, the maximum load power may be determined. Dividing this power by the total supplied DC power will yield the efficiency. The maximum theoretical efficiency of an RC coupled class A amplifier is 25% although real-world circuits may be far less. In fact, the power dissipation of the transistor itself (P_{DQ}) may be greater than the maximum load power, clearly not a desirable condition. Note that the total supplied power is the product of the total supplied voltage and the average total current. In a class A amplifier that is not clipping, the average supplied current is equal to the quiescent DC current. In the case of a dual supply emitter biased circuit, this is simply the collector current and can be measured with a DC ammeter.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(1) Dual Channel Oscilloscope	model:_____ srn:_____
(1) Low Distortion Function Generator	model:_____ srn:_____
(1) Distortion Analyzer	model:_____ srn:_____
(2) Small signal transistors (2N3904)	
(1) 100 Ω resistor ¼ watt	actual: _____
(1) 1 k Ω resistor ¼ watt	actual: _____
(1) 47 k Ω resistor ¼ watt	actual: _____
(1) 470 µF capacitor	actual: _____

Schematic

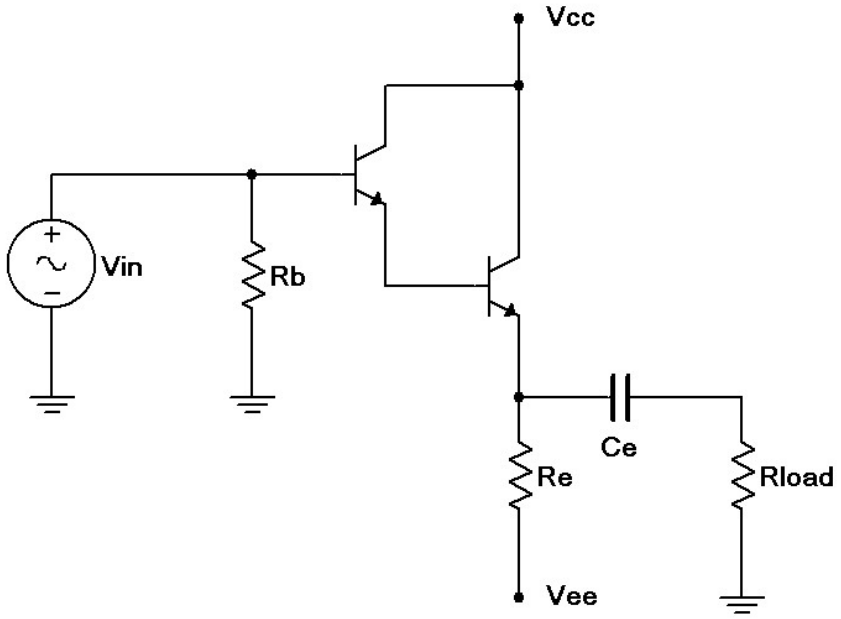

Figure 12.1

Procedure

AC Load Line and Power Analysis

1. Consider the circuit of Figure 12.1 using Vcc = 5 volts, Vee = -12 volts, Rb = 47 kΩ, Re = 1 kΩ, Rload = 100 Ω and Ce = 470 µF. Determine the theoretical I_{CQ}, V_{CEQ}, $v_{CE(cutoff)}$ and $i_{C(sat)}$, and record these in Table 12.1. It is helpful to plot the AC load line for step three. Note that the collector-emitter saturation voltage for a Darlington pair cannot be assumed to be 0 volts, and may be closer to one volt, thus reducing the expecting voltage swing toward the saturation point. It is also worth noting that this amplifier has a *direct coupled* input (i.e., no input capacitor is required due to the very small DC base voltage).

2. Build the circuit of Figure 12.1 using Vcc = 5 volts, Vee = -12 volts, Rb = 47 kΩ, Re = 1 kΩ, Rload=100 Ω and Ce = 470 µF. Disconnect the signal source and measure the DC transistor voltages to ensure the circuit is biased correctly. Record V_{CEQ} and I_{CQ} in Table 12.1 (Experimental).

3. Based on the data recorded in Table 12.1, determine the theoretical maximum unclipped load voltage (compliance) and record it in Table 12.2. Based on this, determine the maximum load power and record it Table 12.2 as well. Also determine and record the expected values for the quiescent power dissipation of the transistor (P_{DQ}), the supplied DC current and power, and the resulting efficiency.

4. Using a 1 kHz sine wave setting, apply the signal source to the amplifier and adjust it to achieve a load voltage that just begins to clip. Reduce the amplitude *slightly* to produce a clean, unclipped wave. Record this level as the experimental compliance in Table 12.2. From this, determine and record the experimental maximum load power. Also, capture an image of the oscilloscope display.

5. Insert an ammeter in the collector and measure the resulting current with the signal still set for maximum unclipped output. Record this in Table 12.2 as $I_{supplied}$ (Experimental).

6. Using the data already recorded, determine and record the experimental P_{DQ}, $P_{Supplied}$, and η. Finally, determine the deviations for Table 12.2.

Clipping and Distortion

7. Increase the signal until both peaks begin to clip. Record these clipping levels in Table 12.3. Make sure the oscilloscope is **DC coupled** for this measurement as any offset is important. Compare these peaks to those predicted by the AC load line. Also, capture an image of the oscilloscope display.

8. Decrease the signal level so that it is about 90% of the maximum unclipped level. Set the distortion analyzer to 1 kHz and % total harmonic distortion (% THD). Apply it across the load and record the resulting reading in Table 12.4 (Normal). Increase the signal by about 20% so that one of the peaks is obviously clipped and take a second distortion reading, recording it Table 12.4 (Clipped).

Multisim

9. Build the circuit in Multisim and run a Transient Analysis. Use a 1 kHz 7 volt peak sine for the source. Inspect the voltage at the load. Record the peak clip points in Table 12.5. Reduce the input signal so that clipping disappears. Add the Distortion Analyzer instrument at the load and record the resulting value.

Data Tables

	Theory	Experimental
I_{CQ}		
V_{CEQ}		
$i_{C(sat)}$		X
$v_{CE(cutoff)}$		X

Table 12.1

	Theory	Experimental	% Deviation
Compliance			
$P_{Load(max)}$			
$I_{Supplied}$			
P_{DQ}			
$P_{Supplied}$			
η			

Table 12.2

Positive Clip	
Negative Clip	

Table 12.3

%THD Normal	
%THD Clipped	

Table 12.4

Positive Clip	Negative Clip	% Distortion

Table 12.5

Questions

1. Does the maximum load power compare favorably to the supplied DC power and the transistor's power dissipation? That is, is the circuit efficient?

2. How does the THD level of the clipped signal compare to that of the unclipped signal?

3. How well do the clip levels measured and simulated compare to the predicted AC load line?

4. How would the circuit performance change if a Darlington pair had not been used? Would this affect the AC load line?

5. Would increasing the Vcc supply increase the output compliance? Why/why not?

13

Class B Power Analysis

Objective

The objective of this exercise is to examine large signal class B operation. A voltage follower will be investigated to determine output compliance, maximum load power, supplied DC power and efficiency. The effects of crossover distortion will be noted by comparing resistor and diode biasing schemes.

Theory Overview

The maximum output signal, or compliance, of a class B amplifier is determined by its AC load line. The peak to peak compliance is roughly equal to the total DC supply voltage(s). As two output devices are used, each conducting for half of the cycle, the quiescent current can remain low, unlike a class A amplifier. This results in vastly improved efficiency, theoretically up to 78.5%. The switchover from one transistor to the other is problematic and can result in crossover or notch distortion. To alleviate this, the transistors are given a small idle current so that each base-emitter junction is just about fully on. While resistors can be used to create this bias, trying to match the linear current-voltage characteristic of a resistor to the logarithmic characteristic of a PN junction is tricky. Consequently, another PN junction, namely a diode, is used instead. The diode will result in a more stable circuit which produces less notch distortion.

Equipment

(1) Dual Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(1) Dual Channel Oscilloscope model:_____ srn:_____
(1) Low Distortion Function Generator model:_____ srn:_____
(1) Distortion Analyzer model:_____ srn:_____
(1) Small signal NPN transistor (2N3904)
(1) Small signal PNP transistor (2N3906)
(2) Switching diodes (1N914 or 1N4148)
(1) 100 Ω resistor ¼ watt actual: _____
(2) 220 Ω resistors ¼ watt actual: _____
(2) 2.2 k Ω resistors ¼ watt actual: _____
(2) 10 µF capacitor actual: _____
(1) 100 µF capacitor actual: _____

Schematics

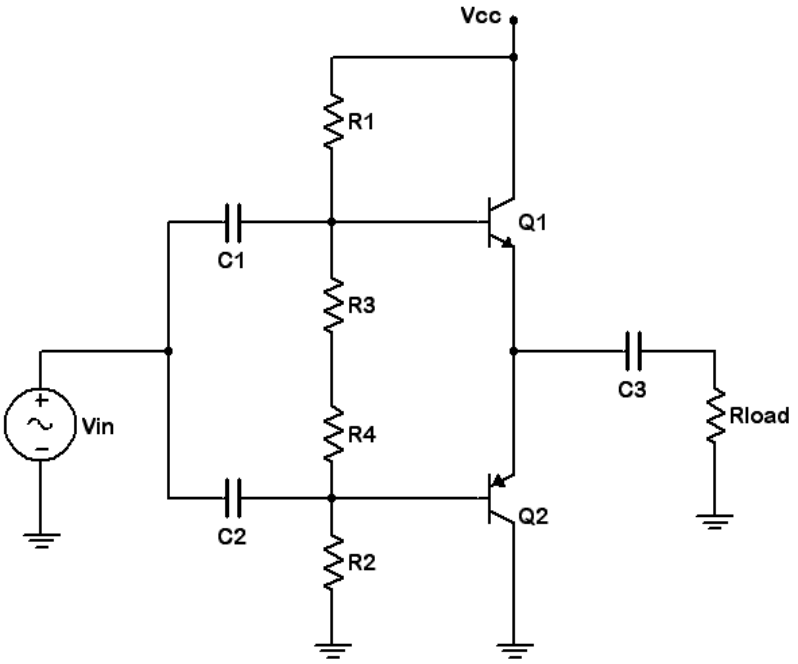

Figure 13.1

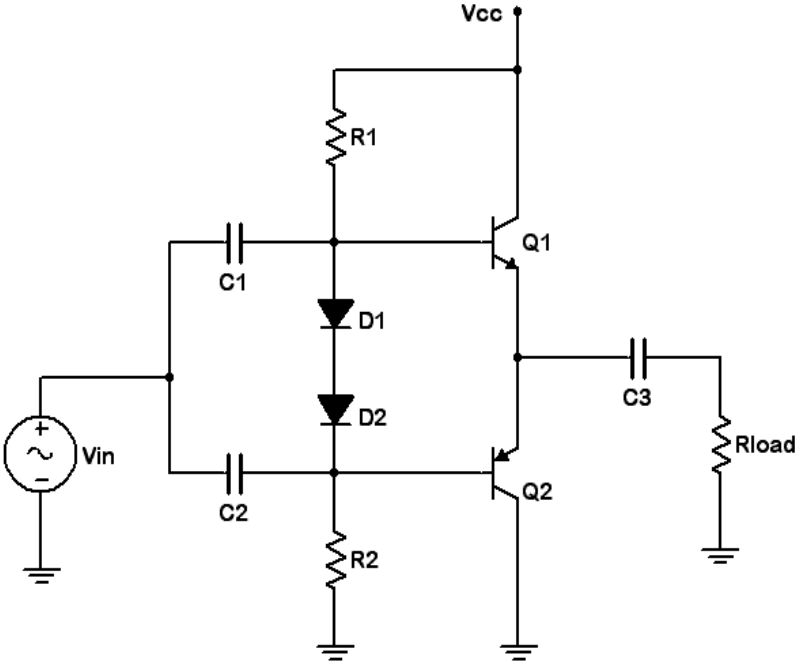

Figure 13.2

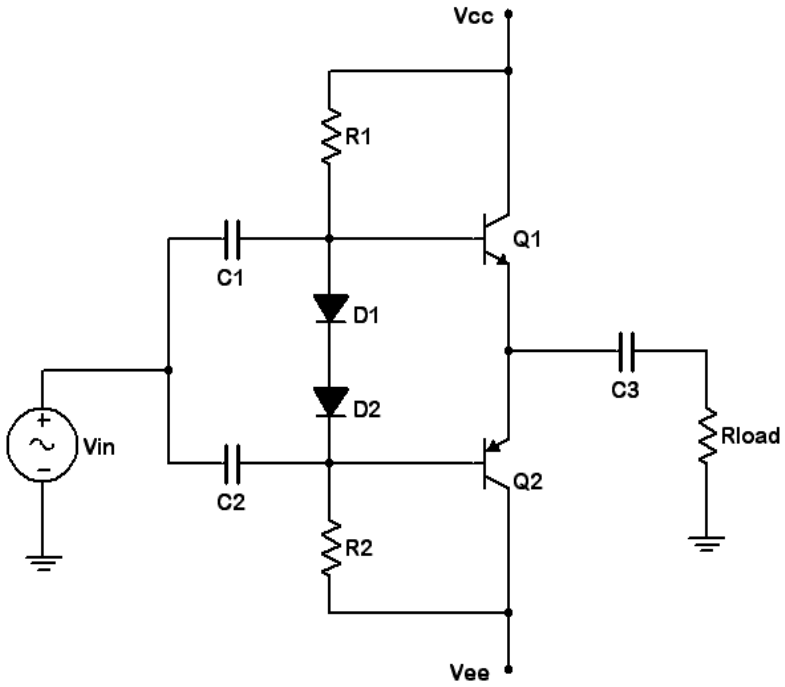

Figure 13.3

Procedure

Resistor versus Diode Bias and Crossover Distortion

1. Consider the circuit of Figure 13.1 using Vcc = 6 volts, R1 = R2 = 2.2 kΩ, R3 = R4 = 220 Ω, Rload=100 Ω, C1 = C2 = 10 μF and C3 = 100 μF. Ideally this circuit will produce a compliance of just under 6 volts peak-peak.

2. Build the circuit of Figure 13.1 using Vcc = 6 volts, R1 = R2 = 2.2 kΩ, R3 = R4 = 220 Ω, Rload=100Ω, C1 = C2 = 10 μF and C3 = 100 μF. Disconnect the signal source and insert an ammeter into the collector of Q1. Record I_{CQ} in Table 13.1.

3. Connect the signal source and apply a 1 kHz sine at 2 volts peak. Look at the load voltage and capture the oscilloscope image. There should be considerable notch or crossover distortion.

4. Cycle through the remaining supply voltages in Table 13.1, repeating steps 2 and 3. Only images of the first and last trials need be captured. As the bias current increases, the notch distortion should decrease.

5. Replace R3 and R4 with switching diodes, as shown in Figure 13.2. Repeat steps 2 through 4 using this circuit and Table 13.2. Overall, the superior matching of the diodes to the transistors should result in decreased notch distortion.

Dual Supply and Power Analysis

6. Add the negative power supply so that the circuit now appears as Figure 13.3. Set the supplies to +/- 6 volts DC. This should produce similar bias and amplification results to the single 12 volt supply circuit of Figure 13.2. Although the output coupling capacitor is no longer needed (one advantage of the dual supply topology), leave it in for safety sake.

7. Based on the I_{CQ} recorded for the 12 volt supply in Table 13.2, determine the theoretical P_{DQ}. Also determine the expected compliance, $P_{Load(max)}$, $I_{supplied}$, $P_{supplied}$ and efficiency. Record these values in the Theoretical column of Table 13.3.

8. Apply the signal source to the amplifier and adjust it to achieve a load voltage that just begins to clip. Reduce the amplitude *slightly* to produce a clean, unclipped wave. Record this level as the experimental compliance in Table 13.3. From this, determine and record the experimental maximum load power. Also, capture an image of the oscilloscope display.

9. Insert an ammeter in the collector and measure the resulting current with the signal still set for maximum unclipped output. Record this in Table 13.3 as $I_{supplied}$ (Experimental). Remove the ammeter.

10. Using the data already recorded, determine and record the experimental P_{DQ}, $P_{Supplied}$, and η. Finally, determine the deviations for Table 13.3.

Distortion

11. Unlike class A distortion which gets worse as the signal increases, notch distortion is relatively fixed. Therefore, it represents a smaller percentage of the overall output signal as the signal increases. To see this effect, adjust the signal level to achieve a load voltage of 8 volts peak-peak. There should be no clipping. Set the distortion analyzer to 1 kHz and % total harmonic distortion (% THD). Apply it across the load and record the resulting reading in Table 13.4 (8 Vpp). Decrease the generator to achieve a load voltage of 1 volt peak-peak and record the resulting THD.

Multisim

12. Build the circuit in Multisim and run a Transient Analysis. Use a 1 kHz 7 volt peak sine for the source. Inspect the voltage at the load. Record the peak clip points in Table 13.5. Reduce the input signal so that clipping disappears. Add the Distortion Analyzer instrument at the load and record the resulting value.

Data Tables

Supply	I_{CQ} - Resistors
6 V	
8 V	
10 V	
12 V	

Table 13.1

Supply	I_{CQ} - Diodes
6 V	
8 V	
10 V	
12 V	

Table 13.2

	Theory	Experimental	% Deviation
Compliance			
$P_{Load(max)}$			
$I_{Supplied}$			
P_{DQ}			
$P_{Supplied}$			
η			

Table 13.3

%THD 8 Vpp	
%THD 1 Vpp	

Table 13.4

Positive Clip	Negative Clip	% Distortion

Table 13.5

Questions

1. Does the maximum load power compare favorably to the supplied DC power and the transistor's power dissipation? That is, is the circuit efficient? How does it compare to class A operation (Exercise 12)?

2. How is the notch distortion affected by the power supply?

3. Compare the resistor bias and diode bias circuits regarding idle current (I_{CQ}) and notch distortion. Compute the I_{CQ} versus V_{CC} stability ($I_{CQ\text{-}MAX}$ / $I_{CQ\text{-}MIN}$) of each circuit using the first and last entries of Tables 13.1 and 13.2.

4. How does the class B circuit distortion compare to class A operation (Exercise 12)?

5. Would increasing the Vcc supply increase the output compliance? Why/why not?

14

Power Amp with Driver

Objective

The objective of this exercise is to examine a typical audio amplifier consisting of a class A driver feeding a class B follower. System gain and clipping limits will be examined along with the audibility of clipping distortion and the shapes of voice waveforms.

Theory Overview

Typical audio amplifiers utilize one or more small signal class A stages to achieve sufficient voltage gain which then feeds a class B power stage connected to the load (normally a loudspeaker). The stage preceding the power section is referred to as the driver stage or simply the driver. The driver is often directly coupled instead of coupled via a capacitor. This maximizes gain and reduces component count.

A typical loudspeaker exhibits a nominal 8 Ω impedance. As such, it demands considerable current. The job of the class B follower is to create a good match to this low impedance and produce sufficient current and power gain to drive it effectively. The voltage gain comes from the prior stages. If any of the amplifier stages clip the waveform, the loudspeaker will reproduce the distorted wave. This distortion can be clearly audible and produce a signal that sounds fuzzy or harsh. Loudspeakers can also be used as microphones (although the quality will not be as high as that achieved with a properly designed microphone). In this experiment, a loudspeaker will be used as a microphone to inspect the waveshapes produced by the human voice; waveshapes that are potentially far more complex than simple sine waves.

Equipment

(1) Dual Adjustable DC Power Supply model:_____ srn:_____
(1) Digital Multimeter model:_____ srn:_____
(1) Dual Channel Oscilloscope model:_____ srn:_____
(1) Function Generator model:_____ srn:_____
(2) Small signal NPN transistors (2N3904)
(1) Small signal PNP transistor (2N3906)
(2) Switching diodes (1N914 or 1N4148)
(2) 100 Ω resistor ¼ watt actual: _____
(1) 1 k Ω resistor ¼ watt actual: _____
(1) 6.8 k Ω resistor ¼ watt actual: _____
(1) 1 k Ω potentiometer or decade box
(1) 1 µF capacitor actual: _____

(1) 100 µF capacitor actual: _____

(1) 8 or 16 Ω general purpose loudspeaker

Schematic

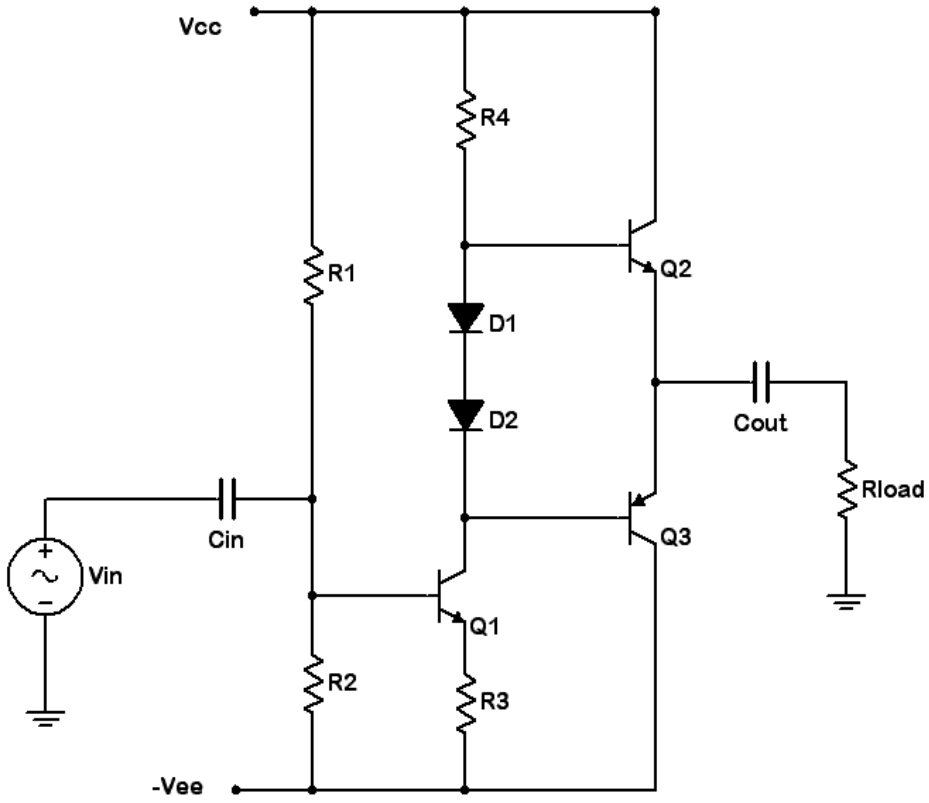

Figure 14.1

Procedure

Bias, Gain and Compliance

1. Consider the circuit of Figure 14.1 using Vcc = 6 volts, Vee = -6 volts, R1 = 6.8 kΩ, R4 = 1 kΩ, R3=100 Ω, Rload = 100 Ω, Cin = 1 µF and Cout = 100 µF. R2 is an adjustable resistance (pot or decade box). For proper bias, the emitters of the output transistors should be at 0 volts DC. For this to be true there must be Vcc-Vbe or approximately 5.3 volts across R4. Ignoring base currents, this establishes I_{CQ} of transistor 1 which in turn creates a potential drop across R3. From this the voltage across R2 may be determined. Knowing the value of R1 and the total supply presented, Ohm's law or the voltage divider rule may be used to compute the require setting for R2. Compute the required value for R2 and record it in Table 14.1.

2. Compute the gain of the driver stage. For the load of Q1, the dynamic resistance of the diodes is small enough to ignore. Also, assume the current gain of the output transistors is approximately 100. Remember, only one output transistor is on at any given time. The gain of the class B stage may be assumed to be unity. Record the theoretical circuit gain in Table 14.1.

3. Ideally, the class B stage will produce a compliance of just under 6 volts peak. It may be less than this as the driver stage might clip sooner. Compute the AC load line for the driver stage and determine its compliance. Note that there will be a voltage divider effect between Re and the load of Q1 which will reduce the compliance from that calculated via the load line. Record the theoretical compliance value in Table 14.1. It should be less than that of the output stage and thus represents the compliance of the entire circuit.

4. Build the circuit of Figure 14.1 using Vcc = 6 volts, Vee = -6 volts, R1 = 6.8 kΩ, R4 = 1 kΩ, R3=100Ω, Rload = 100 Ω, Cin = 1 μF and Cout = 100 μF. Set the pot or decade box (R2) to the value calculated in Table 14.1. Disconnect the signal source and inspect the DC voltage at the load. Adjust R2 until this voltage goes to 0 volts. Record the resulting value of R2 in Table 14.1.

5. Connect the signal source and apply a 1 kHz sine at .2 volts peak. Inspect the load and source voltages with the oscilloscope and capture an image of the pair. From these voltages determine the circuit gain and record it in Table 14.1.

6. Increase the signal level until the output begins to clip. Reduce the level until the signal is undistorted and record the resulting load voltage as the experimental compliance in Table 14.1.

Waveforms: Human Perception and Production

7. Turn down the signal source to about 100 mV peak. Insert the loudspeaker in **series** with the load resistor. Accidentally placing it in parallel will cause excessive current draw and likely destroy the output transistors (after making a particularly loud and irritating squawk). Gradually turn up the signal level while monitoring the load voltage with the oscilloscope. Listen to the sound change as the amplifier begins to clip. Describe this change in Table 14.2. Repeat this with the other frequencies indicated.

8. Remove the loudspeaker and function generator. Reposition the loudspeaker so that it acts as the signal source (i.e., in the original position of the generator). It will now act as a microphone. While examining the load voltage, speak into the loudspeaker and note the typically complex waveshapes. Try holding a few different vowel sounds at different pitches and capture a few of these images. Ordinarily it is difficult for humans to vocalize pure sine waves, however, complex waveforms can be broken down mathematically into a combination of sine waves of differing frequencies, amplitudes and phases. As this is a linear amplifier, superposition holds, and thus if the circuit response to individual sines at differing frequencies can be determined then the response to complex waves such as the human voice and musical instruments can also be determined.

Troubleshooting

9. Remove the loudspeaker and return the generator to the circuit. Consider each of the individual faults listed in Table 14.3 and estimate the resulting DC and AC load voltages. If the DC voltage moves a great deal off of zero, chances are the AC load voltage will be badly distorted and there is no need to attempt to estimate a precise value. Introduce each of the individual faults in turn and measure and record the load voltages in Table 14.3.

Data Tables

	Theory	Experimental
R2		
A_v		
Compliance		

Table 14.1

Frequency	Observations
1 kHz	
500 Hz	
200 Hz	

Table 14.2

Issue	$V_{Load\ DC}$	$V_{Load\ AC}$
R_2 Short		
C_{in} Open		
R_1 Open		
R_3 Open		
D_1 Short		
D_2 Open		
C_{out} Open		
V_{CE} Open		

Table 14.3

Questions

1. Is the maximum output compliance determined solely by the class B output stage?

2. What kinds of distortion are present in this circuit?

3. Calculate the maximum load power and load current of the amplifier if the loudspeaker had accidentally been placed in parallel with the load resistor rather than in series.

4. How do the values calculated in Question 3 compare to the data sheet maximums for the 2N3904/6?

15

JFET Bias

Objective

The objective of this exercise is to examine three methods to bias JFETs and determine which produce a stable Q point. A method of determining I_{DSS} and $V_{GS(OFF)}$ in the lab is also presented.

Theory Overview

Unlike bipolar junction transistors, FETs do not have a fixed forward biased junction potential. This makes bias analysis a little trickier. It is often useful to have a couple of device parameters on hand, namely I_{DSS} and $V_{GS(OFF)}$. As is the case with BJTs, finding the main current (I_D) is the key to finding all other circuit currents and voltages. One convenient aspect of JFETs is that the gate current can be ignored for most bias applications. Self Bias may be analyzed through the use of a Self Bias curve or through an iterative process of estimation of V_{GS} leading to drain currents via Ohm's law and the general FET transconductance equation. Self Bias tends to have modestly stable Q points. Source Bias is an improvement over Self Bias. It tends to swamp out V_{GS} variation via the addition of a negative source bias voltage. This topology also turns out potentially to have a very stable transconductance although it is not examined in this exercise. Finally, Current Source Bias utilizes a BJT to establish a very stable drain current. This turns out this comes at the expense of a stable V_{GS} and transconductance (again, not examined here), so this form of bias is not necessarily the best choice for all applications.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(3) Small signal JFETs (MPF102)	
(1) Small signal BJT (2N3904)	
(1) 2.2 k Ω resistor ¼ watt	actual: _____
(2) 4.7 k Ω resistors ¼ watt	actual: _____
(1) 330 k Ω resistor ¼ watt	actual: _____

MPF102 Datasheet: http://www.onsemi.com/pub_link/Collateral/MPF102-D.PDF

Schematics

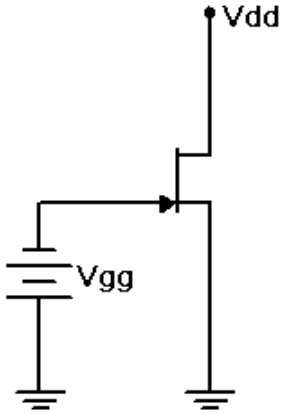

Figure 15.1

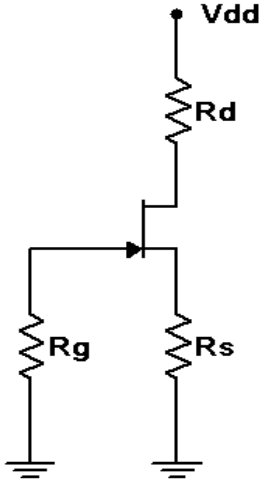

Figure 15.2

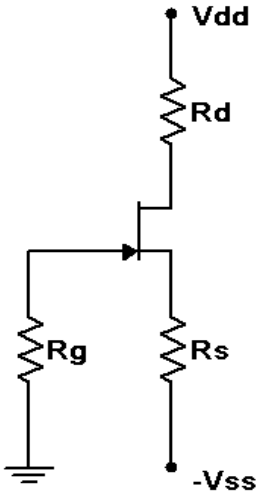

Figure 15.3

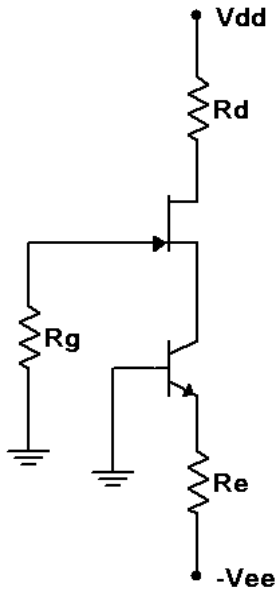

Figure 15.4

Procedure

Determining I_{DSS} and $V_{GS(OFF)}$

1. Consider the circuit of Figure 15.1 using Vdd = 15 volts and Vgg = 0 volts. With nothing else in the circuit, the resulting drain current should equal I_{DSS}. Similarly, if Vgg is gradually changed to a value negative enough to drop the drain current to zero, Vgg must be equal to $V_{GS(OFF)}$.

2. Build the circuit of Figure 15.1 using Vdd = 15 volts and Vgg = 0 volts. Insert an ammeter in the drain and record the resulting current in Table 15.1. Slowly increase the magnitude of Vgg (i.e., make it more negative) until the drain current drops to zero (as a practical point, try to get it under 10 μA, or as low as the ammeter will allow). Record this voltage in Table 15.1. Repeat this process for the other two transistors. Be sure not to confuse the JFETs. Keep them in order.

Self Bias

3. Consider the circuit of Figure 15.2 using Vdd = 15 volts, Rg = 330 kΩ, Rd = 4.7 kΩ, and Rs =2.2 kΩ. Using the values of Table 15.1, calculate and record the expected voltages for JFET 1 in Table 15.2. Also record the expected drain current in Table 15.3.

4. Build the circuit of Figure 15.2 using Vdd = 15 volts, Rg = 330 kΩ, Rd = 4.7 kΩ, and Rs = 2.2 kΩ. Measure and record the voltages for JFET 1 in Table 15.2. Based on V_D, compute and record the experimental drain current in Table 15.3. Also determine and record the drain current deviation.

5. Repeat steps 2 and 3 for the second and third JFETs.

Source Bias

6. Consider the circuit of Figure 15.3 using Vdd = 15 volts, Vss = -3 volts, Rg = 330 kΩ, Rd = 4.7 kΩ and Rs = 4.7 kΩ. A reasonable approximation for V_{GS} in this circuit is -2 volts DC. Based on this, calculate and record the expected voltages for JFET 1 in Table 15.4. Also record the expected drain current in Table 15.5.

7. Build the circuit of Figure 15.3 using Vdd = 15 volts, Vss = -3 volts, Rg = 330 kΩ, Rd = 4.7 kΩ and Rs = 4.7 kΩ. Measure and record the voltages for JFET 1 in Table 15.4. Based on V_D, compute and record the experimental drain current in Table 15.4. Also determine and record the drain current deviation.

8. Repeat steps 5 and 6 for the second and third JFETs.

Current Source Bias

9. Consider the circuit of Figure 15.4 using Vdd = 15 volts, Vee = -5 volts, Rg = 330 kΩ, and Rd = Re = 4.7 kΩ. Calculate and record the expected voltages for JFET 1 in Table 15.6. Also record the expected drain current in Table 15.7.

10. Build the circuit of Figure 15.4 using Vdd = 15 volts, Vee = -5 volts, Rg = 330 kΩ, and Rd = Re = 4.7 kΩ. Measure and record the voltages for JFET 1 in Table 15.6. Based on V_D, compute and record the experimental drain current in Table 15.7. Also determine and record the drain current deviation.

11. Repeat steps 8 and 9 for the second and third JFETs.

Data Tables

JFET	I_{DSS}	$V_{GS(OFF)}$
1		
2		
3		

Table 15.1

JFET	$V_{G\ Thry}$	$V_{S\ Thry}$	$V_{D\ Thry}$	$V_{G\ Exp}$	$V_{S\ Exp}$	$V_{D\ Exp}$
1						
2						
3						

Table 15.2

JFET	$I_{D\ Theory}$	$I_{D\ Experimental}$	%Dev I_D
1			
2			
3			

Table 15.3

JFET	$V_{G\ Thry}$	$V_{S\ Thry}$	$V_{D\ Thry}$	$V_{G\ Exp}$	$V_{S\ Exp}$	$V_{D\ Exp}$
1						
2						
3						

Table 15.4

JFET	$I_{D\ Theory}$	$I_{D\ Experimental}$	%Dev I_D
1			
2			
3			

Table 15.5

JFET	$V_{G\ Thry}$	$V_{S\ Thry}$	$V_{D\ Thry}$	$V_{G\ Exp}$	$V_{S\ Exp}$	$V_{D\ Exp}$
1						
2						
3						

Table 15.6

JFET	$I_{D\ Theory}$	$I_{D\ Experimental}$	%Dev I_D
1			
2			
3			

Table 15.7

Questions

1. Of the three biasing forms presented, which produces the most stable and predictable drain current?

2. Does the precise value of beta for the BJT in the final circuit matter that much? Why/why not?

3. In general, identify two ways of decreasing the drain voltage in the circuit of Figure 15.3.

4. In general, identify two ways of increasing the drain current in the circuit of Figure 15.4.

16

JFET Amplifiers

Objective

The objective of this exercise is to examine common source and common drain (voltage follower) JFET amplifiers. Both voltage gain and input impedance will be investigated.

Theory Overview

In many regards, JFET amplifiers share similar attributes with their bipolar counterparts. Superficially, they look very similar as well. The main functional differences are that JFET based amplifiers tend to have higher input impedances but tend to offer lower voltage gains. Further, without swamping, JFET amplifiers tend to produce lower levels of distortion. As with r'_e impacting bipolar circuit performance, JFET performance is impacted by the transsconductance, g_m. Like the bipolar common emitter amplifier, the common source amplifier exhibits a voltage gain greater than one with inversion. The source follower, like the bipolar emitter follower, shows a voltage gain just under one with no inversion.

Equipment

(1) Dual Adjustable DC Power Supply	model:_____ srn:_____
(1) Digital Multimeter	model:_____ srn:_____
(1) Dual Channel Oscilloscope	model:_____ srn:_____
(1) Function Generator	model:_____ srn:_____
(1) Small signal JFET (MPF102)	
(2) 4.7 k Ω resistors ¼ watt	actual: _____
(1) 22 k Ω resistor ¼ watt	actual: _____
(1) 33 k Ω resistor ¼ watt	actual: _____
(1) 330 k Ω resistor ¼ watt	actual: _____
(2) 10 µF capacitors	actual: _____
(1) 470 µF capacitor	actual: _____

Schematics

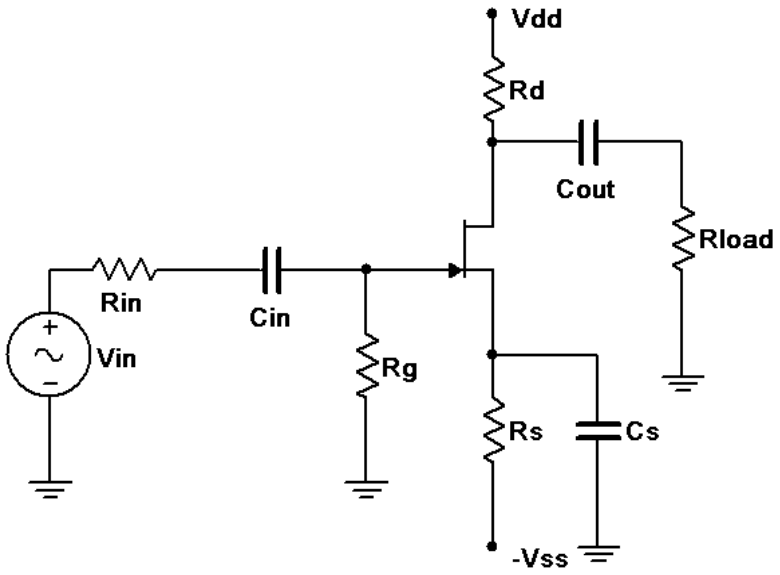

Figure 16.1

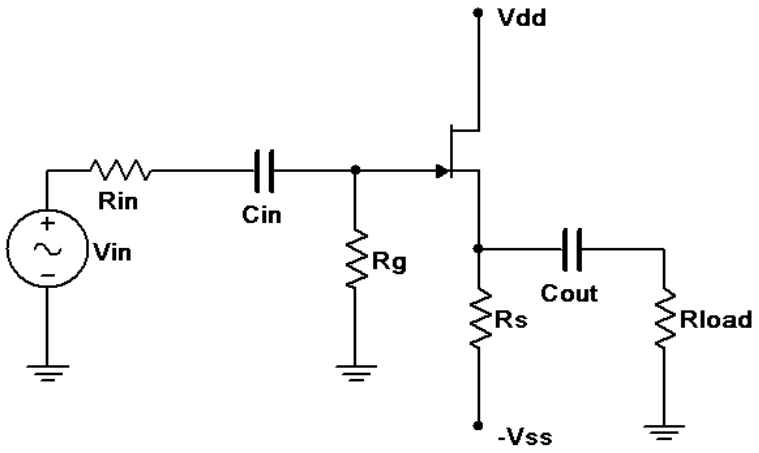

Figure 16.2

Procedure

Common Source Voltage Amplifier

1. Consider the circuit of Figure 16.1 using Vdd = 15 volts, Vss = -3 volts, Rin = 33 kΩ, Rg = 330 kΩ, Rs = 4.7 kΩ, Rd = 4.7 kΩ, Rload = 22 kΩ, Cin = Cout = 10 μF and Cs = 470 μF. Assuming V_{GS} = -2 volts and g_m = 2 mS, determine the theoretical gain and input impedance of the circuit and record these in Table 16.1.

2. Build the circuit of Figure 16.1 using Vdd = 15 volts, Vss = -3 volts, Rin = 33 kΩ, Rg = 330 kΩ, Rs=4.7 kΩ, Rd = 4.7 kΩ, Rload = 22 kΩ, Cin = Cout = 10 μF and Cs = 470 μF. Set Vin to a 100 mV

peak sine at 1 kHz. Measure the voltages at the gate and load, and record these in Table 16.1. Capture images of the input and gate voltages, and the gate and load voltages. Note whether or not the load is inverted compared to the gate signal.

3. Based on the measured gate and drain voltages, determine the resulting theoretical A_v and Z_{in}, and record these in Table 16.1. Note that Zin may be computed using the voltage divider rule or Ohm's law given the gate and input voltages along with the input resistor value. Also determine and record the percent deviations.

4. Repeat steps 1 through 3 for the remaining two JFETs.

Common Drain Voltage Follower

5. Consider the circuit of Figure 16.2 using Vdd = 15 volts, Vss = -3 volts, Rin = 33 kΩ, Rg = 330 kΩ, Rs = 4.7 kΩ, Rload = 22 kΩ, Cin = 10 μF and Cout = 470 μF. Assuming V_{GS} = -2 volts and g_m = 2 mS, determine the theoretical gain and input impedance of the circuit and record these in Table 16.2.

6. Build the circuit of Figure 16.2 using Vdd = 15 volts, Vss = -3 volts, Rin = 33 kΩ, Rg = 330 kΩ, Rs=4.7 kΩ, Rload = 22 kΩ, Cin = 10 μF and Cout = 470 μF. Set Vin to a 100 mV peak sine at 1 kHz. Measure the voltages at the gate and load, and record these in Table 16.2. Capture images of the input and gate voltages, and the gate and load voltages. Note whether or not the load is inverted compared to the gate signal.

7. Based on the measured gate and drain voltages, determine the resulting theoretical A_v and Z_{in}, and record these in Table 16.2. Also determine and record the percent deviations.

8. Repeat steps 5 through 7 for the remaining two JFETs.

Troubleshooting

9. Consider each of the individual faults listed in Table 16.3 and estimate the resulting AC load voltage for circuit 16.1. Introduce each of the individual faults in turn and measure and record the load voltage in Table 16.3.

Data Tables

JFET	$A_{v\ Thry}$	$Z_{in\ Thry}$	$V_{g\ Exp}$	$V_{d\ Exp}$	$A_{v\ Exp}$	$Z_{in\ Exp}$	%Dev A_v	%Dev Z_{in}
1								
2								
3								

Table 16.1

JFET	$A_{v\ Thry}$	$Z_{in\ Thry}$	$V_{g\ Exp}$	$V_{s\ Exp}$	$A_{v\ Exp}$	$Z_{in\ Exp}$	%Dev A_v	%Dev Z_{in}
1								
2								
3								

Table 16.2

Issue	V_{Load}
R_g Short	
C_{in} Open	
R_d Short	
R_d Open	
R_s Open	
C_{out} Open	
C_s Open	
V_{DS} Open	

Table 16.3

Questions

1. Does the common source amplifier produce a considerable amplification effect and if so, are the results consistent across transistors?

2. Does the common source amplifier produce a phase shift at the load? How does this compare with the common drain follower?

3. How do the voltage gains of these circuits compare to their bipolar versions?

4. How do the input impedances of these circuits compare to their bipolar versions?