2 YEAR LIMITED WARRANTY

This product is warranted by CERONIX to be free of defects in material and workmanship for a period of two years from the date of purchase.

In case of a fault, developed during this time, it is the customer's responsibility to transport the defective unit to CERONIX or one of the authorized service centers for repair.
Please attach a note describing the problem.
All parts and labor are free of charge during the warranty period.

CERONIX
12265 Locksley Lane
Auburn, CA. 95602-2055
(530) 888-1044

This warranty does not cover mechanical breakage due to physical abuse.

CERONIX shall not be liable for any consequential damages, including without limitation damages resulting from loss of use.
Some states do not allow limitation of incidental or consequential damages, so the limitation or exclusion may not apply to you.

This warranty gives you specific rights and you may also have other rights which vary from state to state.

Recognized under the Component Program of Underwriters Laboratories Inc. and the Canadian Standards Association.

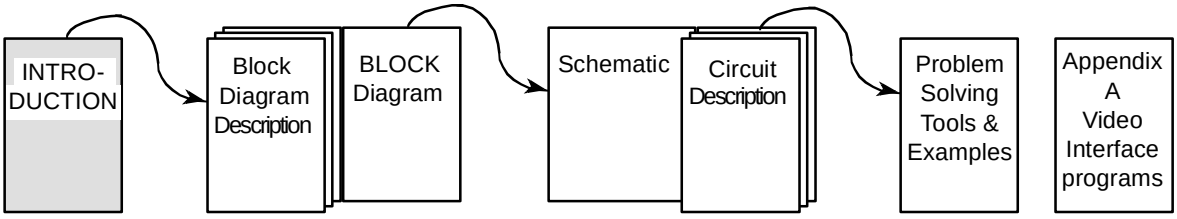
The information contained in this manual is subject to change without prior notice.

ABOUT THIS MANUAL

This manual is specifically written to aid the service technician, repairing CERONIX Models 1492 and 2092 color monitors.

There are three main sections:

1. General Description.
2. Circuit Description.
3. Solutions to Problems.



To understand how the Monitor works, it is best to know what each circuit does and how each circuit relates to the other circuits.
The Block Diagram is presented in a simplified view and a comprehensive view to accomplish the goal of understanding the whole unit.
Once the general picture is clear, the complexity of each circuit will be easier to understand.

The Circuit Description is also written in two views, a simplified view and a detailed view to help give the reader a clear understanding of what each component does. This understanding is most helpful for the more complex problems or multiple problems that sometimes occur.

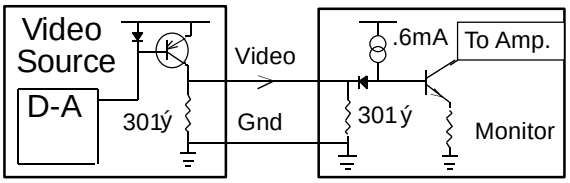
The Trouble Finder section is made up of an index, which lists symptoms of problems, and a list of possible solutions. Part of this section also deals with setting up conditions which make it easier to trouble shoot specific circuits such as the power supply.

TABLE OF CONTENTS

INPUTS

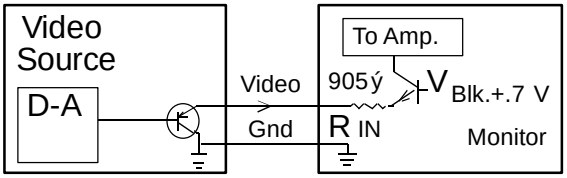
1. Standard Video Configurations, available, are:

A. Positive Analog



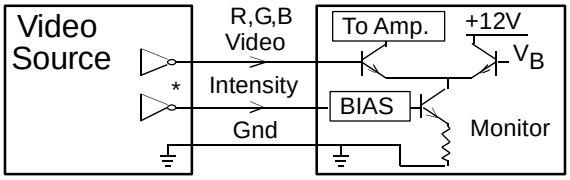
		1492 & 2092		
		Min.	Typ.	Max
Source only	Black level	0V	0V	.05V
	Saturated color	3.1V	3.2V	3.3V
Source and Monitor	Black level	.06V	.09V	.15V
	Saturated color	1.61V	1.69V	1.75V

B. Negative Analog



Red & Green	Black level	5.4V	5.6V	5.8V
Blue	Black level	4.85V	5.05V	5.25V
	Saturated color	.7V	.9V	1.1V

C. 4 Line TTL

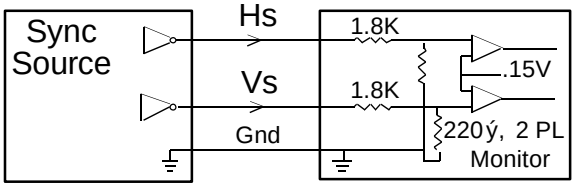


Black level	0V	.2V	.5V
Color on	2.7V	3.5V	6.0V
Low intensity	0V	.2V	.4V
Full intensity	4.5V	4.6V	4.8V

* No pullup resistor on intensity line.

Note: RS170 and other voltage combinations optional for analog video.

2. The Sync signals may be of either polarity and separate or composite.



For composite sync, vertical and horizontal sync lines are connected together.

High input voltage	2.2V	3.5V	20V
Low input voltage	-2.7V	.30V	.80V
Horizontal sync pulse	1.5uS	4.5uS	31uS
Vertical sync pulse	120uS	.5mS	1.5mS
Horizontal frequency	15.3KHz	15.6KHz	15.9KHz
Vertical frequency		60Hz	65Hz
	45Hz	50Hz	

3. The Power to the monitor is to be supplied by a secondary winding of an isolation transformer.

	Model 1492			Model 2092		
	Min.	Typ.	Max.	Min.	Typ.	Max.
115VAC 50Hz or 60Hz	85VAC	115VAC	145VAC	90VAC	115VAC	145VAC
230VAC 50HZ or 60Hz	170VAC	230VAC	290VAC	180VAC	230VAC	290VAC
Power	32W	44W	60W	30W	50W	67W

4. The remote Controls are located on a separate PCB for easy access.

	Model 1492		Model 2092	
	Min.	Max.	Min.	Max.
H SIZE----------Horizontal raster size	9.9"	11.4"	14.8"	16.3"
V SIZE----------Vertical raster size	6.3"	10.3"	10.0"	14.0"
V RAS. POS.-----Vertical raster position	0"	.44"	0"	.60"
H POS-------Horizontal picture position*	.9" Right	2" Left	1.2 right	2.8" left
M GAIN----------Master gain	Dark Screen	Light Screen	Dark Screen	Light Screen

The board Controls are located on the main PCB, and are:
Focus on the flyback transformer and an optional Horizontal hold control.

* For start of horizontal sync 1.7uS after end of picture.

5. Picture

Video response is measured at the tube socket, using low capacitance coupling. The input signal should be fully damped and faster than the expected response.

	Model 1492			Model 2092		
	Min.	Typ	Max.	Min.	Typ	Max.
Rise time	35nS	44nS	49nS	37nS	46nS	52nS
Fall time	32nS	42nS	47nS	35nS	44nS	50nS
Overshoot	0%	0%	2%	0%	0%	2%
Band width	DC	to	8MHz	DC	to	8MHz
Horizontal blank time	12.4uS	12.9uS	13.4uS	12.4uS	12.9uS	13.4uS
Vertical blank time	20H	1.28mS	20H	20H	1.28mS	20H
Horizontal linearity		1%	2%		1%	2%
Vertical linearity		1%	2%		1%	2%
Pincushion		1%	2%		1%	2%

6. Picture tube

	Model 1492		Model 2092	
	Inch	mm	Inch	mm
Useful diagonal	13	328	20	508
Useful horizontal	10.83	275	16	406.6
Useful vertical	8.13	206.5	12	304.8
Useful area	86□	558□	192□	1,239□
Spacing between dot/line trios	.015	.39	.029	.74
Horizontal resolution	680 Pixels		550 Pixels	
Vertical resolution	240 Pixels		240 Pixels	
Interlaced	480 Pixels		480 Pixels	
Deflection angle	90°		90°	
Light transmission at center of glass	Approximately 46%		Approximately 46%	

CRT also features: Enhanced contrast, Internal magnetic shield, and X-Ray output Less than .3mR/hour.

7. Environmental

	Model 1492		Model 2092	
Operating temperature	0° C	70° C	0° C	70° C
Storage temperature	-20° C	85° C	-20° C	85° C
Operating humidity	20%	80%	20%	80%
Storage humidity	10%	95%	10%	95%

The "Drive Signals To The Monitor Input" form is included here for those people who have problems interfacing their drive electronics with the Ceronix Monitor.

DRIVE SIGNALS to the MONITOR INPUT
voltage and waveforms, work sheet.

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Auburn, CA, USA 95602-2055

Company name: _____
Date: _____
Drive signal source
Model number: _____

VIDEO:

For the following measurements use an oscilloscope.

	RED	GREEN	BLUE
With no load the black level voltage is:			
With no load the saturated color voltage is:			

With 301ý load
or other _____ý load.
To GND, or to
voltage_____V.

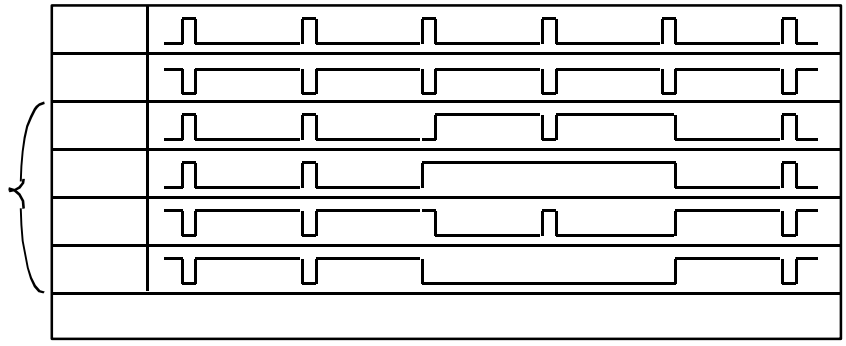
the black level voltage is:			
the saturated color voltage is:			

If available, sketch the video drive circuit on the back of a copy of this form.

Horizontal or composite sync:

Horizontal frequency: _____ Hz "High" voltage: _____ V
Horizontal sync pulse time: _____ uS "Low" voltage: _____ V

Compare your sync to this table and check the best fit.



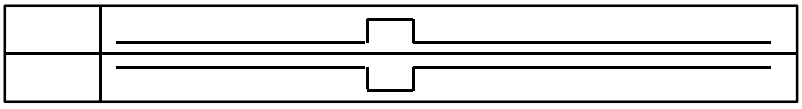
For composite sync.

Sketch if different.

Vertical sync:

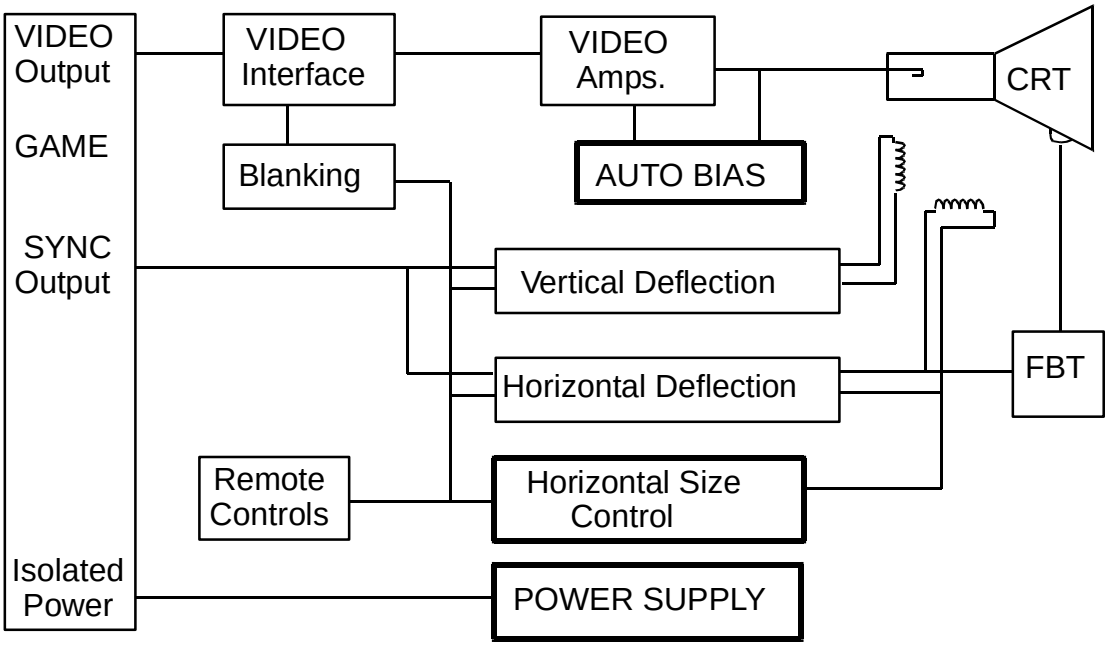
Vertical frequency: _____ Hz "High" voltage: _____ V
Vertical sync pulse time: _____ uS "Low" voltage: _____ V

Check correct polarity.



Complete form and send to: CERONIX, 12265 Locksley Lane
If there are any questions, call (530) 888-1044. Auburn, CA. 95602-2055

1492 and 2092 Simplified Block Diagram



This block diagram gives a broad view of the circuit organization of the 1492 and 2092 monitors. The blocks with the bold outline represent circuits that are quite different than most other monitors.

The auto bias circuit is designed to actively compensate for picture tube and circuit drift which normally cause the color balance to become unbalanced and also brightness variation. This circuit eliminates the need for the color setup procedure.

The horizontal size control circuit permits the horizontal size to be adjusted from a remote control board instead of a coil on the main board. It is also used to compensate for pincushion distortion and acts as an anti-blooming circuit by correcting for horizontal size variations which are caused by the additional load on the flyback transformer under high beam current conditions.

The 1492 and 2092 power supplies differ from most other monitors because of their high efficiency switching mode power supply. It is not difficult to troubleshoot if the techniques presented in this manual are clearly understood. Careful reading of all the information presented in this manual will make trouble shooting of the CERONIX monitor no more difficult than any other monitor and maybe even easier.

Refer to the block diagram on page 13 (foldout) when reading this description.

A

The Video Interface is designed around a custom IC and will accept positive or negative analog video signals and also 4 line TTL. This IC also has a built in multiplier circuit for the master gain control and blanking. Resistors are used to protect the IC and to set the gain. The programmed gain is dependent on the input signal amplitude except on TTL. Solder jumpers are used to program the Video Interface for the type of input signal to be received. The output of the IC drives the video amplifiers. This drive is a current where 0 mA is black and 4.5 mA is a saturated color.

B

The Video Amplifiers are of the push pull type. They are built partly on thick films and partly on the PCB. Spreading out the amplifier reduces the component heat and improves the life of the unit. The bandwidth is 8 MHz with 60Vp-p output. The rise and fall times are .04uS.

C

The Beam Current Feedback circuit directs most of the beam current of each amplifier to the beam current buffer. The only time this current is measured by the auto bias circuit is during the time of the three faint lines at the top of the screen and three lines thereafter. The auto bias circuit is designed to adjust the video amplifier bias voltage such that the beam current of each of the three guns is set (programmed), at this time.

D

The Beam Current Buffer converts the, high impedance low current, beam current signal into a low impedance voltage. This voltage is applied to the auto bias IC through a 200 ohm resistor. After the three lines of beam current are measured, the program pulse from the auto bias IC, produces a voltage drop across this 200 ohm resistor that equals the amplitude of the beam current voltage.

E

The Auto Bias IC is a combination of digital and analog circuitry. The digital part is a counter and control logic which steps the analog circuits through a sequence of sample and hold conditions.
The analog part uses a transconductance amplifier to control the voltage on a 10uF capacitor (one per gun). This voltage is buffered and sent to the video amplifiers as the bias voltage. In monitors without auto bias, this voltage has to be set manually using a setup procedure to set the color balance. With the auto bias, the color balance is set during the end of each vertical blanking time.

The control sequence is:

1. Grid pulse on G1 causes cathode current (3 lines top of screen) which is transmitted by the beam current feedback to the beam current buffer where it is converted to a voltage and applied to the auto bias input pin.
2. Auto bias IC outputs a reference voltage at its input pin which sets the voltage across the coupling capacitor. This coupling capacitor voltage is directly dependent on beam current.
3. After the grid pulse is over, the program pulse matches the

   voltage from the beam current buffer. If the voltage from the beam current buffer, during the grid pulse, is the same as the voltage from the program pulse, the bias is correct and no bias

F

The aging of the picture tube (CRT) not only affects the balance of the cathode cutoff voltage, which is corrected by the auto bias circuit, but it also affects the gain of the CRT. The Auto Bright circuit actively corrects for CRT gain changes by sensing any common bias change from the auto bias circuit and adjusts the screen voltage to hold the average bias voltage constant. The lower adjustment on the flyback transformer is used to set the auto bright voltage to the center of its range. This sets up a second control feedback loop to eliminate picture variation due to the aging of the picture tube.

G

The CRT is a 90° deflection type color picture tube with a 25KV EHT and has integral implosion protection.

H

Blanking is accomplished by setting the gain of the interface IC to zero during blank time. The Horizontal Blanking pulse is generated by amplifying the flyback pulse. The Vertical Blanking pulse is started by the vertical oscillator and ended by the counter in the auto bias IC via the "bias out" pulse. The Master Gain control, located on the remote PCB, sets the gain of the video signal when blanking is not active. The Beam Current Limiter circuit, which is designed to keep the FBT from overloading, will reduce the video gain if the average beam current exceeds .75mA.

I

The Sync Interface can be made to accept separate or composite sync. Two comparators are used to receive sync, one for vertical sync and the other for horizontal sync. Resistor dividers are used to protect the comparator IC from over voltage damage.

J

The Vertical Control circuit consists of:

1. Vertical sync circuit.
2. Vertical oscillator.
3. Linear ramp generator.
4. Output control and bias circuits for controlling the power driver.

The active components that make up these circuits, except for part of the bias circuit, are located in the deflection control IC (LA7851). The vertical sync circuit is capable of accepting either positive or negative going sync pulses without adjustment. The vertical oscillator in the LA7851 is set at 45 Hz and will sync up to 65 Hz without adjustment. The deflection yoke is driven with a linear current ramp which produces evenly spaced horizontal lines on the raster. This linear ramp is generated by supplying a 1uF capacitor with a constant current. The vertical output voltage is held within range (biased) by a timer which partly discharges the 1uF ramp capacitor at the start of vertical retrace. The duration of the timer is controlled by the vertical output voltage and the vertical auto bias circuit.

K

The Vertical Auto Bias circuit greatly increases the range of the bias circuit built into the LA7851. It is made up of a negative peak detector and an amplifier which outputs current to the normal bias circuit, but with a much lower frequency response. This then eliminates the need for adjustments during production and permits the use of 50Hz and 60Hz vertical sync with only a size adjustment on the remote control board.

L

The Vertical Output circuit (LA7830) is a power driver which drives the vertical deflection yoke. It also has a special pump up circuit which doubles the output voltage during vertical retrace. This voltage doubler also doubles the efficiency of the circuit since the high retrace voltage is not present across the power driver during the trace time.

M

The Horizontal Control incorporates a variable sync delay and a phase locked loop to generate the horizontal timing. The H POS. adjustment on the remote control board sets the sync delay time which controls the picture position. The phase locked loop uses the flyback pulse to generate a sawtooth wave which is gated with the delayed sync pulse to control the horizontal oscillator.

N

The Horizontal Driver supplies the high base current necessary to drive the horizontal output transistor which has a beta as low as three.
It also protects the horizontal output transistor since it is a transformer and cannot keep the base turned on for longer than its inductive time constant.

O

The Horizontal Output transistor is mounted to the rear frame which acts as a heat sink. The collector conducts 1,000 volt flyback pulses which should not be measured unless the equipment is specifically designed to withstand this type of stress. A linear ramp current is produced in the horizontal yoke by the conduction of the horizontal output transistor (trace time).
A fast current reversal (retrace time) is achieved by the high voltage pulse that follows the turn off of the horizontal output transistor. This pulse is due to the inductive action of the yoke and flyback transformer.

P

The main function of the Flyback Transformer (FBT) is to generate a 25,000 volt (EHT) potential for the anode of the picture tube. This voltage times the beam current is the power that lights up the phosphor on the face of the picture tube. At .75mA beam current the FBT is producing almost 19 watts of high voltage power. The FBT also sources the focus voltage and the filament power. The FBT has a built in high voltage load resistor which stabilizes the EHT, for the low beam current condition. This resistor also discharges the EHT, when the monitor is turned off, which improves the safety of handling the monitor.

Q

The Remote Control PCB houses the:

CONTROL	DESCRIPTION	CIRCUIT
1. H SIZE	Horizontal raster size	Diode modulator
2. V SIZE	Vertical raster size	Vertical drive
3. V RAS. POS.	Vertical raster position	DC current to V. yoke
4. H POS	Horizontal picture position	H. sync delay
5. M GAIN	Master gain	Video interface

R

The Horizontal Size Control circuit has four inputs:

#	SIGNAL	FUNCTION
1.	Horizontal size ----------	Horizontal size control
2.	Beam current ----------	Blooming control
3.	Vertical linear ramp ----------	(#4)-(#3)=Vertical parabolic
4.	Vertical parabolic + V. linear ramp	(Pincushion)

The horizontal size control circuit sums the four signals at one node to produce the diode modulator control voltage.

S

The Diode Modulator is a series element of the horizontal tuned circuit. It forms a node between GND and the normal yoke return circuit. If this node is shorted to GND, maximum horizontal size is present. A diode is used to control the starting time of the retrace pulse at this node. The reverse conduction time is dependent on the forward current because the current waveform at this node has to exceed the forward current in the diode. A diode, placed in series with the yoke, is then used to control the retrace pulse amplitude across the yoke. The horizontal size, therefore, is controlled by controlling the current to this diode via the horizontal size control circuit.

T

A Voltage Doubler is used in the power supply for two reasons:

1. To improve the efficiency of the power supply.
2. To permit 120 volt and 220 volt operation. For the 220 volt operation the voltage doubler is replaced with a bridge rectifier.

U

The Switching Regulator is synchronized to the horizontal pulse and drives a power MOSFET. Unlike most regulators that have a common GND, this power supply has a common V+ and current is supplied from V- to GND. The MOSFET is connected to V- and signal ground (GND) through a transformer which is used as an inductor for series switchmode regulation. An operational amplifier, voltage reference, comparator, and oscillator in the power supply controller IC are used to accomplished regulation by means of pulse width modulation.

The transformer has two taps on the main winding which are used to generate the +16 volt and +24 volt supplies. It also has a secondary which is referenced to V- and supplies the power supply. Since the power supply is generating its own power, a special start up circuit is built into the power supply controller IC that delays start up until its supply capacitor is charged up enough to furnish the current to start the power supply. This capacitor is charged with current through a high value resistor from the raw dc supply. This is why the power supply chirps when an overload or underload occurs.

V

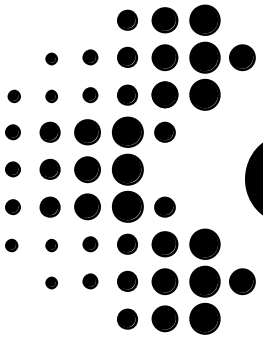
The Load consists of the video amplifiers and the horizontal flyback circuit. The power supply will not operate without the load since the voltage that sustains the power supply comes from a secondary in the power transformer and depends on some primary current to generate secondary current.

W & X

A separate +12V regulator for the video and the deflection circuits are used in this monitor to minimize raster and video interactions. This also simplifies PCB layout, since the video GND loops are separate from the deflection GND loops.

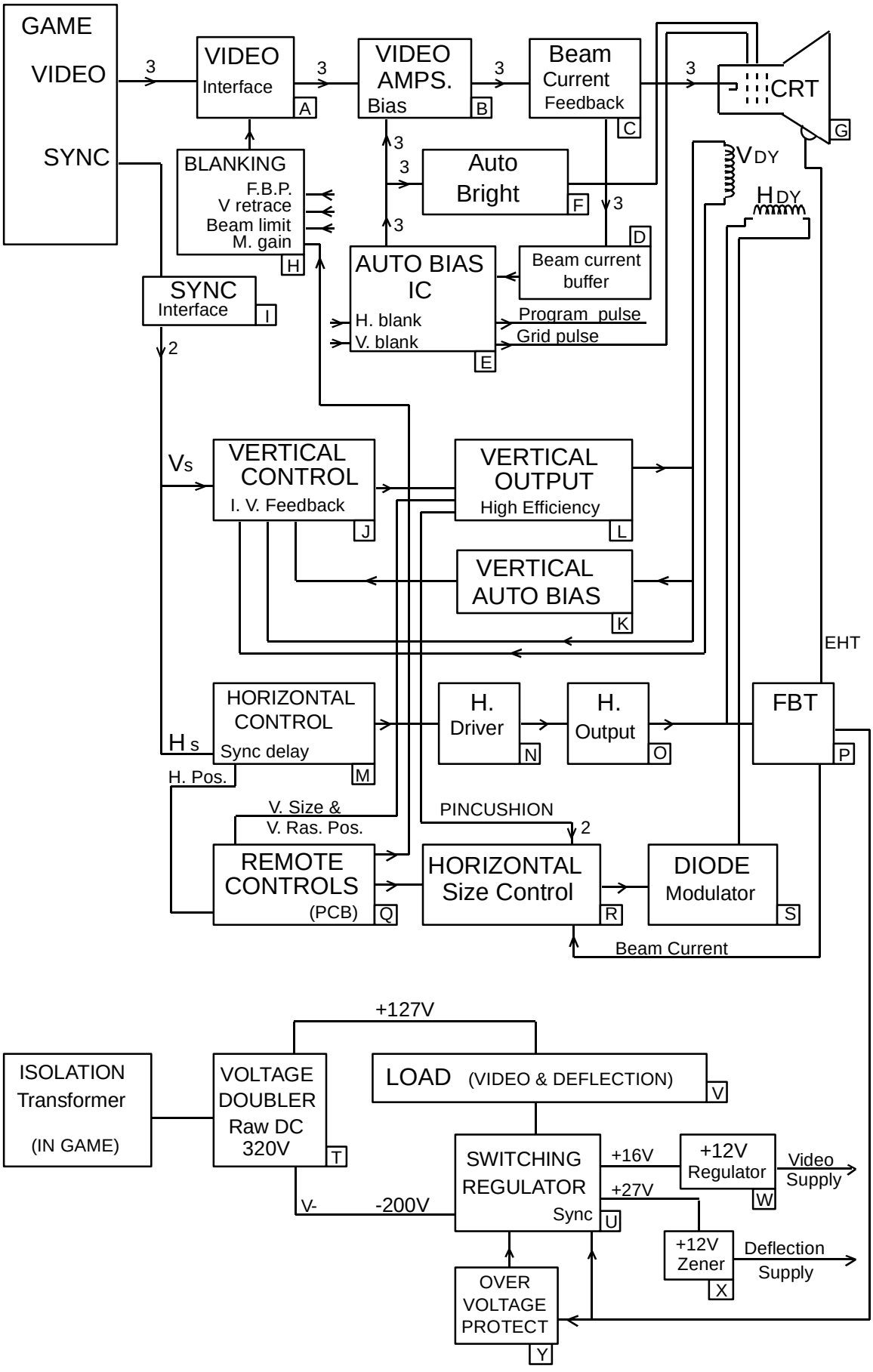
Y

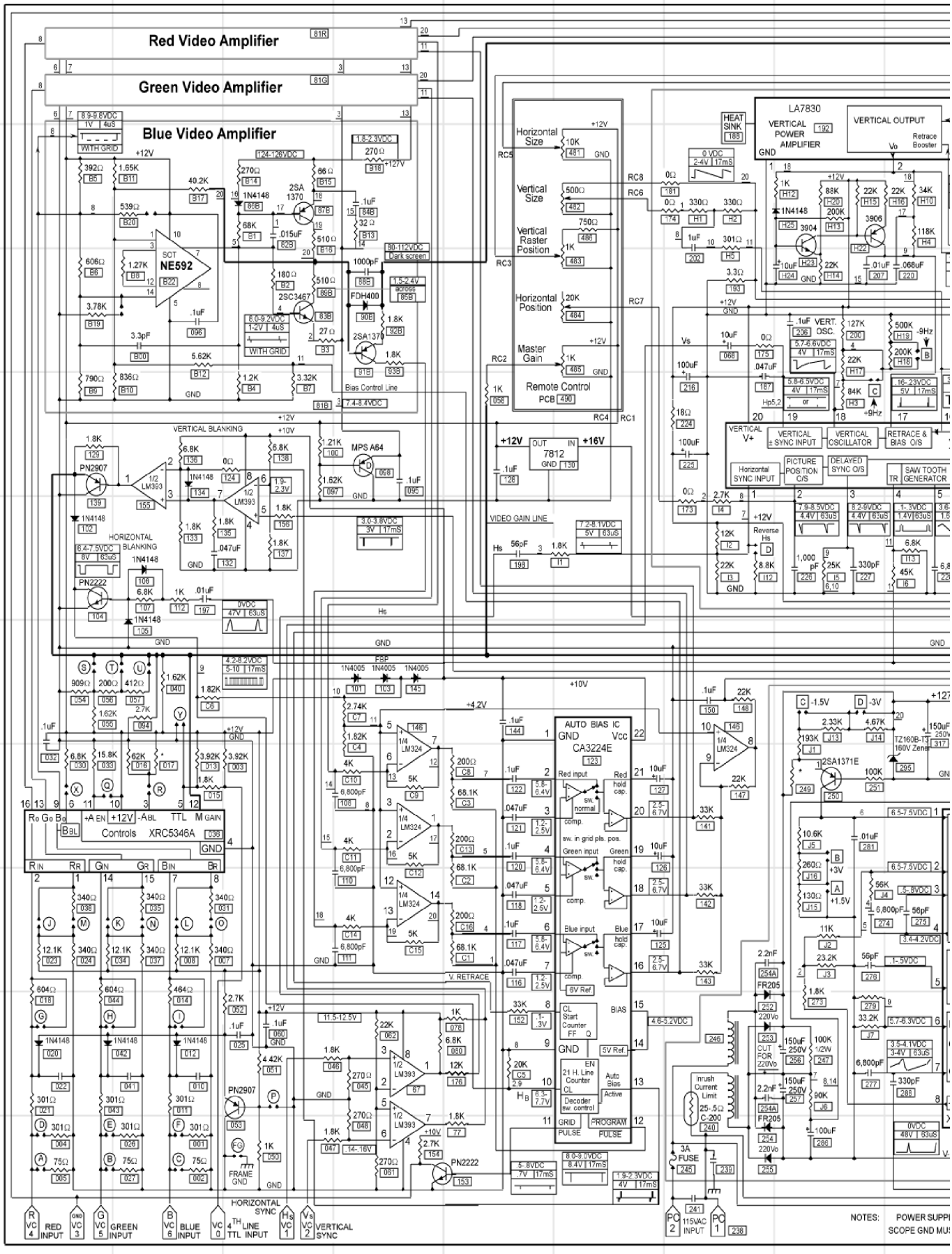
The Over Voltage Protect circuit is built into the power supply and monitors the flyback transformer peak pulse voltage. This circuit will turn off the power supply and hold it off if the EHT exceeds its rated value. This circuit not only provides assurance that the X-ray specifications are met but also protects the monitor from catastrophic failure due to a minor component failure.

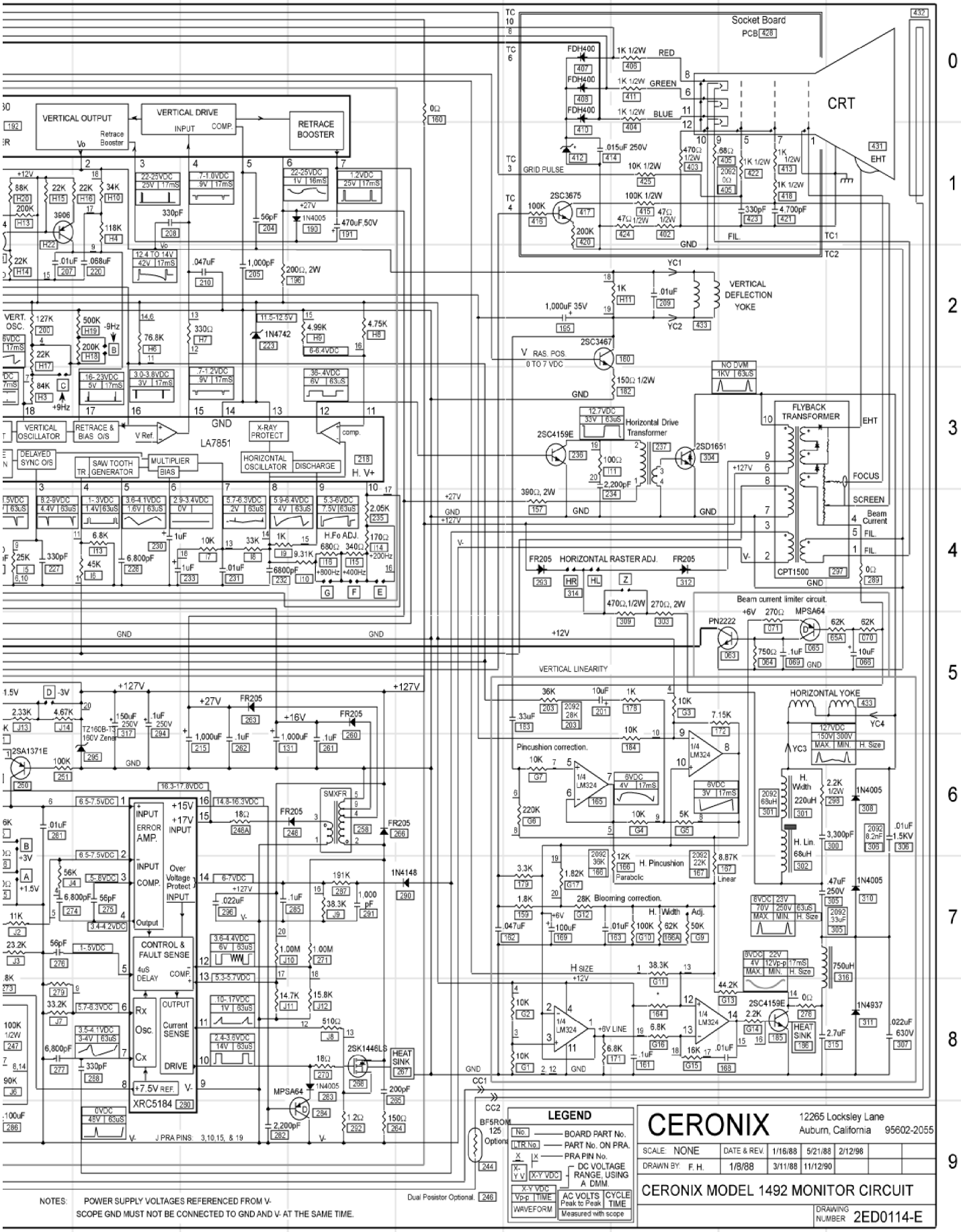


CERONIX

1492 & 2092 Monitor Block Diagram

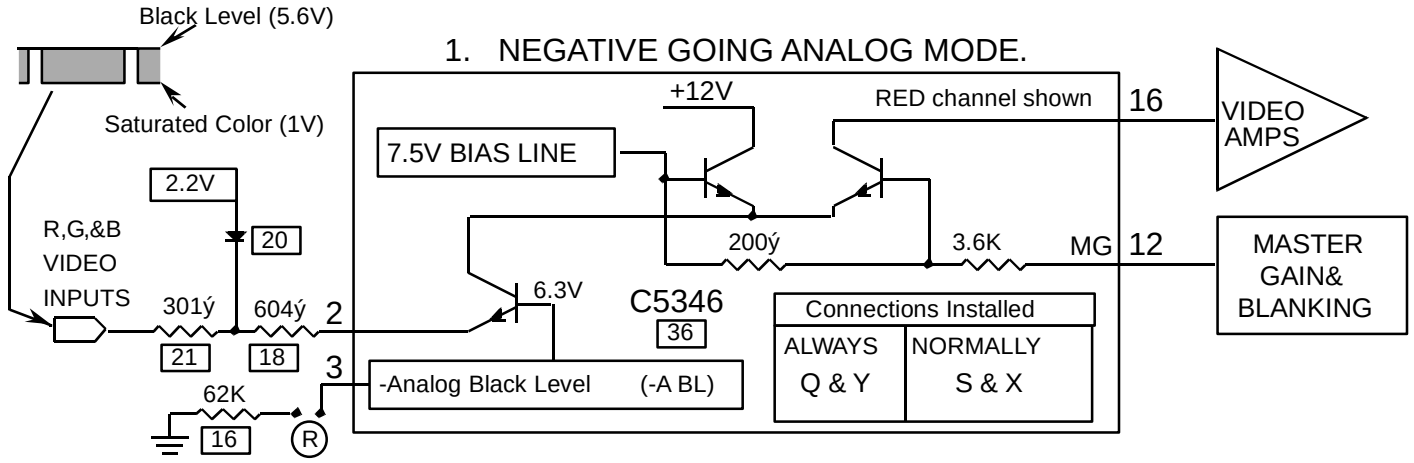



Red Video Amplifier
Green Video Amplifier
Blue Video Amplifier
NE592
2SA 1370
2SC3467
FDH400
2SA1370
LA7830
VERTICAL POWER AMPLIFIER
VERTICAL OUTPUT
Horizontal Size
Vertical Size
Vertical Raster Position
Horizontal Position
Master Gain
Remote Control PCB 490
7812
CA3224E
AUTO BIAS IC
Controls XRC5346A
VERTICAL BLANKING
HORIZONTAL BLANKING
VERTICAL V+
VERTICAL ± SYNC INPUT
VERTICAL OSCILLATOR
RETRACE & BIAS O/S
Horizontal SYNC INPUT
PICTURE POSITION O/S
DELAYED SYNC O/S
SAW TOOTH TR GENERATOR
Bias Control Line
VIDEO GAIN LINE
V. RETRACE
Inrush Current Limit 25-.5Ω C-200
3A FUSE
RED INPUT
GREEN INPUT
BLUE INPUT
LINE TTL INPUT
HORIZONTAL SYNC
VERTICAL SYNC
115VAC INPUT
NOTES:

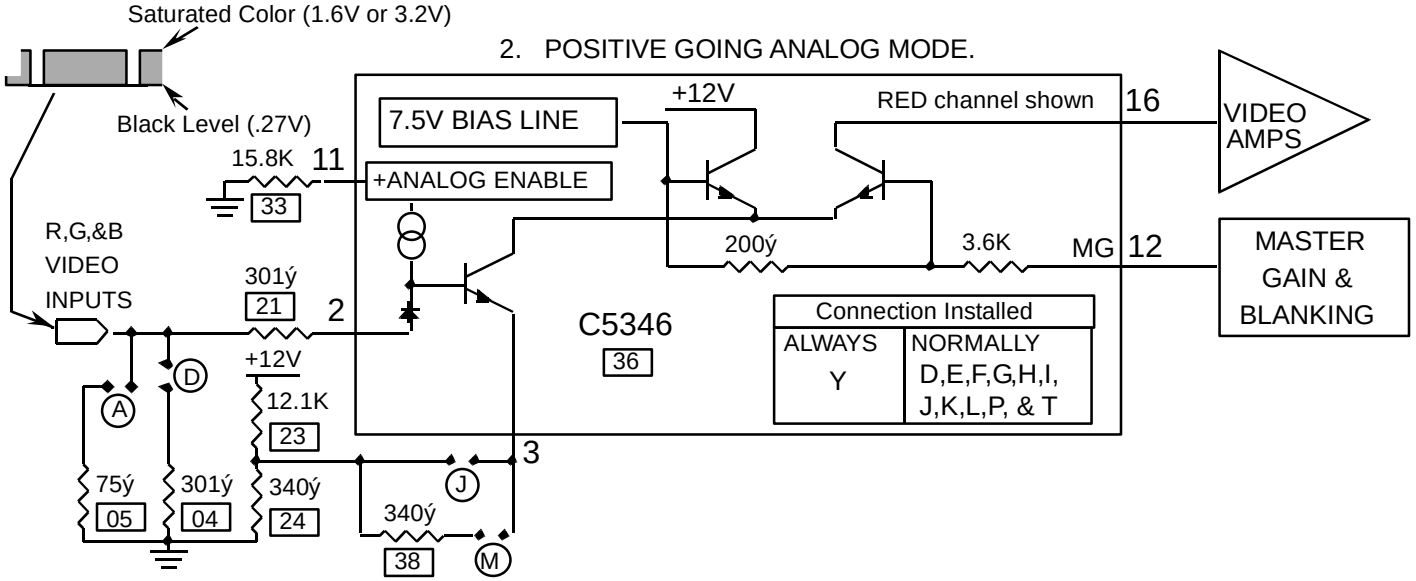

HH II JJ KK LL MM NN PP RR
0 1 2 3 4 5 6 7 8 9
Socket Board
PCB 428
CRT
EHT
GRID PULSE
VERTICAL OUTPUT
VERTICAL DRIVE
RETRACE BOOSTER
VERTICAL OSCILLATOR
RETRACE & BLAS O/S
V Ref.
LA7851
X-RAY PROTECT
HORIZONTAL OSCILLATOR
DISCHARGE
DELAYED SYNC O/S
SAW TOOTH GENERATOR
MULTIPLIER BIAS
H. V+
VERTICAL DEFLECTION YOKE
Horizontal Drive Transformer
FLYBACK TRANSFORMER
FOCUS
SCREEN
Beam Current
HORIZONTAL RASTER ADJ.
Beam current limiter circuit.
VERTICAL LINEARITY
Pincushion correction.
H. Pincushion Parabolic
28K Blooming correction.
H. Width
H. Lin.
HORIZONTAL YOKE
H SIZE
RAS. POS. 0 TO 7 VDC
HEAT SINK
XRC5184
CONTROL & FAULT SENSE
INPUT ERROR AMP.
Over Voltage Protect
Current SENSE
BF5ROM
Dual Posistor Optional.
LEGEND
BOARD PART No.
PART No. ON PRA.
PRA PIN No.
DC VOLTAGE RANGE, USING A DMM.
AC VOLTS Peak to Peak
CYCLE TIME
Measured with scope
NOTES: POWER SUPPLY VOLTAGES REFERENCED FROM V-
SCOPE GND MUST NOT BE CONNECTED TO GND AND V- AT THE SAME TIME.
J PRA PINS: 3,10,15, & 19
CERONIX
12265 Locksley Lane
Auburn, California 95602-2055
SCALE: NONE
DRAWN BY: F. H.
DATE & REV. 1/16/88 5/21/88 2/12/98
1/8/88 3/11/88 11/12/90
CERONIX MODEL 1492 MONITOR CIRCUIT
DRAWING NUMBER 2ED0114-E

VIDEO INTERFACE CIRCUIT DESCRIPTION (+ & - Analog)

The video interface circuit is a general purpose RGB type input circuit. This circuit connects the external video signal to the video amplifiers. It can accept positive going analog, negative going analog, and 4 line TTL. The particular mode of operation is selected by placing solder bridges on the foil side of the PCB. The solder bridge patterns are given in appendix A. Simplified video interface circuit:



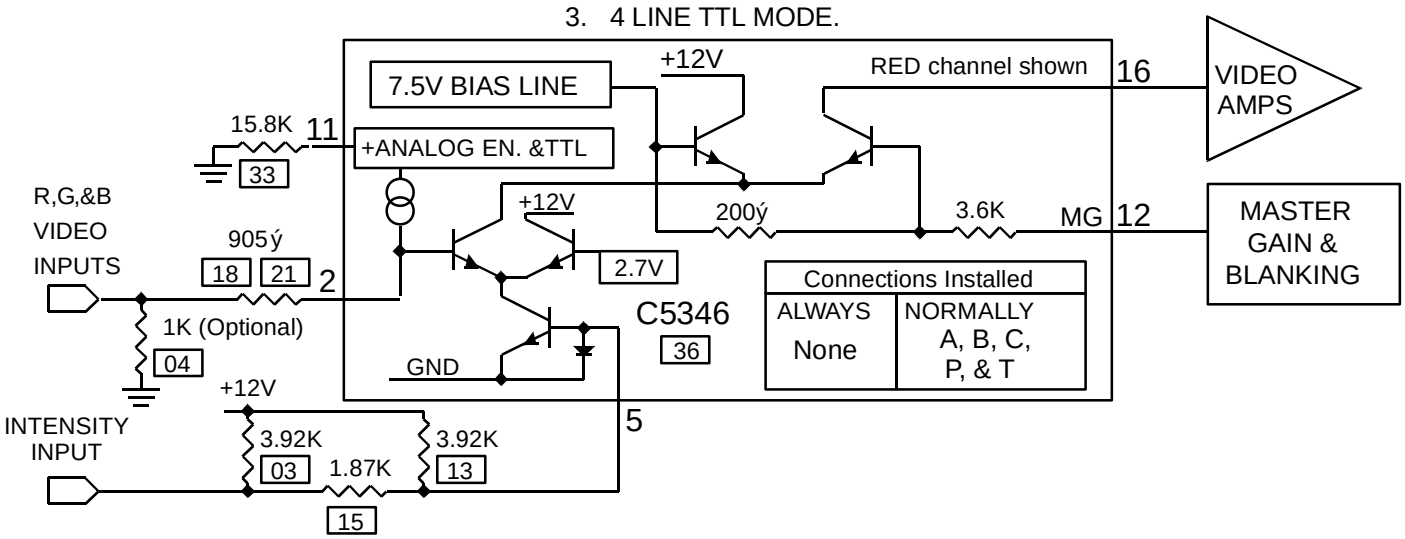
In the negative analog mode, the video signal has a black level which is the -A BL voltage. This voltage is normally 5.6V and may be set to 5.1V by adding solder connection (R). The saturated color is the lowest input voltage (.9V-1.1V). To prevent input line ringing from exceeding the saturated color voltage limit, a clamp diode [20] has been added. The current amplitude to the video amplifiers is defined by resistors [21] [18] and the master gain voltage.



In the positive analog mode, a bias current flows to the input which is set by resistor [33] at the +Analog Enable input. This current produces a voltage, across the parallel resistance of the (game and [04]) plus resistor [21] at the IC pin 2. Without this bias current the black level input voltage to the C5346 would be 0V and resistor [23] would not be needed. With a bias resistor of 15.8K, the bias current is .6mA. If the external source resistance is 300 ohms, the black level voltage at pin 2 is .27V. A black level voltage of .3V is set by resistor divider [23] [24] to compensate for the bias current voltage drop. The input termination resistor [04] reduces video line ringing and sets a dark screen when the video input connector is disconnected. The saturated color is the highest input voltage. There are two standard, saturated color, voltages available: 1.6V (J) connected and 3.2V (M) connected.

VIDEO INTERFACE CIRCUIT DESCRIPTION (TTL)

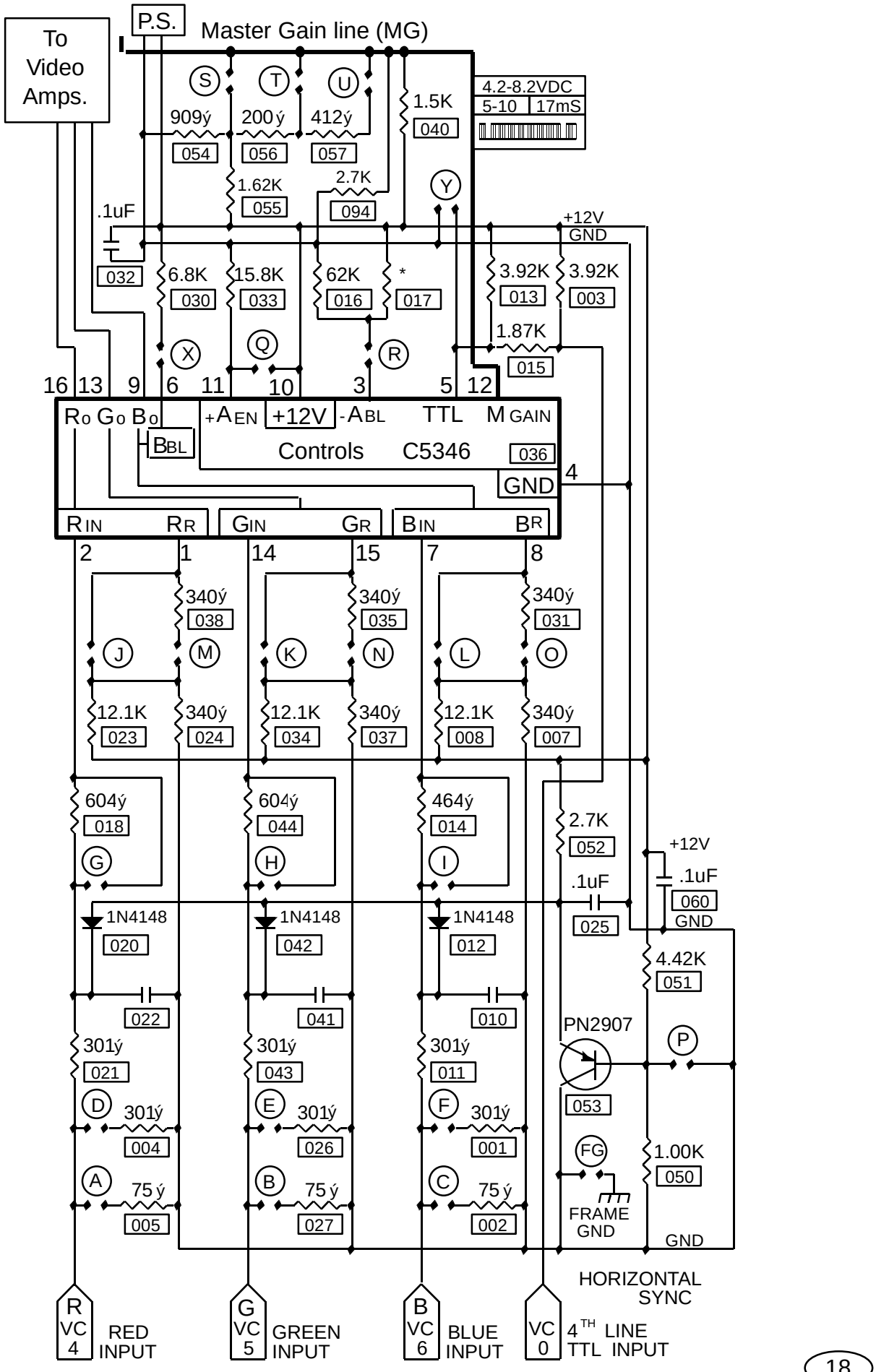
3. 4 LINE TTL MODE.



In the 4 line TTL mode the red, green, and blue video lines will pass color when high. The intensity of the color is set by the fourth TTL line. Saturated color is displayed when the intensity line is high or open, and when it is low, the displayed color is half intensity. Although the R, G, and B lines are logic lines, the intensity line is an analog line. To insure full saturated color, the TTL driver to the intensity line should have no other loads. The, 1K to GND, input resistor on the color lines may be installed to keep the screen dark when no video input cable is connected. The logic 0 voltage at the input is 0 to .4V @ .6mA. The logic 1 voltage at the input is 2.7V to 5.5V @ -2.1mA with the 1K pulldown and .6mA without.

Refer to the video interface schematic to the right for the following component description. Both the blanking and the gain control is accomplished by the Master Gain line to the video interface IC (C5346 pin 12). Resistors 054 055 056 057 & 094 provide five programmable voltages for setting the max. MG voltage. The video gain is also affected by each of the input modes. Resistors 021 018 043 044 011 and 014 set the video gain for the -Analog mode and provide protection to the video interface IC inputs in the +Analog and TTL modes. Resistors 014 and 030 modify the blue video response in the Analog mode. The video gain, for the +Analog mode is set by resistors 023 024 038 034, 037, 035, 008, 007, and 031. The TTL video gain is set by resistors 003 013 and 015. In the +Analog mode, G, H AND I are bridged to reduce the offset voltage caused by the bias current. Also, input termination resistors 004 026 and 001 used to improve input line matching. In the TTL mode resistors 005 027 and 002 may be 1K & programmed in. A clamp circuit is used in the -Analog mode to reduce the effect of line ringing. Resistors 050 and 051 provide a reference voltage which is buffered by PNP transistor 053 load resistor 052, capacitor 025 and applied to diodes 020 042 and 012 to perform this clamping function. P is bridged to reference the clamp to GND for the +Analog and TTL modes. Resistor 016 is used to set the -Analog black level lower than 5.6 volts. If the -Analog black level is set below 4.9 volts, both resistors 016 017 are used to override the chip resistor tolerance. The black level for the blue channel may be increased for all modes by connecting resistor 030 The C5346 036 has, built in, separate circuits for each of the three input modes. These modes are selected by bridge points Q & Y.

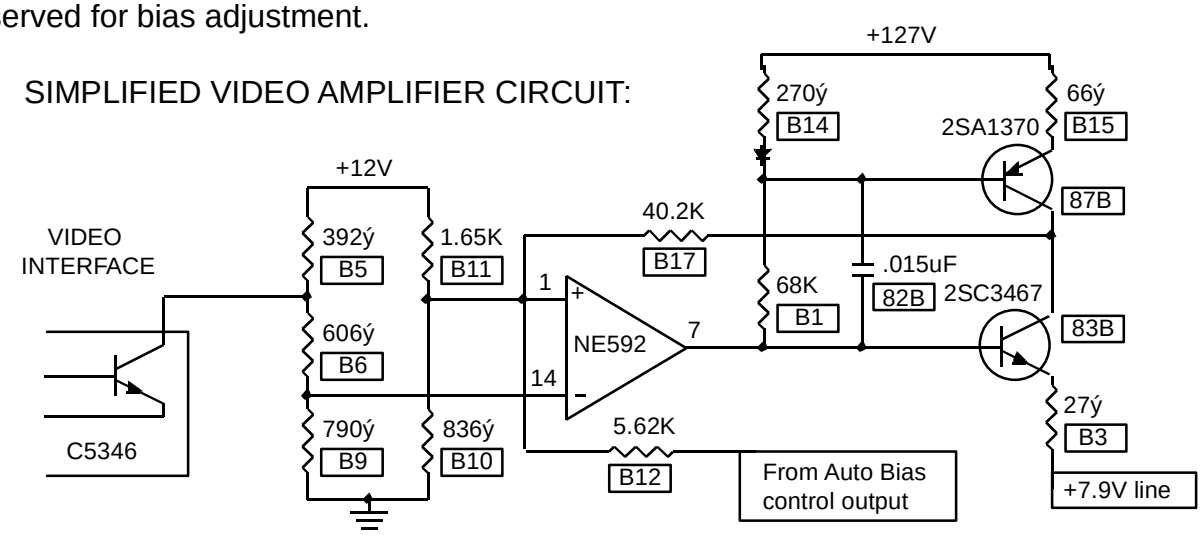
VIDEO INTERFACE SCHEMATIC



VIDEO AMPLIFIER CIRCUIT, FUNCTION, DESCRIPTION

The video amplifier, is a high speed push pull amplifier, which can swing as much as 92 volts. The maximum dynamic output swing is limited to 60 volts. The rest of the output voltage range is reserved for bias adjustment.

SIMPLIFIED VIDEO AMPLIFIER CIRCUIT:



The video amplifier's output voltage, With no input signal, is the black level which is the picture tube cut off voltage. This voltage is set for each of the three video amplifiers by the auto bias circuit. This black level voltage has a range of 80V to 112V.

The voltage swing at the output is 60 volts for a 4.3 mA current signal from the C5346. For this same 4.3 mA current signal the voltage swing at the video amp. input is 1.32 volts and the -input voltage swing at the NE592 is .75 volts. The reason for using the voltage matching resistor B6 is that the C5346 minimum output voltage is 7.7 volts, and the bias voltage at the NE592 input is 5.3 volts.

VIDEO AMPLIFIER CIRCUIT DESCRIPTION

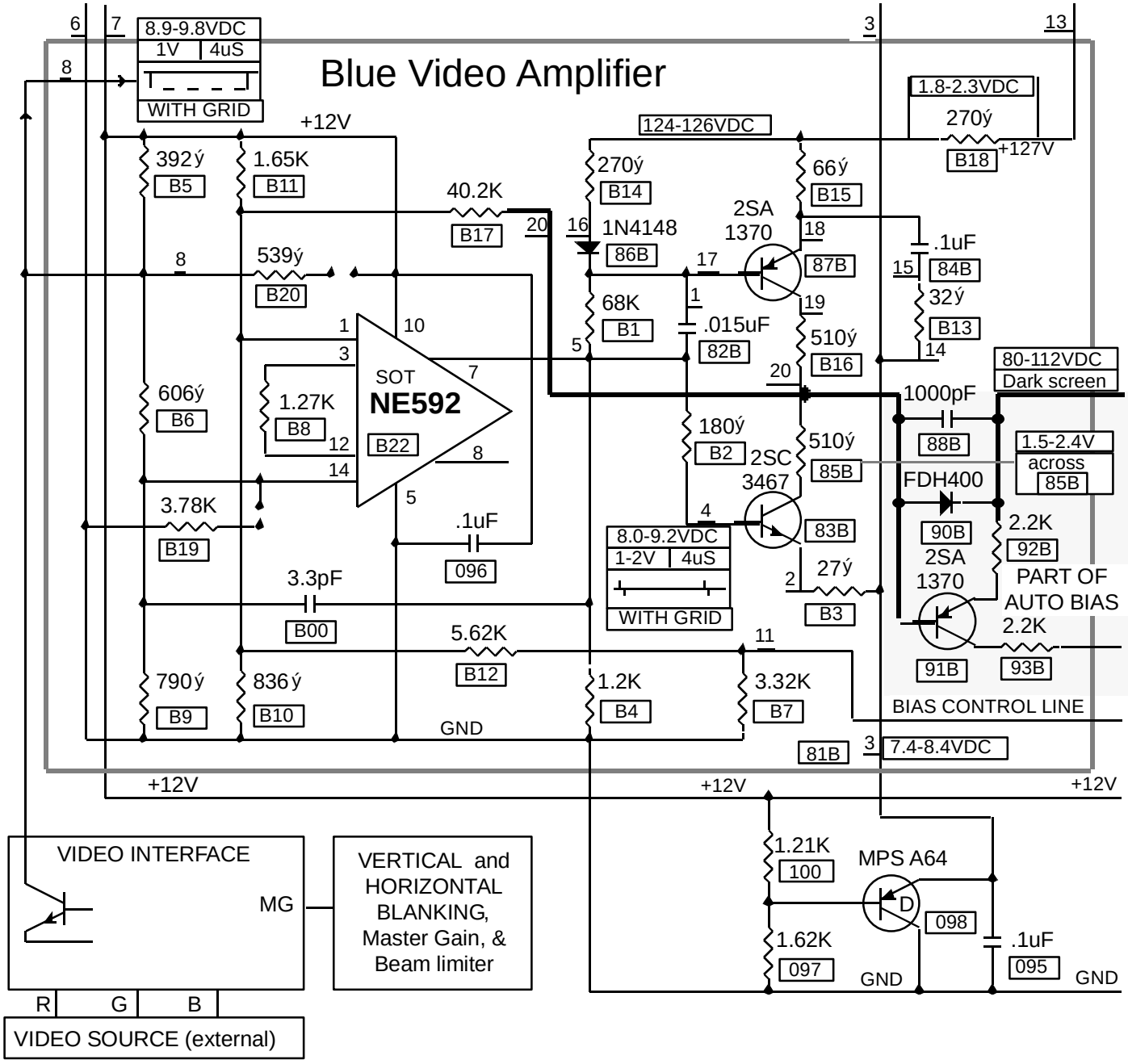
The control circuit for the video amplifier is located on the B PRA (B precision resistor array). The B PRA includes all the Bxx esistors and the NE592. All of the parts labeled RxxR xxG, and xxB, are components located on the circuit board, which are part of the red, green, and blue video amplifiers.

The video amplifier's stability and precise response to the input signal comes from a combination of the geometric layout of the B PRA and the high frequency response of the NE592. The NE592 stabilization capacitor B00 s an integral part of the B PRA conductor layout. Resistor B4 B 4 is used to boost the NE592 drive current to the PNP transistor 87B. The NE592 bias circuit, at the input side, consists of B 5 B5 B6 nd B 9 B9 The negative feedback bias resistors are, B B11 B B10 and B B12 with B B17 s the output feedback resistor. Resistors B B19 nd B B20 re connected to solder pads which, when bridged, permit the 1492 B PRA to be used on the models 1490 and 1491 monitors.

The NE592 gain is set by resistor B8 The drive signal from the NE592, B22 n 7, is coupled to the base of the NPN transistor 83B hrough an impedance matching resistor B2 B2 This drive is also coupled to the base of the PNP transistor 87 87B a a coupling capacitor 82B 82B The NE592 output voltage range is 6V to 10V, which is the reason for the 7.9 volt NPN bias line. The 7.9 volt bias line is generated by buffering a voltage divider, formed by resistors 97 097 and 100, with a PNP darlington transistor 98 098 A capacitor 9 5 095 connected to shunt the high current spikes to GND. This line is common to all three video amplifiers.

The AC current gain is set by resistor B B3 r the NPN output transistor and by B13 B13 for the PNP output transistor which is AC coupled via a capacitor 84B 84B n a positive output transition of the video amplifier, the current of the PNP transistor can go as high as 32mA and on a negative transition the current drops to 0mA

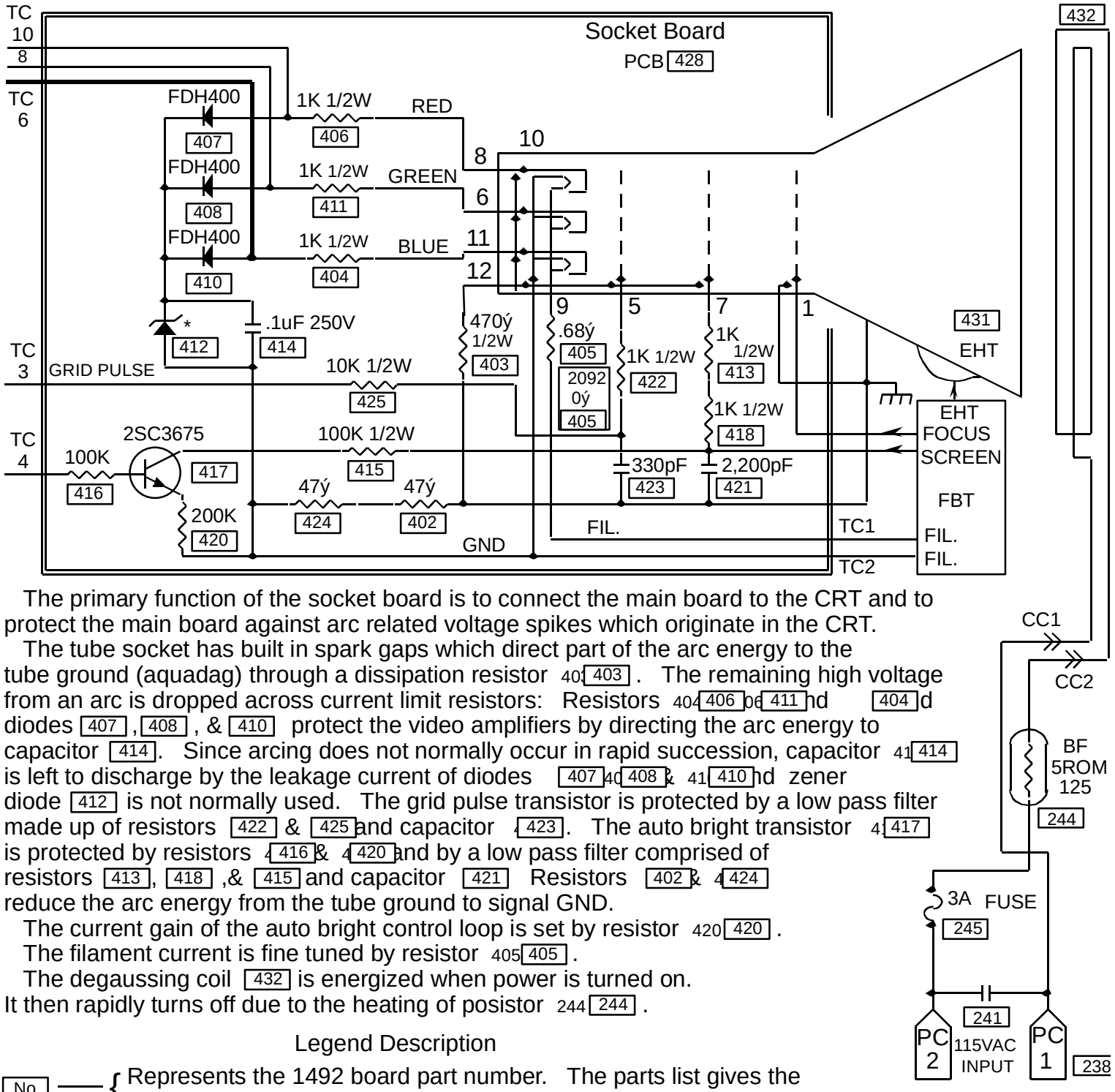
VIDEO AMPLIFIER SCHEMATIC



For low output distortion, the PNP transistor is biased with a 6 mA current. The NPN transistor and resistor B[B17] conduct the PNP bias current to GND. Diode 86B[86B] balances the PNP base to emitter voltage. Resistors [B1] and [B14] set the voltage across B[B15] which define the video amplifier output stage bias current. A quick way to check this current, is to measure the voltage drop across the 510 ohm [85B] The permissible voltage range is listed on the schematic as 1.5-2.4V. The PNP and NPN collector resistors [B16] nd [85B] help stabilize the amplifier and provide some arc protection. Resistor B 18[B18] used to decouple the video amplifiers from the +127V line. Capacitor [096] used to decouple the +12 volt line close to the video amplifiers. If this capacitor or the 7.9V line capacitor [095] pen, the video may be unstable and distorted. Resistor B[B7] s the auto bias output load resistor.

If there is a problem with the video, first check the output waveform of the video amplifier, with the oscilloscope, if ok the problem is not in the video section. If not ok, check the input waveform at B PRA pin 8, if not ok there, check the video interface, If ok at the video amplifier input, refer to this section to help with analyzing the video amplifier problems.

SOCKET BOARD , DEGAUSSING CIRCUIT, AND LEGEND DESCRIPTION



The primary function of the socket board is to connect the main board to the CRT and to protect the main board against arc related voltage spikes which originate in the CRT.

The tube socket has built in spark gaps which direct part of the arc energy to the tube ground (aquadag) through a dissipation resistor 403. The remaining high voltage from an arc is dropped across current limit resistors: Resistors 404, 406, 411 and 404 and diodes 407, 408, & 410 protect the video amplifiers by directing the arc energy to capacitor 414. Since arcing does not normally occur in rapid succession, capacitor 414 is left to discharge by the leakage current of diodes 407, 408, & 410 and zener diode 412 is not normally used. The grid pulse transistor is protected by a low pass filter made up of resistors 422 & 425 and capacitor 423. The auto bright transistor 417 is protected by resistors 416 & 420 and by a low pass filter comprised of resistors 413, 418, & 415 and capacitor 421. Resistors 402 & 424 reduce the arc energy from the tube ground to signal GND.

The current gain of the auto bright control loop is set by resistor 420.

The filament current is fine tuned by resistor 405.

The degaussing coil 432 is energized when power is turned on. It then rapidly turns off due to the heating of posistor 244.

Legend Description

No. — Represents the 1492 board part number. The parts list gives the CERONIX PART NUMBER which is indexed to the board part number.

LTR.No. — Part numbers of the resistors on the PRA indicated by LTR.

X / X — PRA pin number. To determine which PRA the pin number belongs to, look for the nearest PRA part number on that line.

X-Y V / X-Y VDC — DC voltages are measured to GND except in the power supply where V- is the reference. Use a DVM for DC measurements.

X-Y VDC | Vp-p | TIME | WAVEFORM — TIME is the cycle time of the waveform. The waveform is normally checked with a oscilloscope. It has a P-P voltage amplitude of Vp-p.

CAUTION: When making measurements on the power supply be sure that the other scope probe is not connected to GND.

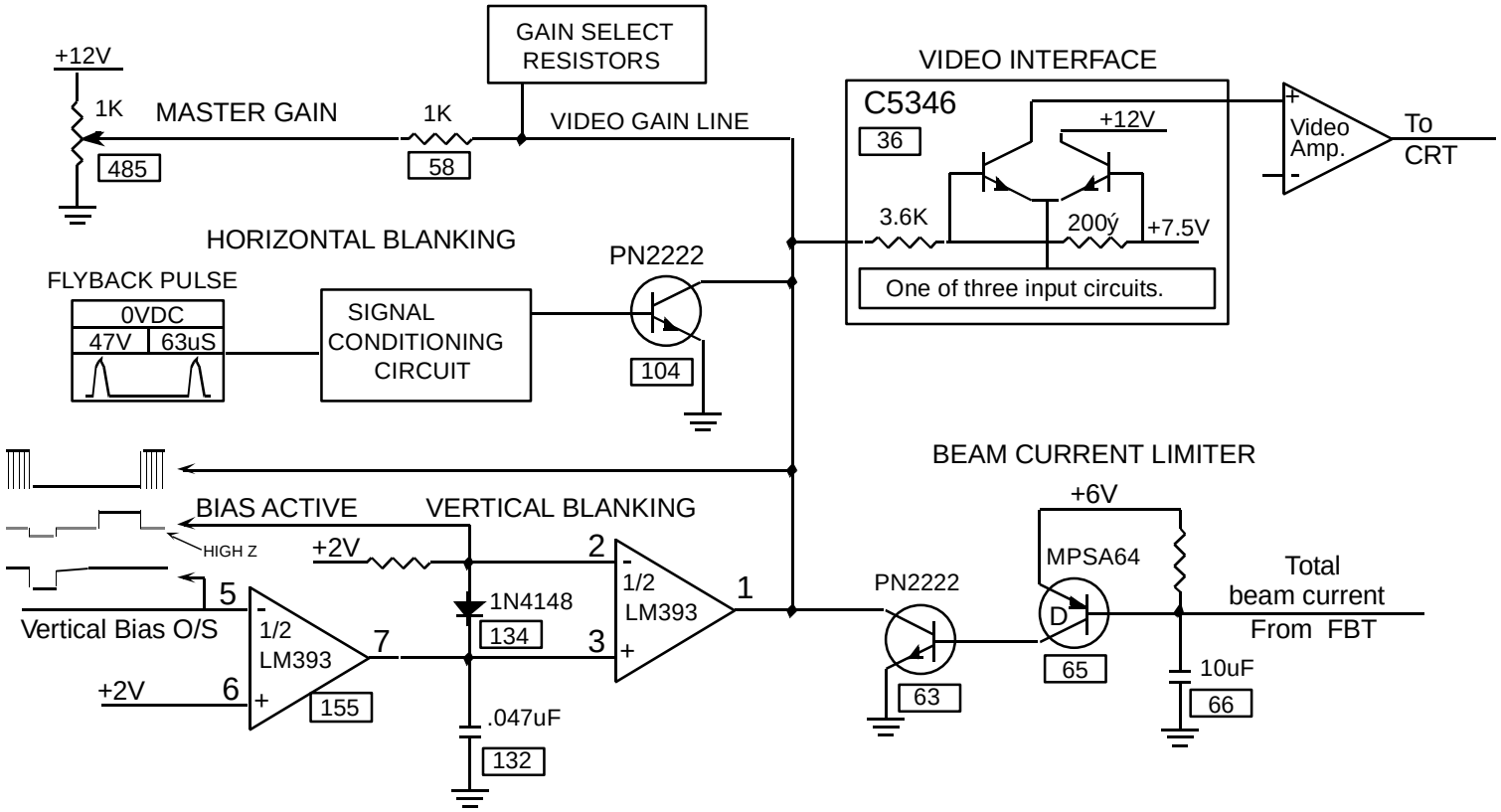
LEGEND

No.	BOARD PART No.
LTR.No.	PART No. ON PRA.
X / X	PRA PIN No.
X-Y V / X-Y VDC	DC VOLTAGE RANGE, USING A DMM.
X-Y VDC / Vp-p | TIME / WAVEFORM	AC VOLTS Peak to Peak | CYCLE TIME; Measured with scope

BLANKING AND MASTER GAIN CIRCUIT, FUNCTION, DESCRIPTION

Blanking in this monitor is accomplished by reducing the video gain to zero during the vertical and horizontal blank time. During video time, the gain is set by the master gain control which is located on the remote control PCB. If the overall beam current exceeds .75mA for more then ten frames, the beam current limiter circuit will reduce the video gain to protect the FBT.

SIMPLIFIED GAIN CONTROL CIRCUIT:



The video P-P voltage amplitude at the cathodes, is the video input signal amplitude times the master gain control setting times the video amplifier gain. The gain select resistors set the maximum video gain via the master gain line. For a greater range of brightness, (highlighting) the video system is allowed to supply high peak video currents which could damage the FBT if sustained. The beam current limiter circuit insures that the long term maximum beam current is not exceeded.

Horizontal blanking is achieved by amplifying the flyback pulse (FBP) with transistor 104 . 104
Vertical blanking starts as soon as the LA7851 starts the vertical retrace sequence and is terminated by the auto bias, bias active signal. A comparator is used to sense the vertical bias O/S, at pin 16 of the LA7851, which goes low when vertical retrace starts. Capacitor 132 132 holds the vertical blanking active, between the vertical bias O/S pulse, and the bias active pulse. When the bias active line goes high, the capacitor 13 132 reset and vertical blanking ends, after the bias active line returns to it's high impedance state.

BLANKING AND MASTER GAIN CIRCUIT DESCRIPTION

The master gain control 485 is connected to the video gain line through a 1K resistor 58. The voltage range of the video gain line is programmable via resistor 094 094 and solder bridges at S, T, & U which may connect resistors 54 54 55 55 56 56 and 57 57 to the video gain line. This arrangement permits a variety of input signals and picture tubes to be used with the same monitor PCB.

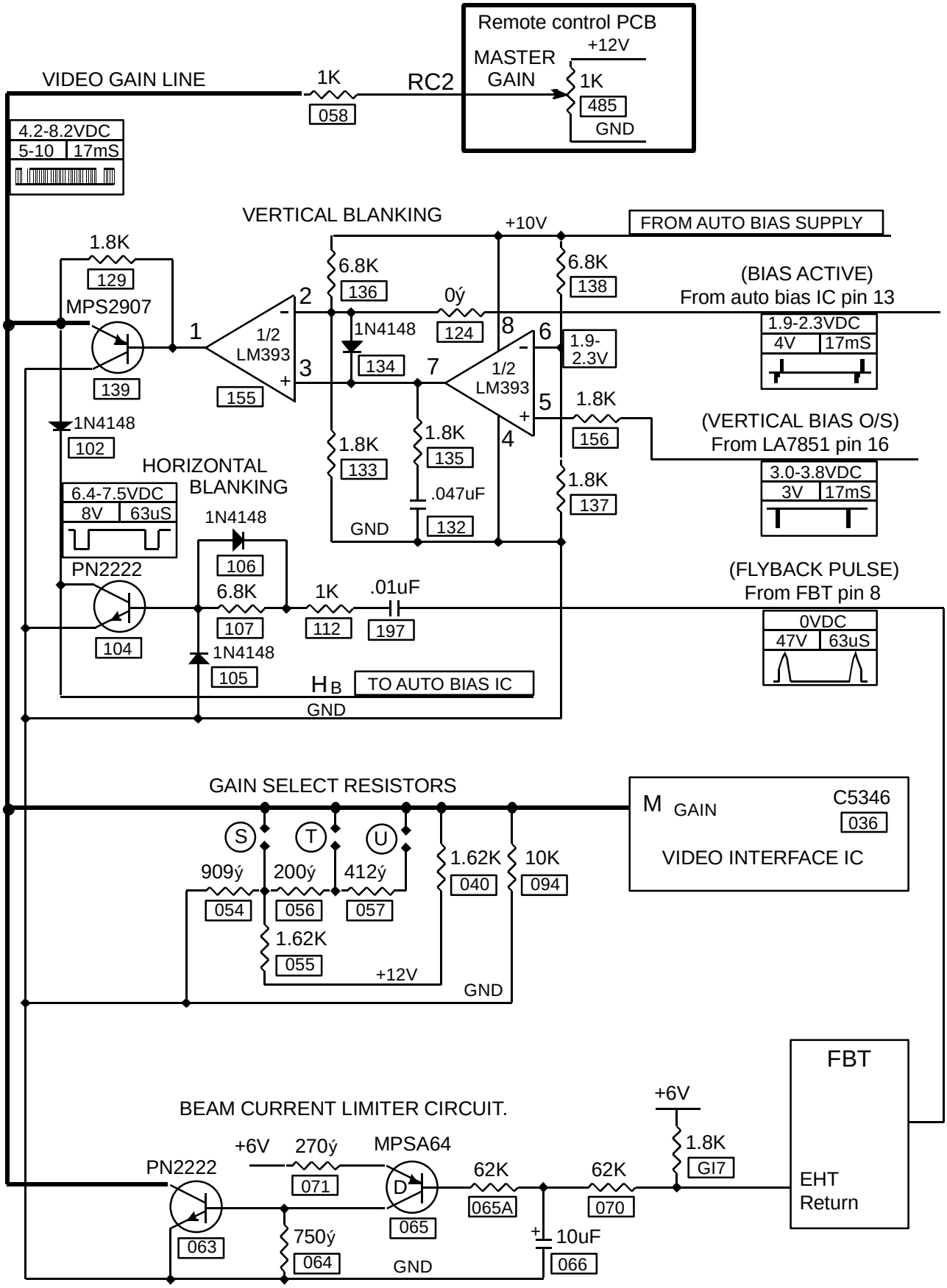
Horizontal blanking (H_B) is added to the gain line by transistors 104 104. This transistor pulls down on the gain line through diode 102 102 when the flyback pulse is high. Capacitor 197 197 is charged by diodes 105 105 106 106 and resistor 112 112 such that, as soon as the flyback pulse starts going positive the NPN transistor 104 104 turns on and horizontal blanking starts. The time constant of capacitor 197 197 and resistors 112 112 and 107 107 are chosen such that the capacitor will lead the FBP on the downward slope and turn the horizontal blanking transistor off just at the end of the FBP.

Vertical blank time is started when a low going pulse from the LA7851 pin 16 causes the output, pin 7, of the dual comparator 155 155 to go low. Capacitor 132 132 is discharged through resistor 135 135 at this time. After the end of the LA7851 pulse, the capacitor 132 132 holds the output, pin 1 of the comparator, low until the bias active pulse recharges the capacitor 132 132 through diode 134 134. During the high time of the bias active pulse, the second comparator output is still low, because of the voltage drop across the diode 134 134. The end of vertical blank time occurs when the bias active line returns to it's high impedance state. The capacitor 132 132 holds the charge from the bias active pulse until the next vertical blank time.

The video gain line will source up to 32mA during blank time, which is the reason for buffering the vertical blank comparator with a PNP transistor 139 139. E-B resistor 129 129. Resistors 137 137 and 138 138 supply a voltage that is midrange relative to the LA7851 pulse for maximum noise immunity. Resistors 133 133 and 136 136 also supply another midrange voltage for the bias active pulse and the, vertical blanking, hold capacitor to work against. Resistors 124 124 and 156 156 are used as jumpers.

The beam current limiter circuit uses the base to emitter voltage of a darlington transistor 65 65 to set the maximum beam current. The beam current is converted to a voltage across resistor G17. This voltage is applied to a long time constant RC circuit, resistor 70 70 and capacitor 66 66 before it is sensed by the darlington transistor. Resistor 65A 65A has been added to protect the darlington transistor from arc energy. The sharpness of the limiting response is set by resistors 64 64 and 71 71. Transistor 63 63 then, reduces the video gain by pulling down on the master gain line upon excessive beam current.

BLANKING AND MASTER GAIN SCHEMATIC



	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
001	CPR0128	A1	BB9	301 ohm ±1%, .25W	.01
002	CPR0124	A1	BB9	75 ohm ±1%, .25W	.01
003	CPR0140	B1	CC6	3.92K ohm ±1%, .25W	.01
004	CPR0128	B1	AA9	301 ohm ±1%, .25W	.01
005	CPR0124	B1	AA9	75 ohm ±1%, .25W	.01
006	CPS1754	C1		6 Conductor Header.	.22
007	CPR0129	A2	BB7	340 ohm ±1%, .25W	.01
008	CPR0144	A2	BB7	12.1K ohm ±1%, .25W	.01
009					
010		A2	BB8	Optional input filter capacitor.	
011	CPR0128	A2	BB8	301 ohm ±1%, .25W	.01
012	CPD1251	A2	BB8	1N4148 10mA, 75V Diode	.01
013	CPR0140	B1	BB6	3.92K ohm ±1%, .25W	.01
014	CPR0131	B2	BB7	464 ohm ±1%, .25W	.01
015	CPR0011	B1	BB6	1.8K ohm ±5%, .25W	.01
016	CPR0018	B1	BB6	62K ohm ±5%, .25W	.01
017		B1	BB6	Optional -BL adjust resistor.	
018	CPR0132	B2	AA7	604 ohm ±1%, .25W	.01
019					
020	CPD1251	B1	AA8	1N4148 10mA, 75V Diode	.01
021	CPR0128	B2	AA8	301 ohm ±1%, .25W	.01
022		B2	AA8	Optional input filter capacitor.	
023	CPR0144	B2	AA7	12.1K ohm ±1%, .25W	.01
024	CPR0129	C2	AA7	340 ohm ±1%, .25W	.01
025	CPC1039	C2	CC8	.1uF ±5% @ 50V	.05
026	CPR0128	C2	BB9	301 ohm ±1%, .25W	.01
027	CPR0124	C2	BB9	75 ohm ±1%, .25W	.01
028	CPR0050	A2		0 ohm Jumper	.01
029					
030	CPR0013	A2	AA6	6.8K ohm ±5%, .25W	.01
031	CPR0129	A2	BB7	340 ohm ±1%, .25W	.01
032	CPC1039	A2	AA5	.1uF ±5% @ 50V	.05
033	CPR0145	A2	AA6	15.8K ohm ±1%, .25W	.01
034	CPR0144	B3	AA7	12.1K ohm ±1%, .25W	.01
035	CPR0129	B2	BB7	340 ohm ±1%, .25W	.01
036	CPI1409	B2	AA6	XRC5346A Custom Video IC	1.51
037	CPR0129	B2	BB7	340 ohm ±1%, .25W	.01
038	CPR0129	B2	AA7	340 ohm ± 1%, .25W	.01
039					
040	CPR0136	B2	BB5	1.62K ohm ±1%, .25W	.01
041		C2	BB8	Optional input filter capacitor.	
042	CPD1251	C2	AA8	1N4148 10mA, 75V Diode	.01
043	CPR0128	C2	AA8	301 ohm ± 1%, .25W	.01
044	CPR0132	C2	AA7	604 ohm ±1%, .25W	.01
045	CPR0004	D1	DD8	270 ohm ±5%, .25W	.01
046	CPR0011	D1	CC8	1.8K ohm ±5%, .25W	.01
047	CPR0011	D1	CC9	1.8K ohm ±5%, .25W	.01
048	CPR0004	D1	DD8	270 ohm ±5%, .25W	.01
049					
050	CPR0009	D1	CC9	1K ohm ±5%, .25W	.01

BOARD No.	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
051	CPR0141	D1	CC8	4.42K ohm ±1%, .25W	.01
052	CPR0012	C1	CC8	2.7K ohm ±5%, .25W	.01
053	CPQ1301	C2	CC8	PN2907 .6A, 40V, .6W, PNP	.06
054	CPR0126	D2	AA5	909 ohm ±1%, .25W	.01
055	CPR0136	D2	AA5	1.62K ohm ±1%, .25W	.01
056	CPR0127	D2	AA5	205 ohm ±1%, .25W	.01
057	CPR0130	D2	BB5	412 ohm ±1%, .25W	.01
058	CPR0009	C2	EE3	1K ohm ±5%, .25W	.01
059					
060	CPC1039	D1	CC8	.1uF ±5% @ 50V	.05
061	CPR0004	D1	DD9	270 ohm ±5%, .25W	.01
062	CPR0015	D1	DD8	22K ohm ±5%, .25W	.01
063	CPQ1303	D1	PP5	PN2222A .6A, 30V, .5W, NPN	.05
064	CPR0007	D2	PP5	750 ohm ±5%, .25W	.01
065	CPQ1302	D2	PP5	MPSA64 .3A, 30V, D-PNP	.08
065A	CPR0018	D2	RR5	62K ohm ±5%, .25W	.01
066	CPC1101	D2	RR5	10uF ±20% @ 50V	.04
067	CPI1410	E1	DD8	LM393 Dual Comparator	.31
068	CPC1101	E2	GG2	10uF ±20% @ 50V	.04
069	CPC1039	D1	PP5	.1uF ±5%, @ 50V	.05
070	CPR0018	E2	RR5	62K ohm ±5%, .25W	.01
071	CPR0004	E2	PP5	270 ohm ±5%, .25W	.01
072		E1			
073		E1			
074		E1			
075		E1			
076		E1			
077	CPR0011	E1	EE9	1.8K ohm ±5%, .25W	.01
078	CPR0009	E2	EE8	1K ohm ±5%, .25W	.01
079					
080	CPR0013	E1	DD8	6.8K ohm ±5%, .25W	.01
81B	CPR0500	C3	CC1	Blue Video Amplifier	1.12
82B	CPC1040	A3	CC1	.015uF ±10% @ 250V	.07
83B	CPQ1308	A3	CC2	2SC3467AE .1A, 200V, 1W, NPN.	.16
84B	CPC1037	C3	DD1	.1uF ±10% @ 250V	.07
85B	CPR0050	B3		0ý Jumper	.01
86B	CPD1251	C3	CC1	1N4148 10mA, 75V Diode	.01
87B	CPQ1309	C3	CC1	2SA1370E .1A, 200V, 1W, PNP	.19
88B	CPC1005	C3	DD2	1000pF ±20% @ 500V	.03
89B	CPR0006	C3	CC2	510 ohm ±5%, .25W	.01
90B	CPD1250	C3	DD2	FDH400 .1A, 200V, Diode	.03
91B	CPQ1309	C3	DD2	2SA1370E .1A, 200V, 1W, PNP	.19
92B	CPR0011	C3	DD2	1.8K ohm ±5%, .25W CF	.01
93B	CPR0011	C4	DD2	1.8K ohm ±5%, .25W CF	.01
094	CPR0012	B3	BB5	2.7K ohm ±5%, .25W	.01
095	CPC1039	A3	DD3	.1uF ±5% @ 50V	.05
096	CPC1039	B3	BB2	.1uF ±5% @ 50V	.05
097	CPR0136	A4	CC3	1.62K ohm ±1%, .25W	.01
098	CPQ1302	A4	DD3	MPSA64 .3A, 30V, D-PNP	.08
099					
100	CPR0134	B4	CC3	1.21K ohm ±1%, .25W	.01

	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
101	CPD1252	A5	DD5	1N4005 1A, 600V, R-Diode	.02
102	CPD1251	A5	AA4	1N4148 10mA, 75V, Diode	.01
103	CPD1252	B5	DD5	1N4005 1A, 600V, R-Diode	.02
104	CPQ1303	B5	AA4	PN2222A .8A, 40V, .5W, NPN	.05
105	CPD1251	B5	BB4	1N4148 10mA, 75V, Diode	.01
106	CPD1251	B5	BB4	1N4148 10mA, 75V, Diode	.01
107	CPR0013	B4	BB4	6.8K ohm ±5%, .25W	.01
108	CPC1028	C5	DD6	6800pF ±10% @ 100V	.03
109					
110	CPC1028	C5	DD7	6800pF ±10% @ 100V	.03
111	CPC1028	C5	DD7	6800pF ±10% @ 100V	.03
112	CPR0009	D5	BB4	1K ohm ±5%, .25W	.01
113					
114	CPS1756	D4		"TC" 10 Conductor Header	.29
115	CPR0506	C5		"C" PRA (Auto Bias)	.68
116	CPC1036	A5	EE7	.047 uF ±5% @ 50V	.04
117	CPC1039	B5	EE7	.1 uF ±5% @ 50V	.05
118	CPC1036	B5	EE7	.047uF ±5% @ 50V	.04
119					
120	CPC1039	B5	EE6	.1uF ±5% @ 50V	.05
121	CPC1036	B5	EE6	.047uF ±5% @ 50V	.04
122	CPC1039	B5	EE6	.1uF ±5% @ 50V	.05
123	CPI1402	A6	FF7	CA3224E Auto Bias IC	1.95
124	CPR0050	A6	CC3	0 ohm Jumper.	.01
125	CPC1101	B6	FF7	10uF ±20% @ 50V	.04
126	CPC1101	B6	FF6	10uF ±20% @ 50V	.04
127	CPC1101	B6	FF6	10uF ±20% @ 50V	.04
128	CPC1039	A7	EE3	.1uF ±5% @ 50V	.05
129	CPR0011	A6	AA3	1.8K ohm ±5%, .25W	.01
130	CPI1407	A7	EE3	NJM7812FA 12V, 1A, Regulator.	.30
131	CPC1104	B7	JJ6	1000uF ±20% @ 35V	.22
132	CPC1036	B7	BB4	.047uF ±5% @ 50V	.04
133	CPR0011	C7	BB4	1.8K ohm ±5%, .25W	.01
134	CPD1251	C7	BB3	1N4148 10mA, 75V, Diode	.01
135	CPR0011	C7	BB4	1.8K ohm ±5%, .25W	.01
136	CPR0013	C7	BB3	6.8K ohm ±5%, .25W	.01
137	CPR0011	C7	CC4	1.8K ohm ±5%, .25W	.01
138	CPR0013	C6	CC3	6.8K ohm ±5%, .25W	.01
139	CPQ1301	A6	AA3	MPS2907 .6A, 40V, .6W, PNP	.06
140	CPR0050	C6		0 ohm Jumper	.01
141	CPR0016	C6	GG6	33K ohm ±5%, .25W	.01
142	CPR0016	C6	GG7	33K ohm ±5%, .25W	.01
143	CPR0016	C6	GG7	33K ohm ±5%, .25W	.01
144	CPC1039	B6	EE5	.1uF ±5% @ 50V	.05
145	CPD1252	C5	DD5	1N4005 1A, 600V, R-Diode	.02
146	CPI1405	C5	GG6	LM324 Quad Op. Amp.	.31
147	CPR0015	C6	GG6	22K ohm ±5%, .25W	.01
148	CPR0015	C6	GG6	22K ohm ±5%, .25W	.01
149					
150	CPC1039	C6	GG5	.1uF ±5% @ 50V	.05
151	CPR0050	D6		0 ohm Jumper	.01
152	CPR0016	C6	EE8	33K ohm ±5%, .25W	.01

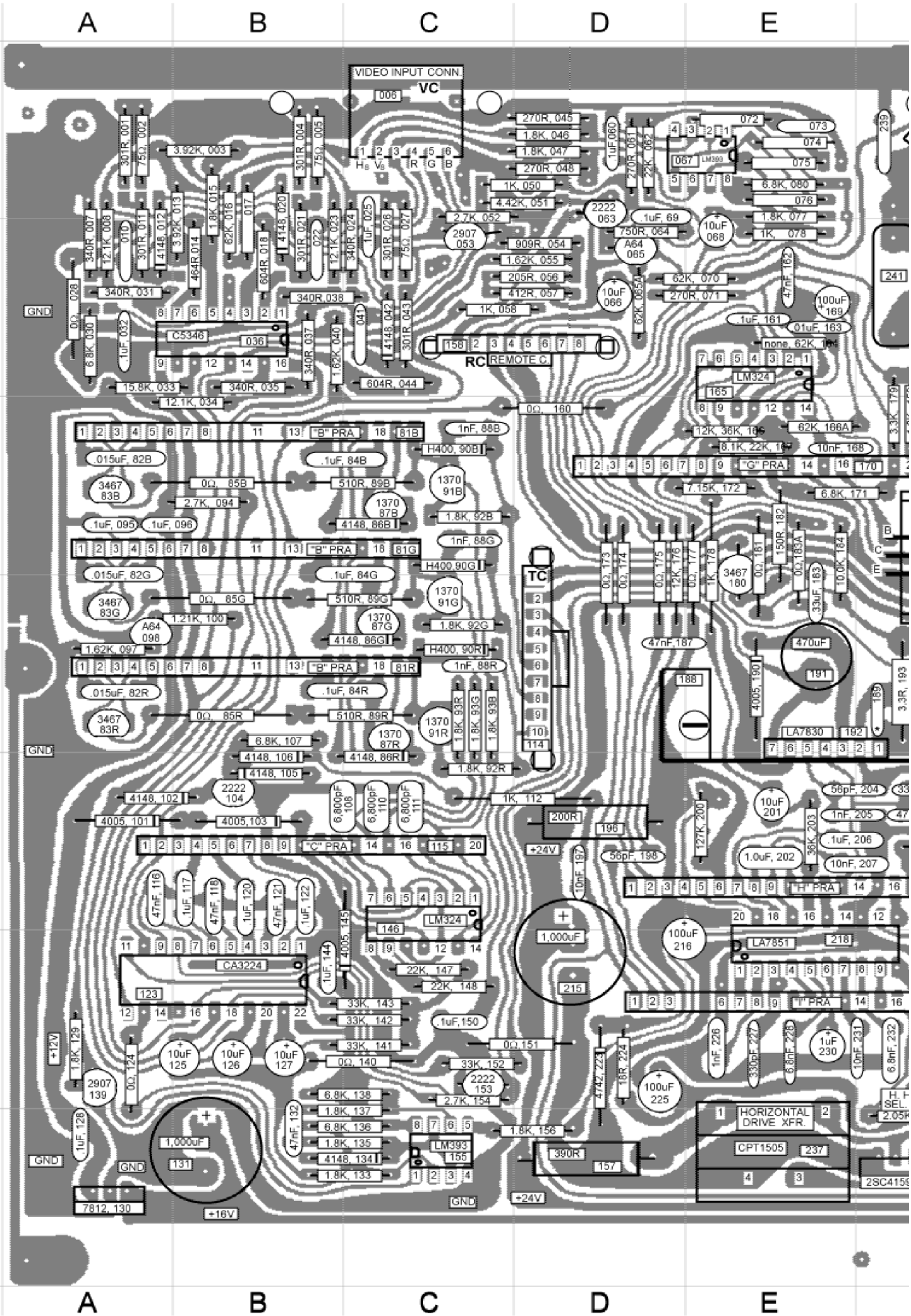
BOARD No.	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
153	CPQ1303	C6	EE9	PN2222A .6A, 30V, .5W, NPN	.05
154	CPR0012	C6	DD9	2.7K ohm ±5%, .25W	.01
155	CPI1410	C7	BB3	LM393 Dual Comparators	.31
156	CPR0011	D7	CC4	1.8K ohm ±5%, .25W	.01
157	CPR0393	D7	MM4	390 ohm ±5%, 2W	.04
158	CPS1755	C2		"RC" 8 Conductor Header	.26
159	CPR0011	F3	MM7	1.8K ohm ±5% (Blooming adjust)	.01
160	CPR0050	D2	LL0	0 ohm Jumper	.01
161	CPC1039	E2	NN8	.1uF ±5% @ 50V	.05
162	CPC1036	E2	MM7	.047uF ±5% @ 50V	.04
163	CPC1032	E2	NN7	.01uF ±5% @ 50V	.04
164	CPR0018	E2	NN8	62K ±5%, .25W (2092 Option)	.01
165	CPI1405	E2	NN7	LM324 Quad Op. Amp.	.31
166	CPR0144	E3	NN7	12.1Ký ±1%.25W (Pin. Adj) 1492	.01
166	CPR0017	E3	NN7	36Ký ±5%, .25W (Pin. Adj) 2092	.01
166A	CPR0018	E3	NN7	62Ký ±5%, .25W (H. Ras. Adj.)	.01
167	CPR0168	E3	NN7	8.06Ký ±1%.25W (Pin. Adj) 1492	.01
167	CPR0015	E3	NN7	22Ký ±5%, .25W (Pin. Adj) 2092	.01
168	CPC1032	E3	PP8	.01uF ±5% @ 50V	.04
169	CPC1102	E2	MM7	100uF ±20% @ 25V	.05
170	CPR0504	F3		"G" PRA (H. Width Control)	.92
171	CPR0013	F3	MM8	6.8K ohm ±5%, .25W	.01
172	CPR0142	E3	NN5	7.15K ohm ±1%, .25W	.01
173	CPR0050	D3	GG4	0 ohm Jumper	.01
174	CPR0050	D3	GG1	0 ohm Jumper	.01
175	CPR0050	D3	GG2	0 ohm Jumper	.01
176	CPR0144	D3	EE8	12.1K ohm ±1%, .25W	.01
177	CPR0050	E3		0 ohm Jumper	.01
178	CPR0009	E3	NN5	1K ohm ±5%, .25W	.01
179	CPR0024	F3	MM7	3.3Ký ±5% .25W (Max. iBeam adj.)	.01
180	CPQ1308	E4	MM2	2SC3467F .1A, 200V, 1W, NPN	.16
181	CPR0050	E3	GG1	0 ohm Jumper	.01
182	CPR0351	E3	NN3	150 ohm ±10%, .5W, CC	.05
183	CPC1041	E4	MM5	.33uF ±5% @ 50V	.08
183A	CPR0050	E3		0 ohm Jumper	.01
184	CPR0143	E3	NN6	10.0K ohm ±1%, .25W	.01
185	CPQ1307	F3	PP8	2SC4159E 1.5A, 180V, 15W, NPN	.36
186	CPM2037	G3	PP8	Heat Sink, H. Width output	.11
187	CPC1036	D4	GG3	.047uF ±5% @ 50V	.04
188	CPM2036	E4	GG1	Heat Sink, V. Deflection out	.13
188A	CPM2037		GG1	Heat Sink (2092 Option)	.11
189		F4			.01
190	CPD1252	E4	KK1	1N4005 1A, 600V, R-Diode	.02
191	CPC1109	E4	KK1	470uF ±20% @ 50V	.19
192	CPI1401	E4	HH1	LA7830 Vert. Def. Output	.67
193	CPR0377	F4	GG2	3.3 ohm ±5%, 1W	.03
194	CPR0050	F4		0 ohm Jumper	.01
195	CPC1104	G4	MM2	1000uF ±20% @ 35V	.22
196	CPR0391	D5	JJ2	200 ohm ±5%, 2W	.04
197	CPC1032	D5	BB4	.01uF ±5% @ 50V	.04
198	CPC1000	D5	EE4	56pF ±5% @ 100V	.03
200	CPR0157	E5	HH2	127K ohm ±1%, .25W	.01

	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
201	CPC1101	E5	MM5	10uF ±20% @ 50V	.04
202	CPC1043	E5	GG2	1.0uF ±5% @ 50V	.17
203	CPR0017	E5	MM5	36K ohm ±5%, .25W 1492	.01
203	CPR0163	E5	MM5	28.0Ký ±1%, .25W 2092	.01
204	CPC1000	F5	JJ1	56pF ±5% @ 100V	.03
205	CPC1005	F5	JJ2	1000pF ±20% @ 500V	.03
206	CPC1058	F5	HH2	.1uF ±5% @ 50V	.05
207	CPC1032	F5	HH2	.01uF ±5% @ 50V	.04
208	CPC1002	F5	II1	330pF ±10% @ 100V	.03
209	CPC1032	F5	NN2	.01uF ±5% @ 50V	.04
210	CPC1036	F5	JJ2	.047uF ±5% @ 50V	.04
211		F5		Vertical Deflection Bias Adj.	
212		F5		Vertical Deflection Bias Adj.	
213	CPS1759	G5		4X .062 Dia. Bead Pins (YC)	.01
214	CPR0503	F5	HH2	"H" PRA Vertical Control	1.26
215	CPC1104	D6	JJ6	1000uF ±20% @ 35V	.22
216	CPC1102	D6	GG3	100uF ±20% @ 25V	.05
217					
218	CPI1400	E6	KK3	LA7851 V. & H. Control IC	1.48
219					
220	CPC1036	F5	II1	.047uF ±5% @ 50V	.04
222	CPR0502	F6	KK4	"I" PRA Horizontal Control	.68
223	CPD1257	D6	JJ2	1N4742 12V ±5%, 1W, Z. DIODE	.05
224	CPR0002	D6	GG3	18 ohm ±5%, .25W	.01
225	CPC1102	D6	GG3	100uF ±20% @ 25V	.05
226	CPC1026	E6	HH4	1000pF ±5% @ 100V	.06
227	CPC1025	E6	HH4	330pF ±5% @ 100V	.06
228	CPC1028	E6	II4	6800pF ±10% @ 100V	.03
229					
230	CPC1100	E6	II4	1uF ±20% @ 50V	.04
231	CPC1032	F6	JJ4	.01uF ±5% @ 50V	.04
232	CPC1027	F6	JJ4	6800pF ±5% @ 100V	.06
233	CPC1100	F6	JJ4	1uF ±20% @ 50V	.04
234	CPC1003	F6	MM3	2,200pF ±20% @ 1KV	.03
235	CPR0138	F7	KK4	2.05K ohm ±1%, Hfo adjust.	.01
236	CPQ1307	F7	MM3	2SC4159E 1.5A, 180V, 15W, NPN	.36
237	CPT1505	E7	NN3	Horizontal Drive Transformer	.60
238	CPS1753	F1	GG9	"PC" 2 Conductor Header	.21
239		F1	GG9	Optional AC noise capacitor.	
240	CPR0426	F1	GG9	C-200-7, 25-.5ý Inrush Current Limiter	.28
241		F2	GG9	Optional AC line capacitor.	
242	CPS1758	F2		"CC" .093 Dia. Bead Pins	.02
243	CPS1758	F2		"CC" .093 Dia. Bead Pins	.02
244	CPRO427	F3	LL9	BF5ROM125 Posistor (Optional)	.96
245	CPR0425	F3	GG9	SS1-3A 3 AMP FUSE	.25
246	CPRO430	G1	LL9	Dual Posistor (Optional)	
247	CPR0366	G2	HH8	100K ohm ±5%, .5W, CF	.01
248	CPD1264	G2	KK6	FR205 2A, 600V, F-Diode	.04
248A	CPR0002	G2	JJ6	18 ohm ± 5%, .25W	.01
249		G2	HH6	Optional 127V line control.	
250	CPQ1310	G3	HH6	2SA1371E .1A, 300V, 1W, PNP	.22
251	CPR0019	H3	HH6	100K ohm ±5%, .25W	.01

BOARD No.	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
252	CPD1264	H1	GG8	FR205 2A, 600V, F-Diode	.04
252A	CPC1003	H1	GG7	2,200pF ±20% @ 1KV	.03
253	CPD1264	H1	GG8	FR205 (220V Option)	.04
254	CPD1264	H2	GG9	FR205 2A, 600V, F-Diode	.04
254A	CPC1003	G2	GG7	2,200pF ±20% @ 1KV	.03
254B	CPR0050	H2		0 ohm Jumper	.01
255	CPD1264	H2	GG9	FR205 (220V Option)	.04
256	CPC1105	H1	HH8	150uF ±20% @ 250V	.88
257	CPC1105	H2	HH8	150uF ±20% @ 250V	.88
258	CPT1503	J1	KK6	Switch Mode Transformer	2.10
259	CPR0050	I1		0 ohm Jumper	.01
260	CPD1264	J1	KK5	FR205 2A, 600V, F-Diode	.04
261	CPC1039	J2	KK6	.1uF ±5% @ 50V	.05
262	CPC1039	J2	JJ6	.1uF ±5% @ 50V	.05
263	CPD1264	J2	JJ5	FR205 2A, 600V, F-Diode	.04
264	CPR0351	I2	KK9	150 ohm ±10%, .5W, CC	.07
265	CPC1006	I2	KK8	200pF ±10% @ 1KV, NPO	.04
266	CPD1264	I2	KK6	FR205 2A, 600V, F-Diode	.04
267	CPM2027	J3	LL8	HEAT SINK , Power Supply	.08
268	CPQ1304	J3	KK8	2SK1446LS 450V, 7A, MOS FET	.94
269	CPR0050	J3		0ý Jumper, to ground PS H. S. 267	.01
270	CPR0002	I2	KK8	18 ohm ±5%, .25W	.01
271	CPR0147	I3	KK7	1.0 Meg ohm ±1%, .25W	.01
272	CPR0501	I3		"J" Power Supply PRA	.68
273	CPR0011	G3	HH7	1.8K ±5%, 127V line adjust.	.01
274	CPC1028	G3	HH7	6800pF ±10% @ 100V	.03
275	CPC1000	G3	II7	56pF ±5% @ 100V	.03
276	CPC1000	G3	HH7	56pF ±5% @ 100V	.03
277	CPC1027	G4	HH8	6800pF ±5% @ 100V	.06
278	CPR0050	G4	PP8	0 ohm Jumper	.01
279		G3	HH8	Power Supply Fo Adjustment.	
280	CPI1403	H4	II6-8	XRC5184 Custom P. S. IC	1.91
281	CPC1032	H3	HH6	.01uF ±5% @ 50V	.04
282	CPC1003	H3	JJ9	2200pF ±20% @ 1KV	.03
283	CPD1252	H3	KK8	1N4005 1A, 600V, R-Diode	.04
284	CPQ1302	H3	KK9	MPSA64 .3A, 30V, D-PNP	.08
285	CPC1039	I3	JJ7	.1uF ±5% @ 50V	.05
286	CPC1102	H3	HH9	100uF ±20% @ 25V	.05
287	CPR0169	I3	KK7	191K ohm ±1%, .25W	.01
288	CPC1002	I4	II8	330pF ±10% @ 100V	.03
289	CPR0050	G3	RR4	0 ohm Jumper	.01
290	CPD1251	I4	LL7	1N4148 10mA, 75V, Diode	.01
291	CPC1026	I3	KK7	1000pF ±5% @ 100V	.06
292	CPR0376	I3	KK9	1.2 ohm ±5%, 1W	.03
293	CPD1264	J3	MM4	FR205 2A, 600V, F-Diode	.04
294	CPC1037	J3	II5	.1uF ±10% @ 250V	.07
295	CPD1256	J3	II5	TZ160B-T3160V ±5%, 1W, Z-Diode	.18
296	CPC1034	I4	JJ6	.022uF ±5% @ 630V	.08
297	CPT1500	I5	PP3	Flyback Transformer	10.64
298	CPR0356	G5	PP6	2.2Ký ±10%, .5W, CC 1492	.07
298	CPR0353	G5	PP6	1Ký ±10%, .5W, CC 2092	.07
300	CPC1035	G5	PP6	3,300pF ±5% @ 200V	.06

	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
301	CPT1523	G5	PP7	220uH Horz. Width Coil. 1492	.60
301	CPT1506	G5	PP7	Horz. Linearity Coil 2092	.60
302	CPT1506	G6	PP6	Horz. Linearity Coil	.60
303	CPR0392	F7	NN4	270 ohm ±5%, 2W	.04
304	CPQ1305	G7	NN3	2SD1651 5A, 1.5KV, NPN	1.48
305	CPC1050	H6	RR7	.47uF ±5% @ 250V 1492	.36
305	CPC1059	H6	RR7	.33uF ±5% @ 250V 2092	.38
306	CPC1030	H6	RR6	.01uF ±3% @ 1.6KV 1492	.26
306	CPC1055	H6	RR6	8,200pF ±3% @ 1.6KV 2092	.37
307	CPC1034	H7	RR8	.022uF ±5% @ 630V	.08
308	CPD1252	I6	RR6	1N4005 1A, 600V, R-Diode	.02
309	CPR0365	H7	NN4	470 ohm ±5%, .5W, CF	.01
310	CPD1252	I6	RR7	1N4005 1A, 600V, R-Diode	.02
311	CPD1253	I6	RR8	1N4937 1A, 600V, F-Diode	.03
312	CPD1264	J6	NN4	FR205 2A, 600V, F-Diode	.04
313	CPR0050	J6		0 ohm Jumper	.01
314					
315	CPC1044	I6	PP8	2.7uF ±10% @ 100V	.32
316	CPT1504	I7	PP7	Horizontal Width Coil	.63
317	CPC1105	J7	II5	150uF ±20% @ 250V	.88
TUBE SOCKET BOARD					
401	CPS1750			CRT SOCKET	1.54
402	CPR0350		NN1	47 ohm ±10%, .5W, CC	.07
403	CPR0352		NN1	470 ohm ±10%, .5W, CC	.07
404	CPR0353		NN0	1K ohm ±10%, .5W, CC	.07
405	CPR0375		PP1	.68 ohm ±5%, 1W 1492	.03
405	CPR0050		PP1	0ý Jumper 2092	.01
406	CPR0353		NN1	1K ohm ±10%, .5W, CC	.07
407	CPD1250		MM0	FDH400 .1A, 200V, Diode	.03
408	CPD1250		MM0	FDH400 .1A, 200V, Diode	.03
409					
410	CPD1250		MM0	FDH400 .1A, 200V, Diode	.03
411	CPR0353		NN0	1K ohm ±10%, .5W, CC	.07
412					
413	CPR0353		PP1	1K ohm ±10%, .5W, CC	.07
414	CPC1040		MM1	.015uF ±10% @ 250V	.07
415	CPR0355		NN1	100K ohm ±10%, .5W, CC	.07
416	CPR0019		MM1	100K ohm ±5%, .25W, CF	.01
417	CPQ1306		MM1	2SC3675 .1A, 1.5KV, NPN	.67
418	CPR0353		PP1	1K ohm ±10%, .5W, CC	.07
419					
420	CPR0029		MM1	200K ohm ±10%, .25W, CF	.01
421	CPC1003		PP1	2200pF ±20% @ 1KV	.03
422	CPR0353		PP1	1K ohm ±10%, .5W, CC	.07
423	CPC1002		PP1	330pF ±10% @ 100V	.03
424	CPR0350		NN1	47 ohm ±10%, .5W, CC	.07
425	CPR0354		NN1	10K ohm ±10%, .5W, CC	.07
426	CPS1769			10 Conductor Cable	.83
	CPS1768			10 Conductor Cable, Double length.	.99
427	CPS1758			.093 Dia. Bead Pin	.02

BOARD No.	CERONIX PART No.	Board Ref.	Schematic Reference	DESCRIPTION	PRICE
REMOTE CONTROL BOARD					
	CPA4102			Remote PCB Assembly.	4.75
485	CPR0400		FF2	1K ohm White Pot	.17
483	CPR0401		FF2	1K ohm Blue Pot	.17
481	CPR0402		FF1	10K ohm Yellow Pot	.17
484	CPR0403		FF2	20K ohm Orange Pot	.17
482	CPR0405		FF1	500 ohm Black Pot	.17
486	CPR0007		FF1	750 ohm ±5%, .25W	.01
487	CPS1767			"RC" 8 Conductor Cable	.87
PCB ASSEMBLIES					
	CPA4100			1492 Main PCB Assembly	105.00
	CPA4103			2092 Main PCB Assembly	115.00
	CPA4101			CRT P.C. Board Assembly	7.50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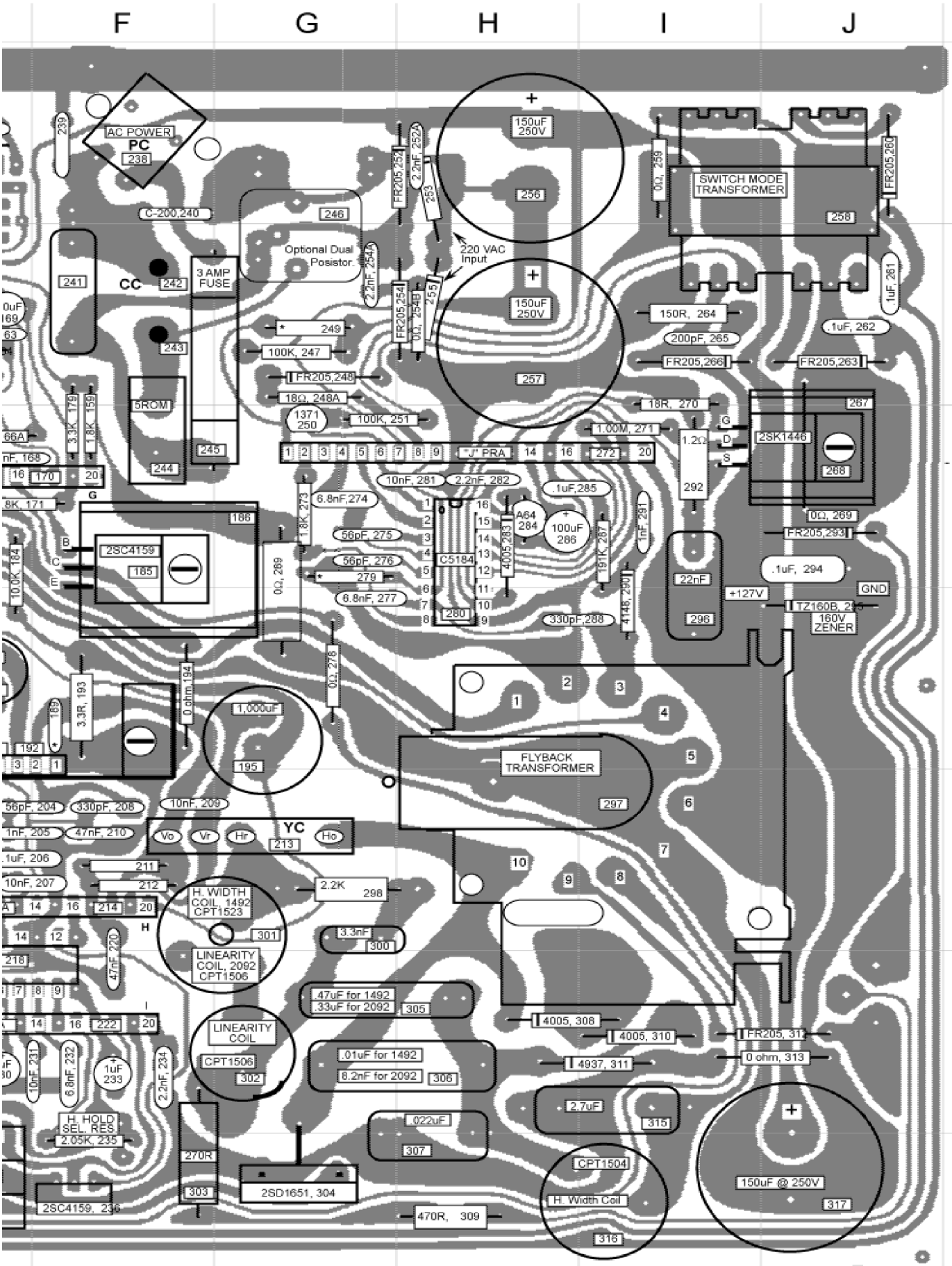
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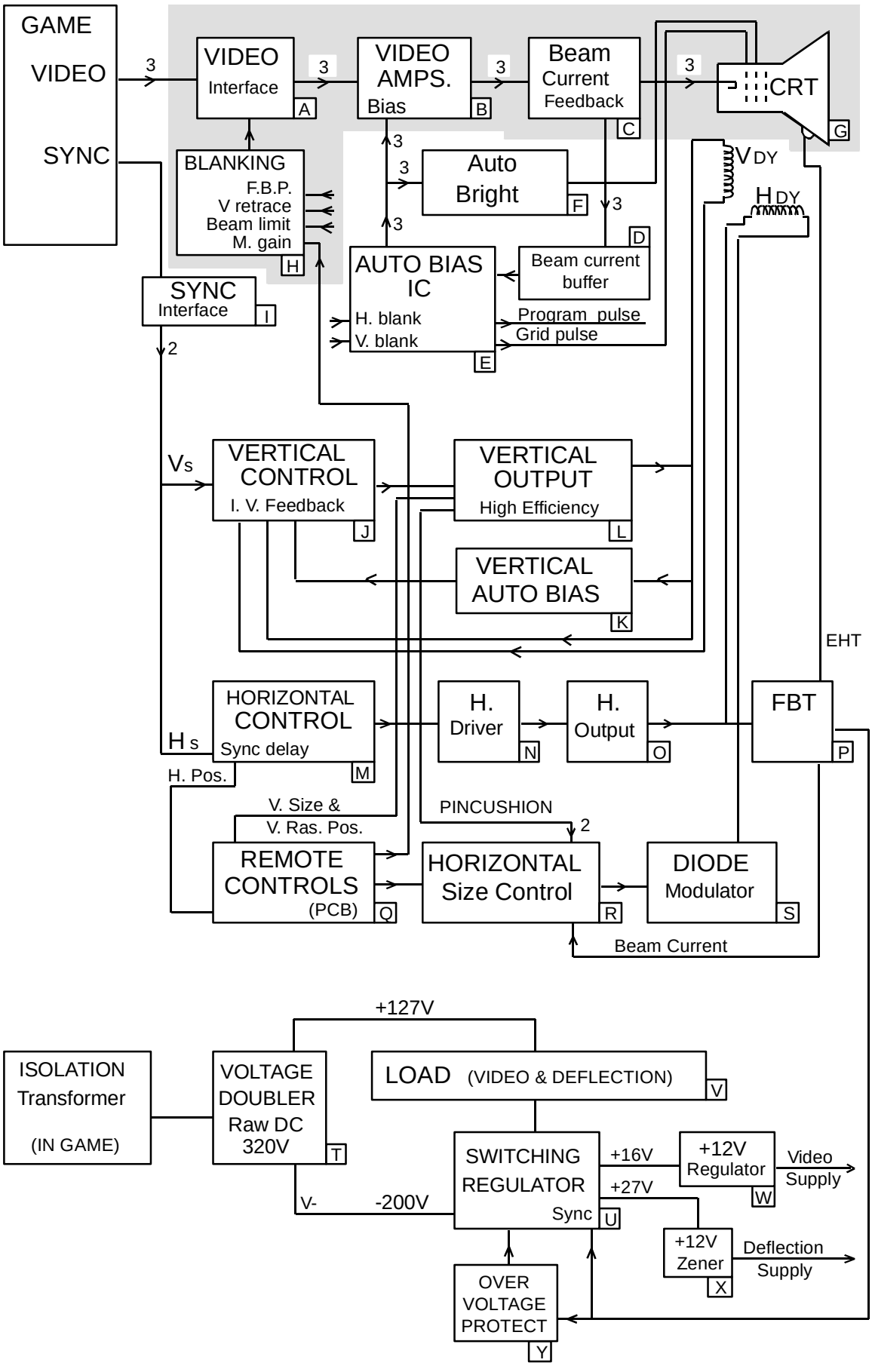
Block Diagram Review

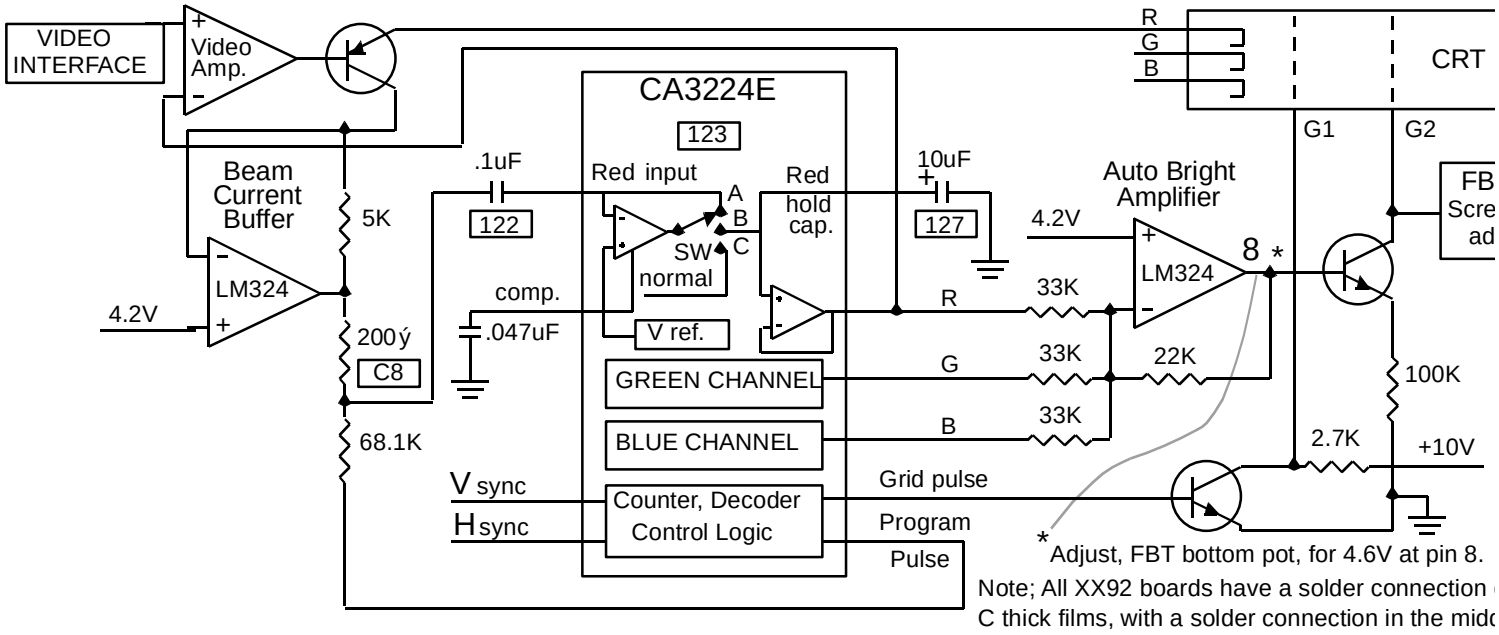


AUTO BIAS AND AUTO BRIGHT CIRCUIT, FUNCTION, DESCRIPTION

The auto bias circuit is a control system that forms a closed loop for controlling the CRT bias voltage. It generates a set of conditions where the current near the cutoff voltage of each gun is measured, and then adjusts the bias voltage of the video amplifiers, to set the correct black level voltage for each gun. This color balance adjustment is necessary, since each gun in the color picture tube can have a different cutoff voltage, which also, will change as the CRT ages.

If the picture tube gain changes, the auto bias circuit would adjust all three guns in the same direction to maintain constant black level. This effect reduces the auto bias voltage range which is needed for the cathode differential voltage adjustment. To prevent this occurrence a second control loop is added to the system. This second control loop is called the auto bright circuit and corrects for CRT gain changes. The auto bright circuit senses any common bias voltage change and controls the screen grid (G2) to hold the common bias voltage constant.

SIMPLIFIED PICTURE TUBE VIDEO BIAS CONTROL CIRCUIT: (One channel shown)



The auto bias circuit performs all of its sensing and bias corrections during the sixteenth to the twenty first horizontal cycle, after the vertical blanking has started. Before the sixteenth cycle, the SW in the auto bias IC is open (SW in "C" position).

During the 16,17, and 18 horizontal cycle, the CRT is brought out of cutoff by the grid pulse. The resulting beam current produces a voltage at the beam current buffer output. This voltage is applied to the coupling capacitor 12[122] At the other side of the coupling capacitor is the channel input, which is clamped to V ref. (SW in "A" position). The voltage amplitude of the amplifier output with the cathode current information is then stored in the coupling capacitor [122] during this time.

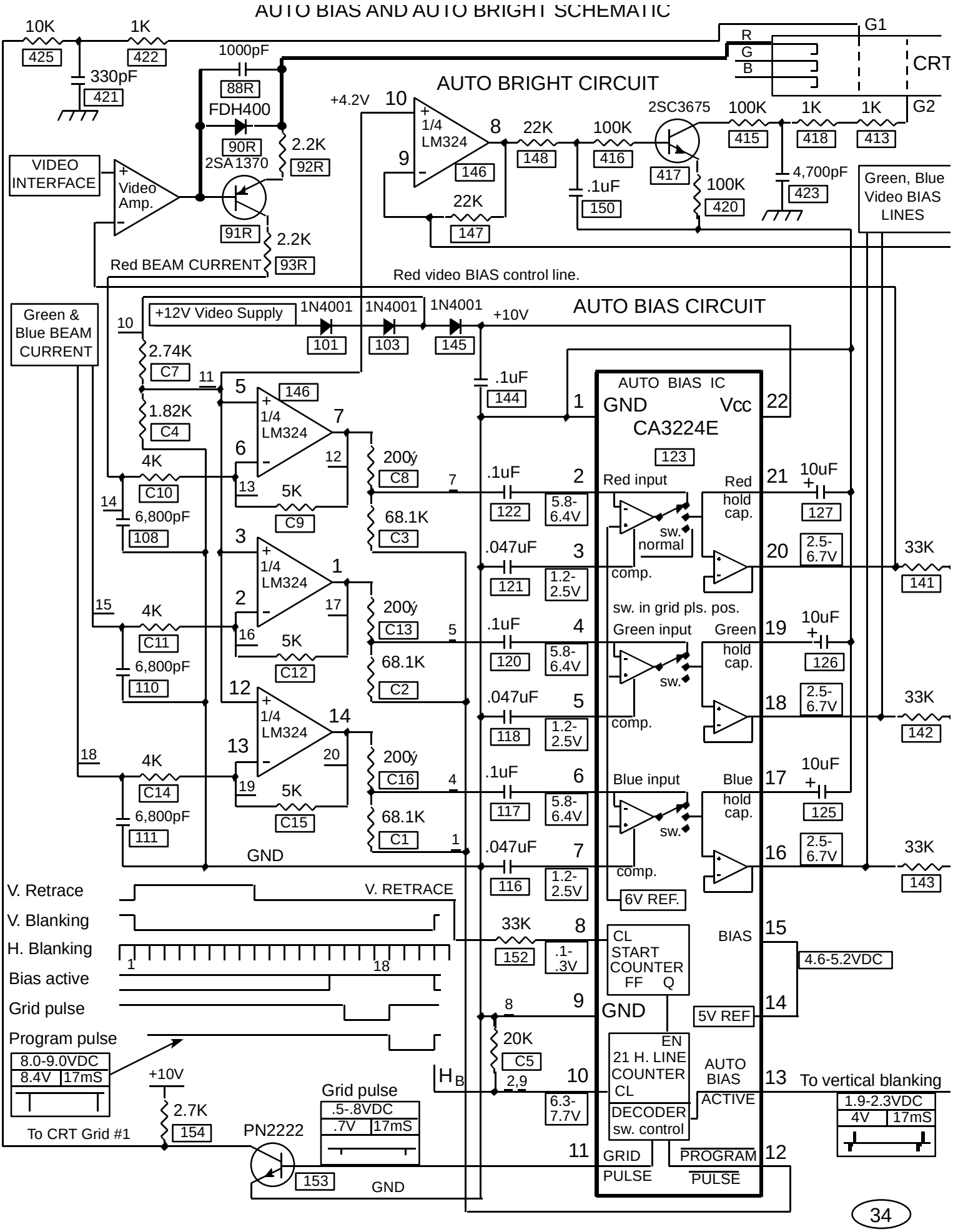
During the next three horizontal cycles (19, 20, and 21), the SW is switched to pass current to capacitor [127] which is the bias voltage storage capacitor. At the same time a program pulse is applied to resistor C[C8] which, if the bias was correct during the previous cycle, exactly balances the voltage stored in the coupling capacitor and no difference is sensed at the channel input. The channel amplifier, in this case, does not output current and the voltage of capacitor [127] stays unchanged.

If the CRT cathode is too far into cutoff, less beam current flows, the beam current buffer puts out a smaller negative pulse, less voltage is stored in the coupling capacitor, the program pulse amplitude (which is constant) is now larger than the stored (beam current) voltage and the channel amplifier will add current to the bias voltage, storage capacitor [127], correcting the low bias voltage which caused the cathode to be too far into cutoff. After the program pulse is over, the SW is switched to the open position again and the next time the bias voltage can be adjusted is during the next vertical blank time.

AUTO BIAS AND AUTO BRIGHT CIRCUIT DESCRIPTION

The beam current feedback circuit uses a PNP video transistor 91 91R direct most of the beam current to the auto bias circuit while passing the voltage waveform, from the video amplifiers to the CRT cathodes. Diode 9 90R and capacitor 88 88R nsure that no video waveform distortion occurs. An additional benefit of this circuit is that it protects the video amplifiers from the destructive arc energy. Resistors 92F 92R d 93F 93R ide energy due to CRT arcing, between the video amplifier transistors and the beam current feedback transistor 9 91R The beam current is filtered by capacitor 108 108 d resistor C10 and is buffered by an operational amplifier, which translates the beam current into a low impedance voltage. This voltage is applied to a coupling capacitor 12 122 through a 200 ohm resistor C8 . The 200 ohm and the 68.1K resistor C C3 orms the program value which sets the black level voltage via the action of the program pulse.
Capacitor 121 is used to stabilize the transconductance amplifier which is used at the channel input of the auto bias IC 12 123 The auto bias IC stores the bias voltage of this channel in capacitor 1 127 at pin 21. This voltage is buffered by an internal amplifier, with output at pin 20, which is connected to the Red video amplifier bias input.

Resistor 141 , 142 , and 143 are part of the auto bright circuit. They are used to sum the bias voltage of each of the three channels via a voltage node at the auto bright amplifier, 14 146 in 9. The resulting output voltage then controls the screen grid via transistor 41 417 Resistors 4 413 nd 41 418 rotect the CRT from excessive current during arcing. Capacitor 42 423 upplies a low AC impedance to GND to insure that the CRT gain is constant during each horizontal line.
Resistor 420 defines the current gain of, and stabilizes, the auto bright control loop.
Resistor 148 and capacitor 150 act as a low pass filter to reduce the chance of damaging the amplifier 1 146 lue to CRT arcing. Resistors 41 415 nd 41 416 otect the auto bright control transistor 41 417 The grid pulse is generated by a discrete transistor 1 153 to protect the auto bias IC from possible arc energy.
Pullup resistor 1 154 supplies the grid pulse voltage during the grid pulse time.
The auto bias IC (CA3224E) is designed for a supply voltage of +10V and since the video amplifier requires +12V, three diodes 10 101 10 103 nd 14 145 e used to supply this IC. Resistors C4 and C7 form a voltage divider which supplies the bias voltage to the LM324 1 146 The green and blue channel circuits are identical to the red channel and are controlled by the timing logic in the same way. Refer to the waveforms at the bottom left of page 34 for the timing relationship. The vertical retrace pulse, from the LA7851, starts the 21 count auto bias state counter. The grid pulse becomes active between the 15 and 18 horizontal cycle and the program pulse is active between the 18 and 21 horizontal cycle. These two pulses in conjunction with the internal control of the transconductance amplifier output switch are what measure and set the video bias.

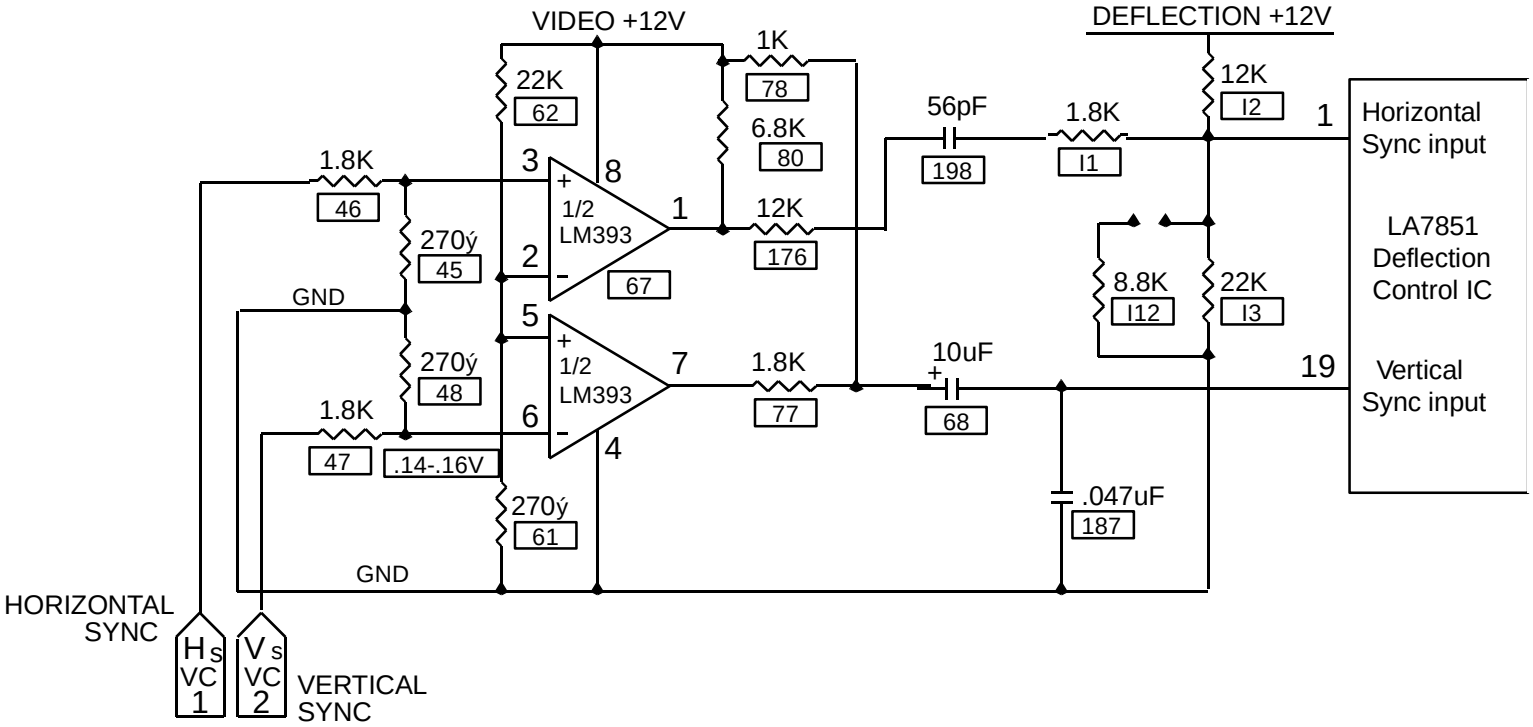

AUTO BIAS AND AUTO BRIGHT SCHEMATIC
AUTO BRIGHT CIRCUIT
AUTO BIAS CIRCUIT
AUTO BIAS IC
CA3224E
GND
Vcc
10K
425
1K
422
330pF
421
1000pF
88R
FDH400
90R
2.2K
92R
2SA1370
91R
2.2K
93R
Red BEAM CURRENT
VIDEO INTERFACE
Video Amp.
Red video BIAS control line.
+4.2V
1/4 LM324
146
22K
148
100K
416
.1uF
150
22K
147
2SC3675
417
100K
420
100K
415
1K
418
1K
413
4,700pF
423
G1
G2
CRT
R
G
B
Green, Blue Video BIAS LINES
Green & Blue BEAM CURRENT
+12V Video Supply
1N4001
101
1N4001
103
1N4001
145
+10V
2.74K
C7
1.82K
C4
4K
C10
6,800pF
108
4K
C11
6,800pF
110
4K
C14
6,800pF
111
200ý
C8
68.1K
C3
200ý
C13
68.1K
C2
200ý
C16
68.1K
C1
5K
C9
5K
C12
5K
C15
.1uF
144
.1uF
122
.047uF
121
.1uF
120
.047uF
118
.1uF
117
.047uF
116
5.8-6.4V
1.2-2.5V
123
Red input
Red hold cap.
sw. normal
comp.
sw. in grid pls. pos.
Green input
Green hold cap.
Blue input
Blue hold cap.
6V REF.
10uF
127
10uF
126
10uF
125
2.5-6.7V
33K
141
33K
142
33K
143
V. Retrace
V. Blanking
H. Blanking
Bias active
Grid pulse
Program pulse
V. RETRACE
33K
152
.1-.3V
CL START COUNTER FF Q
GND
20K
C5
2,9
6.3-7.7V
EN 21 H. LINE COUNTER CL
DECODER sw. control
BIAS
5V REF
AUTO BIAS ACTIVE
4.6-5.2VDC
To vertical blanking
1.9-2.3VDC
4V
17mS
8.0-9.0VDC
8.4V
17mS
+10V
2.7K
154
To CRT Grid #1
PN2222
153
Grid pulse
.5-.8VDC
.7V
17mS
GRID PULSE
PROGRAM PULSE
H_B

VERTICAL AND HORIZONTAL SYNC CIRCUIT DESCRIPTION

The 1492 Monitor has a separate input for horizontal and vertical sync. The horizontal sync pulse is normally positive going. The horizontal deflection control circuit will sync on the rising edge of this pulse. If horizontal sync is negative going, the picture is shifted to the left, and may be out of range of the horizontal picture position adjustment circuit. To sync on the falling edge of horizontal sync, a solder bridge is installed on the I PRA.

The vertical deflection circuit will sync on either a negative or positive sync pulse, provided that the pulse width is between two and twenty horizontal cycles long. Both the vertical and horizontal sync lines are joined for composite sync operation.

VERTICAL AND HORIZONTAL SYNC CIRCUIT



This sync interface incorporates a dual voltage comparator 6 67 and a resistive input circuit for high reliability. For TTL level sync signals, the resistive inputs are seven to one attenuators comprised of resistors 45 , 46 , 47 , and 48 . The comparators are biased to .15 volts by resistors 61 62 which permit direct connection to an RS170 sync source by removing resistors 45 and 48 .

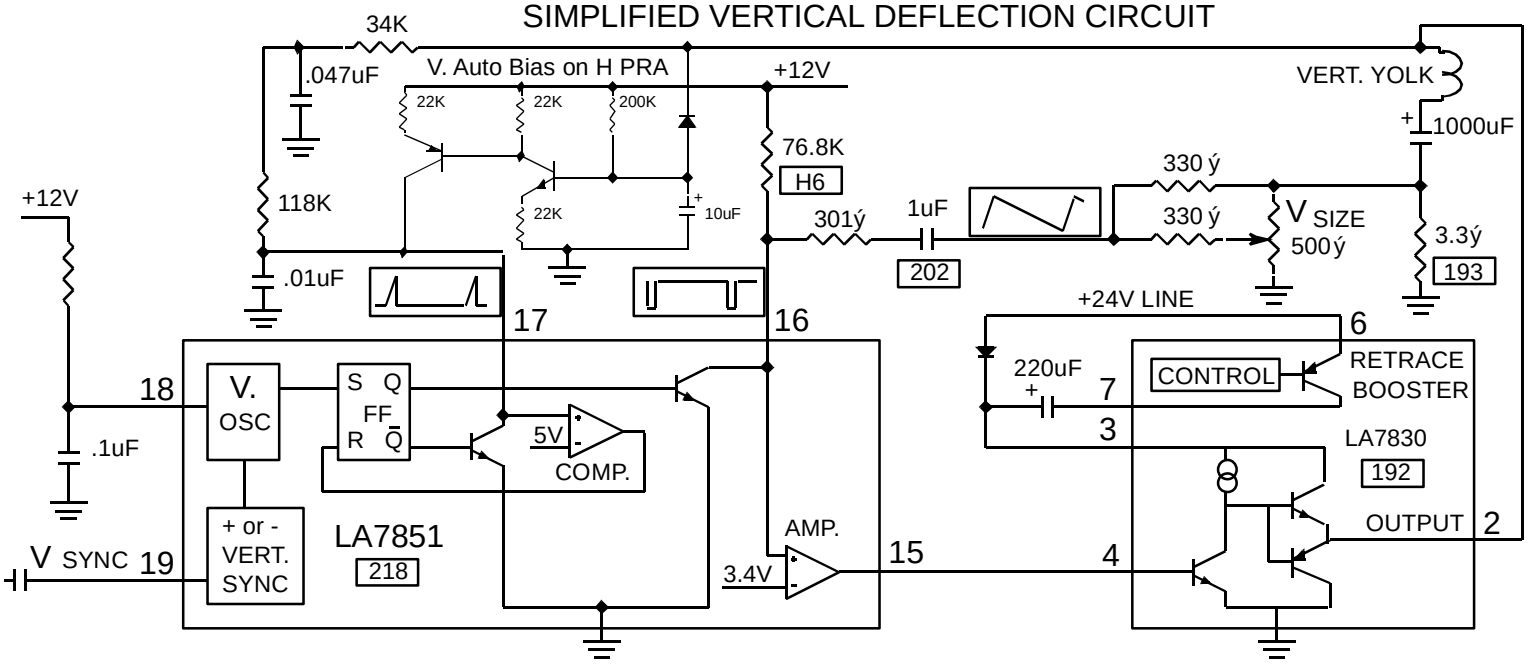
The horizontal sync signal from the comparator output is pulled up by resistor 80 80 attenuated by resistor 176 and I1 for correct drive amplitude. It is differentiated by capacitor 198 and applied to the horizontal sync input, pin 1, of the LA7851. Bias resistors I2 and I3 set up the correct voltage for positive edge triggering. By adding resistor I12 the LA7851 is programmed for negative edge triggering. This is used when the horizontal sync pulses are negative going. Resistor I12 I12 connected by adding a solder bridge to the I PRA solder pads above pin 6.

The vertical sync signal from the second comparator is coupled to the LA7851, vertical sync input, via a coupling capacitor 6 68 Resistor 7 77 nd capacitor 18 187 orm a low pass filter to eliminate false triggering by horizontal sync pulses in the case of composite sync. Resistor 78 and capacitor 77 compliments the comparator open collector output by acting as a pullup. These resistors also form a voltage divider which insures that the capacitor 68 is not reverse biased and provide the proper vertical sync drive amplitude. The LA7851 vertical sync input circuit is designed to accept either positive or negative sync pulses, but will not work with a sync signal that is close to a square wave.

VERTICAL DEFLECTION CIRCUIT, FUNCTION, DESCRIPTION

The LA7851 IC and the H PRA have all the active components to control the vertical deflection. LA7830 is a high efficiency vertical yolk driver IC. Together they form a compact and efficient vertical deflection system.

SIMPLIFIED VERTICAL DEFLECTION CIRCUIT

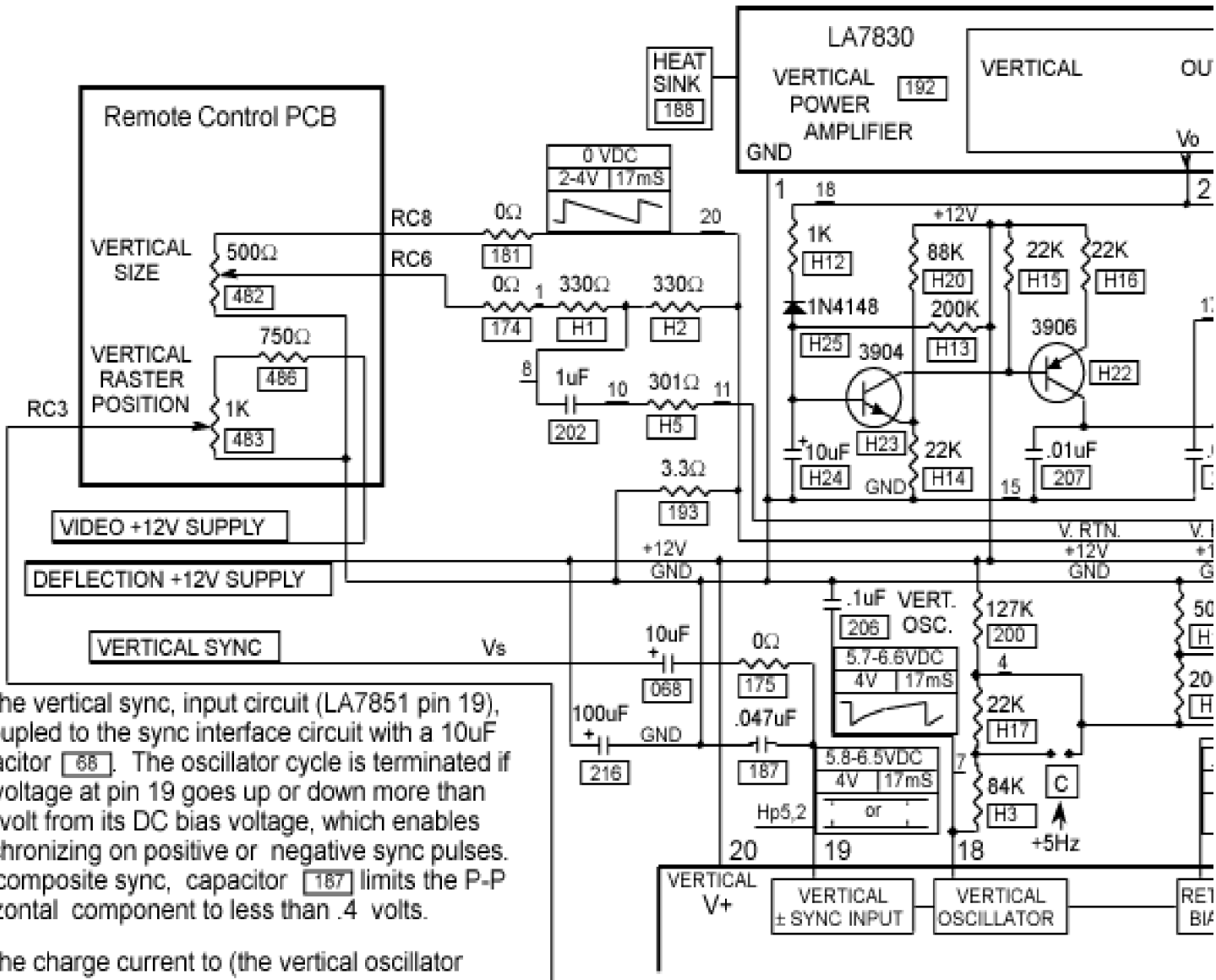


The vertical oscillator supplies the start time for the vertical cycle and when vertical sync is present, sync supplies the start time to the vertical oscillator. The linear vertical ramp current which is necessary for linear vertical deflection is generated by supplying a capacitor 202 with a constant current from resistor H6 H6 a voltage node (pin 16). The voltage at this node is held constant by a system of amplifiers which drive the deflection yoke. The yoke current sensing resistor 193 is connected to the other side of this capacitor 202 and supplies the ramp voltage which balances the current from H6 H6 ring trace time.

To generate the other half of the deflection yoke sawtooth current (vertical retrace), a flip flop is set by the vertical oscillator which partly discharges the capacitor 202 202 and causes the drive voltage across the yoke to reverse. The amount of discharge of capacitor 202 determines the vertical output voltage for the next cycle and is controlled by a timer at pin 17. The time out of the timer is controlled by the vertical output voltage from two different paths. One path is through the 34K and 118K resistors which supplies the higher frequency component for the timer and stabilize the vertical amplifier. The other path is through the vertical auto bias circuit which detects the minimum vertical output voltage over many vertical cycles and supplies a second current source to the timer. This second current source has a wide dynamic range and will hold the vertical output voltage well within operating limits for both 50Hz and 60Hz with no need for manual adjustment.

To better understand the LA7851 bias control loop, imagine the vertical output voltage goes up, the time out shortens which causes the capacitor 2 202 b be less discharged. This raises the voltage on capacitor 202 and lowers the vertical output voltage. This type of vertical bias control system has the advantage of only correcting the bias during retrace which means that it will not cause current ramp distortion during vertical trace time.

The vertical yoke driver LA7830 is the power output stage for the vertical amplifier. It has a built-in voltage booster circuit to reduce vertical retrace time without the power losses associated with a high vertical supply voltage.



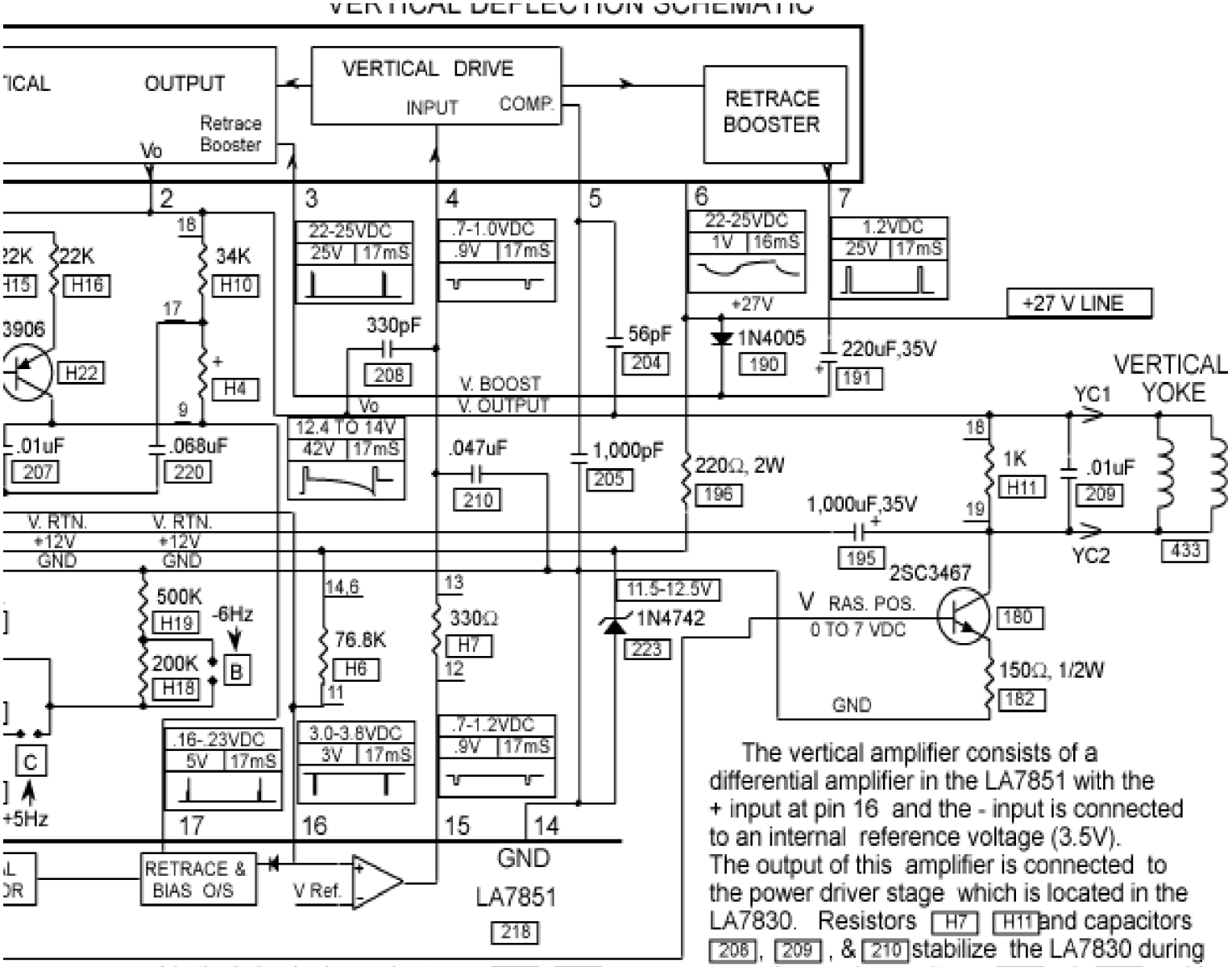
The vertical sync, input circuit (LA7851 pin 19), is coupled to the sync interface circuit with a 10uF capacitor [68]. The oscillator cycle is terminated if the voltage at pin 19 goes up or down more than one volt from its DC bias voltage, which enables synchronizing on positive or negative sync pulses. For composite sync, capacitor [187] limits the P-P horizontal component to less than .4 volts.

The charge current to (the vertical oscillator capacitor) [206] comes from +12V through a combination of five resistors. This resistor network is made up of [200] [H17] [H3] [H18] and [H19] [Solder connection B decreases Vfo by 6Hz and connection C increases Vfo by 5Hz. See page 56 for the location of the solder connections on the H PRA. This adjustment is only used if Vfo is outside the range of 39Hz to 48Hz. The normal vertical sync, frequency range, of the LA7851 is 44Hz (Vfo) to 70Hz.] Upon vertical sync, or when the oscillator waveform reaches 6 volts, the capacitor [206] is rapidly discharged by a transistor and a resistor, inside the LA7851, to 2 volts at which time the cycle starts over. Note the voltage and waveform block above pin 18.

During the discharge time of [206] the retrace and bias one shot (O/S) is triggered. This O/S consists of the flip flop and comparator mentioned in the function description. The time duration of the O/S is set by capacitor [207] and two low pass filters which are connected to the vertical output. The higher frequency filter is made up of resistors [H10], [H4] and capacitor [220]. The lower frequency filter is the Vertical Auto Bias circuit.

The V. Auto Bias senses the lowest point of the vertical output waveform with resistors [H12], [H13] And diode [H25] This voltage Stored by [H24] is converted to a current by transistor [H23] and resistors [H14] & [H20] This current is reflected from the +12V line via resistors [H15] [H16] and transistor [H22]
This current then adds to the charging current of the bias O/S capacitor [207]. The retrace and bias O/S outputs a low pulse, which is conducted by a diode to pin 16 and discharges capacitor [202] through resistor [H5] which causes the system to retrace. The pulse duration determines the extent of the [202] discharge which has to be made up by resistor [H3] during trace time. This balance between the [202] charge during trace time and discharge during retrace is what keeps the vertical output waveform at the proper DC level.

Pin 16 is the minus input of the vertical amplifier that extends to the LA7830 for its output stage. The other input of the vertical amplifier is tied to V ref. (3.5V).



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Vertical size is dependent on H6 202 193, H1, H2, and 462. The vertical yoke current is converted to a voltage across resistor 193 and applied to the ramp generating capacitor 202 through resistor H1 and H2 The ramp waveform on the H1 side of the capacitor 202 is constant for any vertical size because of the constant current from resistors H6. For minimum vertical size, the feedback voltage is present on both resistors H1 and H2. For maximum vertical size H1 grounded and twice the amplitude across the current feedback resistor 193 is required to generate the ramp waveform.

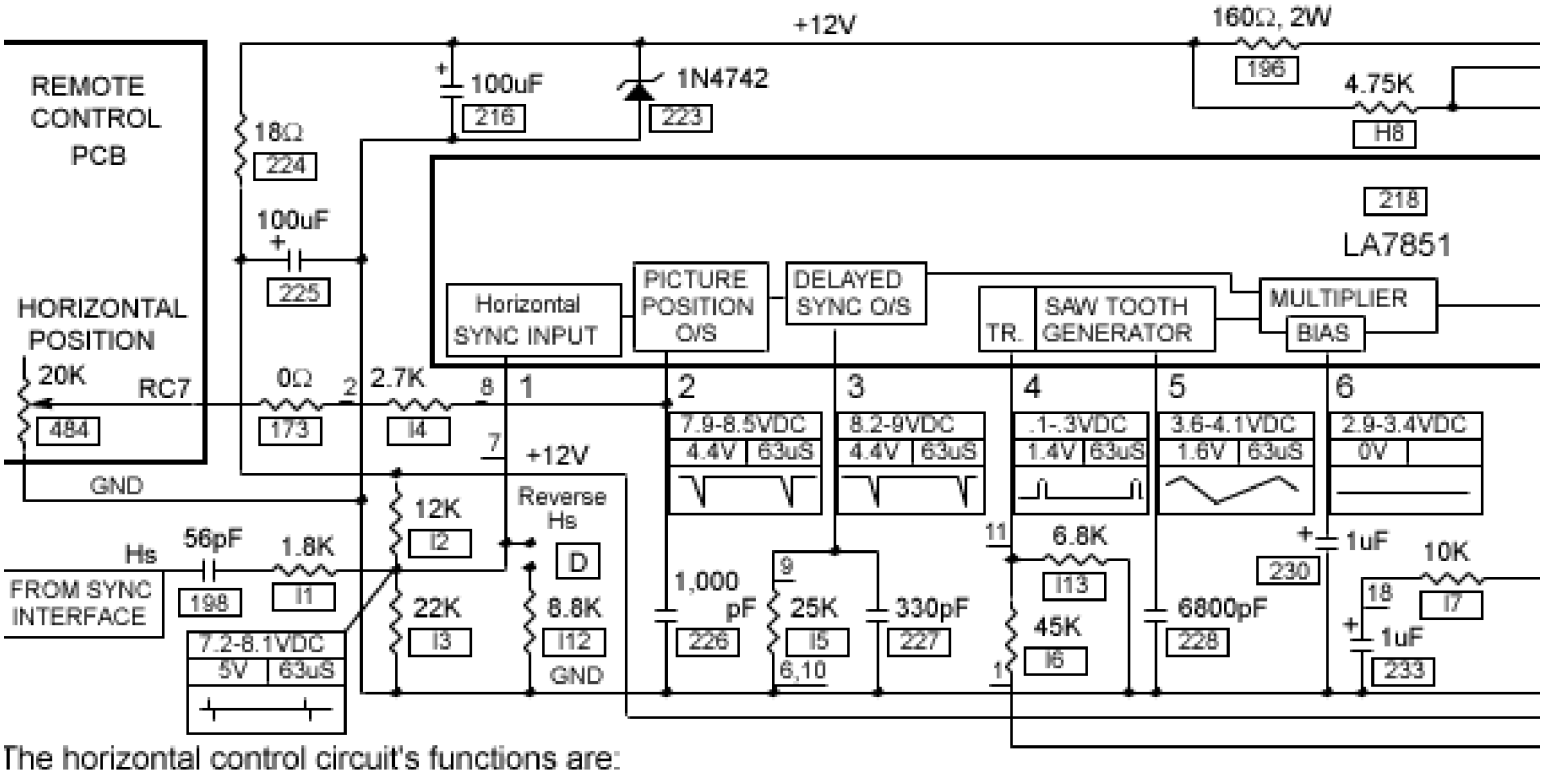
Retrace is started by partly discharging the ramp capacitor 202 through resistor H5 The vertical amplifier responds to the discharge of cap. 202 by outputting a high voltage across the yoke which reverses the yoke current. When the yoke current reaches the new value dictated by the voltage on 202, the vertical cycle starts over.

The vertical amplifier consists of a differential amplifier in the LA7851 with the + input at pin 16 and the - input is connected to an internal reference voltage (3.5V). The output of this amplifier is connected to the power driver stage which is located in the LA7830. Resistors H7 H11 and capacitors 208, 209, & 210 stabilize the LA7830 during trace time and capacitors 204 and 205 provide stabilization during retrace. The retrace booster doubles the 27 volt line voltage during retrace by connecting pin 7 of the LA7830 to the 27 volt line. This raises capacitor 191 7 volts which then applies 54 volts to pin 3 of the LA7830. Pin 3 is the retrace booster input and is connected to the vertical output stage. After the retrace cycle is over, capacitor 191 is recharged through diode 190

The vertical raster position control 463 sets the NPN transistor 180 base voltage. The emitter resistor 182 supplies current to the yoke through transistor 180 The magnitude of this DC current directly effects the vertical raster position.

The yoke return blocking capacitor 195 provides a voltage such that the vertical amplifier can drive the yoke with a + and a - current.

HORIZONTAL DEFLECTION CIRCUIT DESCRIPTION



The horizontal control circuit's functions are:

1. To provide the horizontal output circuit with a stable frequency with or without incoming horizontal sync.
2. To be able to adjust the picture position, horizontally, with respect to the raster.
3. To operate stability through periods of missing horizontal sync pulses.
4. To keep the picture from drifting within the operating temperature range.

All of these functions except for the picture position adjustment are accomplished by the phase locked loop (PLL). Delaying the horizontal sync with an adjustable timer produces the picture position adjustment.

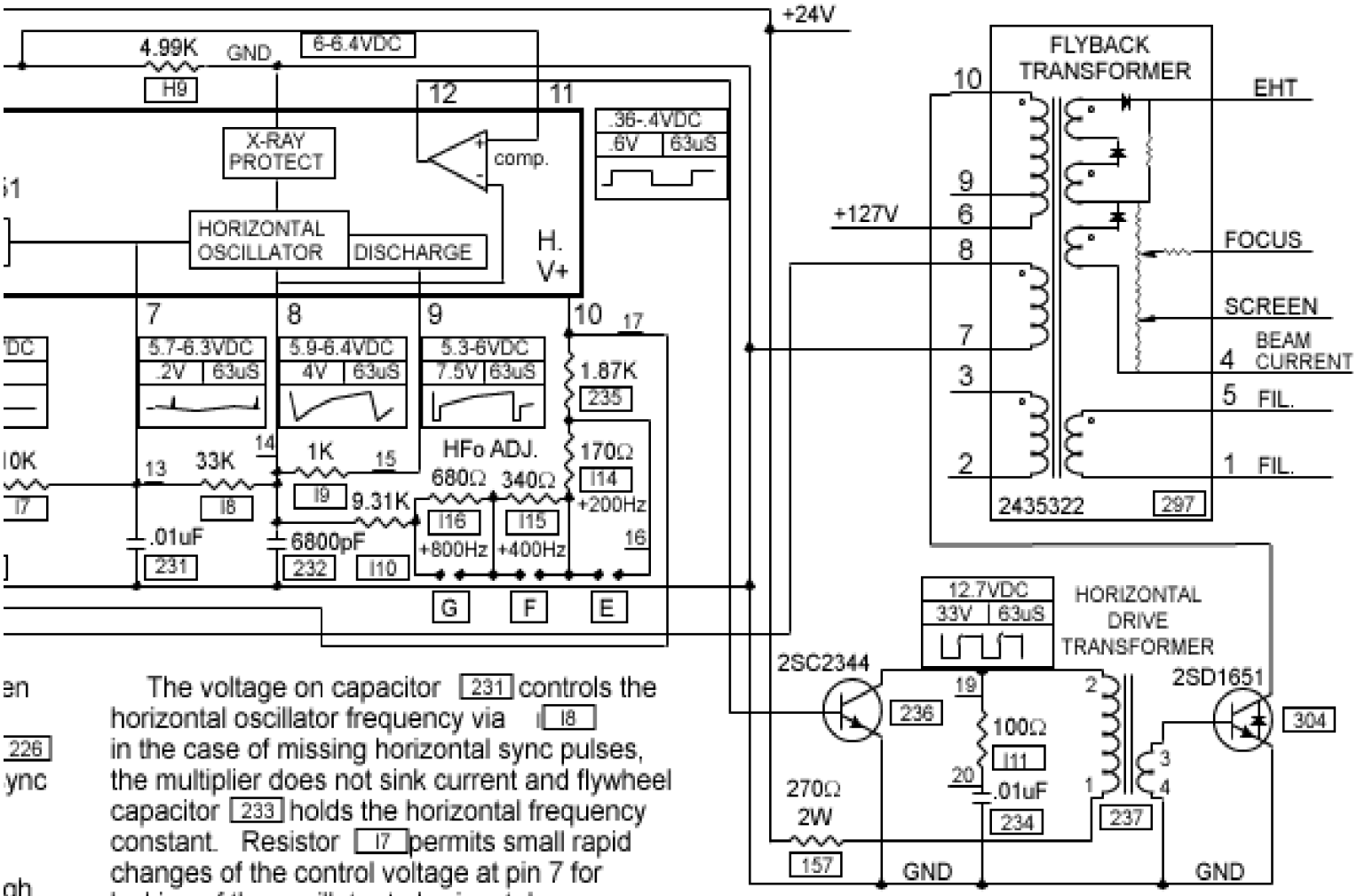
The horizontal sync input circuit (pin 1) will trigger the picture position O/S on either the rising edge, or the falling edge, of the horizontal sync pulse. To accomplish the edge triggering, the sync pulse is differentiated by capacitor 19 198 into two short pulses, one for the rising edge and one for the falling edge of the sync pulse. Which edge is the trigger depends on the bias voltage at pin 1. For positive edge triggering , the bias voltage is set to 7.8 volts by resistors I2 I2 and I3. For negative edge triggering, the bias voltage is set to 4.1V by connecting I12 via a solder bridge on the I PRA.

The picture position O/S clamps timing capacitor 226 to 8.2 volts until horizontal sync triggers this O/S. The voltage on the timing capacitor drops at a rate set by the horizontal position control 4 484 and resistor I4. When the voltage, at pin 2, drops below 4 volts the delayed sync O/S is triggered and capacitor 2 226 is reset to its clamped voltage. The delayed sync O/S functions the same as the picture position O/S with the exception that it is not adjustable.

The flyback pulse, connected to pin 4 through resistor I6, starts the negative slope of the saw tooth generator. When the sawtooth wave, which is produced by a current to capacitor 2 228 drops to 3 volts, the sawtooth generator switches back to the positive slope part of the wave till the next FBP.

During the active part of the delayed sync pulse, the multiplier gates current to capacitor 231 which is dependent on the sawtooth voltage at the delayed sync pulse time. capacitor 230 sets the "0" voltage for the multiplier which is the average value of the sawtooth waveform.

If the delayed sync pulse occurs when the sawtooth is at a low voltage part of its cycle, capacitor 231 discharges and the oscillator frequency lowers. If the delayed sync pulse occurs at the top part of the sawtooth wave no current flows to capacitor 2 231 This action, phase locks the horizontal oscillator to the incoming sync pulses.



The voltage on capacitor 231 controls the horizontal oscillator frequency via I8 in the case of missing horizontal sync pulses, the multiplier does not sink current and flywheel capacitor 233 holds the horizontal frequency constant. Resistor I7 permits small rapid changes of the control voltage at pin 7 for locking of the oscillator to horizontal sync.

The horizontal oscillator capacitor 232 charges to its upper voltage limit through resistors I10 I16 I15 I14 and 235. This capacitor is then discharged to the lower voltage limit through the action of discharge pin 9 and resistor I9. The free running frequency (Hfo) may be adjusted by making solder connections on the I PRA. (see page 56 for the I PRA layout) In some cases where there are many missing horizontal sync pulses, it is necessary to adjust the Hfo closer than ±200 Hz. For fine tuning the Hfo, resistor 235 is replaced with a pot.

The horizontal phase locked loop then consists of an oscillator which sets the flyback timing. The flyback pulse is then compared to the incoming sync pulse and the difference voltage holds the oscillator at the sync frequency.

The duty cycle of the horizontal drive transistor is generated by comparing the oscillator waveform against a fixed voltage. This fixed voltage is set by resistors H8 and H9.

The horizontal output transistor 304 conducts about three amps of horizontal flyback transformer primary current and deflection yoke current. This transistor has a beta as low as three. To supply the high base current a horizontal output transistor drive transformer is used. The drive transformer 237 builds up energy during the on time of the drive transistor, 236 which is the off time of the horizontal output transistor 304. Capacitor 234 and resistor I11 damps the drive transformer primary waveform.

The flyback transformer's main function is to supply EHT to the CRT. It also supplies the focus and screen grid voltages which are taps on the EHT supply. There are three low voltage secondaries. One supplies the filament current. Another supplies sync and EHT information to the power supply. The third secondary supplies sync for the horizontal PLL and drives the horizontal blanking circuit.

HORIZONTAL RASTER WIDTH CONTROL CIRCUIT DESCRIPTION

The purpose of the horizontal width control circuit is to:

1. Provide a convenient means for adjusting the horizontal raster size.
2. Correct pincushion distortion in the vertical axis.
3. Correct horizontal raster distortion caused by periods of high beam current.

The horizontal width control circuit is comprised of two main parts; The control circuit and the diode modulator (DM). The control circuit combines four signals in the monitor to produce the width control circuit. These signals are:

1. Horizontal size From the H. Size Pot.
2. Vertical current (Iv) From the 3.3 ohm vertical current feedback resistor.
3. Vertical parabolic + Iv From the vertical yoke return.
4. Beam current From the EHT return on the FBT.

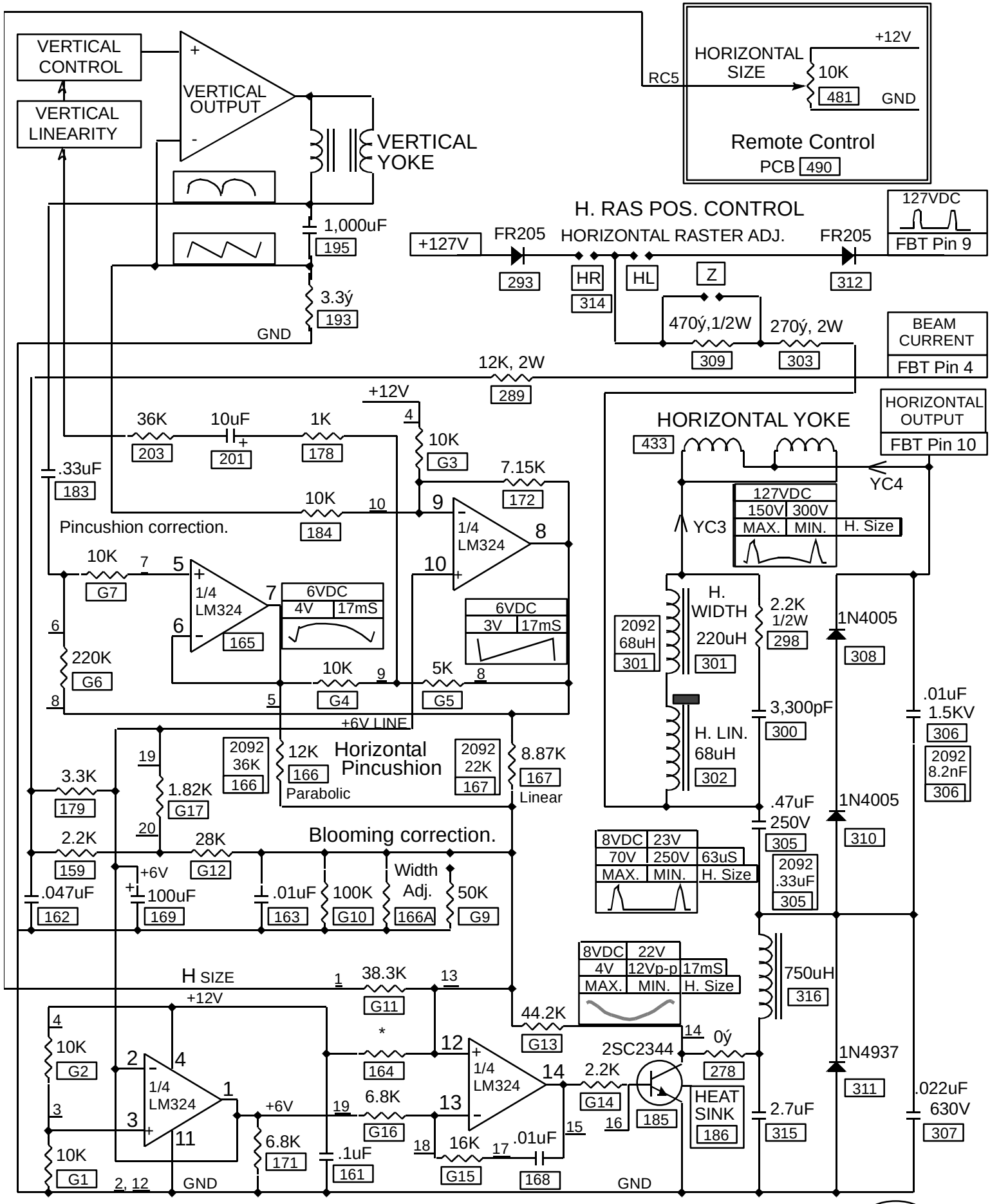
The diode modulator controls the horizontal yoke current which affects the horizontal size. This is accomplished by controlling the start time of the flyback pulse in the diode modulator node at the cathode of 311. The start time of this pulse is then a function of the forward current of the diode 311. This is because the current in the pulse across capacitor 306 must exceed the current in the diode 311 before the pulse in the diode modulator node can start. The current used to control the start time of the pulse comes from the voltage across inductor 316 from the previous horizontal pulse and is controlled by the control circuit.

The horizontal size voltage from the remote control PCB 490 applied directly to the control amplifier summing node (LM324 Pin 12) by resistor G11. For pincushion correction, the vertical parabolic voltage is needed, but it is not directly available since the vertical current,voltage (Iv) is part of the vertical parabolic voltage with respect to GND. The + Iv from the current sensing resistor 193 is inverted by an Op Amp and resistors 184 and 172. Resistor G3 level shifts the inverted Iv to + 6V. The (vertical parabolic + Iv) is AC coupled by capacitor 183 and resistor G6. It is then amplified by an Op Amp connected as a voltage follower. Resistor G7 protects the Op Amp against arc related voltage spikes. The inverted Iv (-Iv) and (parabolic voltage +Iv) are added to the amplifier node by resistors 167 and 166 which then makes up the pincushion correction signal.

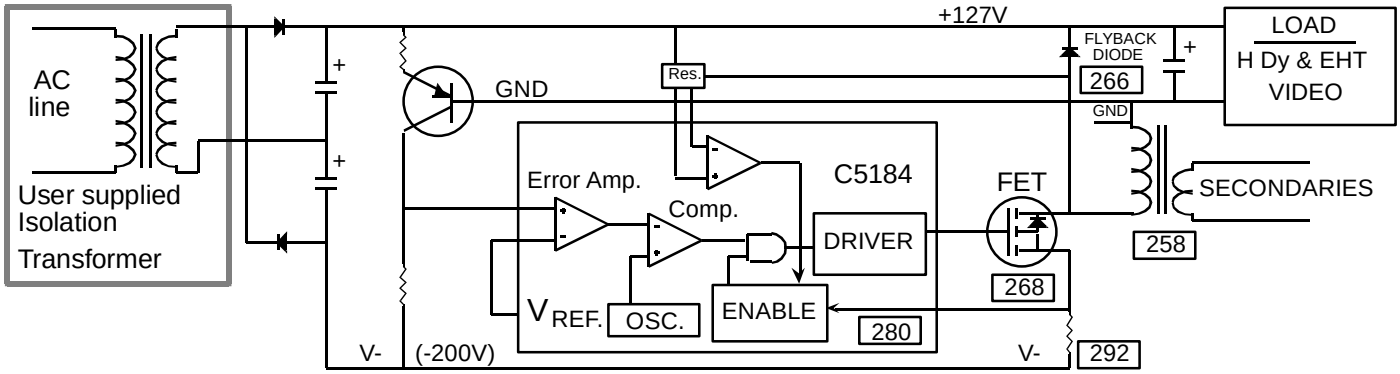
The beam current from the FBT is converted to a voltage by resistors G17, adj. 159 & adj. 179 and is filtered by capacitor 162. Resistor G12 then connects the signal to the width control amplifier node which accomplishes the blooming control function. The control amplifier converts the current at the summing node (LM324 Pin 12) to a voltage across capacitor 315 via feedback resistor G13. A power transistor 185 is necessary since up to 2 watts may be dissipated by the control amplifier. Resistor G15 and capacitor 163 & 168 set the AC gain of the control Op Amp for stable operation. Resistor G14 stabilizes the complete control amplifier by reducing the overall gain. Resistors G9, G10, 164 and 166A provide adjustment for setting the horizontal size range. The fourth Op Amp of the LM324 and resistors G1 and G2 are used to generate a +6 volt ref. voltage for the control circuit. Resistor 171 stabilizes this +6V line with a load to GND. Capacitor 161 decouples the deflection +12 volt supply by the LM324 165. Components G4, G5, 178, 201, and 203 are used to correct a slight nonlinearity in the vertical deflection yoke via the vertical control circuit.

The diode modulator (DM) incorporates diode 311 to control the voltage on the DM main node (cathode of 311) during the flyback pulse time. If the diode 311 has low forward current, the DM node voltage will be high during flyback time and the horizontal size will be small. The forward current in the diode 311 comes from the current buildup in inductor 316 during flyback time and the voltage across the capacitor 315 during trace time. If the voltage is large across the capacitor 315 during trace time, most of the inductor current is discharged before the next retrace cycle and the horizontal size is small. This condition can be checked by connecting a DVM to the vertical heat sink (GND) and to the heat sink 186 (collector 185). The voltage for minimum horizontal size is about 22V. Capacitor 315 supplies a voltage for the inductor 316 to work against similar to the 1,000uF capacitor 195 in the vertical yoke circuit. For max. horizontal size, the voltage across 315 is about 8V, and the diode 311, current before retrace is high Diodes 308 and 310 clamp the DM node to GND to keep the yoke current stable during trace time. Inductor 301 is an additional width coil and 302 is a horizontal linearity coil. Capacitor 300 and resistors 298 keep the coils from ringing after retrace. Capacitors 306 and 307 form the normal Cp. The raster may be shifted by making solder connections: left HL or right HR with increased effect Z. These solder connections introduces a DC current in the horizontal yoke via diode 293 or diode 312. Resistor 303 limits the maximum current and resistor 309 permits fine adjustment.

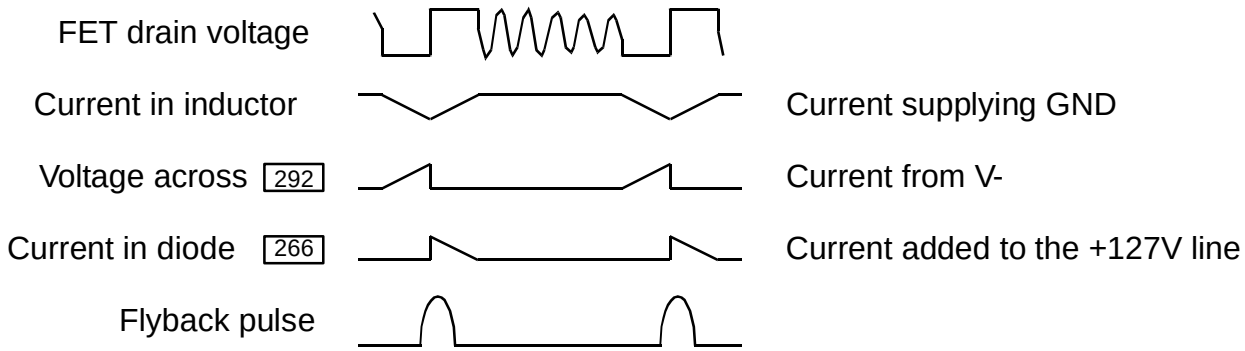
HORIZONTAL RASTER WIDTH and POSITION CONTROL SCHEMATIC



SIMPLIFIED POWER SUPPLY CIRCUIT FUNCTION DESCRIPTION



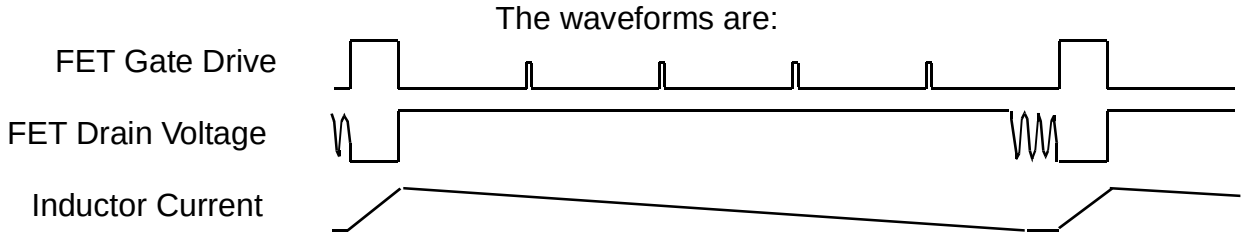
The switching regulator includes the power FET 26[268] which passes current from V- to GND through the inductor 25[258] During the time the FET is on, the current in the inductor is increasing and the inductor is storing energy. When the FET is turned off, the stored energy in the inductor continues supplying current to GND. But in this case, the current path is from V+ to GND, instead of V-to GND. During this part of the cycle, the current in the inductor is decreasing.



As can be seen from the waveforms, the largest number of changes occur when the FET is turned off. Also, the FET drain voltage switches fast due to the high inductor current. To minimize video interference from the power supply, the power supply is synchronized to the horizontal oscillator such that horizontal blanking is coincident with the FET turn off time.

The C5184 [280] is the series regulator IC. All of the control circuits that are built into this IC work together to produce one output signal, which is the FET drive signal. This signal can take on many shapes depending on the load conditions of the power supply. The waveforms for normal operation are shown above.

For the shorted +127V to GND condition, which also occur right on power up,



The first FET pulse is a full on pulse which causes current to flow in the inductor. After the FET is turned off the current in the inductor drops much more slowly than normal since the inductor is discharging into a much lower than normal voltage. If the FET were turned on for full power in the next cycle with current still flowing in the flyback diode, a current spike of 6A would occur, which is a power spike of 2,000W. The reason for this is that the diode stores charge when current flows which turns into reverse current for a short time when the voltage is reversed across the diode.

The FET drive waveform avoids this problem by sensing flyback diode conduction. If the flyback diode conduction is sensed, the low current start mode is selected. this mode turns the FET on, to a current of .1A, for not more than 4uS. If before or during the low current FET on time, the flyback diode breaks free, and the FET drain voltage goes down, the flyback diode voltage comparator will signal the regulator to permit the FET to be turned on for a full power cycle.
The cycle after the last low power cycle in the waveform above is an example of this condition. The flyback diode voltage comparator inputs are located at pins 12 & 13 of the C5184. The two resistor dividers J10, J11 and J12, 271 connect the comparator across the flyback diode. The comparator enables the FET drive only after a 10% voltage drop is measured across this diode.

Another fault condition exists when the FET exceeds 1.6A drain current. This condition can occur if the oscillator frequency is too low, the FET drain is shorted to GND or V+, the transformer has a shorted secondary, or the core is broken. In these cases the voltage across the FET source resistor 292 exceeds 1.6V which is sensed by the over current comparator at pin 11. If pin 11 exceeds 1.6V, the FET drive is set to 0V for the rest of the cycle. In some cases, this condition can produce an output waveform which looks normal, but the voltage across the load (+127V to GND) would be low or unstable. A quick check for this condition is to check the peak voltage across the FET source resistor. CAUTION; Whenever connecting a scope ground to V-, be sure that the other scope probe or common grounded devices are not connected to the monitor GND.

Most of the power supply fault conditions cause the power supply to chirp because the source of +17V for the regulator IC is generated by the power supply. A special circuit is built into the regulator IC, which permits charging the +17V line filter capacitor with only a very low load from the IC. This circuit turns the rest of the IC on only after the voltage at pin 15 reaches 17V. If the transformer does not supply at least 12V to this line before the filter capacitor discharges to 12V, the regulator IC turns off. The reason for the audible chirp, is that, the power supply is not full on for each cycle which produces a frequency low enough to hear.

A 19V to 20V @ 1A, DC, isolated power supply is a tool necessary for trouble shooting CERONIX monitors. When trouble shooting the power supply, it can be connected to V- and the +17V line to keep the power supply running while checking the voltages and waveforms to find the fault. It can also be used to supply the GND to +24V line for checking the horizontal circuit. If the horizontal circuit does not work, the power supply will chirp. Without the horizontal circuit working, there is not enough load on the power supply for transformer action to keep the regulator IC +17V line up to the minimum of +12V. A quick check for this condition is to clip a 2-4K@10W power resistor from GND to +127V line. If the chirping stops, the horizontal is probably not working.

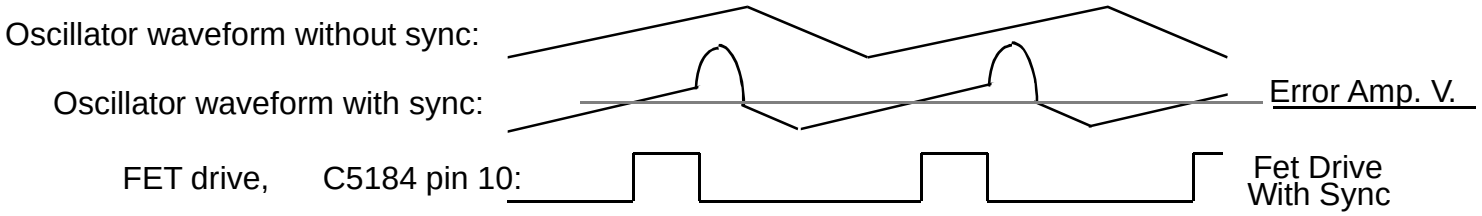
The heart of the power supply is the oscillator which supplies the basic timing. The FET drive is always low during the negative slope of the oscillator or, when synchronized, after the start of the sync pulse. The low to high transition of the FET drive, pin 10, is determined by the voltage at the output of the error amplifier. If the 127V line goes up in voltage, the error amplifier voltage goes up, which then intersects the oscillator waveform at a higher voltage and causes the FET on time to start later and be shorter. This negative feedback accomplishes the control loop of the power supply.

The regulator IC has a built in reference voltage which is used by the error amplifier set and hold the +127V line constant. Solder connections on the J PRA are used to adjust the +127V line in steps of ±1.5V.

The over voltage protect circuit, when activated, turns off the regulator IC until power is disconnected. This circuit is connected to the rectified flyback pulse, which outputs a voltage that is proportional to the EHT. The circuit's main purpose is to protect the user against excessive x-ray which is caused by excessive EHT.

SWITCH MODE POWER SUPPLY CIRCUIT DESCRIPTION

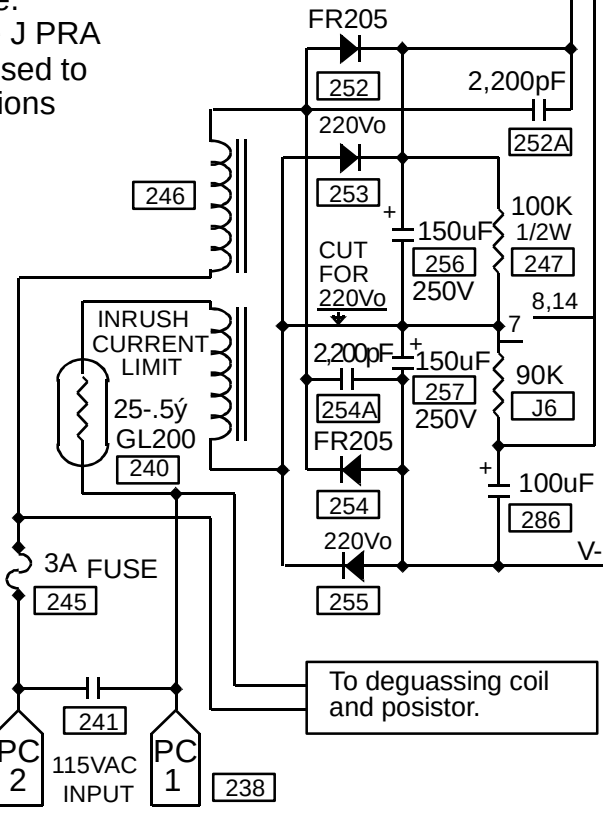
The series regulator IC 280 controls current to the monitor GND by pulse width modulation. A PNP transistor 250 has an emitter current, that is directly proportional to the 127V line voltage due to resistor J1 and adjustment resistors J13 J14 This current is transmitted to the power supply V- line, and is applied to a resistor J5 J15 J16 The voltage across these resistors is compared to a reference voltage by the error amplifier. If the +127V line goes up the output of the error amplifier voltage goes up. The pulse width modulation, which controls the + 127V line voltage, is accomplished by turning the FET drive on at some particular voltage along the rising slope of the oscillator waveform. This particular voltage is the error amplifier output voltage.



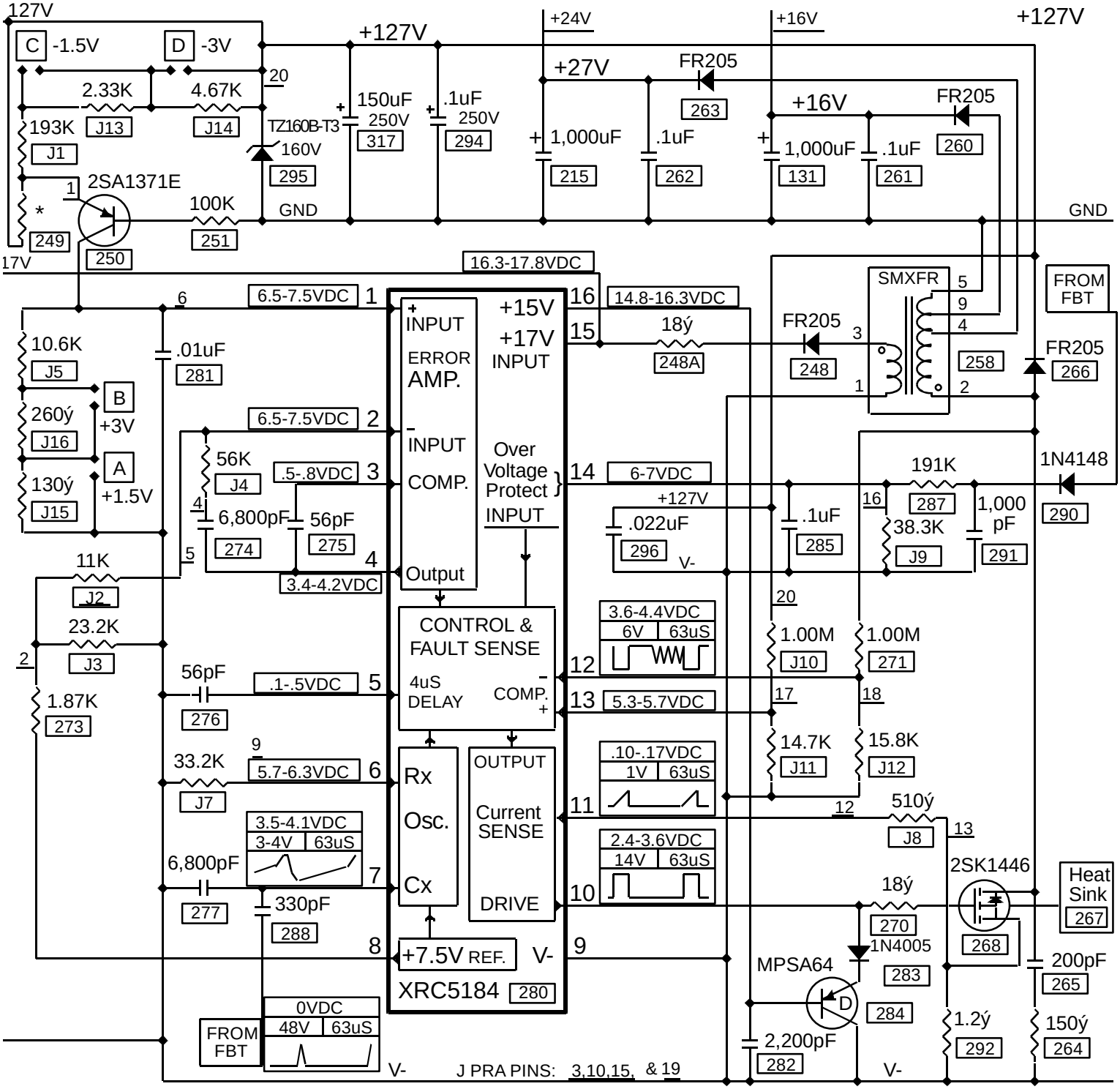
The FET drive is always off during the negative slope of the oscillator, or just after the sync pulse. Since the FET drive pulse is started by the error amplifier voltage and terminated by the end of the oscillator cycle, a control system via pulse width modulation has been established. The oscillator waveform is produced by charging capacitor 277 with a constant current set by resistor J7 to a voltage of 5V and then discharging the capacitor with double the charging current to 2.5V. Adding the flyback pulse, via capacitor 288 to this waveform synchronizes the oscillator, since the oscillator frequency is set below the horizontal frequency.
Resistors J2, J4 and capacitor 274 limit the error amplifier's AC gain, to hold the control loop stable. Capacitor 275 holds the error amplifier stable. Capacitor 281 reduces power supply noise, but, if too large, will cause the power supply to be unstable.

The 127V line is adjusted by making solder connections on the J PRA (refer to page 56 for the layout). Solder connections A and B are used to raise the 127V line up to 4.5 volts in steps of 1.5 volts. Connections C and D lower the 127V line as much as 4.5V. The 127V line should be adjusted if below 125.8V or higher than 128.2V. Resistors 273 and 249 are used for monitors with special 127V line voltages.

The FET 268 works together with the transformer 258 to provide a low resistance current path from V- to GND. This low resistance coupled with no large voltage times current products is what makes the power supply efficient. Resistor 292 provides a means for sensing the FET current. In the low current mode, it is used to set the 100mA current and in the full on mode it is used to sense the max. current. Resistors 264, 270 and capacitor 265 reduce power supply electrical noise. Transistor 284 and diode 283 short the FET drive to V- when the monitor is turned off to protect the FET from conducting current with a still large drain voltage. Resistors J10, J11, J12 and 271 provide a means for checking flyback diode 266 conduction via a comparator. If the comparator measures low flyback diode voltage the FET is turned on to the .1A low current mode. This mode is necessary during power up, since initially the +127V line is 0V and no reverse diode voltage exists. The over voltage protect circuit has a trip voltage of 8V and when it is activated, it shuts down the power supply. The EHT is measured by rectifying the flyback pulse, with diode 290 from a secondary winding of the FBT. Capacitors 291 285 and resistors 287, J9 are connected as a low pass filter to smooth out the simulated EHT voltage which is then applied to the C5184 at pin 14. Resistor J8 protects the IC current sense input from voltage spikes and resistor 251 protects the PNP transistor from momentary overvoltage damage due to line spikes. Zener diode 295 protects the horizontal and video circuits from overvoltage due to power supply failure. If the +127V line exceeds 160V, the zener diode 295 shorts to GND the +127V line.



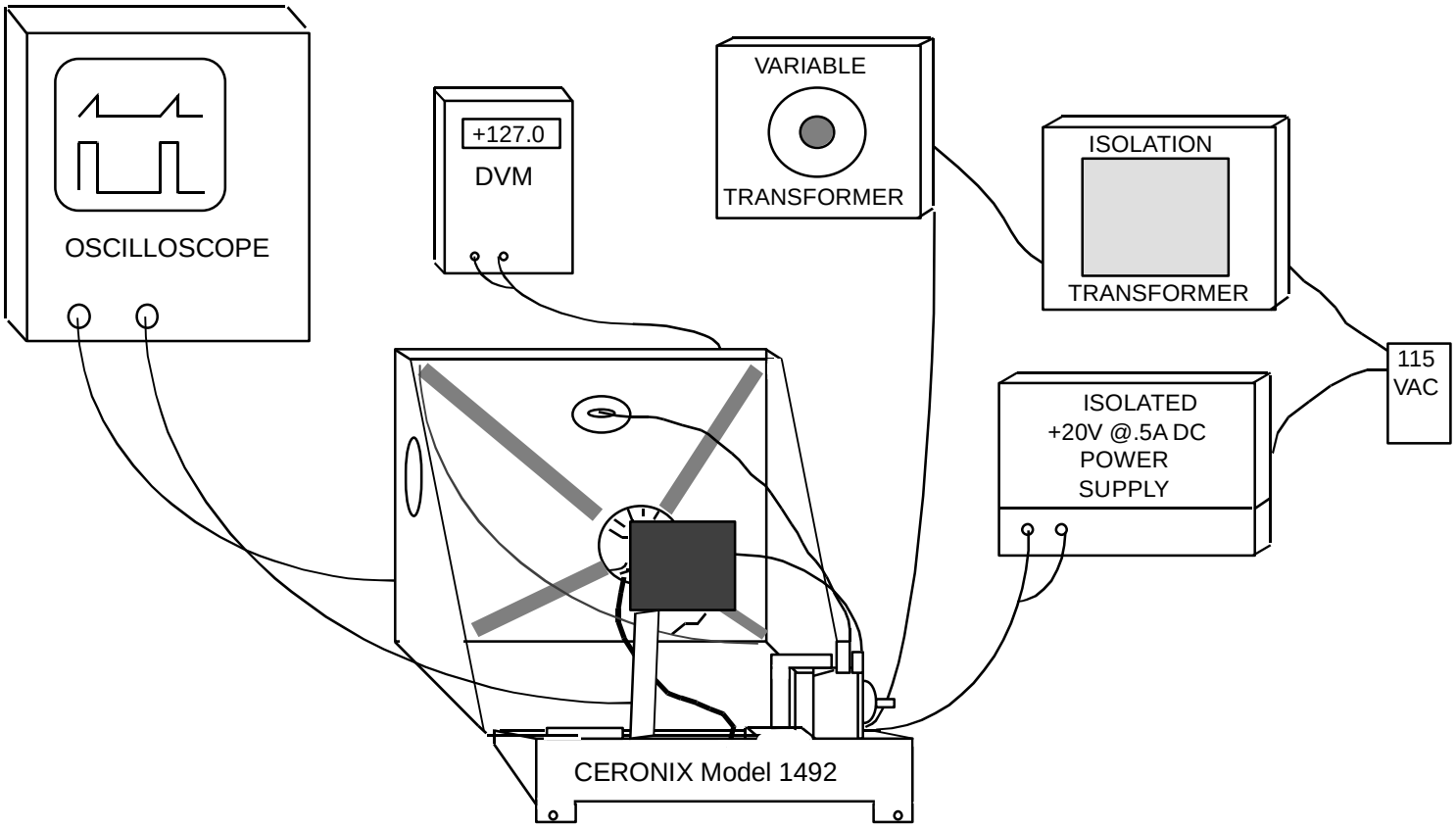
SWITCH MODE POWER SUPPLY SCHEMATIC



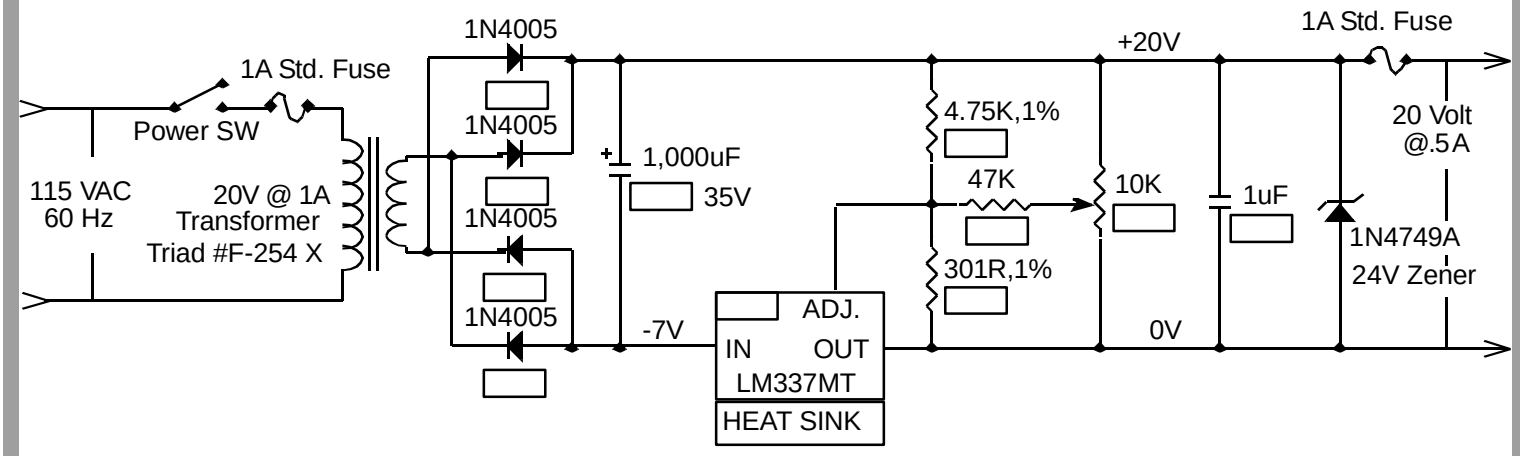
POWER SUPPLY	VOLTAGE	CURRENT	CIRCUIT SUPPLIED	DIODE	FILTER CAP.		NOISE CAP.	
LOW VOLTAGE SECONDARIES	17VDC	7mA	POWER SUPPLY CONTROL	248	100uF	286	NONE	
	16VDC	250mA	VIDEO AND INPUT	260	1,000uF	131	.1uF	261
	27VDC	250mA	V. &H. DEFLECTION	263	1,000uF	215	.1uF	262

At the input to the power supply is a voltage doubler which outputs between 240 to 425VDC depending on the AC line voltage. It has a three amp fuse 24[245] o protect the PCB traces, an inrush current limiter [240] o protect the rectifier diodes 252[252] 54[254] nd optional capacitor 241[241] inductor [246] which can be used to reduce conducted noise from the monitor AC input. For 220VAC operation the voltage doubler is replaced by a full wave rectifier by adding diodes 253[253] 25[255] d cutting the 220Vo trace. [256] & [257] are the raw DC filter capacitors. Resistor J6[J6] pplies the power supply start current and resistor 2[247] alances the series connected filter capacitors for 220VAC operation.

Equipment setup for repairing the Model 1492 Monitor



ISOLATED +20V POWER SUPPLY CIRCUIT.



Problem Solving Tools

SAFETY FIRST; Use only one hand when working on a powered up monitor to avoid electrical shock. Always wear safety glasses.

Many of the failures that cause burnt components and boards are eliminated by the load sensitive switching mode power supply in the CERONIX monitor. This feature can cause problems with servicing the monitor if the proper trouble shooting approach is not used. The equipment setup, shown here, is necessary for efficient trouble shooting of the CERONIX monitors.

Problems that cause the power supply to chirp are:

1. Insufficient +127V line load.
2. Overloaded +127V, +24V, or +16V lines.
3. Shorted +127V, +24V, or +16V lines.
4. Power supply component failure.
5. Raw DC (+127V to V-) voltage too low.

1. A quick check for the insufficient +127V load is to connect a 2K to 4K ohm 10 watt power resistor to GND and the +127V line. If the chirping stops, proceed to check the horizontal deflection circuit. First disconnect the board from the AC supply. Then connect the +20V supply, 0V line to GND, and the +20V line to +127V and +24V lines on the monitor. Now the complete horizontal and vertical circuits can be checked with the oscilloscope and DVM.
The flyback waveform will be about 140Vp–p instead of 1,000Vp–p which permits checking even the horizontal output transistor, collector, waveform.

2. For the overloaded supply line problems, which often occur only when the +127V line is fully powered up, the +20 volt external power supply is used to keep the monitor power supply running. To use the external supply, connect the 0V line to V- (anode of diode 25 254 and the +20V line to the monitor power supply +17V line (cathode of diode 24 248
Connect the oscilloscope GND to V- and the probe to the FET drive (anode of diode 28 283
TAKE CARE NOT TO TOUCH THE OSCILLOSCOPE AND MONITOR CHASSIS DURING THIS TEST, SINCE
THE VOLTAGE DIFFERENCE CAN BE AS HIGH AS 400 VOLTS.
Increase the AC supply, slowly, to the normal operating voltage while monitoring the +127V line to GND voltage with the DVM. The power supply overload condition can be seen on the scope as an almost square wave which can break up into short and long pulses as the AC line voltage is increased. The short pulses are the flyback diode current sense pulses. Sometimes the monitor will operate normally in this mode, in which case, watch for smoke and after a few minutes of operation disconnect the power connections and carefully feel around the conductor side of the board for hot spots. Overload conditions will not harm the power supply unless there is a problem in the power supply.

3. If the +127V crowbar zener 2 295 s shorted, a fault exists in the power supply which permitted the +127V line to exceed +160V. First replace the zener. Never operate the monitor without the crowbar zener installed. Then with the external supply, the DVM, and the scope connected to the power supply (as in 2) slowly increase the AC line and observe the power supply response. Do not exceed +145V on the +127 V line. If the monitor runs normally, a fault may still exist in the power supply power down circuit. Check parts 283 283 d 284 284 the crowbar zener is shorted and the FET is internally shorted, the C5184 IC 280 280 uld also be replaced.
If there is no FET drive waveform, check the voltages and waveforms on the C5184 pins and compare them to the voltages and waveforms on the schematic.
Shorts on the +127V, 24V, and 16V lines other than the crowbar zener are not likely to be connected to the power supply even though the power supply chirps. By operating the power supply with the +20V external power supply many of these problems can be found using the same procedure as are used in trouble shooting monitors with linear power supplies.

4. The power supply may chirp if: The transformer core is broken or a winding is shorted.
The 1.2 ohm current sensing resistor value is too high.
The +17V line is open. (goes away when ext. PS is used)

5. There is a line voltage range of about 60% to 70% AC line voltage where a correctly operating monitor will chirp.

SETUP AND CONVERGENCE PROCEDURE

1. Use a knife to brake free the magnetic rings on the yoke which are locked with red varnish. Bring the adjustment tabs on each pair of magnetic rings in line for the starting point.

2. Loosen the yoke clamp. Remove the yoke wedges and the tape from the CRT.

3. Connect a test generator to the video input and clip the red lead to the +12V line (anode of diode 101).

4. Turn the monitor on. Switch the test generator to red field. Adjust the horizontal and vertical raster size, on the remote control board, for under scan. Let the monitor run for at least half an hour.

5. Check the auto bright control voltage with a DVM connected to GND and pin 8 of the LM324 146. The voltage range is 4.3V to 4.9V. If out of range, adjust this voltage to 4.6V by using pliers to rotate the bottom knob on the FBT.

6. Degauss the picture tube and front part of the frame.

CAUTION: To avoid electrical shock , take care not to touch the yoke conductors or push against the anode cap. Always keep one hand away from unit.

7. Adjust the yoke position, on the CRT neck, to the center of purity. One way to locate this yoke position is to make a felt pen mark on the CRT neck at the rear extreme of purity and another mark at the front extreme of purity. Make a third mark between the two marks and set the yoke to this position. Rotate the yoke to line up, the raster top line, with the top of the picture tube. Tighten the yoke clamp. Tilt the yoke side to side and up and down while watching the red field to verify that purity is good.

8. On the 13 inch CRT, use the purity magnets (closest to the yoke coils) to center the raster horizontally. To accomplish this, find the rotational position where spreading the tabs has the most effect on the horizontal position and spread the tabs a minimum to center the raster horizontally. On the 20 inch CRT, the purity magnets are often needed to optimize purity. The horizontal raster position solder connections are used to adjust the raster position. These solder connections are located on the foil side of the PCB next to the FBT. Connection HR shifts the raster right, HL shifts the raster left and the range of this shift can be increased by making solder connection Z under resistor 309

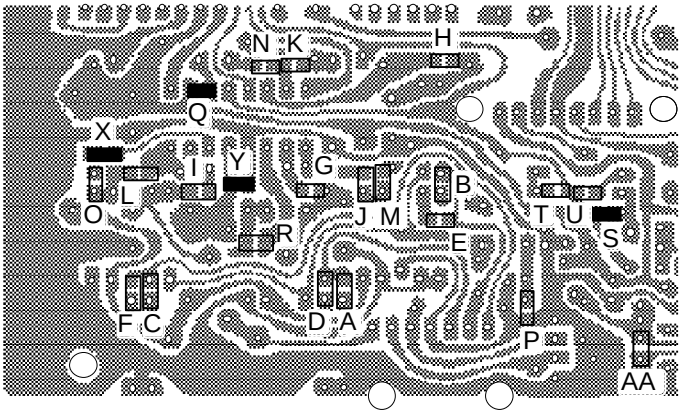
9. Check the purity with red field and with blue field while tilting the yoke side to side and up and down.

10. Switch the generator to red/blue grid. Adjust the 4 pole magnets (center pair) for convergence of the red and blue guns in the center of the screen.

11. Tilt the yoke up and down for the best convergence around the edge of the grid. Insert the top yoke wedge. Tilt the yoke side to side for the best convergence around the edge of the grid and insert the rest of the yoke wedges. Secure the wedges with tape.

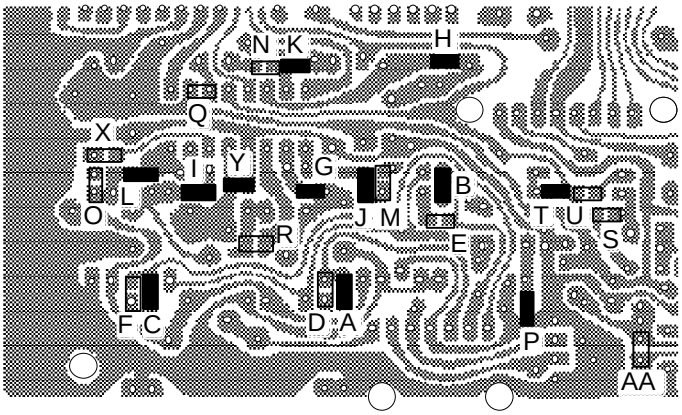
12. Switch the generator to white grid. Adjust the 6 pole magnets (Pair closest to the socket board) for convergence of the green gun. Step #10 and this step may have to be repeated for optimum convergence.

1492 & 2092 VIDEO INTERFACE PROGRAMS



AC Coin & Slot Service; (1492)

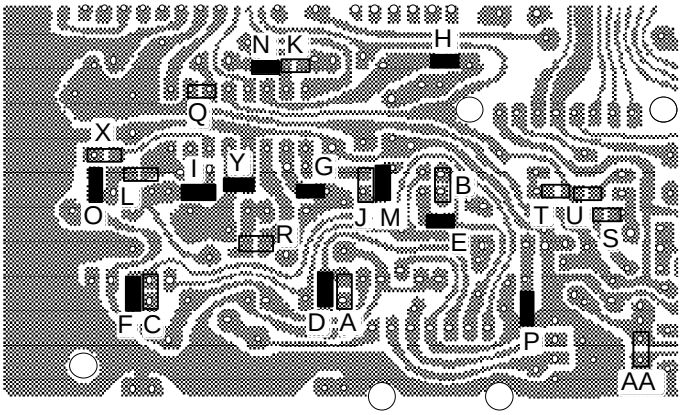
4 Solder Connections: Q, X, Y, & S.
Standard Board.



Advanced Touch Systems; (1492)

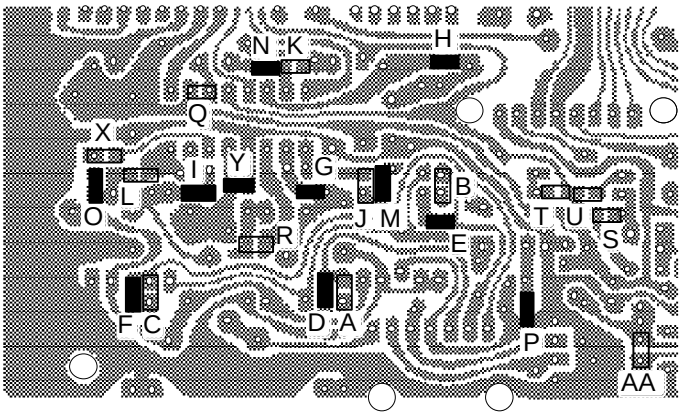
Change 007 , 024 , & 037 from 340ý to 205ý ±1%
Change 008 , 023 , & 034 from 12.1K to 7.15K ±1%,

12 Solder Connections: A, B, C, G, H, I, J, K, L, P, T, & Y.



Aeries International; (1492)

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.
Standard Board.

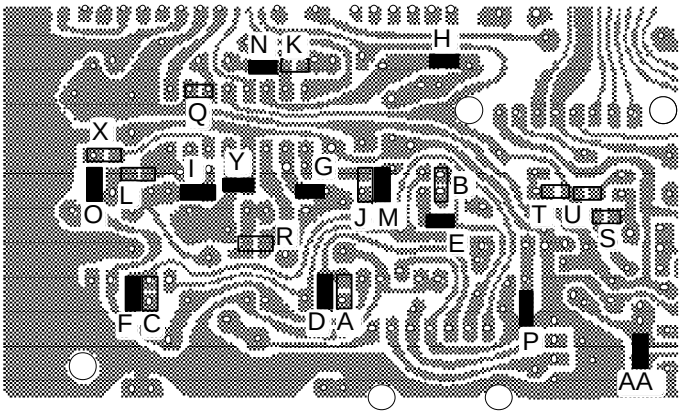


Altec; (1492)

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.
Standard Board.
HFo = 15,370 ±200Hz.

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

1492 & 2092 VIDEO INTERFACE PROGRAMS



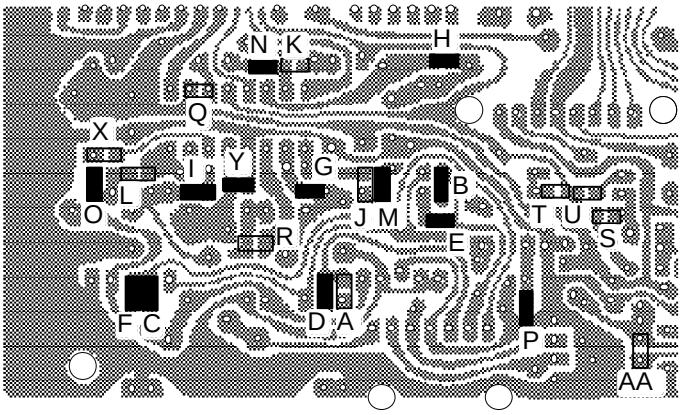
Aristocrat; (1492)

Install three 100pF disc capacitors at 010 , 022 , & 041 .
Invert horizontal sync by adding a solder connection on the "I" PRA above pin 5.
Install posistor at 244 .

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.

Before final test, clip out 045 , 270 ohm resistor, and add one solder connection AA by component no. 060 .

High resolution board.



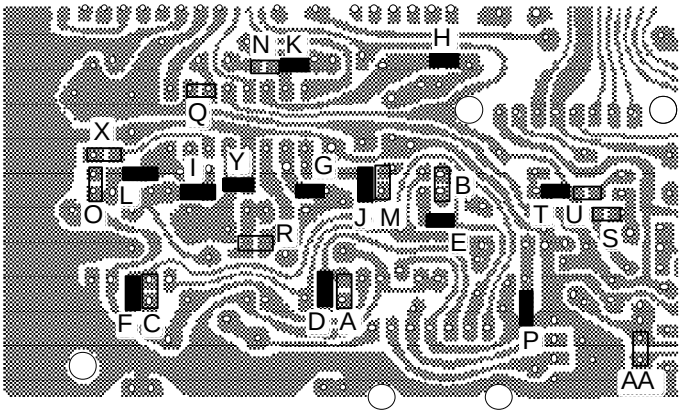
Automation; (1492)

Change 002 From 75ý to 130ý..
Change 027 From 75ý to 47ý.
Change 094 from 2.7K to 10K.
Install posistor 244 .

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y

Before final test add solder connections B & C.

High resolution board.



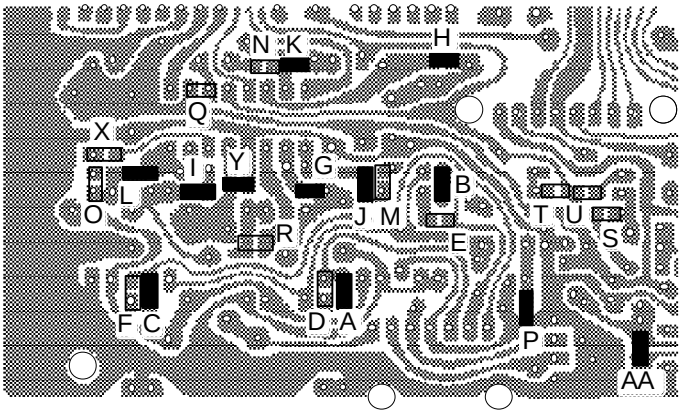
Bally; (1492)

12 Solder Connections: D, E, F, G, H, I, J, K, L, P, T, & Y.

Add a solder connection on the "I" PRA above pin 5.

Install posistor at 244 .

High resolution board.



Brunswick; (1492)

Change 007 , 024 , & 037 from 340ý to 301ý ±1%
Change 235 , from Hfo set resistor to 3K pot.
Remove the 2.7K resistor at 094 .
Add a solder connection on the I PRA above pin 5.

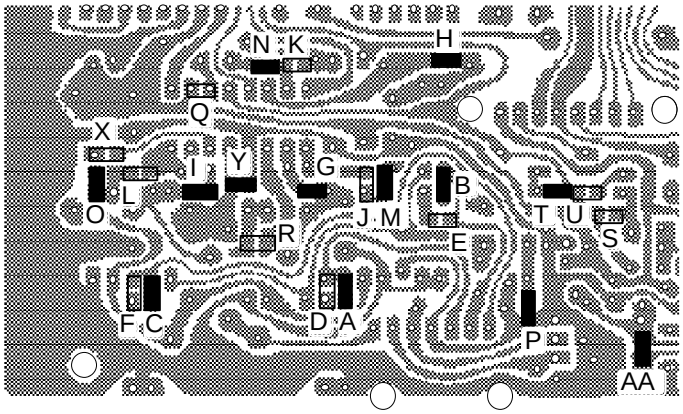
11 Solder Connections: A, B, C, G, H, I, J, K, L, P, & Y.

Before final test, add the AA solder connection and cut out the 270ý resistor at 045 .

Standard board.

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

1492 & 2092 VIDEO INTERFACE PROGRAMS



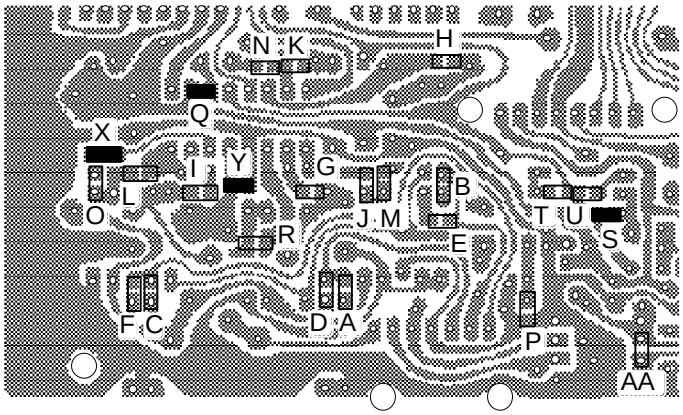
By Video; (2092)

Change 008 , 023 , & 034 from 12.1K to 2.67K,1%
Change 002 , 005 , & 027 from 75ý to 2.7K, 5%, 1/4W
Change 203 from 36K, 5% to 24.3K, 1%.
Install posistor at 244 .

12 Solder Connections: A, B, C, G, H, I, M, N, O, P, T, & Y.

Before final test, clip out 045 , 270 ohm resistor, and add one solder connection AA by 060 .

For the 13" CRT monitor, Add solder connection S, and omit T . do not change resistor 203



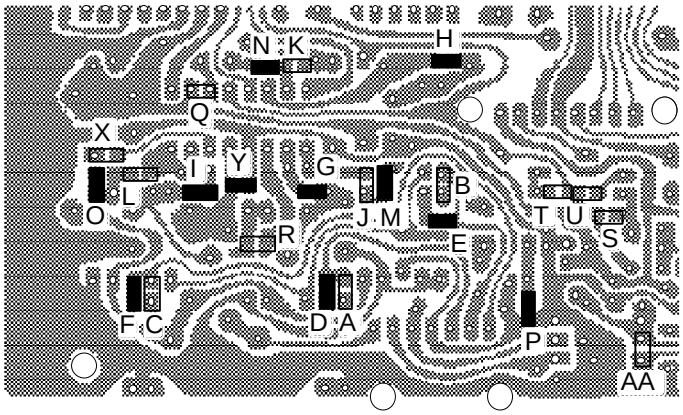
12 Solder Connections: Q, X, Y, & S.

Carson Valley Inn; (1492)

Change 200 from 127K to a 200K pot.

4 Solder Connections: Q, X, Y, & S.

High resolution board.

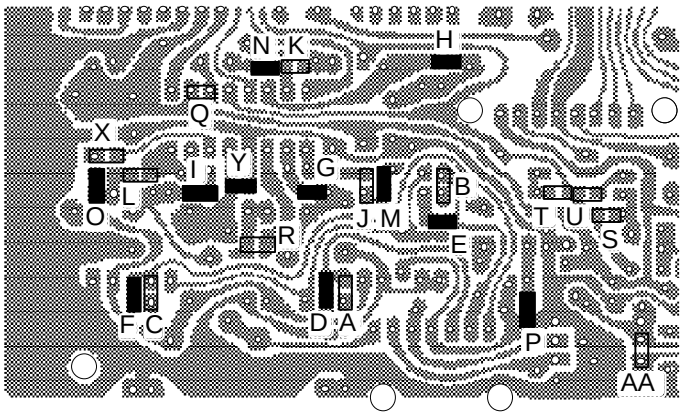


CAS Ltd.; (1492)

Add a solder connection on the I PRA above pin 5.
Change 094 from 2.7K to 10K.

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.

Standard board.



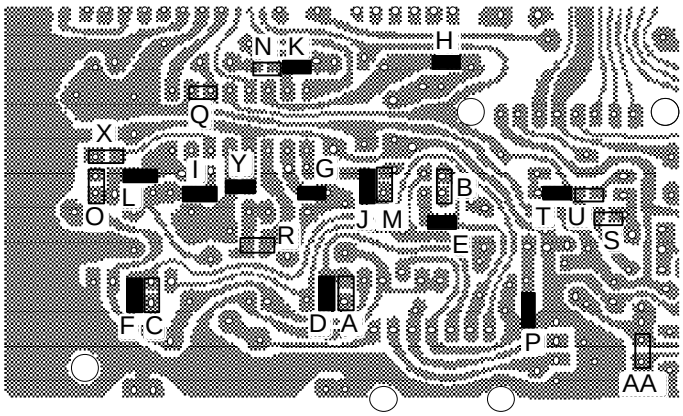
CEI; (1492)

Change 094 from 2.7K to 10K.
Install the posistor at 244 .

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

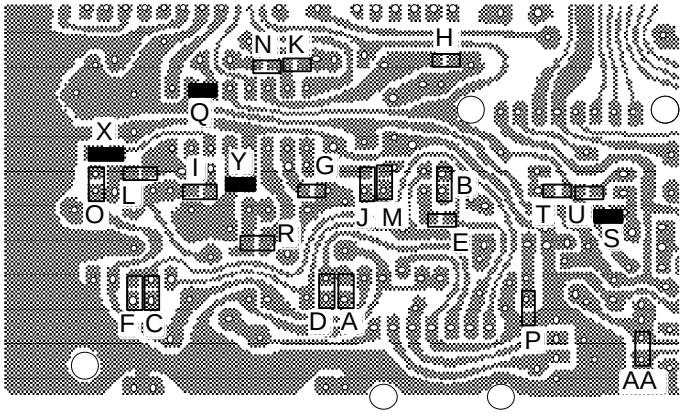
1492 & 2092 VIDEO INTERFACE PROGRAMS



Games of Nevada; (1492)

12 Solder connections: D, E, F, G, H, I, J, K, L, P, T, & Y.

High resolution board.

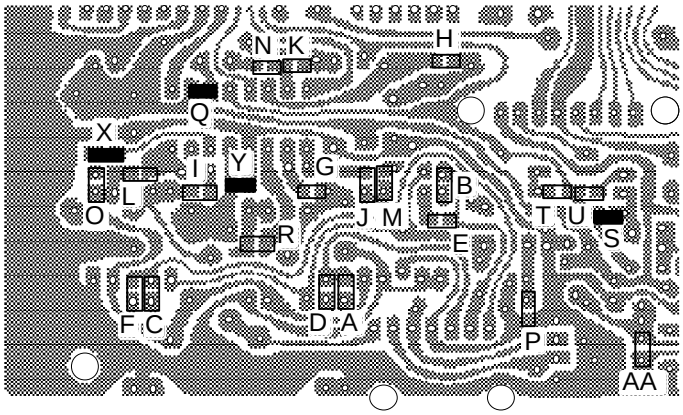


IGT; (1492)

Delete degaussing circuit.

4 Solder Connections: Q, S, X, & Y.

High resolution board.



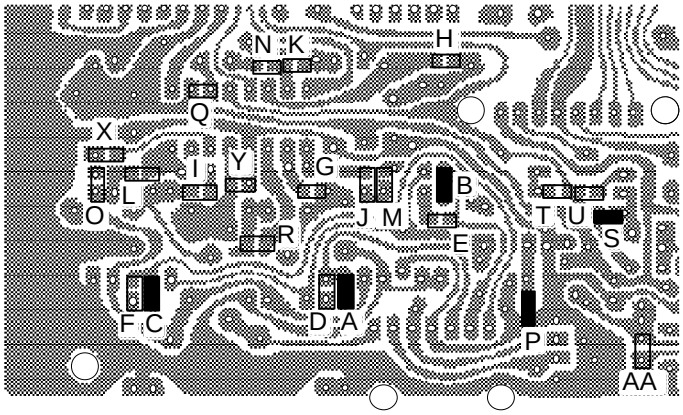
Keevex; (1492)

Install posistor at 244 .

4 Solder Connections: Q, S, X, & Y.

Horizontal frequency is 17,182Hz

High resolution board.



Mast Keystone; (1492)

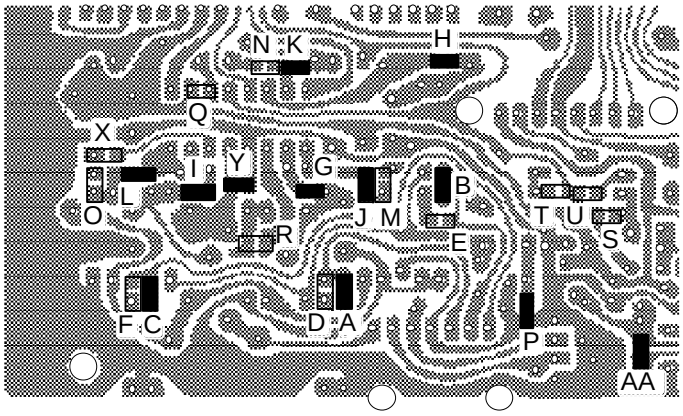
Change 002 , 005 , & 027 from 75ý to 1K ±5%.

5 Solder Connections: A, B, C, P, & S.

Standard Board.

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

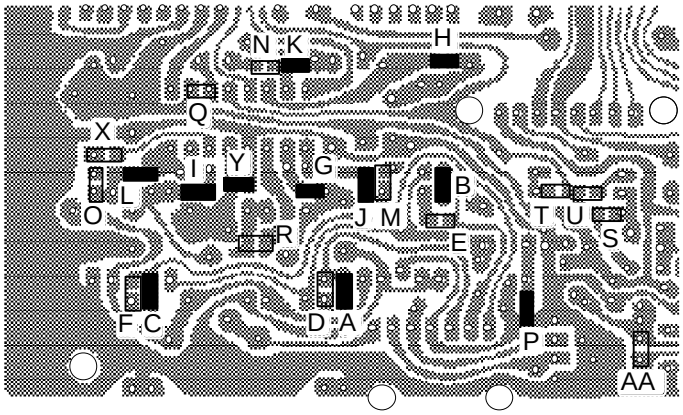
1492 & 2092 VIDEO INTERFACE PROGRAMS



RS 170; (1492)

Change 007 , 024 , & 037 from 340 ohm to 140 ohm ±1%.
Change 008 , 023 , & 034 from 12.1K to 3.32K ±1%.
Remove 045 , 046 , 047 , & 048 .
Add a 2.2K resistor to hole by video connector 006 pin 5 and hole between resistors 050 & 051 .

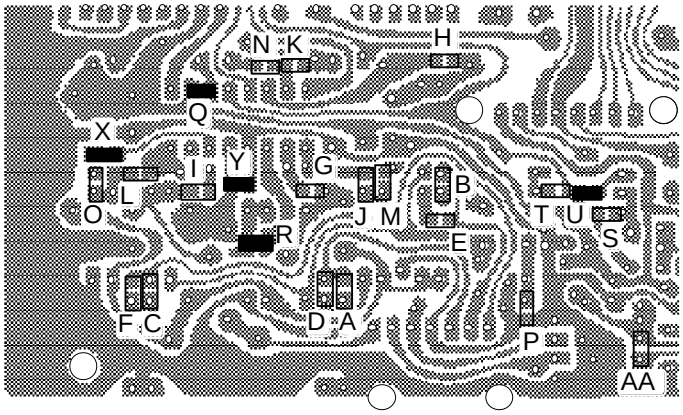
12 Solder Connections: A, AA, B, C, G, H, I, J, K, L, P, & Y.



Semi-Conductor; (1492)

Change 002 , 005 , & 027 from 75ý to 27ý ±1%.
Change 007 , 024 , & 037 from 340ý to 140ý ±1%.
Change 008 , 023 , & 034 from 12.1K to 3.32K ±1%.
Change 064 from 2.7K to 10K ±5%.
Install posistor at 244 .

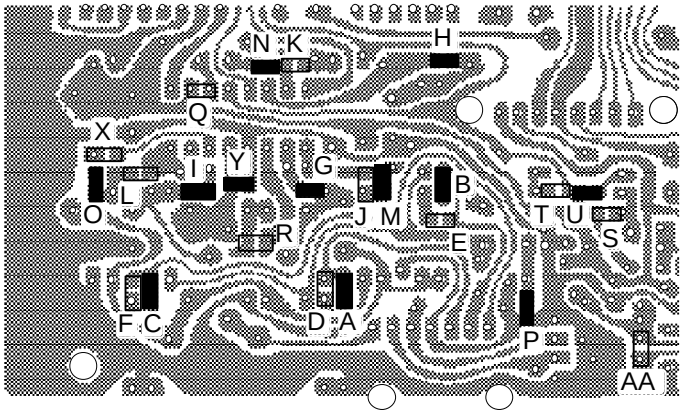
11 Solder Connections: A, B, C, G, H, I, J, K, L, P, & Y.
High resolution board.



Syntec; (2092)

Change 203 from a 36K ±5% to a 24.3K ±1% resistor.
Change 094 from 2.7K to 10K ±5%.
Delete degaussing circuit.

5 Solder Connections: Q, U, R, X, & Y.



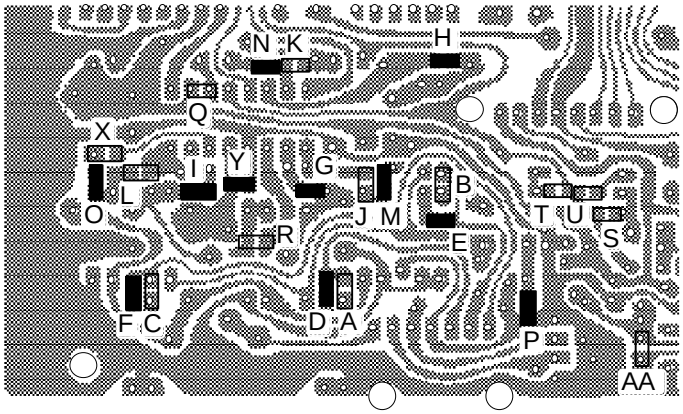
United Tote; (1492)

Change 002 , 005 , & 027 from 75ý to 1K ±5%.
Change 008 , 023 , & 034 from 12.1K to 4.42K ±1%.

12 Solder Connections: A, B, C, G, H, I, M, N, O, P, U, & Y.

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

1492 & 2092 VIDEO INTERFACE PROGRAMS



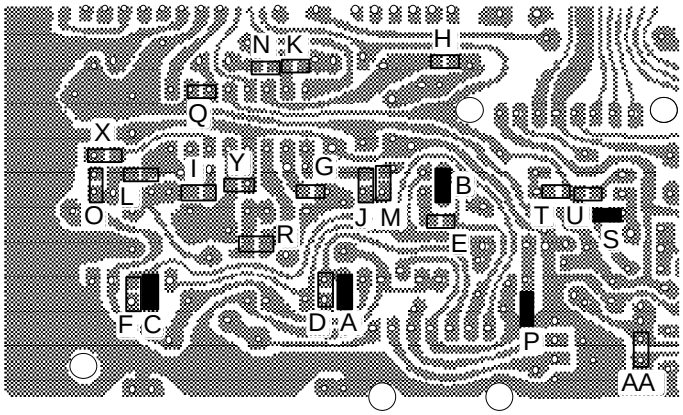
Western Amusement (1492)

Change 094 from 2.7K to 10K, ±5%.

Install posistor 244 .

11 Solder Connections: D, E, F, G, H, I, M, N, O, P, & Y.

Standard board.

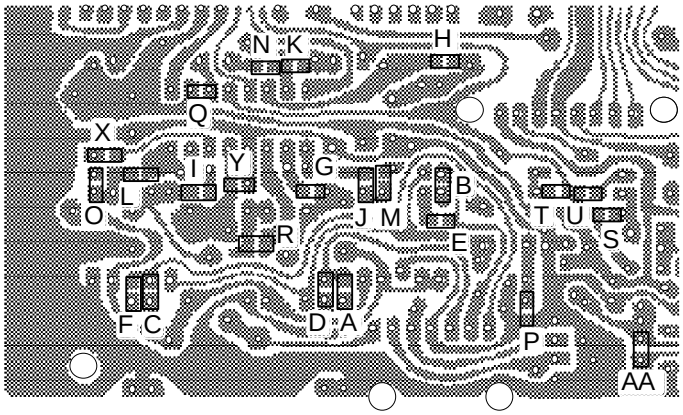


4 Line TTL; (1492)

Change 002 , 005 , & 027 from 75ý to 1K ±5%.

Change, the video input connector, 006 from a 6 conductor to a 7 conductor header.

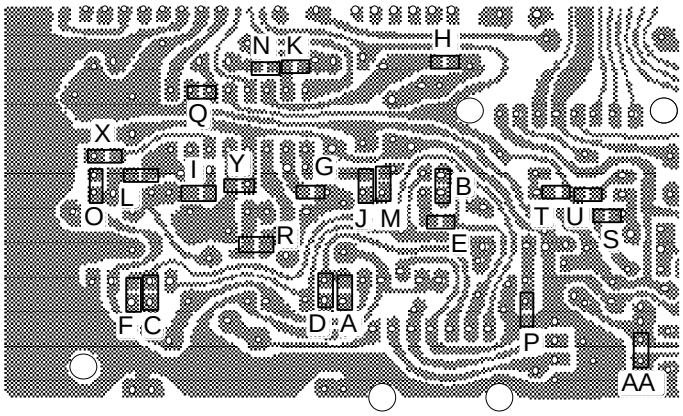
5 Solder Connections: A, B, C, P, & S



___ Solder Connections: _____

_____

_____



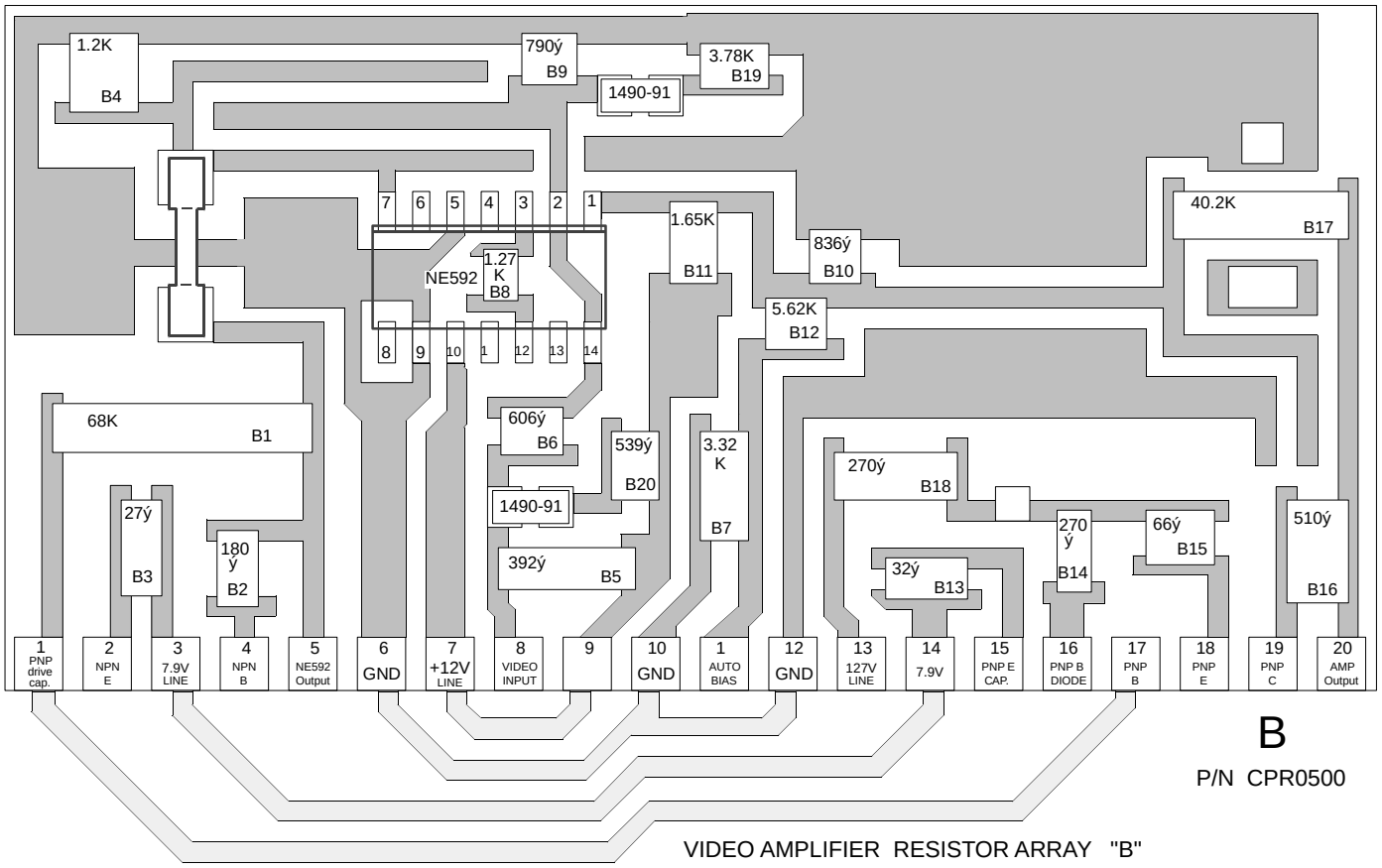
___ Solder Connections: _____

_____

_____

NOTE: Solder connections S, T, & U, and resistor 094 set the video gain and may change due to component variations.

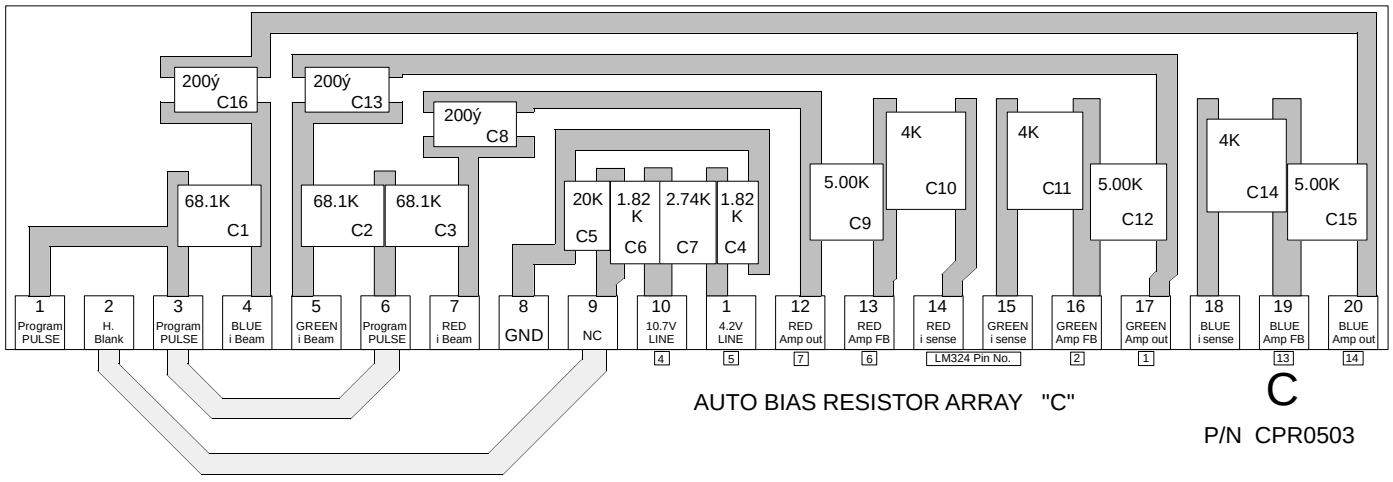
NOTES:



B

P/N CPR0500

VIDEO AMPLIFIER RESISTOR ARRAY "B"

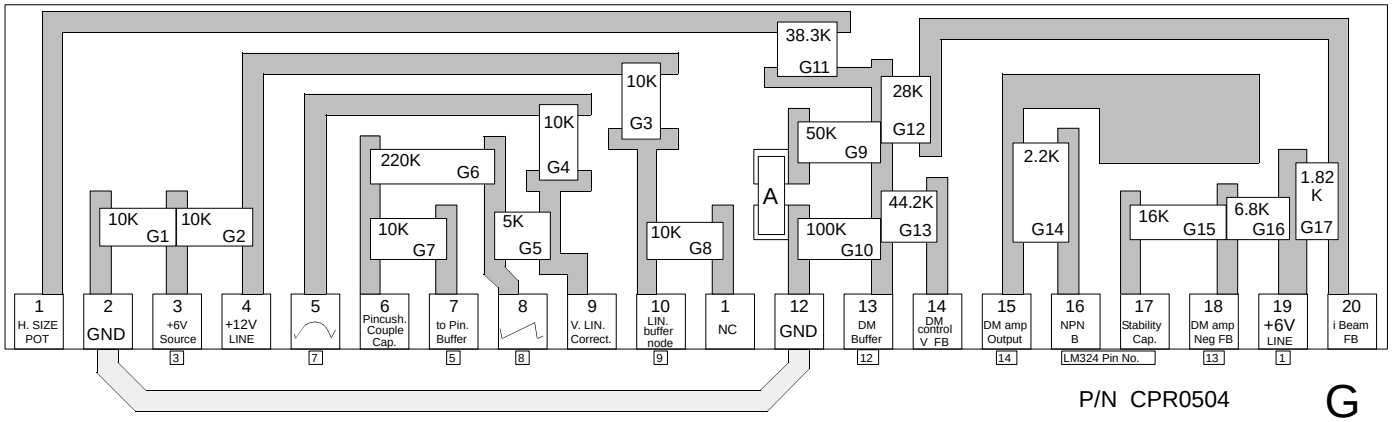


AUTO BIAS RESISTOR ARRAY "C"

C

P/N CPR0503

Solder connection A reduces the horizontal raster size.



P/N CPR0504

G

HORIZONTAL WIDTH CONTROL RESISTOR ARRAY "G"