

### 21<sup>st</sup> Century Computer Architecture

#### Mark D. Hill, Univ. of Wisconsin-Madison 6/2016 @ Architecture 2030 @ ISCA

- 1. Whitepaper Content (tell a story)
- Process, Impact & Computing Community Consortium (CCC)

A CCC community white paper

http://cra.org/ccc/docs/init/21stcenturyarchitecturewhitepaper.pdf

- Information & Commun. Tech's Impact
- Semiconductor Technology's Challenges
- Computer Architecture's Future
- Pre-Competitive Research Justified

# Was **21<sup>st</sup> Century Computer Architecture** NEW (even in 2012)??

# Our Task: Telling a "New" Story

- Was 21<sup>st</sup> Century Computer Architecture NEW?
  - **No**
  - Resulted in more \$50M in funding in USA

#### In Communication of the China Computer Federation (CCF)

#### 译文 中周計算我學會通訊 第8卷 第12期 2012年12月

#### 21世纪计算机体系结构 计算机体系结构共同体白皮书\*

关键词:计算机体系结构

译者:计算机体系结构国家重点实验室(筹)

#### 引言与概要

信息通信技术(information and communication technology, ICT)从医疗、教育、科技、商业、政 府、国防和娱乐等各个领域改变着我们的世界。如 今,人们已经差不多忘记了20年前人们找资料的第 一步是设法到达图书馆,10年前社交网络还主要指 持续地让单个芯片在功耗与成本几乎维持不变的情况下(Dennard scaling,丹纳德微缩)容纳了越来 越多的晶体管(摩尔定律)。而计算机体系结构发 明了各种创新技术来利用快速增长的晶体管资源, 扩展了处理器的性能,缓解了内存系统带来的性能 损失。在过去几十年,两者结合的效果让信息通信

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# Our Task: Telling a "New" Story

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  - **No**
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- Why?
  - New to **others**
  - Told a story that mattered to others
- Develop a New-to-Others Message as a Story
  - Why Important to Others?
  - Why Now?
  - How Might Research Make a Difference?
- This is our task now not developing ideas new to us

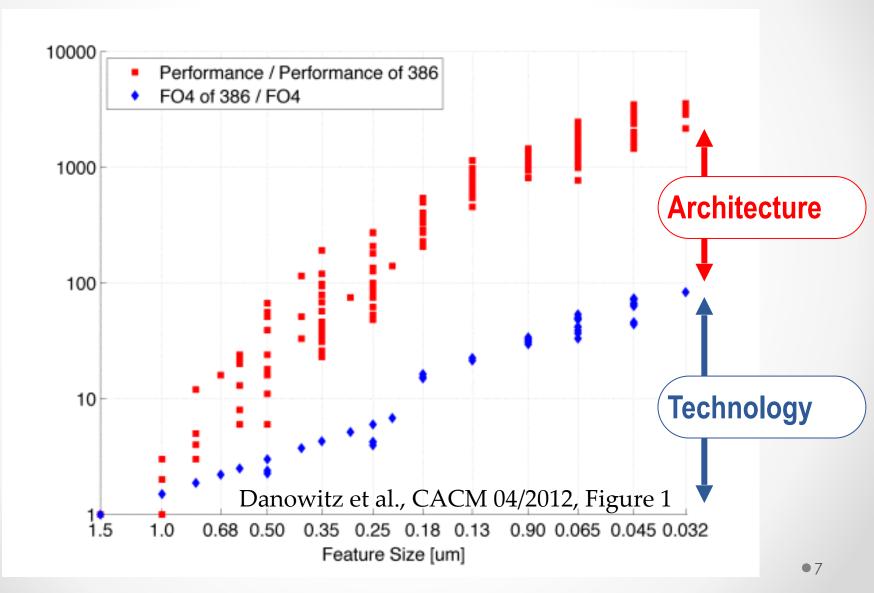
# 20<sup>th</sup> Century ICT Set Up

 Information & Communication Technology (ICT) Has Changed Our World

<long list omitted>

- Required innovations in algorithms, applications, programming languages, ..., & system software
- Key (invisible) enablers (cost-)performance gains
   Semiconductor technology ("Moore's Law")
   Computer architecture (~80x per Danowitz et al.)

#### Enablers: Technology + Architecture



### 21<sup>st</sup> Century ICT Promises More



#### Data-centric personalized health care



Human network analysis

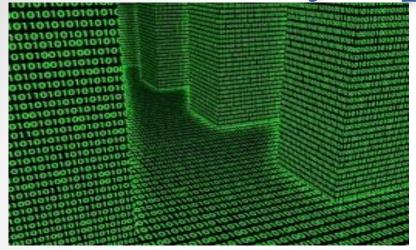


#### Computation-driven scientific discovery



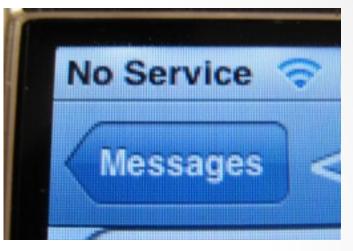
#### Much more: known & unknown

### 21<sup>st</sup> Century App Characteristics



**BIG DATA** 





#### **ALWAYS ONLINE**



# Whither enablers of future (cost-)performance gains? •?

# Technology's Challenges 1/2

Late 20 <sup>th</sup> Century	The New Reality	
Moore's Law — 2× transistors/chip	Transistor count still 2× BUT	
Dennard Scaling — ~constant power/chip	<b>Gone.</b> Can't repeatedly double power/chip	

# Technology's Challenges 2/2

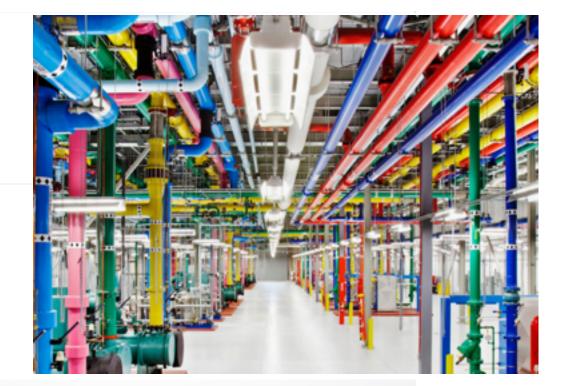
Late 20 <sup>th</sup> Century	The New Reality
Moore's Law — 2× transistors/chip	Transistor count still 2× BUT
Dennard Scaling — ~constant power/chip	<b>Gone.</b> Can't repeatedly double power/chip
Modest (hidden) transistor unreliability	Increasing transistor unreliability can't be hidden
Focus on computation over communication	<b>Communication (energy)</b> more expensive than computation
1-time costs amortized via mass market	<b>One-time cost</b> much worse & want <b>specialized</b> platforms

How should architects step up as technology falters?

# 20th Century21st CenturySingle-chip in<br/>generic<br/>computer

Performance via invisible instr.-level parallelism

Predictable technologies: CMOS, DRAM, & disks



#### 21<sup>st</sup> Century

Single-chip in generic computer

20<sup>th</sup> Century

Architecture as Infrastructure: Spanning sensors to clouds Performance + security, privacy, availability, programmability, ...

Performance via invisible instr.-level parallelism Predictable

technologies: CMOS, DRAM, & disks



#### 20<sup>th</sup> Century

Single-chip in generic computer

Performance via invisible instr.-level parallelism

Predictable technologies: CMOS, DRAM, & disks



#### 20<sup>th</sup> Century

#### 21<sup>st</sup> Century

Single-chip in generic computer

Performance via invisible instr.-level parallelism

Predictable technologies: CMOS, DRAM, & disks



### 21<sup>st</sup> Century Comp Architecture

20 <sup>th</sup> Century	21 <sup>st</sup> Century	
Single-chip in stand-alone computer	Architecture as Infrastructure: Spanning sensors to clouds Performance + security, privacy, availability, programmability,	Cross- Cutting:
Performance via invisible instrlevel parallelism	<ul> <li>Energy First</li> <li>Parallelism</li> <li>Specialization</li> <li>Cross-layer design</li> </ul>	Break current layers with
Predictable technologies: CMOS, DRAM, & disks	<b>New technologies</b> (non-volatile memory, near-threshold, 3D, photonics,) Rethink: memory & storage, reliability, communication	new interfaces

### What Research Exactly?

- Research areas in white paper (& backup slides)
  - 1. Architecture as Infrastructure: Spanning Sensors to Clouds
  - 2. Energy First
  - 3. Technology Impacts on Architecture
  - 4. Cross-Cutting Issues & Interfaces
- Much more research developed by future PIs!

### **Pre-Competitive Research Justified**

- Retain (cost-)performance enabler to ICT revolution
- Successful companies cannot do this by themselves
  - Lack needed long-term focus
  - Don't want to pay for what benefits all
  - Resist transcending interfaces that define their products

#### Corroborates

- Future of Computing Performance: Game Over or Next Level?, National Academy Press, 2011
- DARPA/ISAT Workshop Advancing Computer Systems without Technology Progress with outbrief http:// www.cs.wisc.edu/~markhill/papers/isat2012\_ACSWTP.pdf

#### "Timeline" from DARPA ISAT New Technology System Capability (log) Our Focus CMOS **Fallow Period** 80s 90s **00s** 10s 30s **40**s 20s **50s**

Source: Advancing Computer Systems without Technology Progress,

ISAT Outbrief (http://www.cs.wisc.edu/~markhill/papers/isat2012\_ACSWTP.pdf) Mark D. Hill and Christos Kozyrakis, DARPA/ISAT Workshop, March 26-27, 2012.

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The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.



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### White Paper Participants

Sarita Adve, U Illinois \* David H. Albonesi, Cornell U David Brooks, Harvard U Luis Ceze, U Washington \* Sandhya Dwarkadas, U Rochester Joel Emer, Intel/MIT Babak Falsafi, EPFL Antonio Gonzalez, Intel/UPC Mark D. Hill, U Wisconsin \*,\*\* Mary Jane Irwin, Penn State U \* David Kaeli, Northeastern U\* Stephen W. Keckler, NVIDIA/U Texas Christos Kozyrakis, Stanford U Alvin Lebeck, Duke U Milo Martin, U Pennsylvania

José F. Martínez, Cornell U Margaret Martonosi, Princeton U\* Kunle Olukotun, Stanford U Mark Oskin, U Washington Li-Shiuan Peh, M.I.T. Milos Prvulovic, Georgia Tech Steven K. Reinhardt, AMD Michael Schulte, AMD/U Wisconsin Simha Sethumadhavan, Columbia U Guri Sohi, U Wisconsin Daniel Sorin, Duke U Josep Torrellas, U Illinois \* Thomas F. Wenisch, U Michigan \* David Wood, U Wisconsin \* Katherine Yelick, UC Berkeley/LBNL \*

Thanks of CCC, Erwin Gianchandani & Ed Lazowska for guidance and Jim Larus & Jeannette Wing for feedback

# White Paper Process

- Late March 2012
  - CCC contacts coordinator & forms group
- April 2012
  - Brainstorm (meetings/online doc)
  - Read related docs (PCAST, NRC Game Over, ACAR1/2, ...)
  - Use online doc for intro & outline then parallel sections
  - Rotated authors to revise sections
- May 2012
  - Brainstorm list of researcher in/out of comp. architecture
  - Solicit researcher feedback/endorsement
  - Do distributed revision & redo of intro
  - Release May 25 to CCC & via email
- Later
  - CCC & NSF Outbriefs
  - HPCA/PPoPP/CGO/ICS Keynotes
  - ASPLOS & ISCA-Workshop Panels

### \$15M NSF XPS 2/2013

#### Exploiting Parallelism and Scalability (XPS)

#### PROGRAM SOLICITATION NSF 13-507



National Science Foundation

Directorate for Computer & Information Science & Engineering Division of Computing and Communication Foundations Division of Information & Intelligent Systems Division of Computer and Network Systems

Office of Cyberinfrastructure

Full Proposal Deadline(s) (due by 5 p.m. proposer's local time):

February 20, 2013

At the same time, a main driver of continued performance improvement is ending: semiconductor technology is facing fundemental placed with the second single processor performance has plateaued. Two

recent reports, "21<sup>st</sup> Century Computer Architecture" commissioned by the Computing Communey Consortium (http://cra.org/ccc/docs/init/21stcenturyarchitecturewhitepaper.pdf) and the 2011 NRC report on "The Future of Computing Performance: Game Over or Next Level?" (http://www.nap.edu /centing.cho2record\_id=12980) highlight this development and its impact on science, the economy and

society. The reports pose the question of new to enable the computational systems that will support emerging applications without the benefit of near-perfect performance scaling from hardware

improvements. NSF's Advanced Computing Infrastructure: Vision and Strategic Plan (http://www.nsf.gov /pubs/2012/nsf12051/nsf12051.pdf) published in February 2012 describes strategies that address this challenge for NSF and the research community. The XPS program is part of the larger NSF CIF21

#### + \$15M for 2/2014 + later years

#### Award Information

Anticipated Type of Award: Standard Grant or Continuing

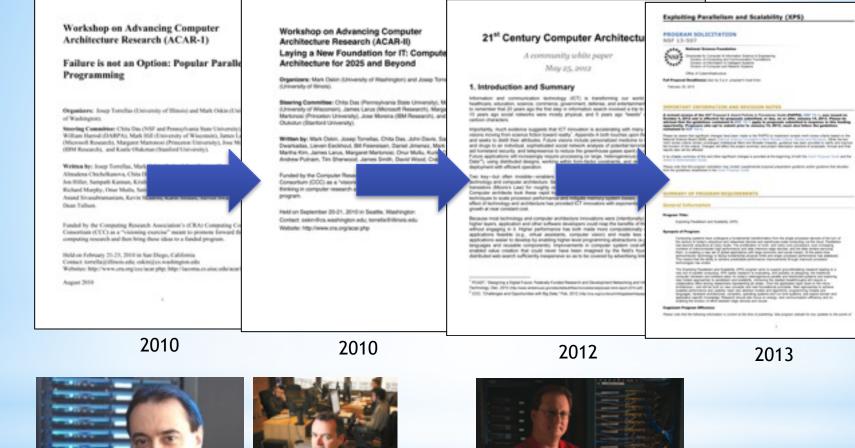
Estimated Number of Awards: 20

Approximately 20 awards of up to \$750,000 for periods up t availability of funde

Anticipated Funding Amount: \$15,000,000

\$15,000,000 is an acipated to be awarded, subject to availab

#### **Catalyzing and Enabling: Architecture**





Mark Hill

Wisconsin

Mark Oskin

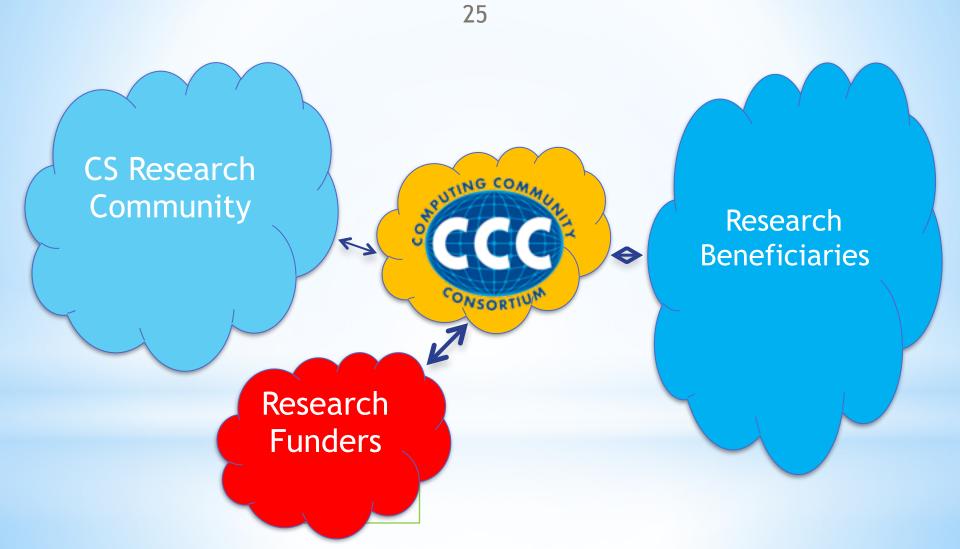
Washington

Josep Torrellas

UIUC



#### **Computing Community Consortium**





http://cra.org/ccc



#### CCC & You

#### 

- Chair Greg Hager  $\rightarrow$  Beth Mynatt
- ■Vice Chair Beth Mynatt → Mark Hill
- ~20 Council Members



- Standing committee of Computing Research Association
- CRA established via NSF cooperative agreement

#### You

- Be a rain-maker & give forward
- White papers
- Visioning
- And more





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