A 0.6-V 82-dB Delta-Sigma Audio ADC Using Switched-RC Integrators

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***Abstract*—A 0.6-V 2-2 cascaded audio delta-sigma ADC is described. It uses a resistor-based sampling technique which achieves high linearity and low-voltage operation without subjecting the devices to large terminal voltages. A low-distortion feed-forward topology combined with nonlinear local feedback results in enhanced linearity by reducing the sensitivity to opamp distortion, and allows increased input amplitude, resulting in higher SNDR. The modulator achieves 82-dB dynamic range and 81-dB peak SNDR in the A-weighted audio signal bandwidth with an OSR of 64. The total power consumption of the modulator is 1 mW from a 0.6-V supply. The prototype occupies 2.9 mm^2 using a 0.35-μm CMOS technology.**

***Index Terms*—Delta-sigma ADC, low voltage, switched-RC.**

I. Introduction

CMOS technology is continuously scaled down to achieve low-cost, high-density, low-power and high-speed digital systems. With the ever-increasing demand for portable devices used in applications such as wireless communication, mobile computing, consumer electronics, etc., the scaling down of the CMOS process to deep-submicron dimensions becomes even more important. However, this downscaling also requires similar shrinking of the supply voltage to insure device reliability [1]. The International Technology Roadmap for Semiconductors [2] predicts a maximum supply voltage equal to 0.8 V for 2007, and only 0.7 V for 2010 for state-of-the-art CMOS digital technology. This aggressive supply scaling requires low-voltage operation for the on-chip interface circuitry (analog-to-digital and digital-to-analog data converters) as well.

Low-voltage operation of ADCs poses three major challenges. First, the floating switches required in conventional switched-capacitor implementations are not operational for very low supply voltages. Since the threshold voltage is not proportionally scaled with supply voltage, the floating switch severely limits the signal range. Furthermore, excess gate overdrive voltage of the floating switch may violate the reliability constraints of the technology. This consideration prevents the use of voltage multiplication to drive these switches. Second, device noise due to both sampling switches and amplifiers poses a difficult design challenge at low supply voltage if high SNR must be achieved. Finally, amplifier distortion also limits the overall performance. In low-distortion applications, signals can be scaled down at the expense of lower signal power. However, with sub-1-V supply, the conflicting requirements of large signal swing and low distortion make a challenging design task. The main purpose of this work is to introduce low-voltage design techniques that enable high-performance analog circuit operation in deep-submicron processes. Architectural and circuit design techniques are presented for switched-RC circuits operating under very low supply voltage conditions. To demonstrate the proposed techniques, a wide-dynamic-range audio delta-sigma ADC with sub-1-V supply and low (1 mW) power consumption is designed. While the realization is demonstrated in a 0.35-μm CMOS technology, the key principles of the proposed techniques, which depend on the relative voltages of transistor threshold and supply, are directly migratable to finer linewidth submicron CMOS processes.

Section II describes the problems associated with floating switches in low-voltage switched-capacitor (SC) circuits, and the proposed solution using switched-RC branches. Section III discusses the architecture chosen for the audio ADC, and Section IV describes the details of the circuit implementation. The experimental results are shown in Section V. Finally, Section VI summarizes the conclusions drawn from the project.

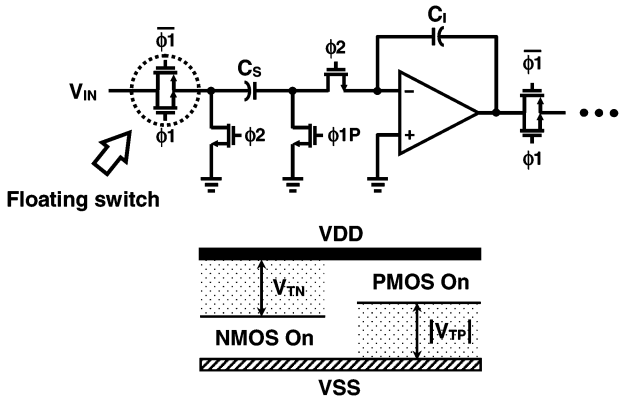

Fig. 1. Conventional switched-capacitor integrator with the floating switches.

II. Switched-RC Technique

The switched-capacitor (SC) technique provides an accurate and robust way of designing CMOS analog circuits. However, the realization of a low-voltage SC circuit becomes difficult, since

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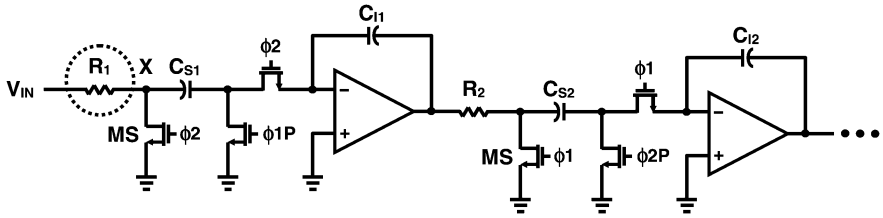

Fig. 2. Low-voltage integrator with switched-RC input branch.

the floating switches required in conventional SC circuits are not operational for very low supply voltages. Fig. 1 shows a typical SC integrator with its floating input and output switches. Limited gate voltage under low supply restricts the operating range of these switches. For example, the NMOS switches are "on" only when the input signal is lower than $V_{\rm DD}-V_{\rm TN}$. Similarly, the PMOS switches are "on" only when the input signal is higher than $|V_{\rm TP}|$. Both transistors turn off in the mid-input signal range. For proper operation, the gate overdrive voltage must be larger than the sum of the CMOS switch threshold voltages and the input signal amplitude. Thus, higher gate overdrive voltage has been used in previous low-voltage SC circuits, using global clock boosting or bootstrapping by voltage multiplication for the clock signals [1], [3], [4]. However, both techniques require extra circuitry and need careful design to avoid reliability problems. There are several circuit techniques which are fully compatible with low-voltage submicron CMOS processes, such as switched-opamps (SO) [5]–[9] and the opamp-reset switching technique (ORST) [10]–[12]. However, SO circuits face a tradeoff between speed and accuracy due to slow transients, while ORST stages have higher power consumption and settling issues due to unity gain feedback during the reset phase.

In this work, a different solution based on the switched-RC technique is proposed, and is applied to the design of an audio delta-sigma ADC. The basic concept is illustrated in Fig. 2. As shown, the input SC branch of the conventional structure is replaced by a switched-RC branch, in which the floating switch of the conventional integrator is replaced by a resistor R_1. This modification results in two advantages. First, it obviates the need for the floating switch, and second, the linearity of the input sampling is improved. The operation of this circuit is as follows. During the $\phi 1$ phase, the signal is sampled into the capacitor C_{S1} through resistor R_1. During the following $\phi 2$ phase, the signal charge is transferred to the integrating capacitor C_{I1} by connecting the bottom plate of C_{S1} to ground through switch MS. During this phase, the voltage V_X at node X is determined by the ratio of the ON resistance $R_{\rm ON}$ of the MS switch and the resistor R_1

$$V_X\left(n+\frac{1}{2}\right)=\frac{R_{\rm ON}}{R_1+R_{\rm ON}}V_{\rm IN}\left(n+\frac{1}{2}\right). \tag{1}$$

The output voltage of the integrator can be found from charge conservation as

$$V_{\rm OUT}\left(n+\frac{1}{2}\right)=V_{\rm OUT}(n)+\frac{C_{S1}}{C_{I1}}V_{\rm IN}(n) -\frac{C_{S1}}{C_{I1}}\frac{R_{\rm ON}}{R_1+R_{\rm ON}}V_{\rm IN}\left(n+\frac{1}{2}\right). \tag{2}$$

The gain error due to the ON resistance of switch MS is the last term in (2). For sufficiently high oversampling ratio (OSR), $V_{\rm IN}(n+(1/2))$ will be very close to $V_{\rm IN}(n)$, and the error can then be approximated by

$$\text{Gain Error}=\frac{C_{S1}}{C_{I1}}\frac{R_{\rm ON}}{R_1+R_{\rm ON}}. \tag{3}$$

Note that the gain error introduced by the nonideal ground at node X does not necessarily result in large distortion, as shown next. In (3), $R_{\rm ON}$ is the only nonlinear term, and hence the sole source of nonlinearity. Its value is given in (4), which shows that $R_{\rm ON}$ is a function of $V_{\rm DS}=V_X$:

$$R_{\rm ON}=\frac{1}{\mu_n C_{\rm OX}(W/L)\left[(V_{\rm GS}-|V_{\rm TH}|)-V_{\rm DS}\right]}. \tag{4}$$

Even though V_X changes with the input signal, the signal variation at node X is attenuated by the ratio of R_1 and $R_{\rm ON}$ [see (1)], and hence, the change in $R_{\rm ON}$ is small compared to that of a floating switch. Both the nonlinearity of the input sampling and the gain error can be reduced by making the linear resistor R_1 much larger than the variable ON resistance of the reset switch MS. However, there is a tradeoff. Larger R_1 results in improved gain accuracy and lower distortion during the $\phi 2$ phase, but during the $\phi 1$ phase, a large R_1C_{S1} time constant degrades the sampling accuracy. Thus, R_1 should be small enough to satisfy the settling requirement during the sampling phase.

The gain of the opamp in a switched-RC (SRC) integrator changes significantly between the phases. During the $\phi 1$ phase, the amplifier drives the resistive load R_2, which results in a low DC gain due to the low load impedance. However, during this reset phase, the charge stored in C_{I1} will be preserved, and the output voltage of the integrator will be recovered in the following $\phi 2$ phase, when the gain of amplifier returns to its high value as its resistive load is removed. The virtual ground voltage therefore also returns to its low value needed for the charge transfer. Hence, the effective DC gain of the amplifier in an SRC integrator can be the same as in a conventional SC one. Note also that the voltage between any two nodes is always less than the supply voltage, and therefore this technique is free from device reliability problems.

As illustrated in Fig. 2, the phasing of the clock signals in adjacent SRC integrators must be shifted. Thus, there is a $T/2$ delay between the input and the output of the integrator, where $T=1/f_{\rm clk}$ is the clock period.

III. Modulator Architecture

As discussed in Section I, there are three main problems in low-voltage analog IC design. A circuit solution is proposed in

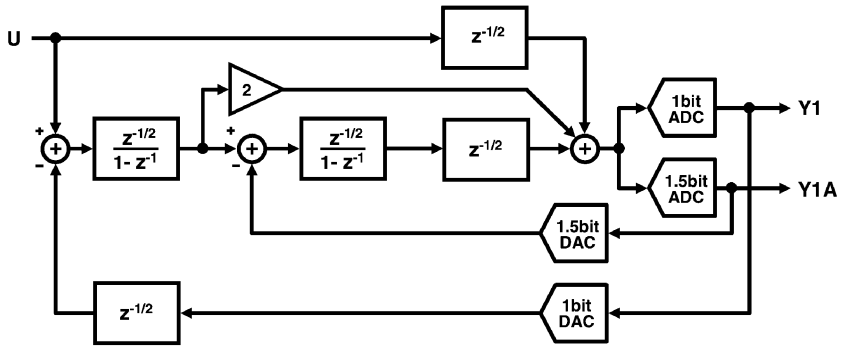

Fig. 3. Low-distortion feed-forward second-order delta-sigma modulator with local feedback.

Section II for the problem associated with floating switches. For the other two problems—distortion and noise—architectural solutions can be found. These are discussed in this section, in the context of an audio ADC.

For the targeted performance (13–14 ENOBs) and relatively narrow bandwidth, delta-sigma ADC converters seem to be optimal. The achievable SNR with such converters improves with increased order, higher resolution internal quantizer, and higher OSR. Internal resolution higher than 1 bit requires digital correction or filtering of the nonlinearity of the internal DAC, which increases the complexity and power dissipation. Choosing a single-bit internal quantization, and using the Schreier Toolbox in MATLAB [13], it was found that a fourth-order modulator combined with a relatively low oversampling ratio $(\text{OSR} = 64)$ is adequate to meet the required performance.

A 2-2 MASH architecture is selected, as it allows a larger input signal for stable operation than a single fourth-order loop. This structure consists of two stages, each containing a second-order delta-sigma modulator. The first stage converts the input signal into one bit stream with filtered quantization noise Q1, while the second stage converts only Q1, and adds its own filtered quantization noise Q2.

The configuration chosen for both stages of the MASH is the low-distortion feed-forward topology proposed in [14]. In this architecture, under ideal conditions, the loop filter processes only the shaped quantization noise and so there is no distortion introduced by the integrator. Hence, the linearity requirements on the opamps are relaxed. This is an important advantage for low-voltage operation with nonlinear amplifiers.

In the proposed modulator topology, this feed-forward architecture is implemented with half delay integrators. Since the integrators used the SRC circuits introduced in Section II, they provide a $T/2$ delay between stages, as opposed to the usual T or 0 delay. This necessitates the inclusion of additional $T/2$ delays ($z^{-1/2}$ blocks) in the architecture, to insure synchronized charge transfer [6]. These delays are implemented in the SRC input branches of the comparators and in the digital feedback, and do not require extra amplifiers. Though additional $T/2$ delays are used for the synchronization, this proposed modulator topology with half delay integrator allows signal transfer from input to the integrator. This results in a first-order shaped signal transfer function through the integrators. This shaping can be ignored if the OSR is high enough. Inaccurate matching of gain coefficients of the modulator due to nonideal parameters also causes residual input signal component in the loop filter. These signal terms propagating through the integrator path will cause distortion and limit the linearity of the system.

For further linearity enhancement with large input signal, the nonlinear local feedback arrangement proposed by Fujimori *et al.* [15], containing a 1.5-bit quantizer, is used. The local feedback continuously monitors the integrator output and restricts the signal swing range by feeding back a quantized error signal to the input of the second integrator. The second-stage overloading can be prevented by choosing proper decision levels of the 1.5-bit local feedback quantizer. Since the second stage is not overloaded, the distortion caused from saturated integrator output of the first stage can be cancelled out by cascaded second stage output with digital noise cancellation logic. The quantization noise of the local feedback can be subtracted by digital noise cancellation logic similar to the 1-bit quantization error. The local feedback is not activated if the input signal of quantizer is between the decision levels of the two comparators used in the 1.5-bit internal quantizer. Note that the 1.5-bit DAC used in the local feedback loop has relaxed linearity requirements, since the nonlinear error at the input of the second integrator is shaped by the loop. The resulting block diagram of the second-order stage is shown in Fig. 3. The combination of these two linearity enhancement techniques of the delta-sigma architecture improves both the distortion and noise immunity of the converter.

Fig. 4(a) illustrates the overall block diagram of the MASH ADC. Due to the low-distortion configuration used, the second integrator output of the first stage (V_1) can be directly connected to the second stage without using any additional subtraction. The coefficients of all integrators and feed-forward paths were found so as to maximize the input signal range without overloading the amplifiers. Fig. 4(b) shows the block diagram of the digital noise cancellation logic. It is implemented off-chip, using post-processing in MATLAB.

The overall output signal of the ADC is given by

$$Y = z^{-3/2}(3 - 3z^{-1} + z^{-2})U + 15(1 - z^{-1})^4 Q_2. \quad (5)$$

Note that the signal transfer function, in addition to a delay, has a small gain variation which is negligible in the signal band.

Behavioral simulations performed by modeling amplifiers with 50-dB DC gain, 50-dB SFDR, and 0.4% capacitor

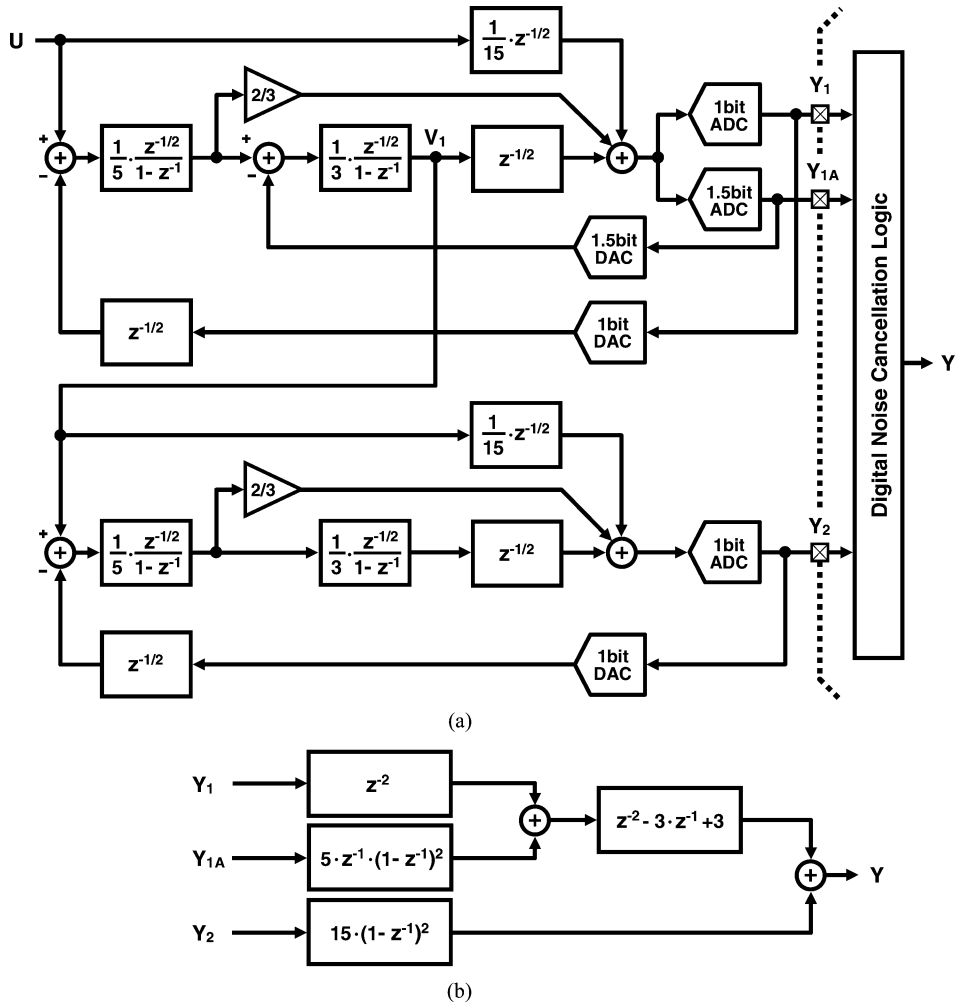

Fig. 4. (a) Block diagram of two-stage cascaded delta-sigma modulator. (b) Digital noise cancellation logic.

matching indicate higher than 100-dB SFDR of the complete converter. More than 1.5-dB improvement in the permissible peak input signal due to local feedback is also observed in these simulations.

IV. Circuit Implementation

While the principle of the SRC circuit has been described in Section II, its actual implementation in our ADC is somewhat different, since the input branches are also used for common-mode adjustments and feedback. The implemented circuits will be discussed next.

A. Split Switched-RC Input Branch

In a low-voltage integrator, it is desirable to set the common-mode (CM) level of the input and output at the middle of the supply voltage, i.e., $V_{\rm CM} = (V_{\rm DD} + V_{\rm SS})/2$, to maximize signal swing. At the same time, any DC bias voltage connected to the sampling capacitors must be close to $V_{\rm DD}$ or $V_{\rm SS}$ in order to avoid any floating switching problem. For this reason, two different input common-mode levels were applied to the integrator during the sampling and the integrating phases. Such use of two different input CM voltages resulted in a large amount

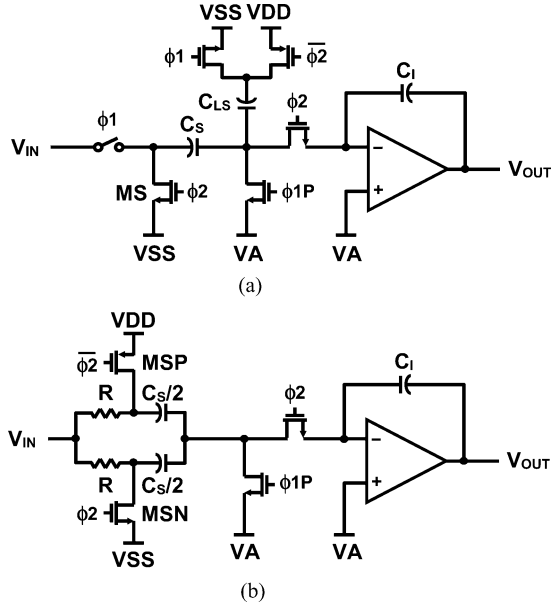

Fig. 5. (a) Traditional low-voltage switched-capacitor integrator. (b) Low-voltage integrator with split switched-RC technique.

of common-mode charge injection. Thus, the input or inter-stage branches of all integrators should also perform a level

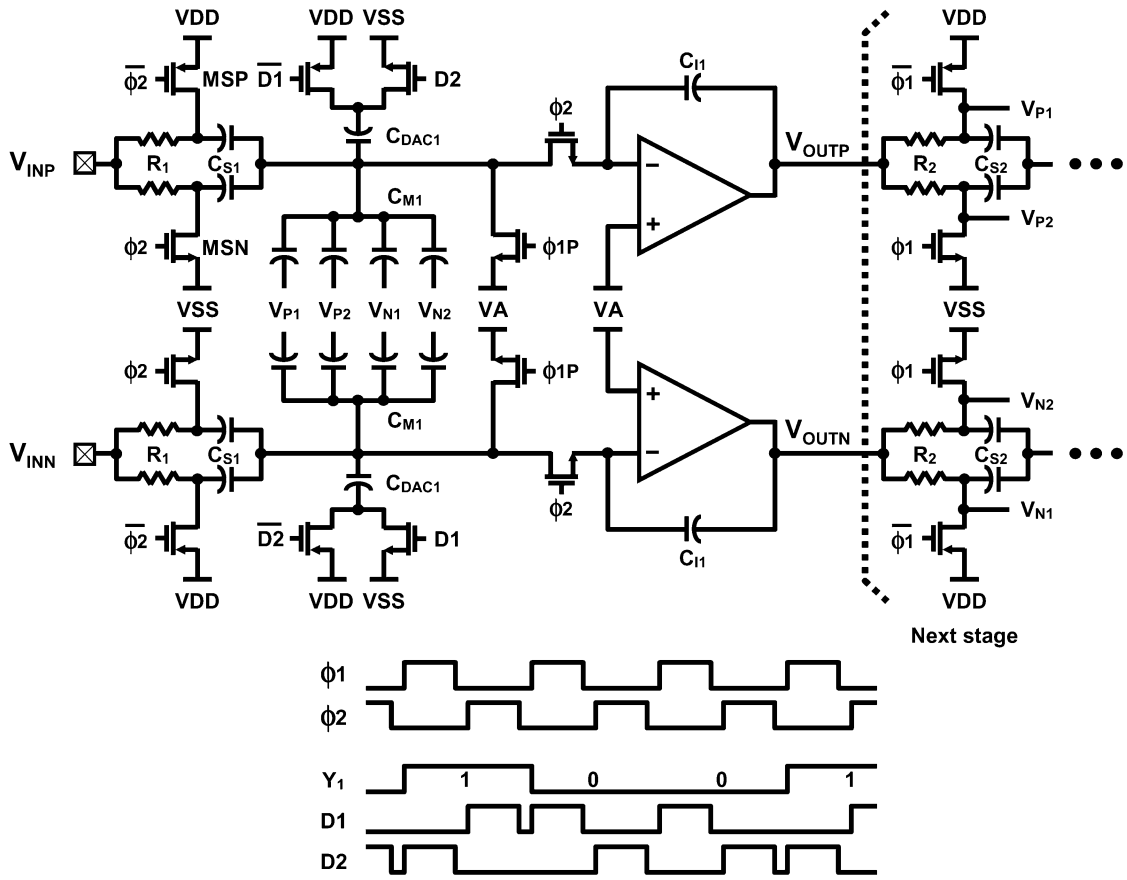

Fig. 6. Schematic of pseudo-differential low-voltage integrator with switched-RC technique.

shifting operation, in addition to sampling and transfer/amplification of the input signal. Fig. 5(a) shows an earlier implementation of this level shifting in a low-voltage SC integrator [7]. A level-shifting capacitor $C_{\rm LS}$ is used to cancel the common-mode charge injection, by providing an opposite polarity charge. However, this added SC branch adds more kT/C noise and also increases the opamp noise gain.

In our implementation, a split input switched-RC branch is used to keep constant CM level of the integrator, as shown in Fig. 5(b). During the integrating phase, one half of the sampling capacitor is connected to $V_{\rm DD}$, while the other half is connected to $V_{\rm SS}$. This results in a constant input common-mode level of $V_{\rm DD}/2$ for the integrator during both phases, obviating the need for an additional level-shifting capacitor without any noise penalty.

B. Pseudo-Differential Integrator Using Switched-RC Technique

Fig. 6 shows the complete schematic of a pseudo-differential integrator using the switched-RC technique, and an example timing diagram. Split switched-RC input branches are used to maintain a constant input common-mode voltage. The effective DAC reference voltage is doubled by alternating the connection of the DAC capacitors $C_{\rm DAC1}$ from $V_{\rm DD}$ to $V_{\rm SS}$ or *vice versa*, depending on the comparator's output. This helps to reduce the size of $C_{\rm DAC1}$ resulting in lower noise. This is because the input-referred kT/C noise due to $C_{\rm DAC1}$ is scaled by ${C_{S1}}^2$, and the opamp noise will be amplified by the ratio of C_{S1} and the total capacitance connected to the virtual ground node.

A pseudo-differential architecture is used to circumvent challenging design issues associated with low-voltage common-mode feedback circuit design. Capacitors C_{M1}s, connected to the switched-RC branches of the next stage, are used for the common-mode feedback. The basic operation of the switched-RC common-mode feedback is similar to that proposed for pseudo-differential circuits earlier in [16], except for the use of switched-RC branches. Fig. 7 shows the operation during two different phases of common-mode feedback loop formed with the following stage switched-RC branches. During $\phi 1$, the desired output common-mode reference $V_{\rm CM}$ is sampled onto capacitors C_{M1} by connecting half of them to $V_{\rm DD}$ and the other half to $V_{\rm SS}$. During the following $\phi 2$ phase, the difference between $V_{\rm CM}$ and the actual output common-mode voltage is fed to all opamp inputs, and integrated in both pseudo-differential paths. This forces the output CM of all opamps to $V_{\rm CM}$.

Fig. 8 shows the complete schematic of the first-stage modulator, implemented in a pseudo-differential architecture. To insure less than $-$85-dB kT/C noise level, a total of 4.8-pF input sampling capacitance is used and 8-kΩ R_1 is used to guarantee linear input signal sampling. The 1.5-bit DAC needed for local feedback uses two capacitors $C_{\rm DAC2}$ to double the effective DAC reference voltage, each one acting as a 1-bit delay-free DAC. During the $\phi 2$ phase, each capacitor is charged to $V_{\rm DD}$ or $V_{\rm SS}$. During the following $\phi 1$ phase, depending on the output (-1, 0, or 1) of the 1.5-bit local feedback quantizer, the voltage at the bottom plate of the $C_{\rm DAC2}$ capacitors will be changed. If output is "-1", then the capacitor earlier connected to $V_{\rm DD}$ will

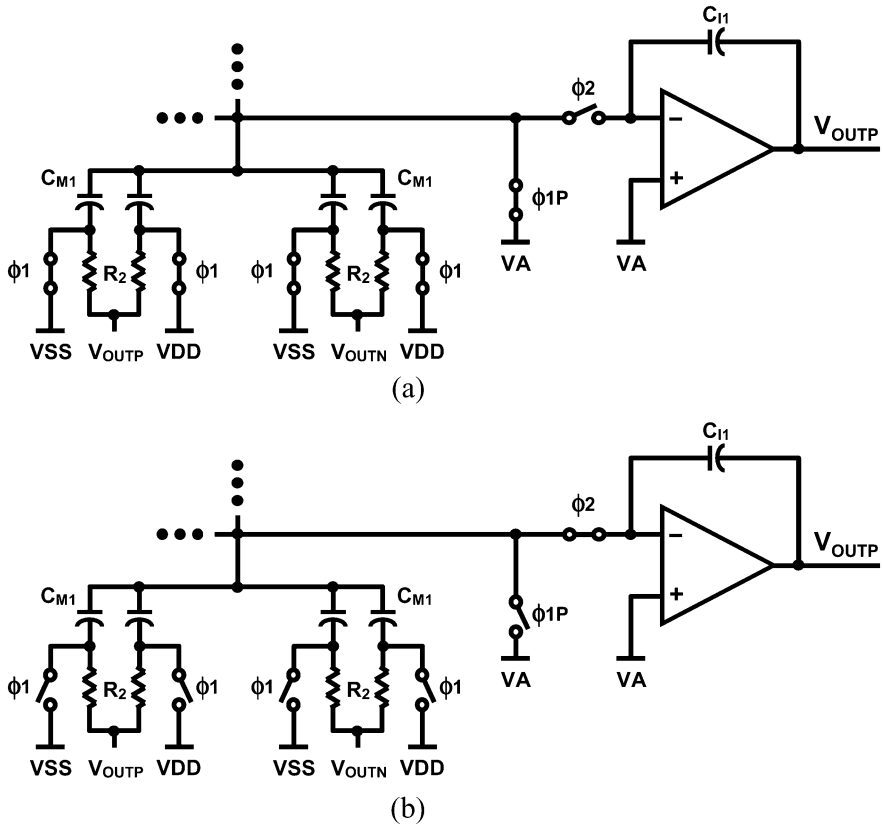

Fig. 7. Common-mode feedback with switched-RC technique. (a) $\phi 1$ phase. (b) $\phi 2$ phase.

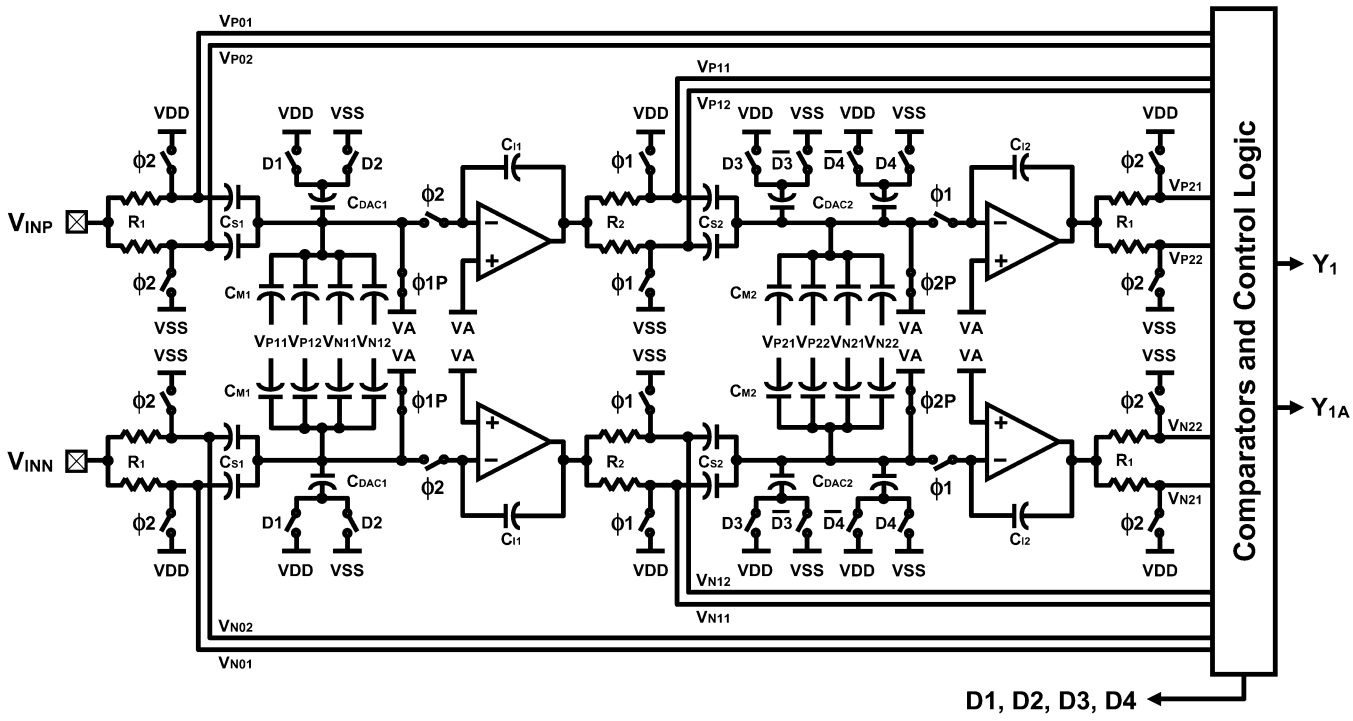

Fig. 8. First-stage delta-sigma modulator.

be reconnected to $V_{\rm SS}$. If it is "1", then the capacitor connected to $V_{\rm SS}$ will be switched to $V_{\rm DD}$. However, if the quantizer output is "0", then the connection of the $C_{\rm DAC2}$ capacitors will not be changed.

The gain coefficients of the feed-forward paths from the ADC input and from the output nodes of each integrator to the quantizer input are realized simply by scaling the capacitors in the comparators, as shown in Fig. 9. The switched-RC

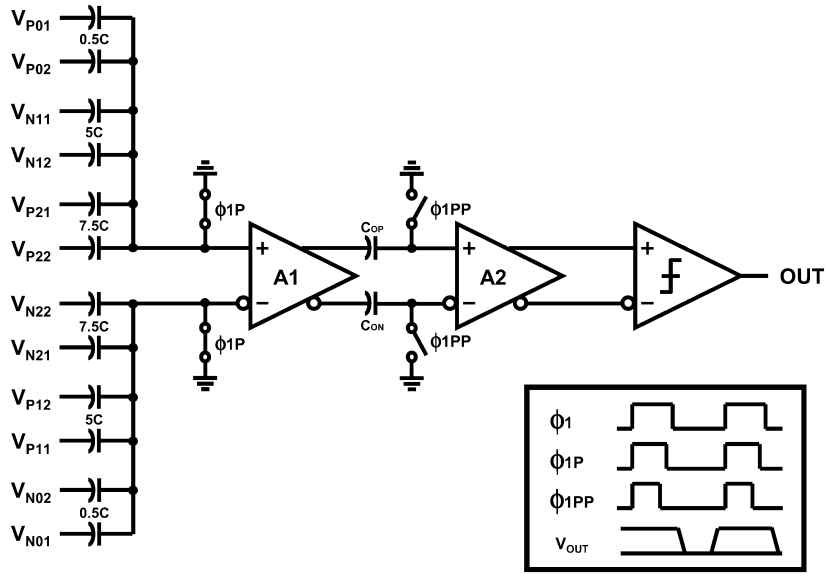

Fig. 9. Schematic of the comparator.

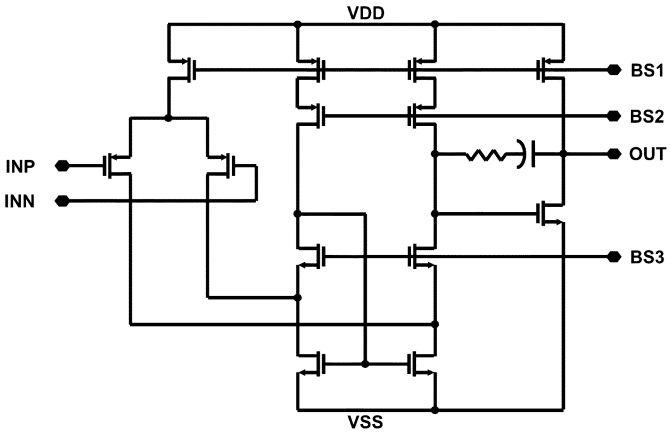

Fig. 10. Schematic of the amplifier.

output branches of the integrators are shared with the comparators' input sampling branches. Because of this, the input common-mode level of the comparators is also kept constant, together with the output CM level of the integrators.

Using a low-offset comparator is important to achieve a large signal range in low-voltage delta-sigma modulator design. Depending on the comparator offset, the center of the integrator output histogram can move out from the middle of the supply voltage range, resulting in overloading. The offset cancellation of the comparators is performed at the output of amplifier $A1$, while amplifier $A2$ is used as a preamplifier, to suppress the kickback from the latch. The output voltages V_{P21}, V_{P22}, V_{N21}, and V_{N22} of the second integrator drive the second stage of the MASH directly.

C. Amplifier Circuitry

To achieve high gain and large output swing, internally compensated two-stage amplifiers are used. Their circuit diagram is shown in Fig. 10. The amplifiers contain a folded-cascode first stage and a common-source second stage. The simulation

TABLE I
SIMULATED PERFORMANCE OF THE AMPLIFIER

Power supply voltage	0.6 V
DC gain	60 dB
Unity gain frequency	10 MHz
Phase margin	65 °
Slew rate	10 V/μs

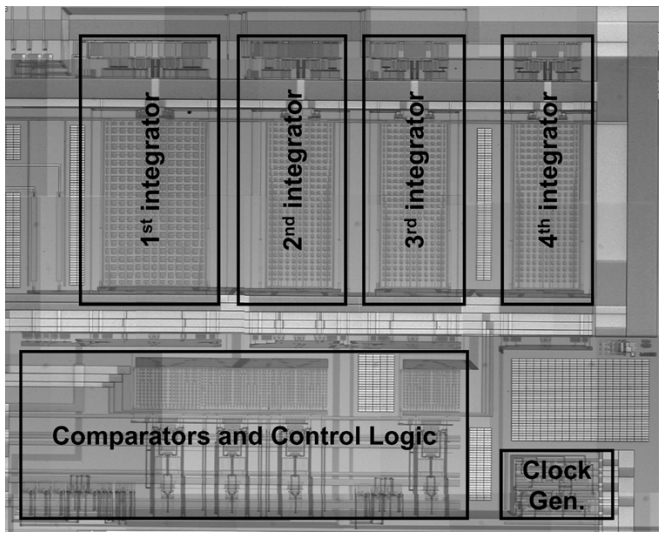

Fig. 11. Die photograph.

result shows more than 60-dB SFDR with full-scale output swing (0.8-Vpp fully differential) under 0.6-V supply voltage. Though this amplifier provides relatively modest linearity under low-supply voltage operation, its nonlinearity error is reduced by the architectural features of the modulator, as explained in Section III. The main performance parameters of the opamp are given in Table I.

TABLE II
PERFORMANCE SUMMARY

Power supply voltage	0.6 V
Signal bandwidth	24 kHz
Clock frequency	3.072 MHz
Oversampling ratio	64
Total power consumption	1 mW (including digital and I/O)
Input range	0.8 Vpp (differential)
Peak SNR	77 dB @ BW = 24 kHz 78 dB @ BW = 20 kHz 81 dB @ BW = 20 kHz, A-weighted
Peak SNDR	77 dB @ BW = 24 kHz 78 dB @ BW = 20 kHz 81 dB @ BW = 20 kHz, A-weighted
Dynamic range	78 dB @ BW = 24 kHz 79 dB @ BW = 20 kHz 82 dB @ BW = 20 kHz, A-weighted
Active die area	1.8 X 1.6 mm^2
Technology	0.35 μm CMOS (V_{TN}=0.34 V, V_{TP}=-0.31 V)

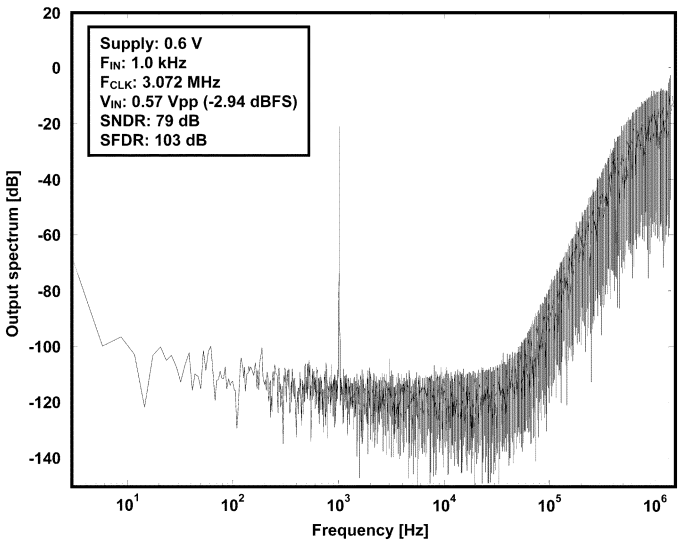

Fig. 12. Measured output spectrum.

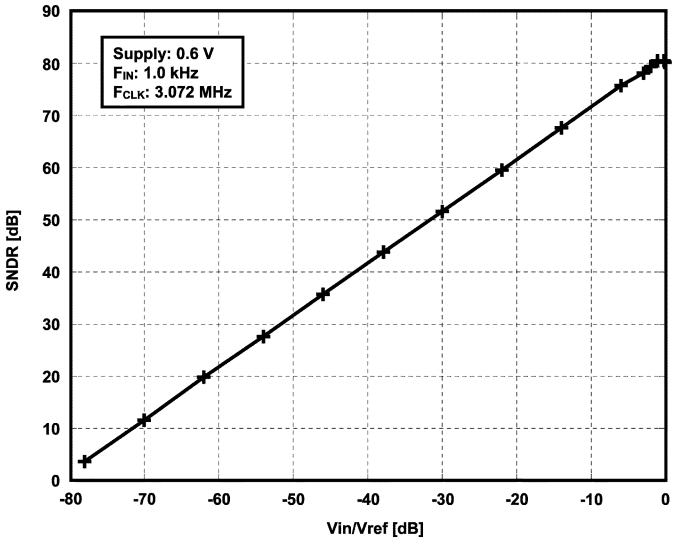

Fig. 13. Measured SNDR.

V. EXPERIMENTAL RESULTS

The prototype ADC was fabricated in a 0.35-μm CMOS technology, with double-poly and triple-metal layers. Fig. 11 shows the die photograph of the prototype IC. The core area, excluding bonding pads, is 1.8×1.6 mm^2. Fig. 12 shows the measured power spectrum of the output for a 1-kHz 0.57-V peak-to-peak differential input sine wave, with a 0.6-V power supply. 79-dB SNDR and 103-dB SFDR is achieved over the audio band, largely due to the proposed switched-RC technique and the low-distortion loop. The SNDR versus input amplitude curve is illustrated in Fig. 13. This result indicates linear operation, up to a -1-dBFS input level. The measured performance is summarized in Table II. In the A-weighted audio band, the prototype achieves 81-dB peak SNDR and 82-dB dynamic range with a 0.6-V supply voltage and 1-mW power consumption. A 3.072-MHz clock frequency is used, resulting in an OSR of 64. Fig. 14 shows the SFDR and SNDR versus power-supply voltage curves (signal reference/swing fixed). The performance is unaffected by the variation of the supply voltage from 0.6 to 1.8 V.

VI. CONCLUSION

Design techniques are proposed for low-voltage analog CMOS integrated circuits. They do not affect the reliability of fine-linewidth devices by overstressing their gate oxides. Using the proposed techniques, a 2-2 MASH delta-sigma audio ADC operating with a 0.6-V supply is designed and implemented. In the device, linear and large input signal sampling is achieved with switched-RC technique. The overall linearity of the modulator is improved by applying a low-distortion feed-forward

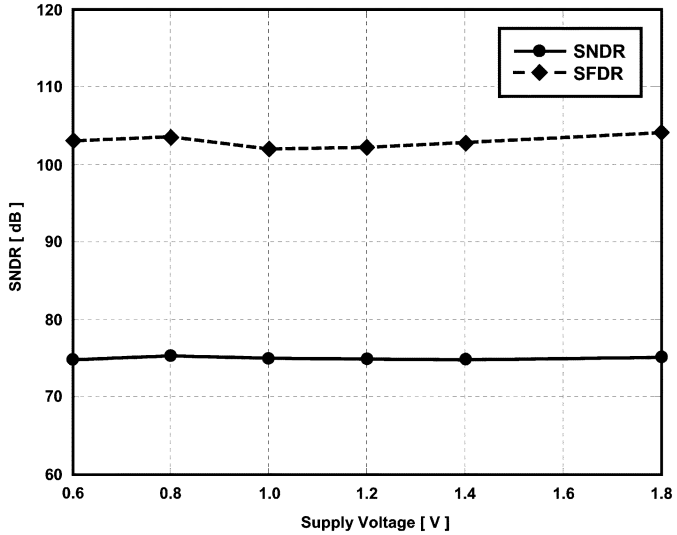

Fig. 14. SNDR and SFDR versus supply voltage.

topology, while the peak SNDR is enhanced by increasing the input signal range using quantized local feedback. The measured results of prototype IC fabricated in a 0.35-μm CMOS technology verify the validity of the proposed design techniques for low-voltage and high-performance operation.

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REFERENCES

[1] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[2] International Technology Roadmap for Semiconductors, Semiconductor Industry Association (2004). [Online]. Available: http://public.itrs.net/

[3] Y. Nakagome *et al.*, "A 1.5 V circuit technology for 64 Mb DRAMs," in *Dig. Symp. VLSI Circuits*, Jun. 1990, pp. 17–18.

[4] T. Cho and P. Gray, "A 10 b 20 Msamples/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[5] J. Crols and M. Steyaert, "Switched opamp: An approach to realize full CMOS SC circuits at very low supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.

[6] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900-mV low-power $\Delta\Sigma$ A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.

[7] A. Baschirotto and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1979–1986, Dec. 1997.

[8] M. Waltari and K. Halonen, "1-V 9-bit pipelined switched-opamp," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 129–134, Jan. 2001.

[9] B. Vaz, J. Goes, and N. Paulino, "A 1.5-V 10-b 50 MS/s time-interleaved switched-opamp pipeline CMOS ADC with high energy efficiency," in *Dig. Symp. VLSI Circuits*, Jun. 2004, pp. 432–435.

[10] M. Keskin, U. Moon, and G. Temes, "A 1-V 10-MHz clock-rate 13-bit CMOS $\Delta\Sigma$ modulator using unity-gain-reset opamps," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 817–823, Jul. 2002.

[11] D. Chang, G. Ahn, and U. Moon, "A 0.9 V 9 mW 1 MSPS digitally calibrated ADC with 75 dB SFDR," in *Dig. Symp. VLSI Circuits*, Jun. 2003, pp. 67–70.

[12] D. Chang and U. Moon, "A 1.4-V 10-bit 25 MSPS pipelined ADC using opamp-reset switching technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1401–1404, Aug. 2003.

[13] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*. New York: Wiley/IEEE Press, 2004.

[14] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737–738, Jun. 2001.

[15] I. Fujimori, K. Koyama, D. Trager, F. Tam, and L. Longo, "A 5 V single-chip delta-sigma audio A/D converter with 111 dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 329–336, Mar. 1997.

[16] L. Wu, M. Keskin, U. Moon, and G. Temes, "Efficient common-mode feedback circuits for pseudo-differential switched-capacitor stages," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. V, May 2000, pp. 445–448.

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