Full-Wave Simulation of an Electrostatic Discharge Generator Discharging in Air-Discharge Mode Into a Product

Dazhao Liu, Argha Nandy, Fan Zhou, Wei Huang, Jiang Xiao, Byongsu Seol, Jongsung Lee, Jun Fan, *Senior Member, IEEE*, and David Pommerenke, *Senior Member, IEEE*

Abstract—This paper introduces a methodology to simulate the currents and fields during an air discharge electrostatic discharge (ESD) into a product by combining a linear description of the behavior of the DUT with a nonlinear arc resistance equation. The most commonly used test standard IEC 61000–4-2 requires using contact-mode discharges to metallic surfaces and air-discharge mode to nonconducting surfaces. In the contact mode, an ESD generator is a linear system. In the air-discharge mode, a highly nonlinear arc is a part of the current loop. This paper proposes a method that combines the linear ESD generator full-wave model and the nonlinear arc model to simulate currents and fields in air-discharge mode. Measurements are presented comparing discharge currents and fields for two cases: ESD generator discharges into a ground plane, and ESD generator discharges into a small product.

Index Terms—Air-discharge mode, cosimulation, electrostatic discharge (ESD) generator, full-wave modeling.

I. INTRODUCTION

S IMULATING electrostatic discharge (ESD) allows predicting the currents and fields seen within a device under test (DUT) during an ESD, thus it helps to predict failure levels [1], [2]. The most commonly used test standard IEC 61000–4-2 [3] requires using contact-mode discharges to metallic surfaces and air-discharge mode to nonconducting surfaces. If an air discharge is attempted to a nonconducting surface, a discharge to a conducting part can occur.

In contact mode, the output waveform is proportional to the charge voltage, thus, the ESD generator can be analyzed as a linear system in both time domain (TD) and frequency domain (FD) [4]. Those models [5]–[8] for contact mode differ in the software used, the upper frequency limits, and if a specific commercial model of an ESD generator is simulated. However, the numerical modeling of an air discharge is more complex due to the highly nonlinear behavior of the arc [9]–[14]. The generator

Manuscript received September 6, 2009; revised February 3, 2010; accepted September 10, 2010. Date of publication November 18, 2010; date of current version February 16, 2011.

D. Liu, A. Nandy, F. Zhou, W. Huang, J. Xiao, J. Fan, and D. Pommerenke are with the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO 65401 USA (e-mail: dlhbf@mst.edu; and23@mst.edu; fzm73@mst.edu; wh57f@mst.edu; xiaoj@mst.edu; jfan@mst.edu; davidjp@mst.edu).

B. Seol and J. Lee are with the Samsung Electronics, Suwon 442-742, Korea (e-mail: byongsu.seol@samsung.com; js7582.lee@samsung.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TEMC.2010.2087025

needs to be separated into the linear sections comprising the metallic elements, resistors, capacitors, and the nonlinear arc. It has been shown that the arc can be modeled as a time-varying resistor valid for the first tens of nanoseconds [13]. This model needs to be integrated into the numerical model.

Air-discharge currents badly repeat. Even if the voltage and speed of approach are kept the same, ESD currents will vary strongly from discharge to discharge. The variations are due to different arc lengths and not a direct result of corona or speed of approach [13]. In [12], a method to combine the arc model from Rompe and Weizel with an equivalent circuit of the discharging object is shown. This methodology is expanded in this paper to combine a linear full-wave model of the ESD generator and the DUT with a nonlinear arc model. Currents and fields are obtained.

Section II introduces the methodology. Sections III and IV verify the methodology by comparison to measured data. Section V discusses the application and the limitations of this method.

II. METHODOLOGY

In general, different processes are possible for coupling SPICE to a full-wave solver: Simultaneous solution exchanges voltage and current information with a SPICE-like solver after every time step of the full-wave solution [15], [16]. Sequential solutions first calculate the S-parameters of the linear section of the circuit and then combine them with the nonlinear part of the circuit in SPICE. We use the second method. It allows reusing the S-parameters to save calculation time, if only the arc parameters are changed.

More in detail, a four-step process is used, which simulates linear parts in full wave and nonlinear in SPICE. The arc attaches at two points: at the ESD generator tip and at the DUT. These two points are used to define a port. In the first step, the impedance at this port is calculated. This is the impedance looking into the DUT and a Noiseken ESD generator (ESS-2000). The simulation is performed using computer simulation technology (CST) [17]. Both the TD and FD solver can be used. Although the impedance Z_{11} is calculated in the full-wave model for a given distance (0.7 mm) between the ESD generator and the DUT, different distances will influence the result little as long as the distance is in the arc length range (0.3–3.0 mm). The tip to ground capacitance is small relative to the distributed capacitance of the rod. This impedance is transformed into a form suitable for TD simulation. Here, the commercial software

TABLE I				
FOUR-STEP PROCESS FOR SIMULATING AIR DISCHARGE				

Steps	Method			
1	Obtain Z11 from the two points at which the arc attaches			
	(looking into ESD generator and the DUT) using a full wave			
	model. The DUT's inner details are not of concern in this			
	step, as one only needs to know the impedance seen by the			
h	Spark. Obtain a time domain simulation suitable description of 711			
2	The IDEM (Identification of Electrical Magnemodels) tool			
	The IDEM (Identification of Electrical Macromodels) tool			
	[20] and Broadband SPICE [21] have been utilized.			
3	Combine the equivalent sub-circuit with the arc length model			
	in SPICE to simulate the time domain discharge current			
	waveform.			
4	Re-import the discharge current waveform [I(t)] back into the			
	full wave model as a port excitation signal and simulate V(t)			
	(for verification against the V(t) obtained from SPICE), E-			
	field(t), and H-field(t) in the full wave simulation. In this step			

a much more detailed model of the DUT can be used.



Fig. 1. Definition of the port used for the Z_{11} calculation.

Broadband SPICE [21] was used. An order of 28 was selected to generate the circuit. SPICE then combines the impedance description from step 1 with an arc model based on the law of Rompe and Weizel. This law describes the arc during the first tens of nanoseconds as a resistance and has been validated for ESD applications [18], [19]. The resulting current is reimported into CST as the excitation waveform of the current port, which is placed between the two points that had been previously selected to define the impedance port to calculate Z_{11} to obtain fields and currents within the ESD generator and the DUT. The process is summarized in Table I.

The detailed combination in SPICE is now shown (see Fig. 2). The Z_{11} describes the linear part of the system. Once the Z_{11} has been obtained, it needs to be transformed into a form suitable for TD simulation. Software tools like IDEM [20] or Broadband SPICE [21] have been used successfully in this research. The subcircuit created from Z_{11} is not unique. Its complexity can be user defined, which depends on the transformation algorithm, the error, and the order of interest.



Fig. 2. Structure of the SPICE model with the nonlinear arc [12].

The arc of an ESD can be modeled by breaking it down into different phases. The first phase is the resistive phase. The arc is best modeled by a time varying resistance. In the second phase, which is usually reached after a few tens of nanoseconds, the impedance of the external circuit is larger than the impedance of the arc. In this case, the arc often acts more as a constant voltage drop of about 25–40 V. The rising edge of the ESD is the main contributor to the radiated and inductive coupling into DUTs. For this reason, we concentrate on the resistive phase and do not model other aspects (e.g., how the arc extinguishes). Multiple models describe the resistive phase or arcs [18], [19], [22]. In [13], it has been shown that the model of Rompe and Weizel is the most suitable for ESD simulation, as it can correctly describe the effect of the arc length on the rise time and peak current. The arc resistance can be calculated as follows [13]:

$$R(t) = \frac{d}{\operatorname{sqrt}(2a\int_0^t i(\xi)^2 d\xi}$$
(1)

where *R* is the arc resistance (Ω), *d* is the arc length (m), *a* is the empirical constant, most empirically derived values are *a* = (0.5–1)×10⁻⁴ m²/V² s, and *i*(ξ) is the discharge current (A).

The structure of the SPICE model is shown in Fig. 2. A step function having a rise time of approximately 30 ps was used as the source. The rise time is selected by two criteria. If it is too long, then it will influence the current rise time. The current rise time should be determined only by the arc resistance law and the linear equivalent circuit. Further, the rise time cannot be too small, if the pulse contains strong frequency components beyond the range, in which the impedance is calculated, it can lead to instabilities in the SPICE simulation. The fast voltage rise starts the arc resistance model. The current rise time is not determined by the rise time of the step function, but by the arc resistance model. The subcircuit represents Z_{11} . The user provides the voltage and the arc length to calculate the discharge currents. The longest possible arc length in a homogeneous field is given by the Paschen law [13]. Such arc lengths would occur in air discharge for low approach speeds or in humid air conditions. The long arc length leads to slow rise times and lower peak values. Longer arc lengths than the length given by Paschen's equation are possible in strongly nonhomogeneous fields, e.g., if the discharge is between an ESD generator and a sharp edged metal part, or if the discharge is gliding on a nonconducting

70 Capacitive Region 65 Mag(Z11) / dBΩ 60 55 50 45 40 Resistitive Region 35 30 10⁸ 10 10 10 10⁹ Frequency / Hz

Measurement -Short GND Strap

CST Model -Short GND Strap SPICE Model of Fig. 2

Fig. 3. Comparison of $Mag(Z_{11})$ obtained from different methods.

surface. Very short arc lengths occur at high approach speeds and in dry air [9], [13], [23], leading to fast rise times and very high peak current values.

In the following, we will first apply this methodology to a discharge to a ground plane, mainly for verification purposes, and then to a discharge to a small MP3 player.

III. CASE 1: ESD GENERATOR DISCHARGE TO A GROUND PLANE

A. Z_{11} *Between the Tip of the ESD Generator and the Ground Plane*

The structural and discrete elements of the ESD generator are linear with respect to voltage. We further assume that the DUT acts linearly. For obtaining the current injected by the arc, this does not require that no nonlinear effects take place inside the DUT; it only requires that the current injected into the DUT is proportional to the charge voltage. For example, if an internal ESD protection device would clamp a trace voltage while the ESD current is injected into the ground system of the DUT, then, this clamping would have hardly any effect on the current, thus, the DUT would act as a linear device, as seen by the ESD generator. However, if secondary breakdown occurs, e.g., a spark within an attached two-wire power supply, then this could strongly affect the ESD current, thus, the modeling approach might lead to wrong results.

Both TD and FD solvers can be used to obtain Z_{11} . We observed the FD simulation giving a more reasonable Z_{11} result and using less simulation time. The simulated Z_{11} for the structure of the ESD generator above a ground plane is shown in Fig. 3 as the dotted line. This result is verified by comparison with measurement and an approximate SPICE model of this ESD generator [4]. The model contains sufficient detail for achieving a good match to measured impedance data, and correctly represents the 110-pF capacitor and 330- Ω resistor structure inside



Fig. 4. Equivalent circuit of an ESD generator [4]. *Rt* and *Ri* represent the current target resistance and input impedance of the oscilloscope, respectively.



Fig. 5. Comparison of $\text{Real}(Z_{11})$ and $\text{Imag}(Z_{11})$ obtained from different methods.

the ESD generator at lower frequencies. The calculation takes about 15 h on a PC (CPU 3.20 GHz, 16G RAM).

ESD generators have long ground straps. It increases the simulation time if the full length is included into the simulation domain. As most disturbances are caused by the fast changing parts of the currents and fields, one may not need to include the full ground strap into the model. The ground strap mainly influences the falling part of the waveform. The SPICE model shown in Fig. 4 includes a 3500-nH inductor to model the ground strap. A shorter ground strap will reduce the time between the first and the second peak of the discharge waveform.

The first step obtained the impedance representing an ESD generator discharges to a large ground plane. In the next step,

85

75



Fig. 6. Simulated discharge currents of an ESD generator discharging to a ground plane in air-discharge mode at a 5-kV charge voltage.

the impedance is transformed into the TD suitable form and combined with a nonlinear arc equation in SPICE.

B. SPICE Simulation for the Discharge Current

Fig. 6 illustrates the effect of the arc length on the current waveform. It shows SPICE-simulated discharge currents for a 5-kV charge voltage. An arc length of 1.1-mm equals the Paschen length, such a discharge current would be expected at high humidity and slow approach speeds. A more typical value at moderate approach speeds is 0.7 mm. At this value, the rise time will be somewhat similar to the rise time of an ESD, as given in the IEC 61000–4-2 standard (about 850 ps). A more extreme case is given by the 0.3-mm arc length simulation. Very dry air and high approach speeds might lead to such a discharge. The simulated current peak value is 26 A and the rise time is 150 ps.

C. Reimport of Currents Into CST

For obtaining the fields, one needs to reimport the discharge current into the full-wave model as the excitation waveform. This is discussed and validated in the second case example.

D. Validation by Measurement Results

The current into the large ground plane was measured using an ESD current sensor, as described in [3]. In Fig. 7, the SPICEsimulated discharge currents are compared to the measured data for different approach speeds. Even if the exact approach speed or arc lengths are not known, it shows that the ranges of arc lengths used in the simulation are representative for discharge currents obtained in the experiment. A more in-depth comparison based on measured arc length values can be found in [13].



Fig. 7. Comparison of discharge currents discharging to ground plane.

IV. CASE 2: ESD GENERATOR DISCHARGE INTO A SMALL PRODUCT

A. Z_{11} Between the Tip of the ESD Generator and the DUT Surface

This case simulates a discharge into an MP3 player, a small, nongrounded DUT. The whole geometry is shown in Fig. 8. The MP3 player model includes the main blocks of the DUT similar to [24]. In brief, the major blocks of the player (metal frame, battery, display, PCBs) are modeled as metal blocks connected at the locations of connectors and frame connection points.



Fig. 8. Full-wave model of the ESD generator and MP3 player.



Fig. 9. Location of the Z_{11} port.

The DUT is placed on a dielectric sheet above a larger ground plane. This forms a capacitor having a capacitance of about 25 pF, leading to a higher value of Z_{11} at lower frequencies. The value for Z_{11} was obtained, as shown in Fig. 9. The comparison between Z_{11} of the ESD generator and the large ground plane and Z_{11} of the ESD generator with the MP3 player is shown in Fig. 10. It mainly shows the smaller capacitance at lower frequencies; at higher frequencies the impedance of the 25-pF capacitor formed by the player against the ground plane is lower than the source impedance of the ESD generator, thus, the impedance in case 2 is similar to the impedance seen in case 1, the discharge to a large ground plane.

B. SPICE Simulation for the Discharge Current

The Z_{11} defined between the discharge tip and the MP3 player was transformed into a subcircuit using Broadband SPICE. The subcircuit combined with the arc model gave the simulated discharge current for different user-defined charging voltage and arc length. The simulated discharge current at the 5-kV charge voltage with different arc lengths is shown in Fig. 11.



Fig. 10. Simulated Z_{11} of the ESD generator discharging to a small product.



Fig. 11. Simulated discharge current of the ESD generator discharging into the MP3 in the air-discharge mode at a 5-kV charge voltage.

The obtained peak values and rise times are tabulated in Table II. The arc length has a very strong effect on the parameters shown, especially, the current derivative.

C. Reimport of Currents Into CST

To obtain transient fields, the current waveform obtained from the SPICE simulation is reimported into CST as the excitation waveform. The current source port is placed between the two points that had been previously selected to define the impedance port to calculate Z_{11} . One check is worthwhile: If the Z_{11} representation used in SPICE would perfectly match the Z_{11} from the FD full-wave simulation, then the port voltage obtained during the full-wave simulation using the reimported current would

Arc Length	peak value (A)	rise time (ps)	max di/dt (A/ns)
0.3 mm	21.7	200	105.19
0.7 mm	12.4	780	16.617
1.1 mm	8.1	2260	4.5170

TABLE II

COMPARISON OF ARC LENGTH EFFECT



Fig. 12. Comparison of the port voltage in the SPICE model and the CST model of case 1.

match the port voltage (= voltage across the arc) in the SPICE simulation.

For case 2, the SPICE-simulated current was imported back to the CST model as the current source. The comparison of the port voltage in the SPICE model and the port voltage in the CST model in Fig. 12 shows a good match.

The simulation using the reimported current allows simulating the fields within and around the MP3 player by placing appropriate monitor probes. If these probes are placed close to the metallic surfaces of the MP3 player, then they represent the surface current densities and the displacement current densities, which can be used to estimate the coupling into bond wires of an IC, traces, and flex cables for predicting ESD upset threshold levels. Before current and field results are shown, the measurement methods are introduced.

D. Validation by Measurement Results

The current was injected into the small product, and the magnetic field was measured. To capture the current injected into the MP3 player, an F-65 (1 MHz–1 GHz) current probe was used, as shown in Fig. 13. The magnetic field was measured using a small shielded loop and a Tektronix 7404 (4 GHz BW, 20 GS/s) oscilloscope.



Fig. 13. Measurement setup. The F-65 current clamp was placed around the discharge tip and above the product.



Fig. 14. Measurement setup. The foam prevents direct contact of the current probe with the MP3 player or the ESD generator. The H-field probe was placed about 5 cm away from the discharge point.

At 5-kV charge voltage, a NoiseKen ESD generator was discharged into the player. The player was placed above a large GND plane with a dielectric sheet between them. Figs. 13 and 14 illustrate the setup.

The relationship between approach speed, humidity, and arc length is not of deterministic nature, but given by the influence of the humidity on the statistical time lag [13]. Thus, on an average, one will observe shorter arc lengths with increasing approach speeds for a given charge voltage. For achieving short arc length discharges without reducing the humidity, the surface had been cleaned using alcohol and fast approach speeds have been used, longer arc lengths are achieved by slow approach speeds. Shown are examples of the captured waveforms for different approach speeds.

1) Measured Discharge Current: The current clamp's frequency response falls off above 1-GHz bandwidth, thus, the fastest rise time of a step response signal would be approximately 300 ps. Fig. 15 shows the measured discharge currents for different approach speeds.



Fig. 15. Measured discharge current of short ground strap.



Fig. 16. Simulated discharge current for a 0.3-mm arc length and measured current for a fast approach speed.

The simulation results are compared to the measured results for verification. The fast rise time result is shown in Fig. 16. The simulated discharge current for a 0.3-mm arc length and 5-kV charging voltage gives a discharge current with a rise time of about 200 ps and a peak value of 21 A. The measured discharge current has a rise time of about 300 ps and a peak magnitude of about 22 A. The difference can be explained by the limited bandwidth of the F-65 clamp. Due to the difficulty in measuring arc length, we can only approximately compare measured and simulated results. Nevertheless, the comparison shows that the simulated and measured data are within the same ranges.

In Figs. 17 and 18, the comparison of simulation discharge current for 0.7-mm and 1.1-mm arc lengths is shown. They match well with the measured results.



Fig. 17. Simulated discharge current for a 0.7-mm arc length and measured current for a medium approach speed.



Fig. 18. Simulated discharge current for a 1.1-mm arc length and measured current for a slow approach speed.

2) Measured Magnetic Field: This is to confirm the last step of the process: Injecting the SPICE simulated current back into the full-wave simulation for obtaining fields. A shielded loop was placed 5 cm away from the product (see Fig. 14). A deconvolution was performed to obtain the field strength from the captured voltage at the probe output. The deconvolution is mainly an integration process, having two deviations from the ideal integration. At lower frequencies, high-pass filtering is performed to avoid the accumulation of the oscilloscope's small but relevant dc offset during the integration. Second, at higher frequencies, the self-inductance of the probe in conjunction with the 50- Ω load, leads to a self-integration, thus, no external integration is needed above 3 GHz. The resulting magnetic fields are shown in Fig. 19. The data match well. The measured rise time



Fig. 19. Measured and simulated magnetic field at 5 cm away from the discharge point.

is about 250 ps. By using the SPICE model, one can estimate the arc length from the rise time. Repeated simulations indicate an arc length of about 0.4 mm. The Paschen length for 5 kV is about 1.1 mm at sea-level air pressure. Thus, the combination of the speed of approach and the statistical time lag reduced the arc length in this measurement to 35% of the Paschen value, leading to a very fast rising ESD current.

Several field probes were placed in the full-wave model to monitor the magnetic field. A probe that is 5 cm away from the discharge point gives the H-field data shown in Fig. 19. The result matches well with the measured data.

V. DISCUSSION

The methodology allows predicting the currents and fields in and around a product. There are three types of limitations in the methodology.

The most obvious one results from the limited ability of simulating details in the product and within the ESD generator. As with every simulation, the number of unknowns and the ratio of the smallest to the largest detail will limit the size of the model. The methodology allows circumventing this at least partially, especially for small products. If the product is small, then the fields inside the product will be dominated by the fields caused from the injected current and not by fields directly coupling from the body of the ESD generator. Those fields would especially be significant in the contact mode, in which the field components that are greater than 1 GHz are often caused by the rapid voltage breakdown in the gas-filled relay that initiates the discharge. As this analysis is for an air discharge, one will find the strongest high-frequency components directly at the arc, as with further distance from the arc high-frequency components will be attenuated by both frequency-dependent loss and radiation. If the fields are dominated by the injected current, then one can use a relatively simple model of the product just to determine the

current, but in the last step, in which the current is reinjected into the product, a more complex model of the product can be used, but a very simple model of the ESD generator (and a forced current).

The second limitation results from the need for providing the arc length for the arc resistance calculation. Although possible, arc length measurements are difficult to implement. In a simulation, we suggest the following approach. At first, an arc length should be selected that leads to an air-discharge current that is similar to the contact-mode discharge current, as specified in the IEC 61000–4-2 standard. For 5 kV, this is about 0.8-mm arc length. Values for other voltages can be found in [13]. As a very slow rising current, the Paschen value can be selected, leading to discharges of lower severity and as extremely fast rising current; a value of about 30% of the Paschen length is suggested. This value is based on experimental evidence. In measurements that captured the arc length [13], we found it possible even under very dry air and clean surface conditions to obtain arc lengths of less than 30% of the Paschen value.

The third limitation is related to the stability of the TD SPICE simulation. In this simulation, a very rapid change of resistance is combined with a SPICE impedance model created from fullwave simulation. If instabilities occur, one should inspect the SPICE model for passivity and causality, in addition, one can simulate the discharge using longer arc lengths first, as these show a slower change of the arc resistance.

The main application of this model lies in the simulation of ESD to products. For example, it is known that the arc length tends to be small for fast approach speeds in dry air. The short arc length leads to fast rise times and high peak values. Using this model, one can quantify the fields inside a product for different arc lengths. Further applications are the simulation of grounding conditions of products on the arc, and thus, the current. Further, the model can be extended to the case of secondary breakdown, e.g., an ESD occurs to an ungrounded metal part leading to a second discharge from this ungrounded part to the main part of the DUT.

VI. CONCLUSION

This paper proposes a method for simulating an ESD generator discharging in air-discharge mode into a product. The linear and the nonlinear part of the problem are separated to simulate the linear part in a full-wave solution and the nonlinear arc in SPICE. The SPICE results are reimported into the full-wave problem as the excitation. This allows the fields inside a product during an air discharge to be obtained. The method has been verified by the comparison of simulated current and transient field results with measurements.

REFERENCES

- S. Caniggia and F. Maradei, "Circuit and numerical modeling of electrostatic discharge generators," *IEEE Trans. Ind. Appl.*, vol. 42, no. 6, pp. 1350–1357, Nov./Dec. 2006.
- [2] G. Cerri, R. De Leo, and V. M. Primiani, "ESD indirect coupling modeling," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 3, pp. 274–281, Aug. 1996.

- [3] IEC 61000–4-2 Ed. 2.0, Electromagnetic Compatibility (EMC)—Part 4–2: Testing and Measurement Techniques—Electrostatic Discharge Immunity Test, 2008–12-09.
- [4] J. Koo, Q. Cai, G. Muchaidze, A. Martwick, K. Wang, and D. Pommerenke, "Frequency-domain measurement method for the analysis of ESD generators and coupling," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 3, pp. 504–511, Aug. 2007.
- [5] H. Tanaka, O. Fujiwara, and Y. Yamanaka, "A circuit approach to simulate discharge current injected in contact with an ESD-gun," in *Proc. 3rd Int. Symp. Electromagn. Compat.*, May 21–24, 2002, pp. 486–489.
- [6] K. Wang, D. Pommerenke, R. Chundru, T. V. Doren, J. L. Drewniak, and A. Shashindranath, "Numerical modeling of electrostatic discharge generators," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 2, pp. 258– 271, May 2003.
- [7] F. Centola, D. Pommerenke, K. Wang, T. V. Doren, and S. Caniggia, "ESD excitation model for susceptibility study," *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 1, pp. 58–63, Aug. 2003.
- [8] R. Jobava, D. Pommerenke, D. Karkashadze, P. Shubitidze, R. Zaridze, S. Frei, and M. Aidam, "Computer simulation of ESD from voluminous objects compared to transient fields of humans," *IEEE Trans. Electromagn. Compat.*, vol. 42, no. 1, pp. 54–65, Feb. 2000.
- [9] Y. Taka and O. Fujiwara, "Verification of spark resistance formula for human ESD," in Asia-Pacific Symp. Electromagn. Compat. 19th Int. Zurich Symp. Electromagn. Compat., May 2008, pp. 152–155.
- [10] R. Jobava, D. Pommerenke, D. Karkashadze, P. Shubitidze, R. Zaridze, S. Frei, R. Beria, and A. Gheonjian, "Computer simulation of ESD from cone," in *Proc. III Int. Semin./Workshop Direct and Inverse Problems of Electromagn. Acoust. Wave Theory (DIPED)*, Nov. 1998, pp. 111–113.
- [11] R. Zaridze, D. Karkashadze, R. G. Djobava, D. Pommerenke, and M. Aidam, "Numerical calculation and measurement of transient fields from electrostatic discharges," *IEEE Trans. Compon., Packag., Manuf. Technol. C*, vol. 19, no. 3, pp. 178–183, Jul. 1996.
- [12] D. Pommerenke and M. Aidam, "To what extent do contact-mode and indirect ESD test methods reproduce reality," in *Proc. Electr. Over*stress/Electrostatic Discharge Symp., 12–14 Sep., 1995, pp. 101–109.
- [13] D. Pommerenke, "ESD: Transient field, arc simulation and rise time limit," *J. Electrostatics*, vol. 36, no. 1, pp. 31–54, 1995.
- [14] O. Fujiwara and H. Seko, "FDTD computation modeling based on sparkresistance formula for electromagnetic fields due to electrostatic discharge," in *Proc. Int. Wroclaw Symp. Exhibition Electromagn. Compat.*, 2002, pp. 421–424.
- [15] N. Orhanovic, R. Raghuram, and N. Matsui, "Full wave analysis of planar interconnect structures using FDTD–SPICE," in *Proc. 51st Electron. Compon. Technol. Conf.*, 2001, pp. 489–494.
- [16] N. Orhanovic, R. Raghuram, and N. Matsui, "Nonlinear full wave time domain solutions using FDTD_SPICE for high speed digital and RF," in *Wireless Opt. Broadband Conf.*, 2001.
- [17] Microwave Studio, Computer Simulation Technology. (2010, Nov. 4). [Online]. Available: http://www.cst.com/.
- [18] J. M. Meek and J. D. Craggs, *Electrical Breakdown of Gases*. New York, U.K.: Wiley, 1978.
- [19] G. A. Mesyats, V. V. Kremnev, G. S. Korshunov, and Y. B. Yankelevich, "Spark current and voltage in nanosecond breakdown of a gas gap," *Sov. Phys.*—*Tech. Phys.*, vol. 14, no. 1, pp. 49–53, 1969.
- [20] M. Bandinu, F. Canavero, S. Grivet-Talocia, and I. S. Stievano, "IdEM & MπLOG: Macromodeling tools for system-level signal integrity and EMC assessment," in *Eur. IBIS Summit Meet.*, Apr. 19, 2007.
- [21] Broadband SPICE, Sigrity. (2010, Nov. 4). [Online]. Available: http://www.sigrity.com/ products/bds/bds.htm.
- [22] D. L. Lin and T. L. Welsher, "From lightning to charged-device model electrostatic discharges," in *Electr. Overstress/Electrostatic Discharge Symp.*, 1992, pp. 68–75.
- [23] S. Atsushi, Y. Takahiro, and M. Noriaki, "Effects of the relative humidity on ESD from the charged metal," *Seidenki Gakkai Koen Ronbunshu*, vol. 2006, pp. 43–44, 2006.
- [24] Q. Cai, J. Koo, A. Nandy, D. Pommerenke, J. S. Lee, and B. S. Seol, "Advanced full wave ESD generator model for system level coupling simulation," in *IEEE Int. Symp. Electromagn. Compat. (EMC)*, Aug. 18– 22, 2008, pp. 1–6.



Dazhao Liu received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2008. He is currently working toward the Ph.D. degree at the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla.

His research interests include electrostatic discharge, advanced RF measurement, and signal integrity.



Argha Nandy received the B.S. degree from the West Bengal University of Technology, Kolkata, India, in 2007. He is currently working toward the Master of Science degree in electrical engineering at the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla.

His research interests include electrostatic discharge, electromagnetic compatibility, and numerical calculation.



Fan Zhou received the B.S.E.E. from the Department of Electrical Engineering, Hunan University, Changsha, China, in 2004, and the M.S.E.E. degree from the Department of Electrical Engineering, Beihang University, Beijing, China. He is currently working toward the Master of Science degree in electrical engineering at the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla.

His research interests include electrostatic discharge modeling, giant magnetoimpedance probe, and signal integrity.



Wei Huang received the B.S. degree in communications engineering from the Beijing University of Posts and Telecommunications, Beijing, China, in 2007. He is currently working toward the Master of Science degree in electrical engineering at the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, since 2007.

His research interests include system and scanning level electrostatic discharge measurement and analy-

sis, probe design and analysis, electromagnetic compatibility/electromagnetic interference measurement and analysis, advanced RF design, and instrumentation for high voltage.

Mr. Huang is a member of Electrostatic Discharge Association. He is also International Association for Radio, Telecommunications and Electromagnetics (iNARTE) Certified Associate EMC Engineer.



Jiang Xiao received the B.S. and M.S. degrees from the Beijing Institute of Technology, Beijing, China, in 2001 and 2003, respectively, and the Ph. D. degree from the Chinese Academy of Sciences, Beijing, China, in 2006.

He is currently a Postdoctoral Fellow at the Electromagnetic Compatibility Laboratory, Missouri University of Science and technology (formerly University of Missouri-Rolla), Rolla. He was also an Assistant Professor at the Chinese Academy of Sciences, Beijing, for two years. His research interests include

electrostatic discharge, electromagnetic compatibility, advanced RF measurement, and antenna design for communication and radar, image, and signal processing.



Byongsu Seol received the B.S. and M.S. degrees from Chungbuk National University, Cheongju, Korea, in 1992 and 1995, respectively.

In 1994, he joined the IC packaging technology group of LG Semicon, Cheongju, Korea, which later became a part of Hynix Semiconductor. In 2000, he joined Tessera Technologies, San Jose, CA, as a signal integrity Engineer. Since 2003, he has been with Samsung Electronics, Suwon, Korea. His current research interests include high-speed system designs, electrostatic discharge analysis methods, and elec-

tromagnetic compatibility design for electronic products.



Jongsung Lee received the B.S. and M.S. degrees in electrical engineering from the University of California Irvine, Irvine, in 2002 and 2004, respectively.

Since 2004, he has been with Samsung Electronics, Suwon, Korea. His current research interests include signal integrity, electrostatic discharge, and electromagnetic compatibility in both measurement and simulation.



Jun Fan (S'97–M'00–SM'06) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, in 2000.

From 2000 to 2007, he was a Consultant Engineer at NCR Corporation, San Diego, CA. In July 2007, he joined the Missouri University of Science and Technology, where he is currently an Assistant

Professor at the Electromagnetic Compatibility Laboratory. His research interests include signal integrity and electromagnetic interference (EMI) designs in high-speed digital systems, dc power-bus modeling, intrasystem EMI, and RF interference, printed-circuit-board noise reduction, differential signaling, and cable/connector designs.

Dr. Fan was the Chair of the IEEE EMC Society TC-9 Computational Electromagnetics Committee from 2006 to 2008, and was a Distinguished Lecturer of the IEEE EMC Society in 2007 and 2008. He is currently the Vice Chair of the Technical Advisory Committee of the IEEE EMC Society. He is also the recipient of the IEEE EMC Society Technical Achievement Award in August 2009.



David Pommerenke (M'98–SM'03) received the Ph.D. degree from the Technical University of Berlin, Berlin, Germany, in 1996.

After working at Hewlett Packard for five years, he joined the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla) Rolla, in 2001, where he is currently a Tenured Professor. His research interests include electromagnetic compatibility (EMC), electrostatic discharge (ESD) measurement techniques, electromagnetic interference anal-

ysis methods, and numerical methods and instrumentation for EMC and high voltage. He is the author or coauthor of more than 100 publications and is the holder of 7 patents. He is the U.S. representative of the ESD standard setting group within the International Electrotechnical Commission TC77b.