FROM RESEARCH TO INDUSTRY

cea tech

leti

3D TECHNOLOGY FOR IMAGING SENSOR AT CEA-LETI

Gabriel Parès April 2015 | LAL presentation


AGENDA

- **Leti brief overview**
- **Post-processing Leti 3D technology modules state of the art & development**
  - Chip's Interconnections : micro-bumps/pillars
  - Chip intra-connections: TSV
- **3D examples: imaging sensor application**
  - Image sensor for visible
  - Image sensor for high energy particles
- **Conclusion**

LETI AT A GLANCE

clinatec®

Bio medical plateform

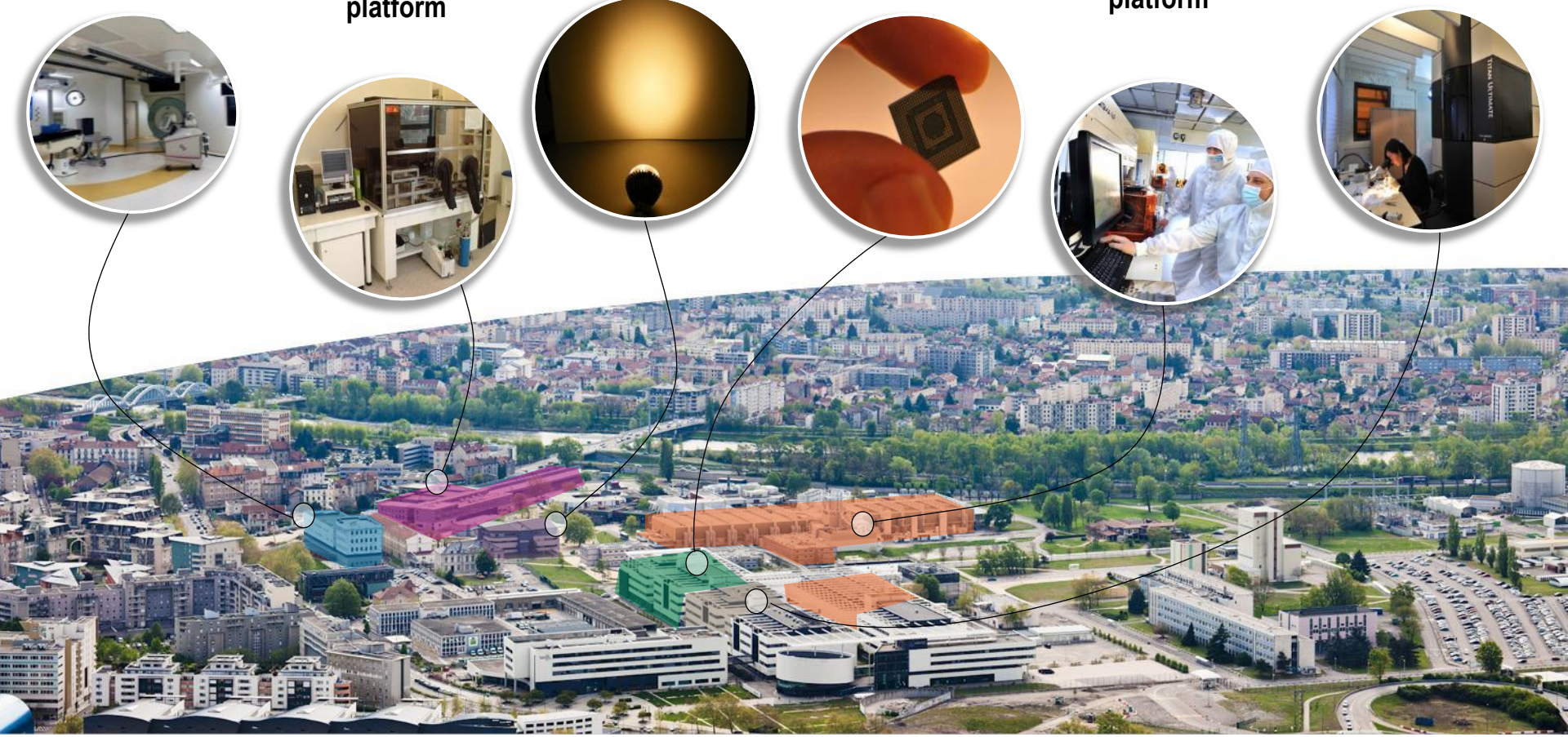
Chemical & material platform

Photonic plateform

Embedded systems

Micro & Nanoelectronic platform

Nanocharacterisation platform



Imaging @ LETI – a global offer

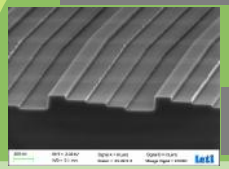
From material to system

➔ from photon to decision

System

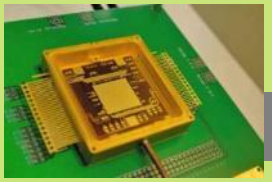
Image processing

Characterization

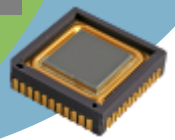


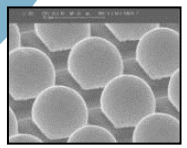
Optics

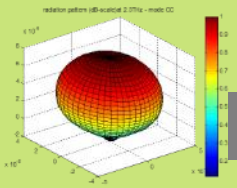
Component



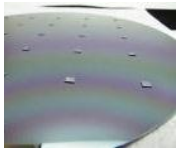
Integration - packaging

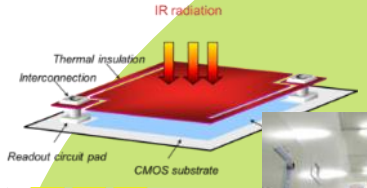


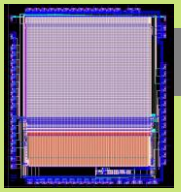




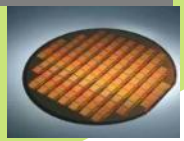
Modeling - simulation



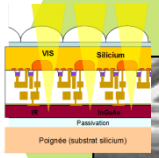


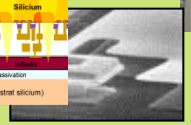


ROIC design



Technologies



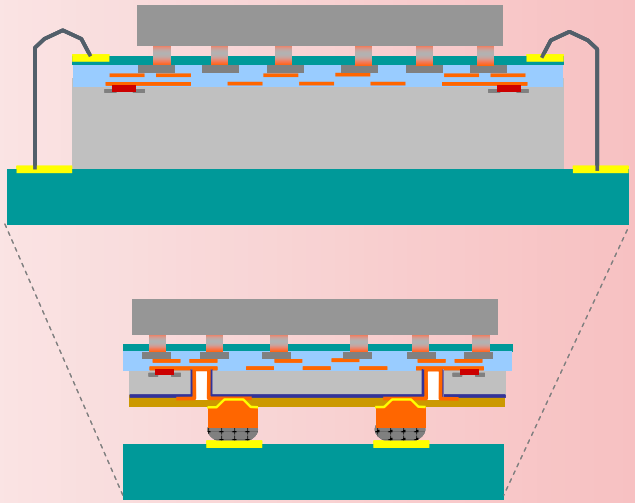


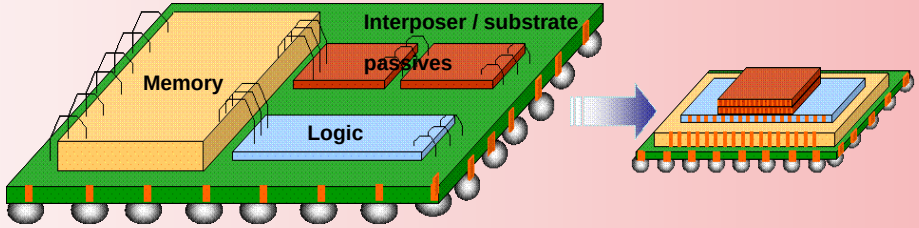
Detection materials

Continuous transfer

WHY DO WE NEED 3D INTEGRATION ?

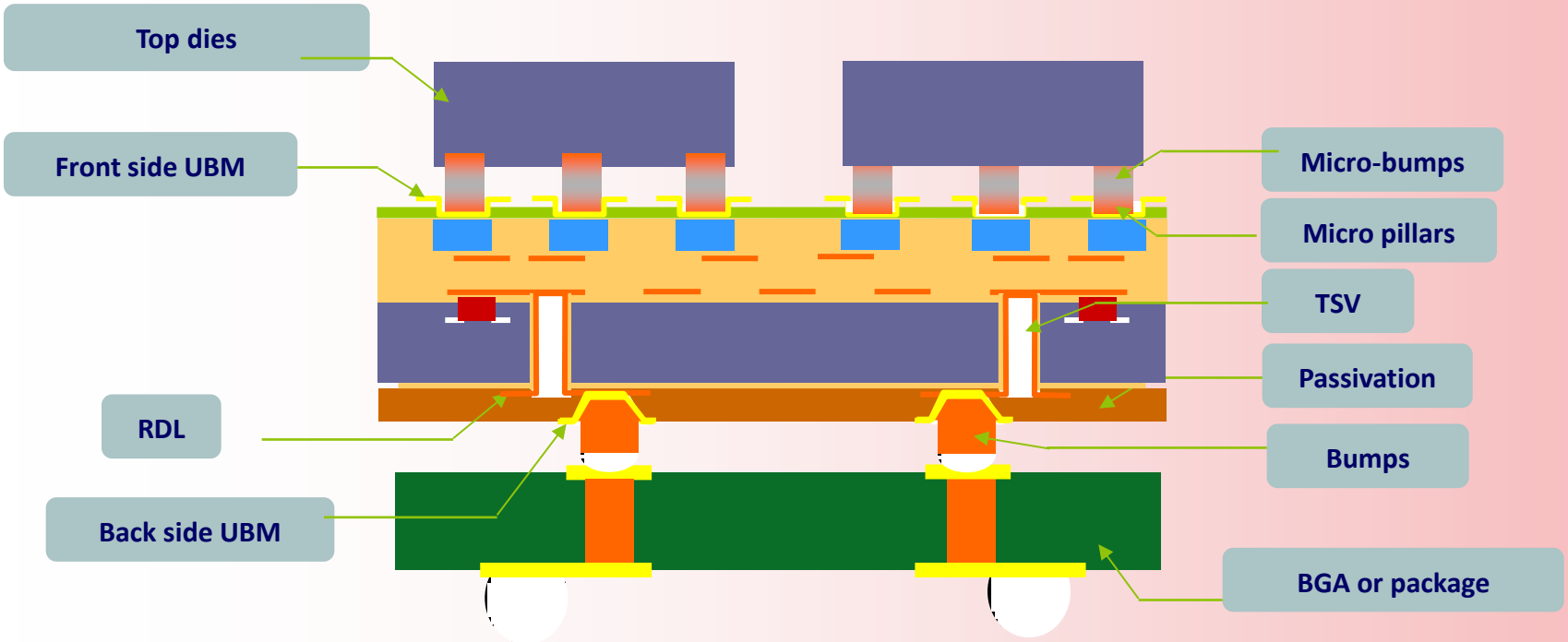
- To solve the following issues :
  - Form factor decrease :
    - X & Y axis
    - Z axis
  - Performances improvement
    - Decrease R, C, signal delay
    - Increase device bandwidth
    - Decrease power consumption
  - Heterogeneous integration
    - Integration of heterogeneous components in the same system
  - Cost decrease
    - Si surface decrease
    - Reuse of existing Packaging, BEOL & FEOL lines



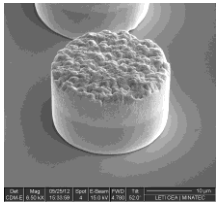
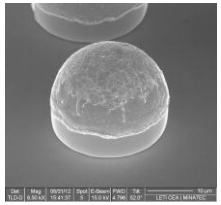


3D Technological modules :

- Through Silicon via (TSV)
- Redistribution layer (RDL)
- Under Bump Metallization (UBM)
- 3D Interconnections: µbump/µpillar
- Wafer bonding: temporary or permanent
- Wafer thinning
- Components stacking
- Wafer level packaging



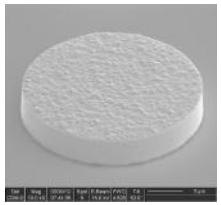
THE 3D INTERCONNECTIONS

Top Die

Post ECD Cu/SnAg *Post Reflow*

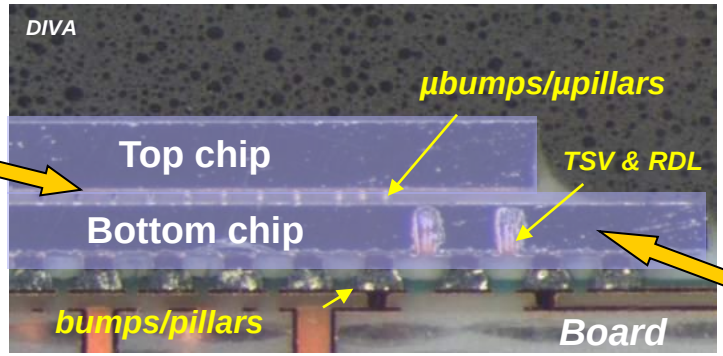
Die to Die µBumps (Φ20µm)



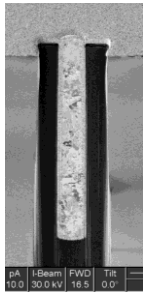
Bottom Die

Post ECD Ni/Au

Die to Die µPillars (Φ20µm)

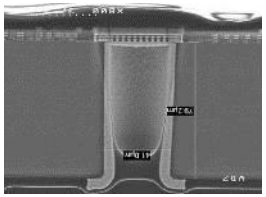


Heterogeneous 3D integration on interposer

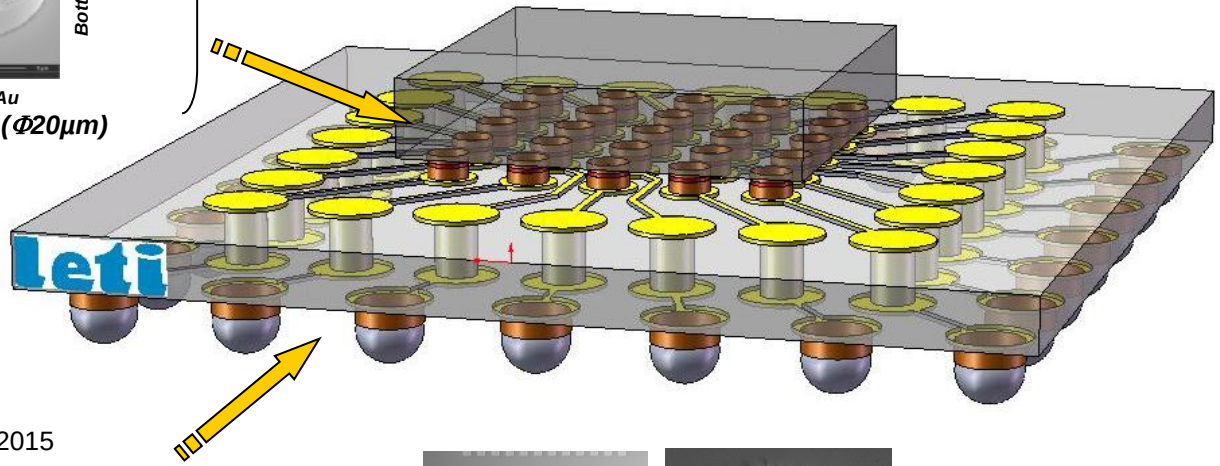



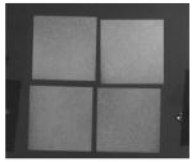
6x55 µm *10x80 µm*

TSV Middle

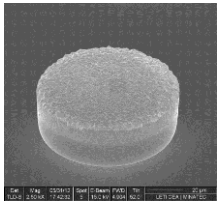
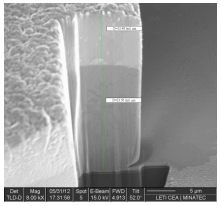
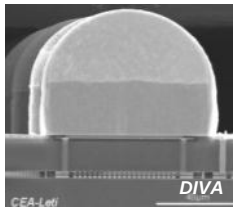


TSV Last



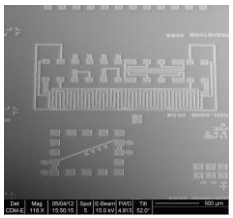
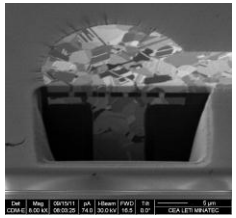


From C. Ribière CEA-Leti 2015

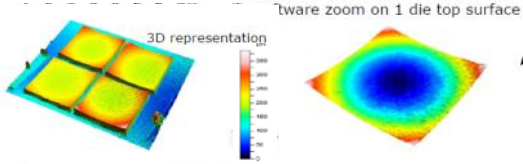
Post ECD Cu/SnAg *Post Reflow*

Die to Substrate Bumps (Φ55µm)

Back side : RDL *Front side : Damascene*

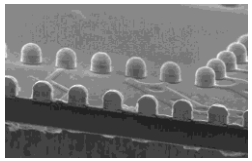
Intradie interconnexions: RDL and TSV

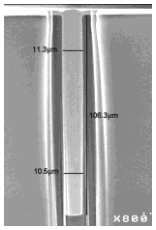
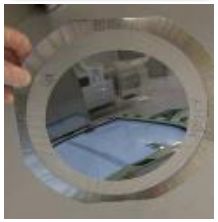


Back side material and stress management

THE GENERIC TOOLBOX FOR 3D

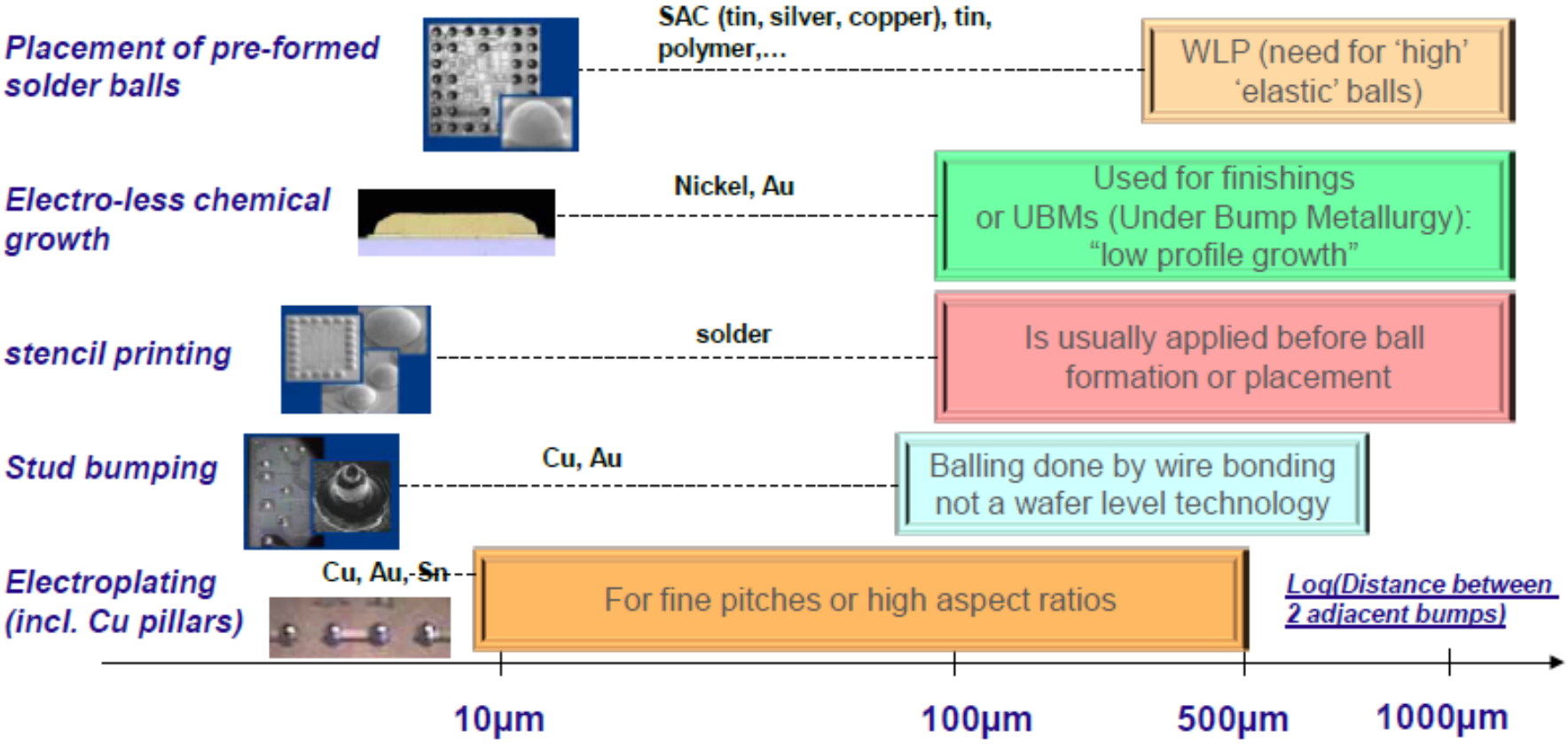
Connecting	Die to Substrate	TSV	Handling thinning	Die Placement	WL Molding
Solder balls	*Wire Bonding*	TSV First	handling	High throuput P&P	Thick Polymer molding
Copper Pillars	Solder balls	TSV Middle AR10	Temp Bonding (Zonebond)	High precision P&P	Thin Polymer molding
Via belt	Copper pillar	TSV Last AR2.5	High temp. bonding	Self Assembly	Thin Oxide planarization
µtubes		TSV Last AR5	Permanent bonding	Wafer To Wafer	WLUF
Cu-Cu		TSV Last High temp	Thinning		Capillary Underfill
Rdl Thick Cu		TSV Last High density	Super thinning		



THE DIE-TO-DIE VERTICAL INTER-CONNECTIONS: MICRO-BUMP/MICRO PILLARS/UBM

Usual Bumping Technologies and Pitches



Courtesy of Nexx

- Galvanic growth (electroplating) is the most suited technology to make fine-pitch bumps at the wafer level with a high aspect ratio. High aspect ratio bumps are useful to get more "elasticity" for reliability. Copper pillars (made by electroplating) are increasingly being used for flip chip BGA as the first level interconnect technology of choice.

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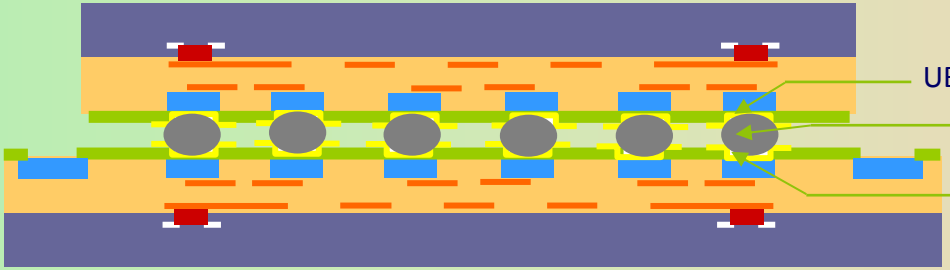
STANDARD FLIP CHIP STACKING OPTIONS

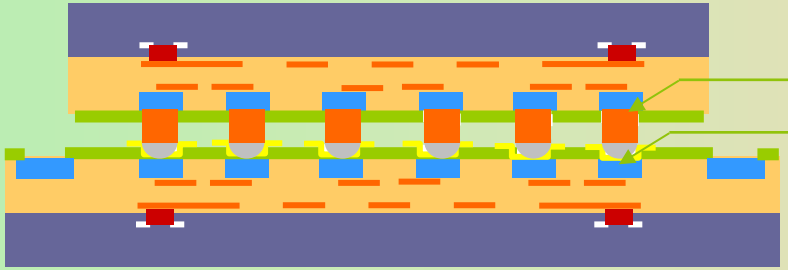
Solder balls with UBM on both dies



Example : Medipix

Usual pitch limited to 140 µm (70/70)
feasibility proven ~ 70 µm (omegapix)

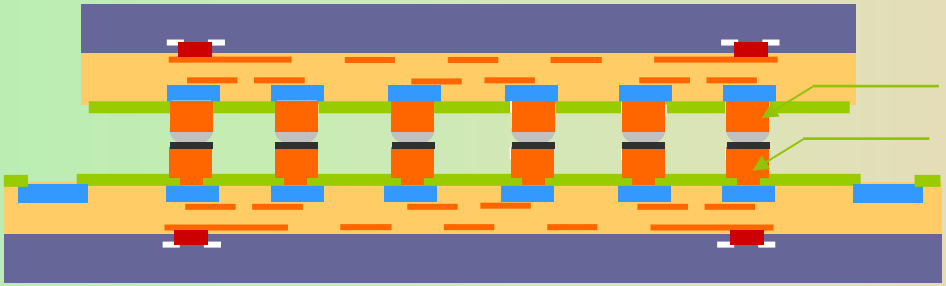
µbump and UBM, usually µbump are on top chips



Example : FEI4/sensor

Usual pitch limited to 40 µm (20/20)
feasibility proven ~ 20 µm

µbump and µpillar (or Cu post), usually µbump are on top chips



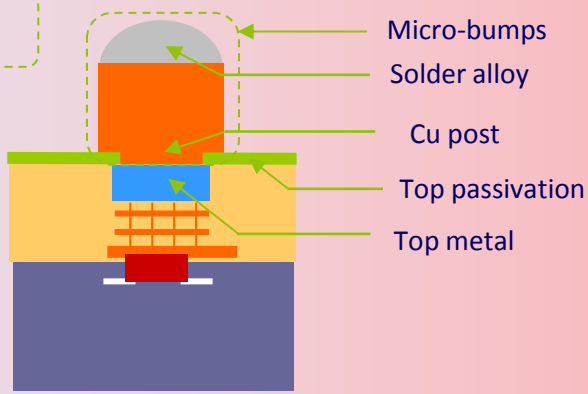
CMOS/CMOS

Usual pitch limited to 40 µm (20/20)
feasibility proven ~ 20 µm

MICRO-BUMPS PORTFOLIO VS CMOS NODES

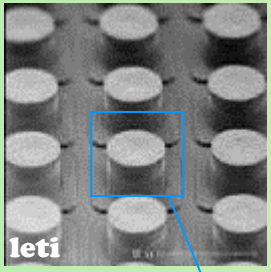
Micro-bumps DRM & schematic

- Wafer size : **300 - 200 mm**
- Micro-bumps material : **Cu post / SnAg 305 solder**
- Minimum pitch : **40 µm**
- Minimum micro-bumps diameter : **20 µm**
- Micro-bumps thickness (typical): **Cu 10µm / SnAg 10µm**

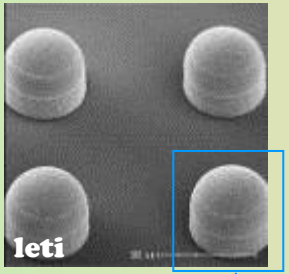


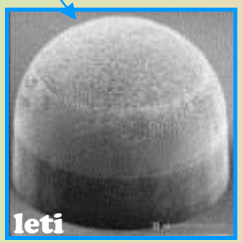
Micro-bumps Morphological illustrations

Micro-bumps before reflow

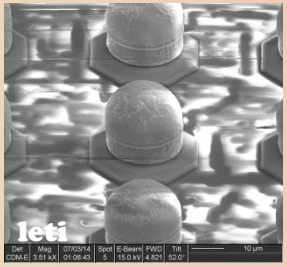


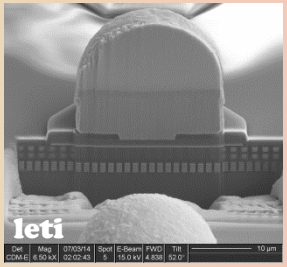
Micro-bumps after reflow



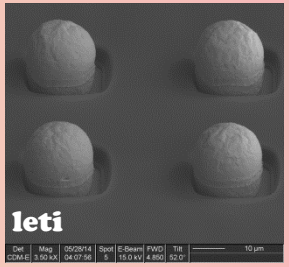


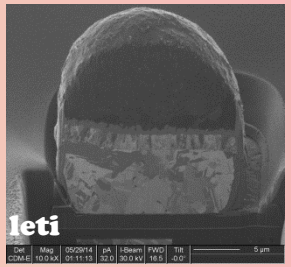
Micro-bumps **on C65**
D= 25 µm





Micro-bumps on **FDSOI28**
D= 18 µm

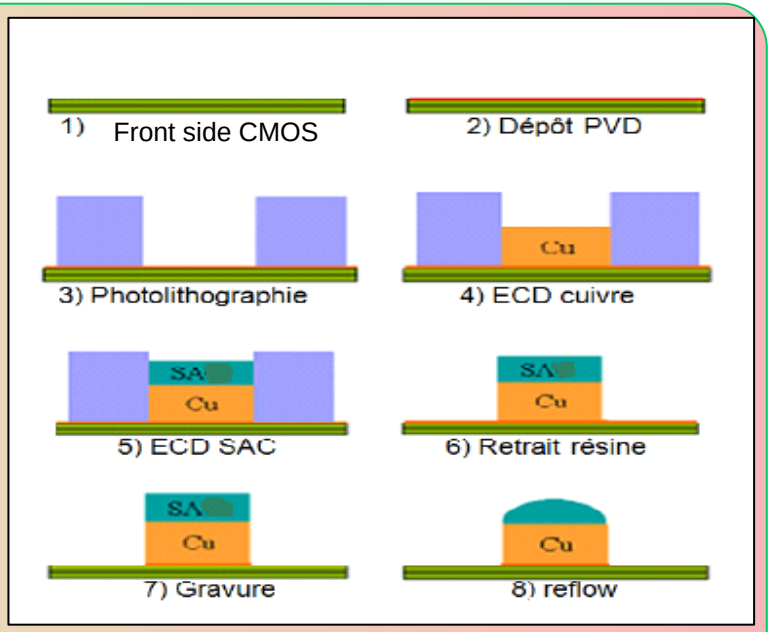




PROCESS OF THE SOLDER BUMPS

Semi-additive electroplating growth:

- Full sheet seed PVD deposition Ti-Cu
- Photolithography with thick resist (>0 or <0)
- Electroplating of the metals: Cu-(Ni)-SnAg- (Au)
- Resist stripping
- Seed wet/dry etching
- Reflow



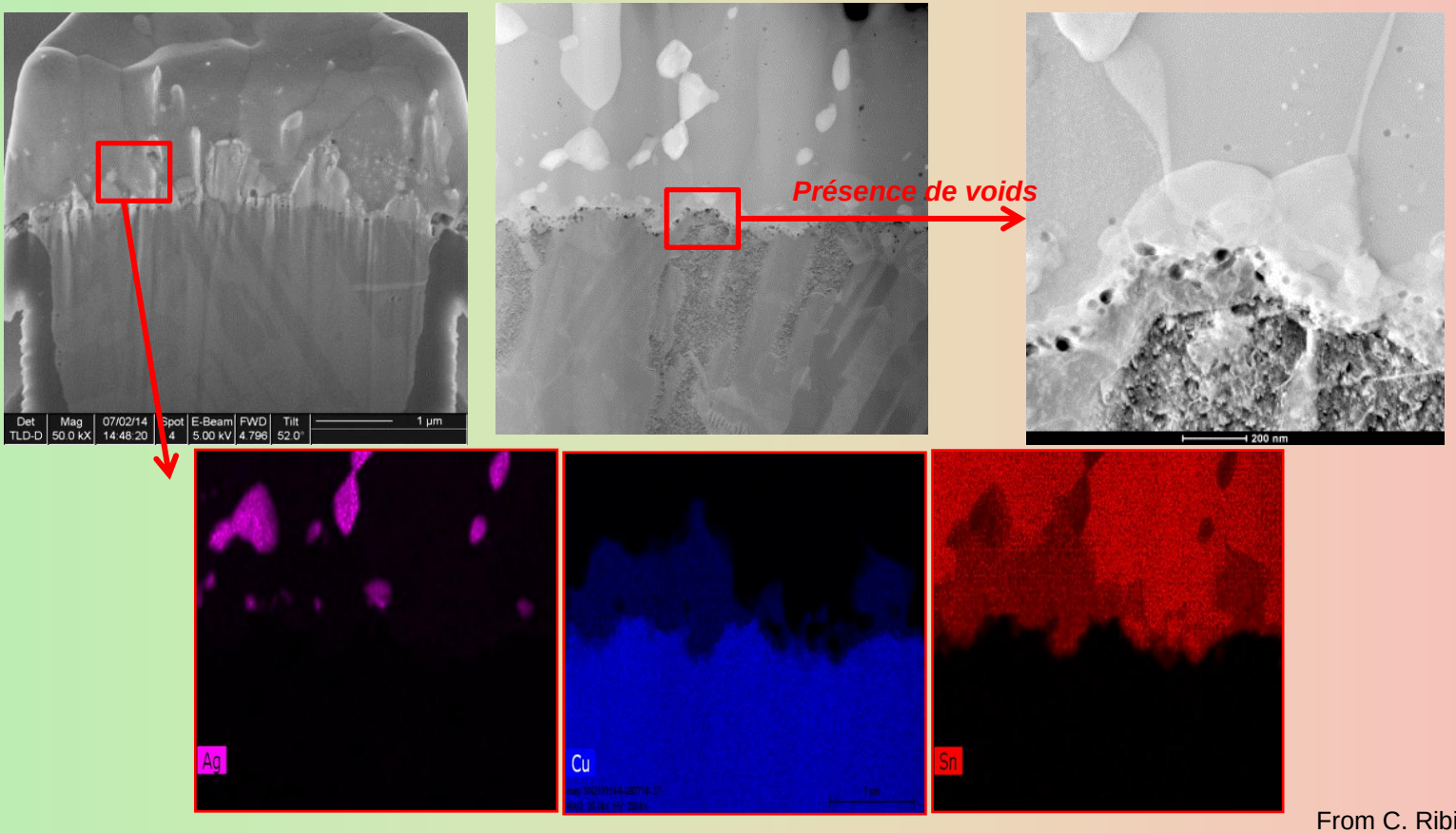
From C. Ribière CEA-Leti 2015

Challenges for fabrication of microbumps << Ø20µm:

- New thick resist with better definition
- Limitation of the seed layer under-etching
- Control of the IMC Cu/SnAg for reliability (mechanical and EMG)

THE IMC FORMATION DURING REFLOW CYCLE

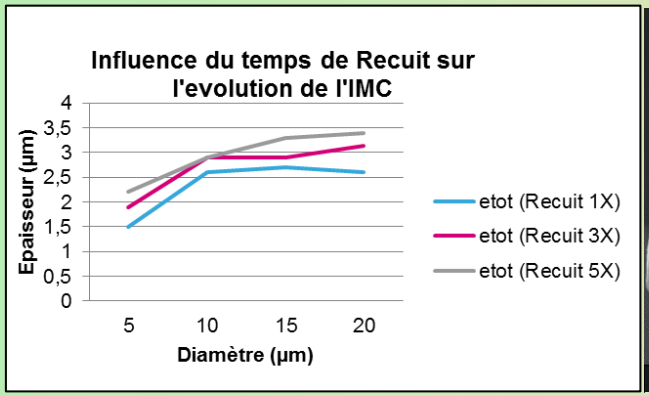
- Copper diffuses inside SnAg
- Formation of Cu_6Sn_5
- Formation of some voids (Kirkendall) at the interface and of Ag_3Sn precipitates : can lead to reliability issue

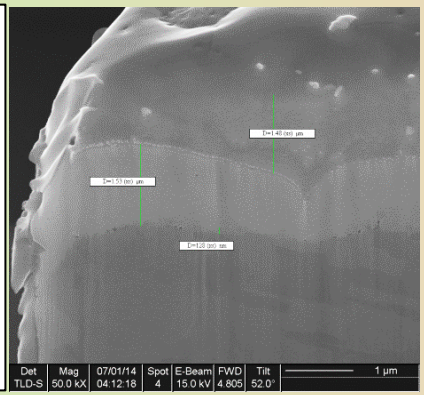


From C. Ribière CEA-Leti 2015

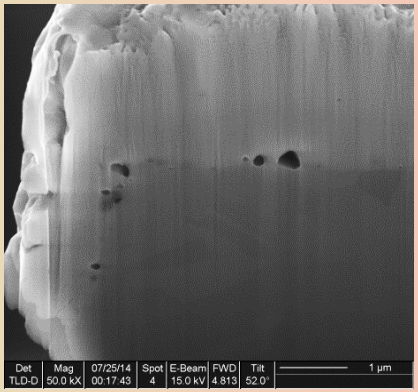
EFFECT OF X REFLOWS

- Growth of IMC CU_6Sn_5 and creation of Cu_3Sn phase.
- Increase of Kirkendall voids at Cu_3Sn interface

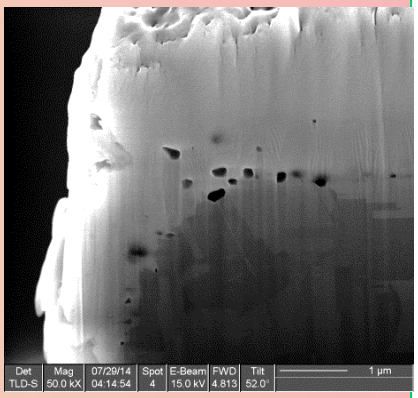




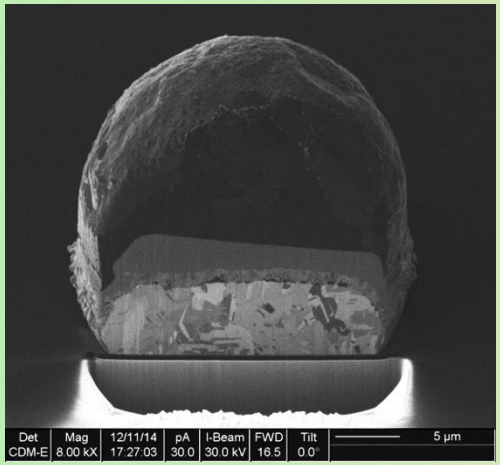
Reflow 1X

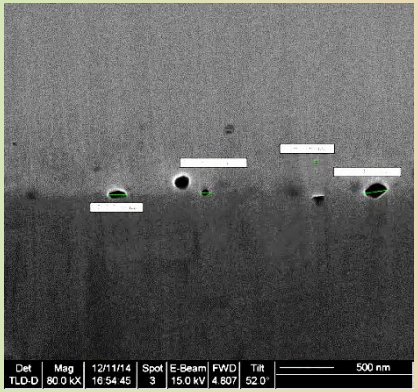


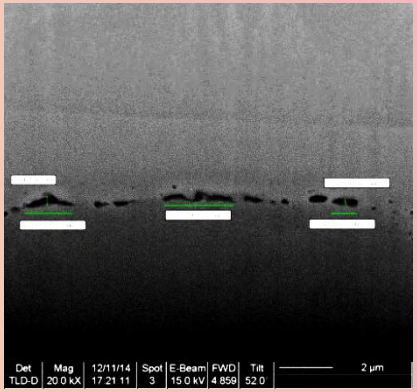
Reflow 3X



Reflow 5X



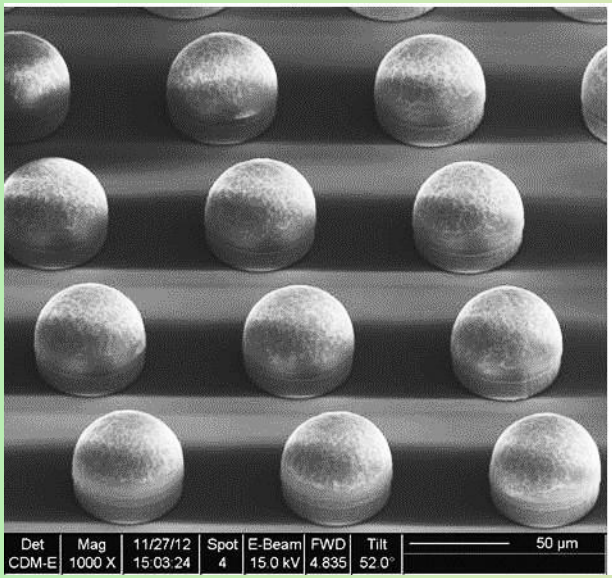


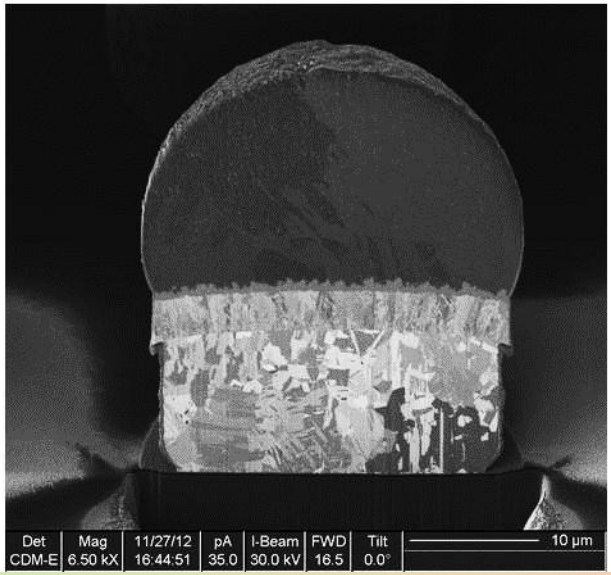


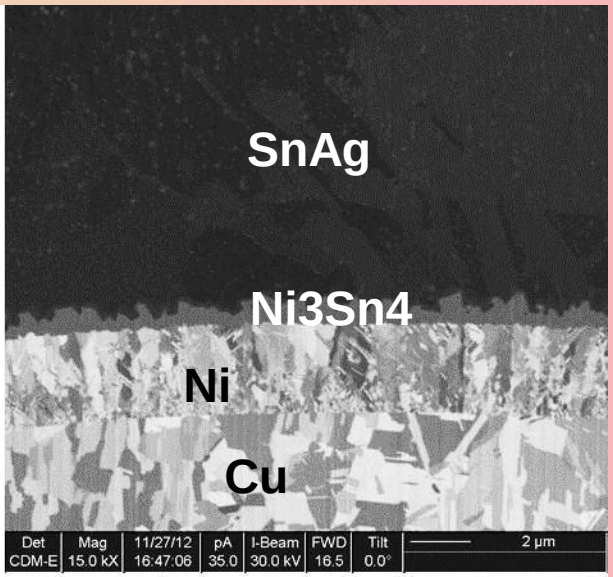
From C. Ribière CEA-Leti 2015

THE EFFECT OF NI INTERLAYER

- Only Ni_3Sn_4 IMC with slow reaction.
- No Kirkendall voids.
- But Ni_3Sn_4 IMC is more fragile // Cu_6Sn_5 (literature) : impact on reliability needs to be more studied for small diameters



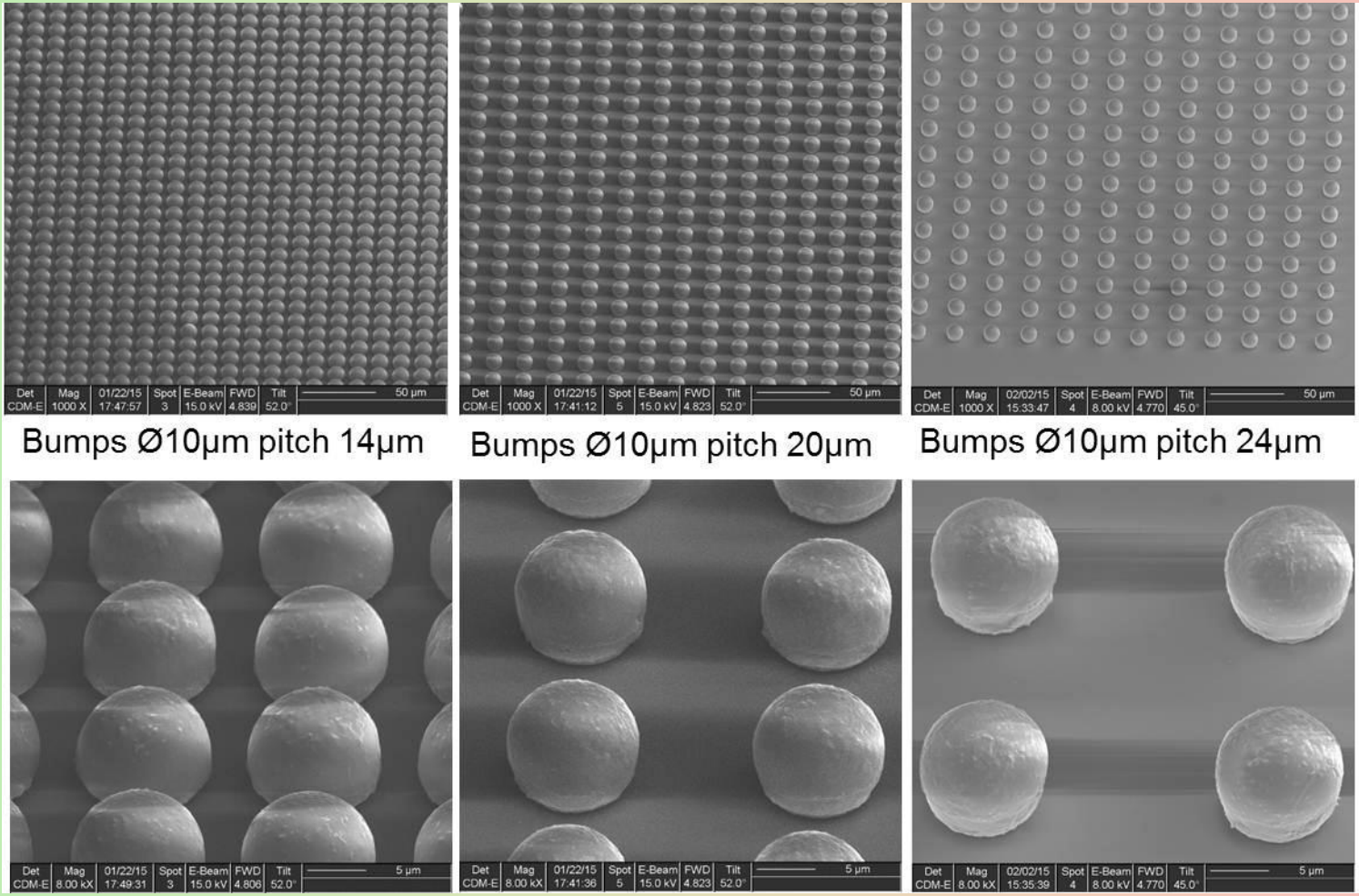




Depotion ECD Cu/Ni/SnAg

From C. Ribière CEA-Leti 2015

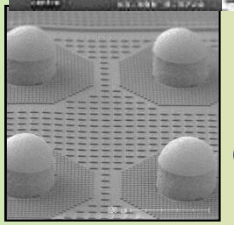
FINE PITCH µBUMPS DEVELOPMENT



From C. Ribière CEA-Leti 2015

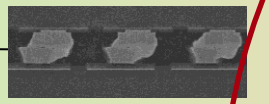
TECHNOLOGY FOR VERY LOW PITCH INTERCONNECTION

High volume manufacturability (HVM) (300mm compatibility, high speed P&P)



Cu pillars

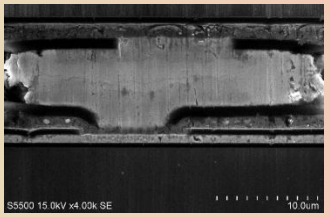
Pre-applied underfill

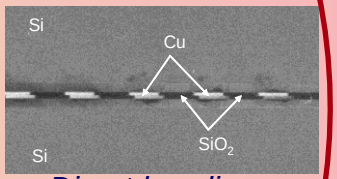


Current technologies

Advanced technologies

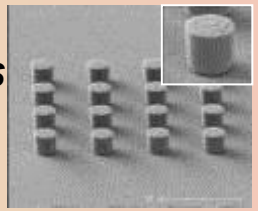
TLP(Cu/Sn)





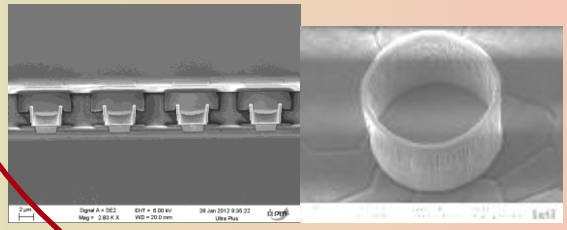
Direct bonding WtW or DtW

Room T Insertion



Solder-free µinserts

Nickel Micro-insertion



µtubes

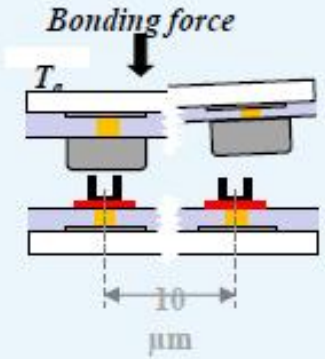
Microinsertion

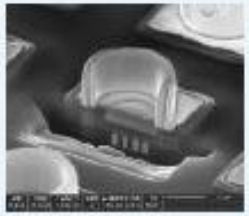
100-30 µm range

30-5 µm range

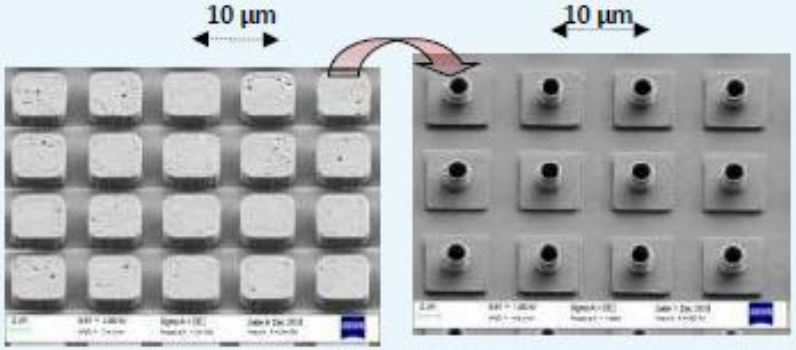
Down to 1µm

- **Available technologies for fine pitches interconnections :**
  - **Micro tubes – pitch 10µm**
    - Applications : IR sensors for defense and space
    - Room temperature assembly using thermo-compression
    - Multi materials approach possible for insertion : In / Au / Al / Cu
    - Reliable demonstration for XGA detector (10µm pitch)
    - Developments on going for ultra low pitches (5 µm)
    - capillary underfill / pre underfill under developement





10 µm pitch

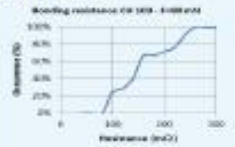


Connect. Yield	Shorts	CH103 Mean R = 180 mΩ	Rmin (mΩ)	Rmax (mΩ)
100%	0%	Force 8 mN	101	264

Connection yield (%)

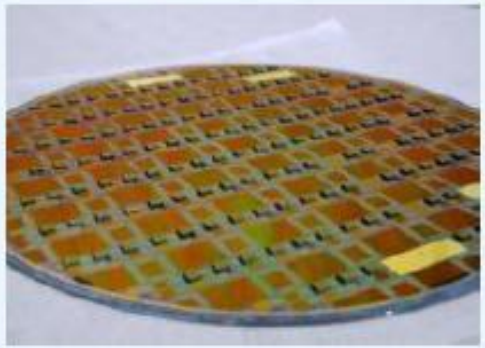
100	100	100	100	100	100
98	100	100	100	100	100
100	100	100	100	100	100
100	100	100	100	100	100
100	100	100	100	100	100
100	100	100	100	100	100
100	100	100	100	100	100
100	100	100	100	100	100

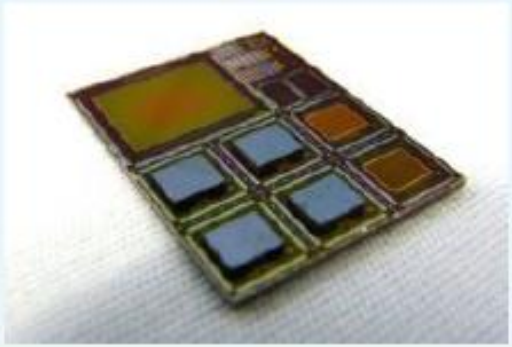
Good yield
100% connected cells



42 cell plotted

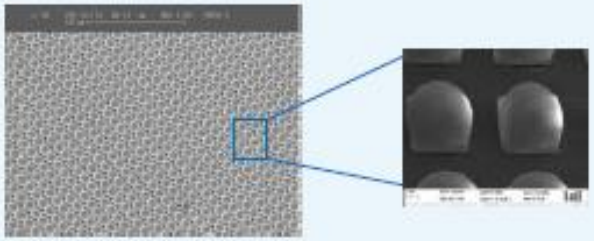
Figure 13: Connection yield/access resistance (8mN)

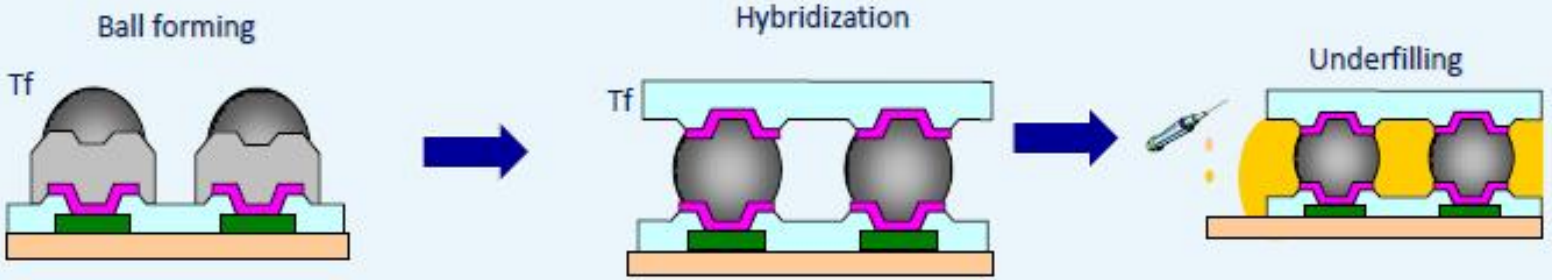


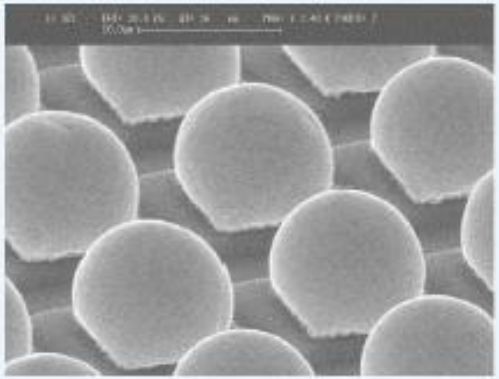


FINE PITCH INTERCONNECTION WITH INDIUM BUMPS

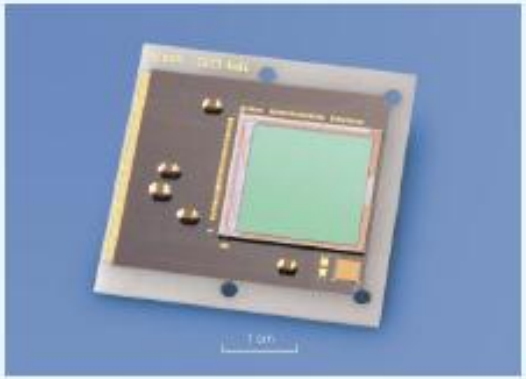
- **Available technologies for fine pitches interconnections :**
  - **Indium micro-balls from 30µm pitches to 10µm**
    - Applications : IR sensors for defense and space
    - assembly by low temperature reflow
    - Capillary underfill





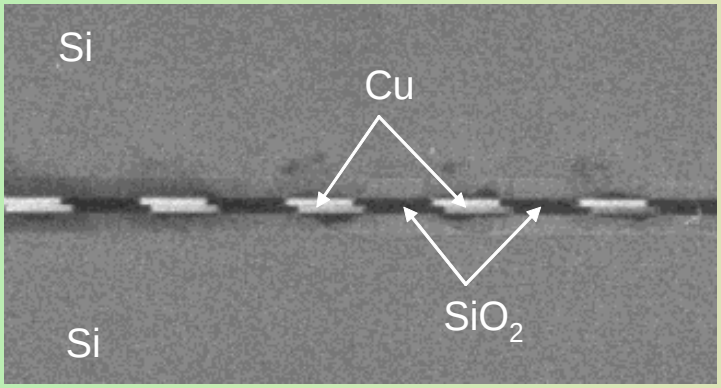


15 µm pitch micro-balls

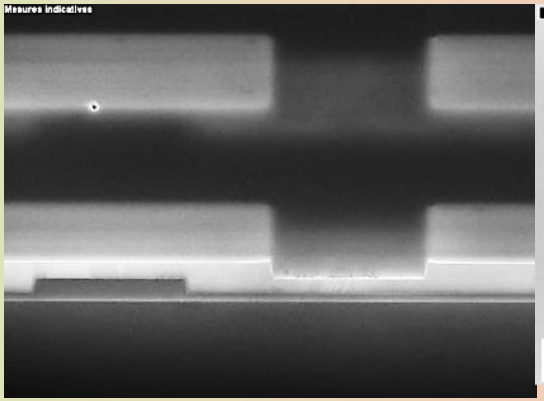


1000x1000 pixels matrix with 15 µm pitch micro-balls

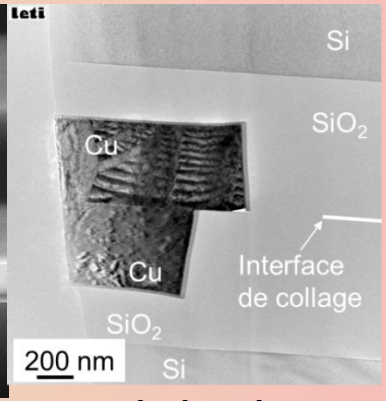
DIRECT BONDING FOR ULTRA LOW PITCH INTERCONNECTION



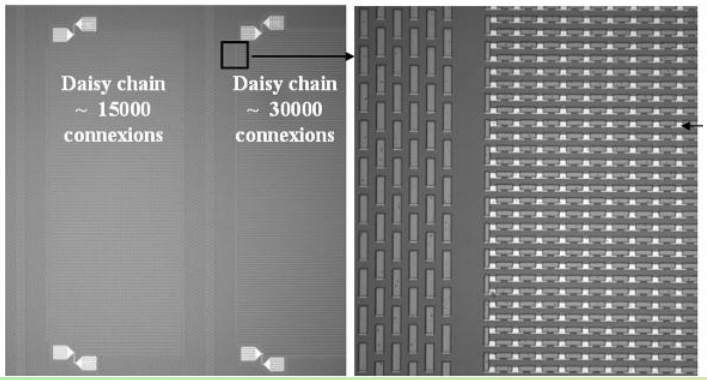
Direct bonding
WtW or DtW
Composite Cu/SiO2 interface



SEM of bonded patterned structure (hybrid oxide-metal) at 400°C



transmission electron imaging of the copper pad bonding



14µm pitch along x
7µm along y

Perfect ohmic contact: 22.5mΩ.µm2
(Equivalent to bulk copper)
Measured resistance of 29422 interconnect daisy chain:
→88.5% yield, 1,2% standard deviation

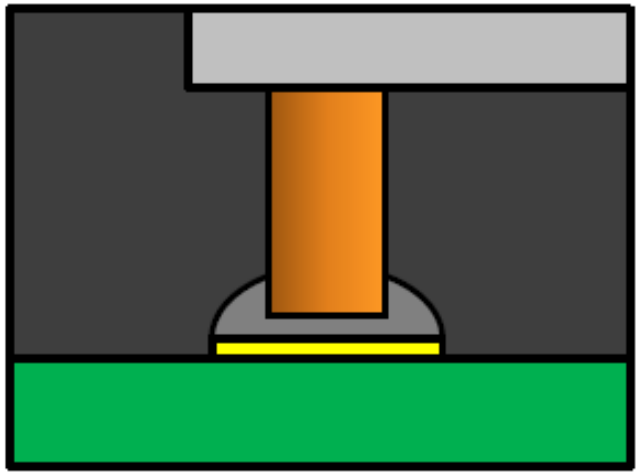
→ Roadmap to Pitch lower than 2 µm, In Progress

Post bonding annealing	Min (Ω)	Max (Ω)	Average resistance (Ω) DC5	Standard deviation (%)
400°C for 2h	2162	2291	2202	**1.18**

Source: "200°C direct bonding copper interconnects : Electrical results and reliability", L. Di Cioccio et al, IEDM 2011

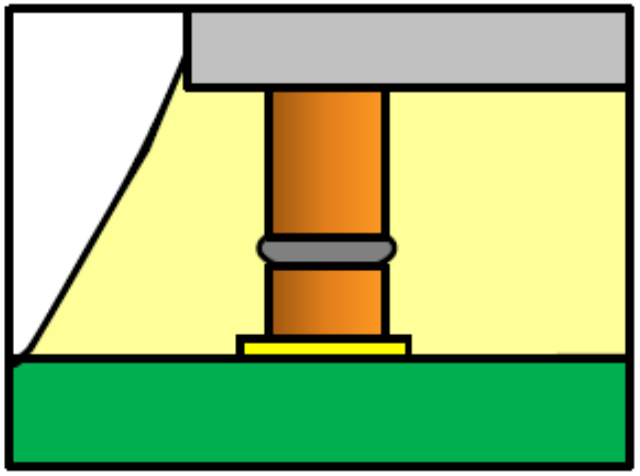
2 die bonding techniques with copper pillars

Thermal Bonding



- Fluxing fllowed by device level reflow soldering.
- Post bond underfill (capillary or MUF)
- High bonding accuracy (pitch > 70µm for capillary and 120µm for MUF)
- uph = 2000-3000
- Applications:
  - Low cost flip chip (especially in mobile applications)
  - Flip chip on leadframes (PMUs, power devices)

Thermo Compression Bonding



- No fluxing, thermo compression with local reflow
- NUF (pre-bond underfill)
- Very high bonding accuracy. Pitch down to 20µm in the coming years
- uph=500
- Applications:
  - Low cost flip chip with high IO density
    - On current CSP and BGA substrates
    - On coreless substrates
    - Silicon to silicon microbumping

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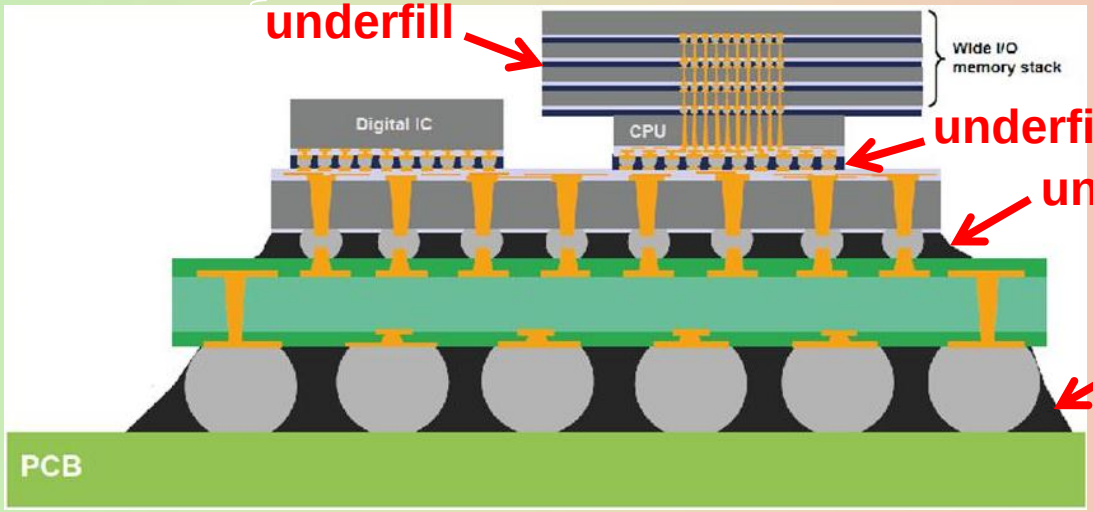
<u>Underfill</u> = material filling the gap created by interconnections between two parts (chip or substrate)

Used for different purposes:

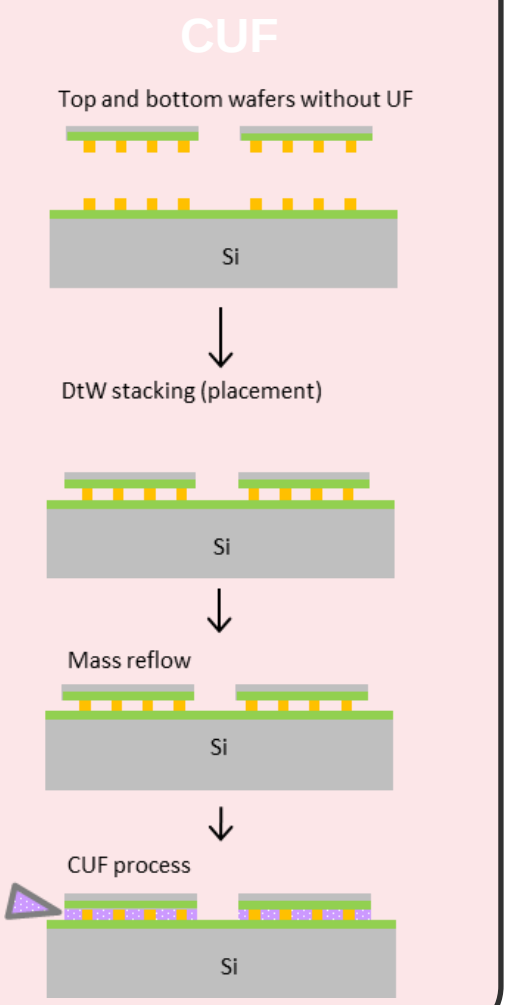
- **physical barrier to moisture to avoid corrosion**
- **filling the air gap around the interconnections before overmolding**
- **lowering strains and stresses in the interconnections when subjected to thermo-mechanical fatigue**



Source: Yole Développement

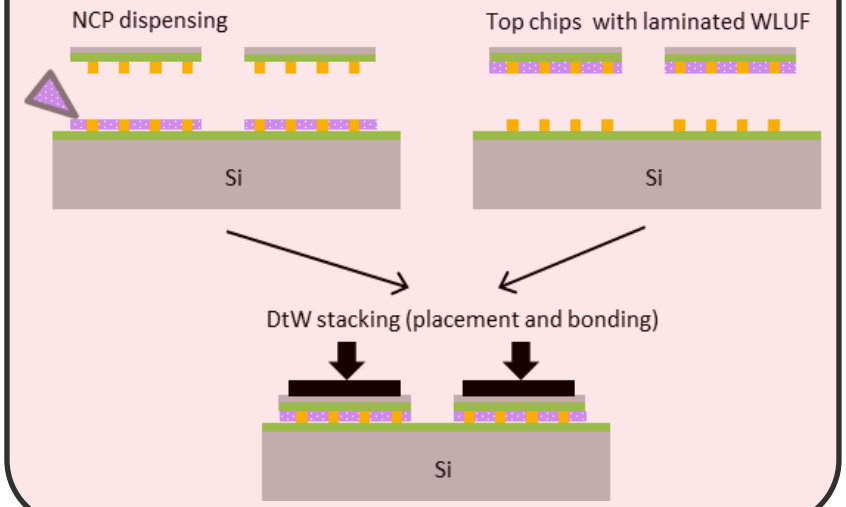
UNDERFILLING TECHNIQUES DEVELOPMENT

Post-applied underfill



Limited for fine pitch

Pre-applied underfills



Source: A. Garnier, ECTC 2014

Pro:
- High density/fine pitch
- Narrow stand off
- No flux

Cons:
- Low througput
- Underfill entrapment
- Process sensitive to interco layout

THE INTRA CHIP CONNECTIONS: THROUGH SILICON VIA (TSV)

VIA LAST TECHNOLOGY FOR POST-PROCESSING 3D INTEGRATION

TSV : VIA-LAST, VIA-FIRST OR VIA-MIDDLE … ARE APPLICATION DEPENDANT

Post process vias or via last

CMOS FE

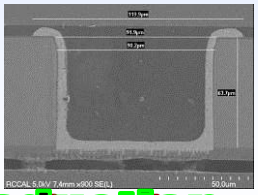
CMOS BE

Vias

Packaging

Low temp. process
Technology flexibility
Very Low resistance

Copper liner



In production
no dedicated design
Density limitation

Mid process vias

CMOS FE

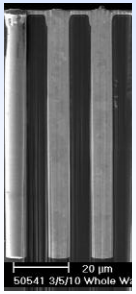
Vias formation

CMOS BE

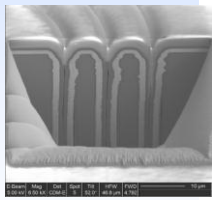
Vias exposure

Packaging

BEOL comp.
Technology cost
Low resistance



Holes filled with W/Cu



Dedicated design
High density capability

Pre process vias Or Via first

Vias formation

CMOS FE

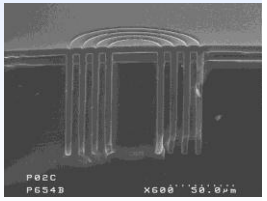
CMOS BE

Vias exposure

Packaging

FEOL/BEOL comp.
Technology cost
medium resistance

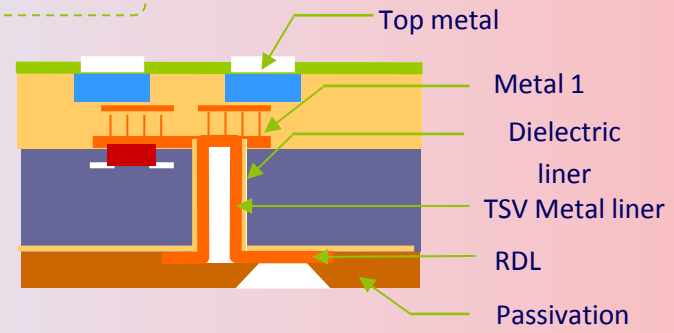
Annular rings filled with polysilicon



Application specific
Density limitation

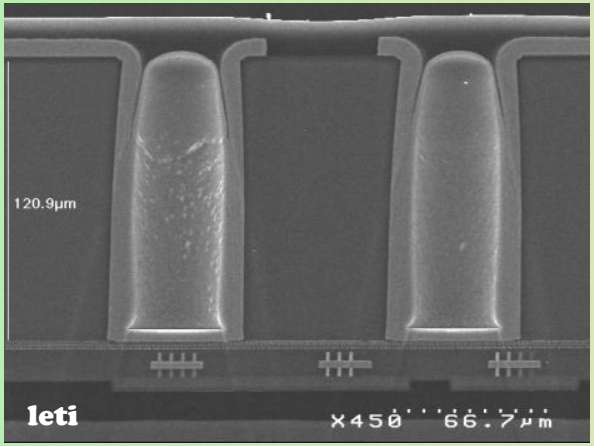
TSV DRM & schematic

- Wafer size : **200 mm**
- Wafer thickness : **50- 200 µm**
- TSV type : **via last / Cu liner**
- TSV diameter : **40 - 80 µm**
- Minimum pitch : **2 X diameter**
- Aspect Ratio (AR) : **from 1:1 to 1:5**



TSV morphological & electrical results

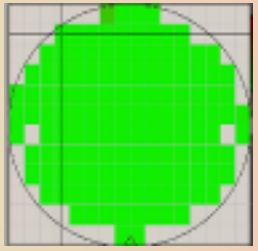
TSV-last AR 2:1

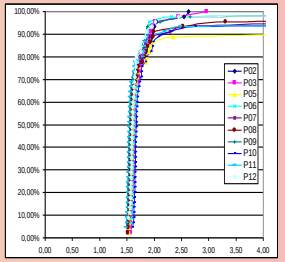


TSV characteristics

TSV geometry	R (mΩ)	C (pF)	Elec. Yield	Insul. (MΩ)	I_{leak} (A)
$TSV_{60/120}$	19.1	0.82	100 %	> 100	$1.3\ 10^{-9}$ **@ 10V** $3.1\ 10^{-9}$ **@ 50V**

Electrical tests results

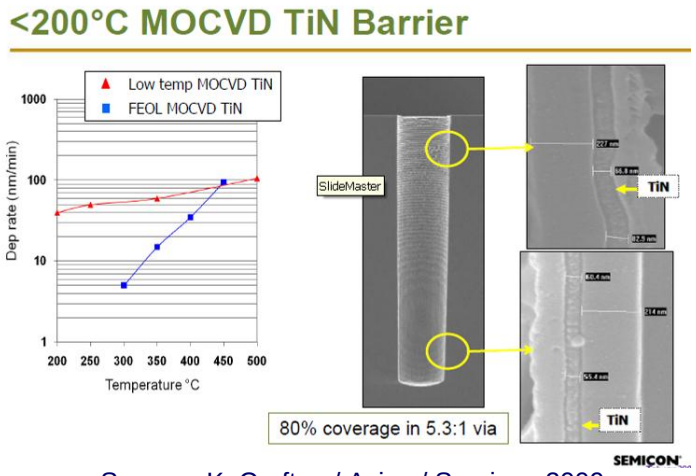




VIAS LAST / MEDIUM DENSITY ISOLATION/METALLIZATION

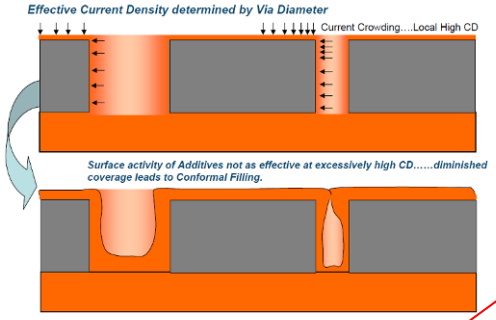
Isolation and Metallization : due to temporary bonding technique use of low temperature processes (< 250°C / < 200 °C) is required

- Isolation dielectric : Low temperature CVD SiON with high conformity deposition (~50%)

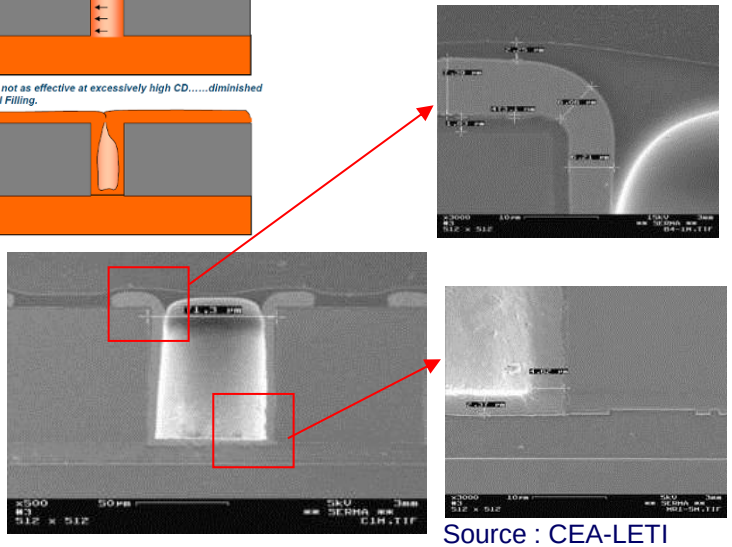


Source : K. Crofton / Aviza / Semicon 2009

- Barrier / seed layer deposition :
  - PVD ➔ AR <= 2:1
  - MOCVD Ti/Cu deposition ➔ AR > 2:1



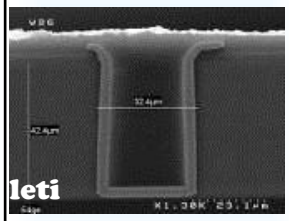
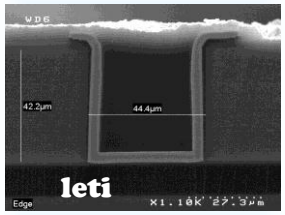
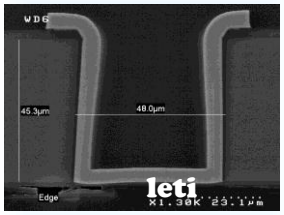
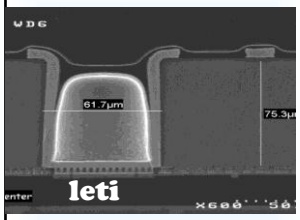
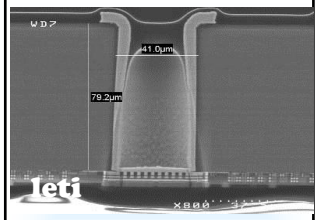
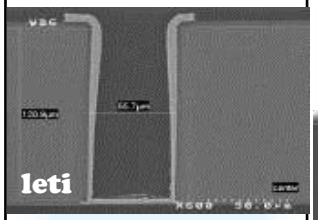
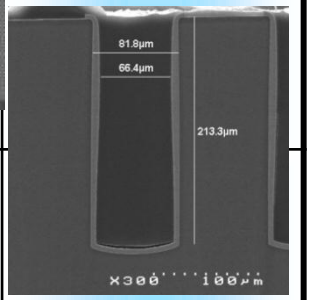
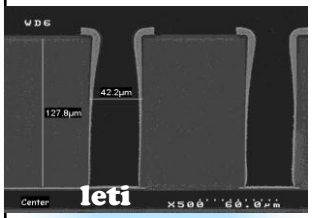
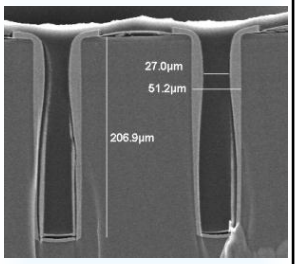
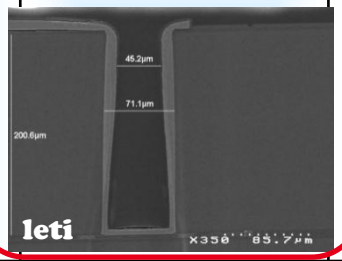
Source : Dow



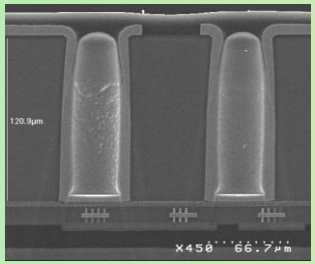
Source : CEA-LETI

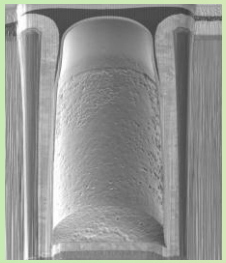
- Electroplating
  - Cu liner or Cu filling
  - Choice of electrolyte : 2 or 3 additives
  - DC or pulse current
  - Hydrodynamic conditions

TSV-LAST PORTFOLIO

TSV diameter	30 µm	40 µm	50 µm	60 µm	80 µm
AR 1:1 & 1.5:1					
AR 2:1	Not yet demonstrated		Available Not yet required		
AR 3:1	Not yet demonstrated		Available Not yet required		
AR 5:1	Available Not yet required		Not yet demonstrated		

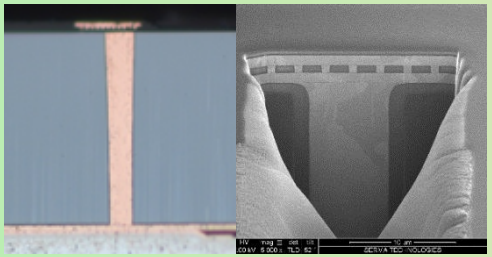
VERTICAL PASS-THROUGH CONNECTING TECHNOLOGY - CURRENT DEVELOPMENT





TSV Last : high reliability driven

- Increased Si thickness with High AR TSV -> 3 to 5
- TSV mineral passivation (harsh environment)
- TSV polymer filling



TSV mid : high density driven

- Increased Si thickness with High AR TSV -> 10 -> 15 -> 20
- Alternative technology AR20 (development 2015)

Temporary bonding

- Zone bond 200 & 300mm
- Low temperature (200°C)
- High temperature (400°C) ongoing development on disruptive technology

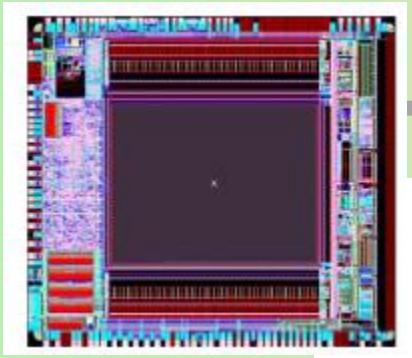
APPLICATION EXAMPLES
IMAGE SENSORS

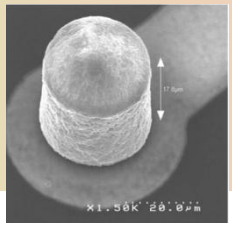
3D IMAGE SENSOR APPLICATIONS

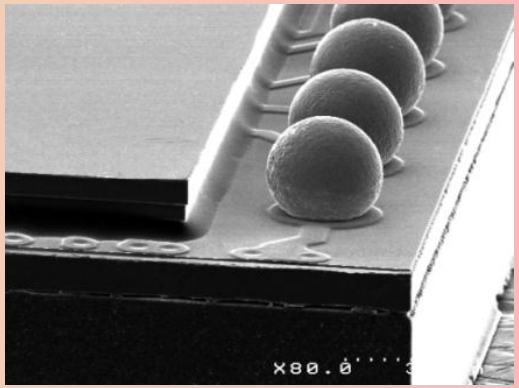
- **Visible light**
  - Cmos Image Sensors for consumers (mobile): CIS
- **X-rays / Elementary particles**
  - CERN: Medipix experiment
  - CERN: ATLAS experiment

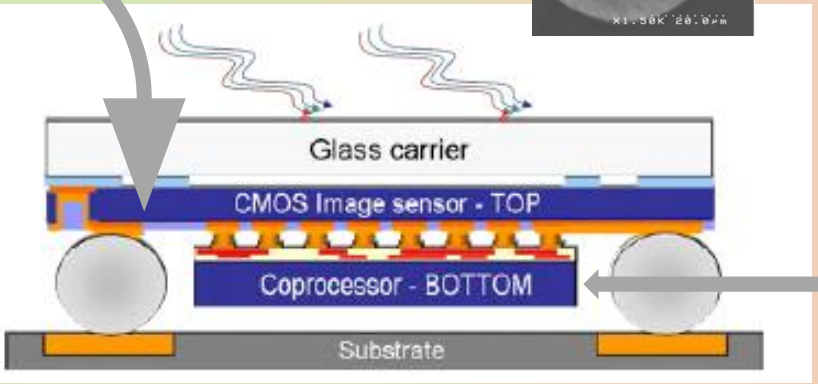
CMOS images sensor 3D demonstration (2012)

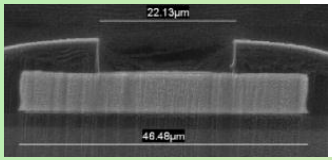
- The market is ready and 3D WLP supply chains exist
- 3D stack of 2 partitionned dies
- 65nm processor reported below a 130nm image sensor

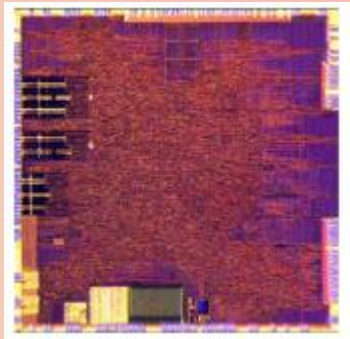


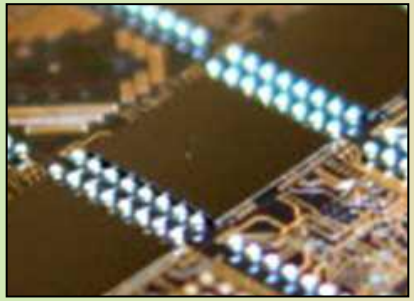












	CMOS	BEOL	I/O count	Dimensions
Image sensor	130 nm	3ML + AP	80	5.0x4.4 mm^2
Coprocessor	65 nm	7ML + AP	164	3.4x3.5 mm^2

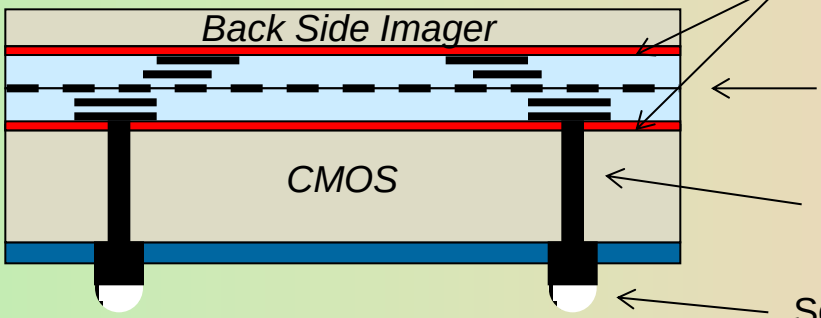
From, P. Coudrain et al. ECTC 2013

ANR 3D-IDEAS project - 2012

TOWARDS HIGH DENSITY 3D BSI IMAGERS

- Step 1 : ***2-layer 3D imager*** (Back Side imager stacked on CMOS)
  - Leti objective : demonstration in 2014-15, technology in production in 2016-2017

Collaboration with ST



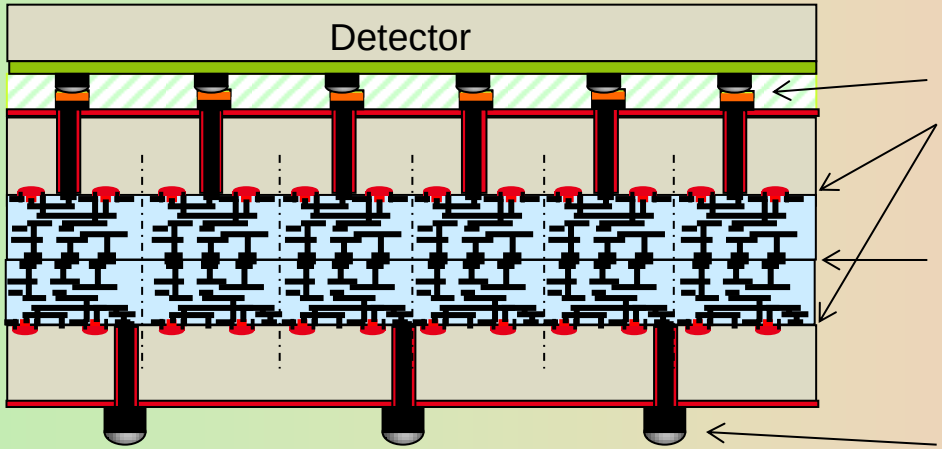
transistors

Hybrid Cu and SiO2, face-to-face, bonding
Pitch 5-10µm

TSV (10µmx80µm), pitch 40µm

Solder bumps, connection to board (or interposer)

- Step 2 : ***3-layer 3D imager*** : detector on 2 CMOS layers
  - Leti objective : demonstration in 2015-2016, technology in production in 2018-2019



Connection to detector, pitch 40µm

transistors

Hybrid Cu and SiO2, face-to-face,
bonding, Pitch 5-10µm

Solder bumps, connection to board,
interposer or 3D package

3D IMAGE SENSOR APPLICATIONS

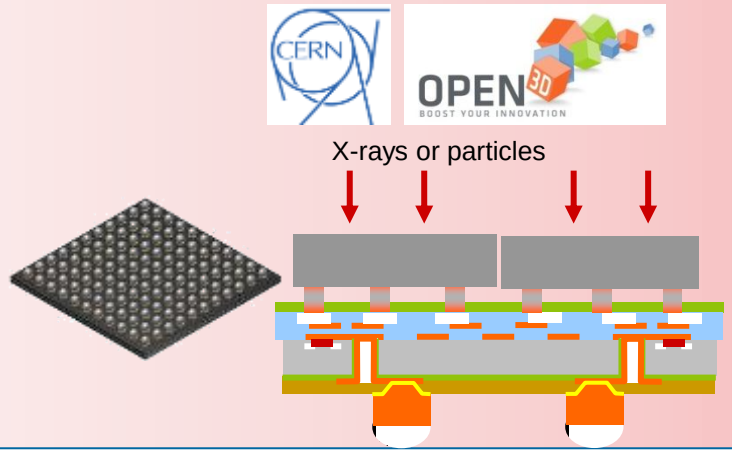
- **Visible light**
  - Cmos Image Sensors for consumers (mobile): CIS

- **X-rays / Elementary particles**
  - CERN: Medipix experiment
  - CERN: ATLAS experiment

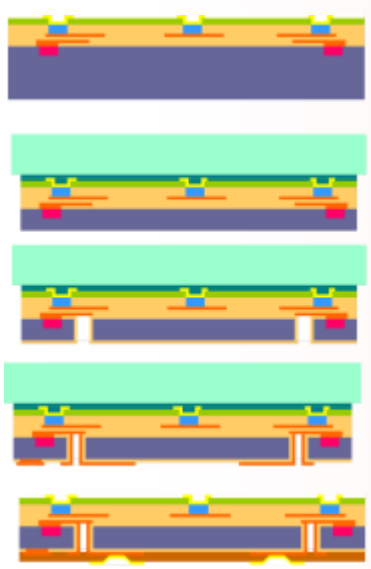
X-RAYS/PARTICLES DETECTOR: BUTTABLE DETECTORS ON ROIC

CERN – LETI project summary 2011 -2015

- Product : hybrid pixel detector for medical applications
- TSV-last made in Medipix3 - Medipix RX – timepix3 wafers (130nm)
- Suppression of lateral wire bonding
- Buttable sensors assembly: no dead zone between sensor

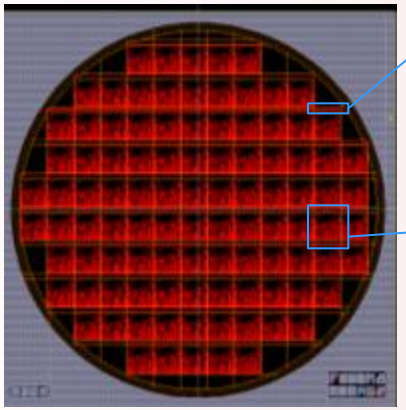


Medipix specifications



Process Flow

Design



Wafer view

Test structures

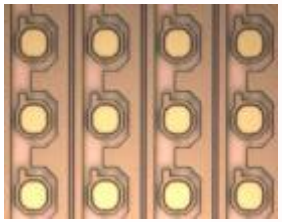
Single chip

- Wafer diameter: 200mm
- Wafer thickness: ~725um
- IC Technology: 130 nm / IBM
- Top Surface: Al + Nitride
- Chip size : 14100 x 17300 µm
- TSV per chip: ~100
- TSV aspect ratio :
  120:60 µm (MEDIPIX RX)
  50: 40 µm (timepix3)

TSV Medipix3/RX results – 2012-2015

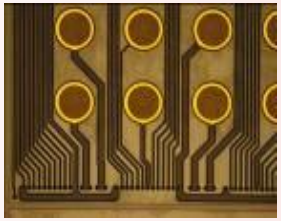
➔ 6 lots run at LETI

Technology

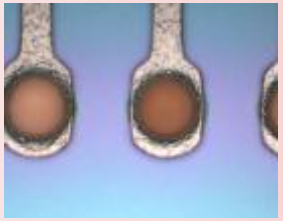


Medipix wafer after front side UBM

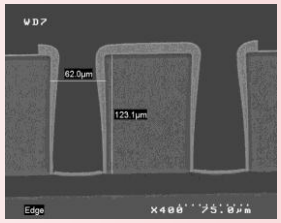
Back side UBM



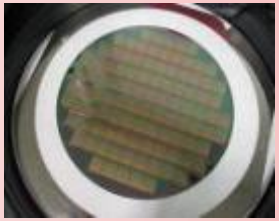
Accoustic image of the bonding interface



RDL Cu 7 µm



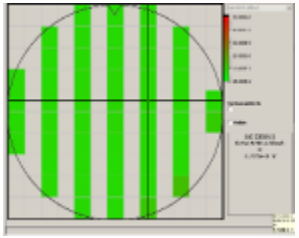
TSV
60µm
x120µm

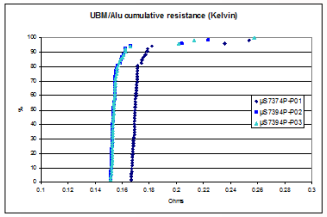


Thin wafer debonded on tape

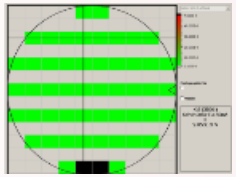
Electrical Tests

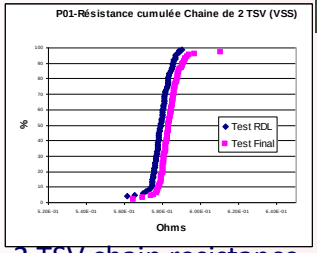
Contact UBM



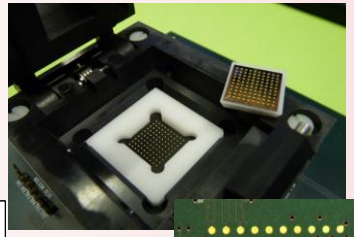


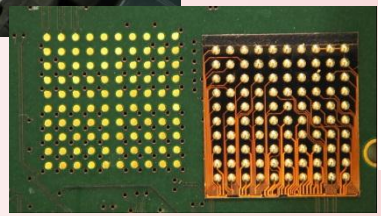
TSV:



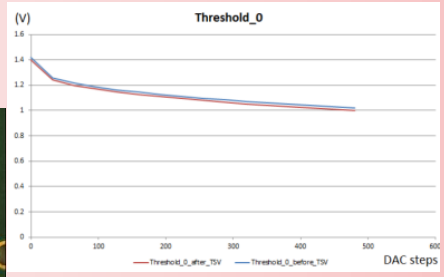


2 TSV chain resistance



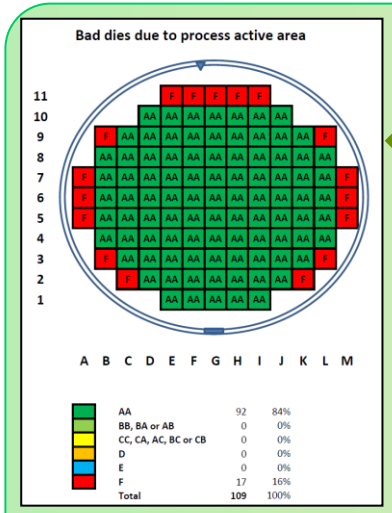


Functionnal tests on ASICS



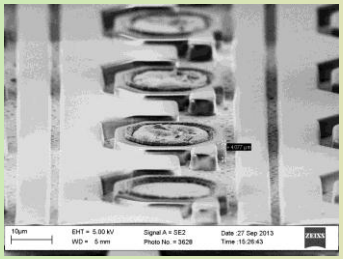
TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments
D. Henry(1), J. Alozy(2), A. Berthelot(1), R. Cuchet(1), C. Chantre(1), M. Campbell(2) ECTC 2013

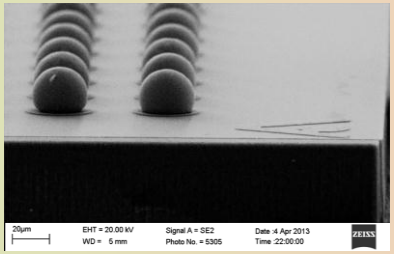
MEDIPIX3 FUNCTIONAL RESULTS (2013-2014)

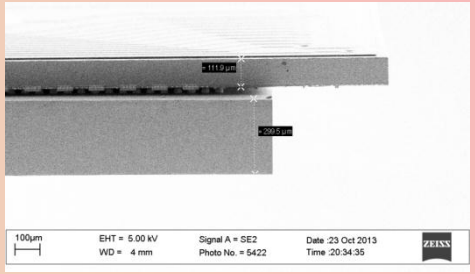


Using the same test program as Wafer probing, generating the same classification. (Readout interface is a Fitpix USB device)
2 Wafers tested chip by chip (1 day of measurement per wafer)
➔ **No yield loss due to TSV technology except on wafer edge due to process edge exclusion**

One TSV processed wafer was sent to ADVACAM company for :
-Dicing of thinned wafer and selection of “good” chip candidates
-Sn-Pb solder spheres were processed on Edgeless Sensor


Pixel pad on ROC


Sensor with Sn-Pb solder bumps
After reflow process

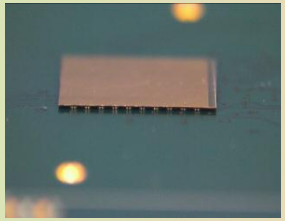

First Edgeless-TSV assembly
5 were provided to CERN in October 2013

SEM images courtesy of Advacam

BGA pads on the back side redistribution layer have been prepared with low temperature solder spheres

Assembly has been done manually for several chip and the obtained “BGA” components could be mounted using standard equipment but with some care due to its fragility

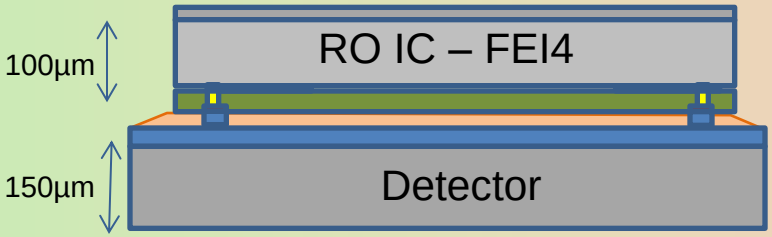
Courtesy of Jerome ALOZY

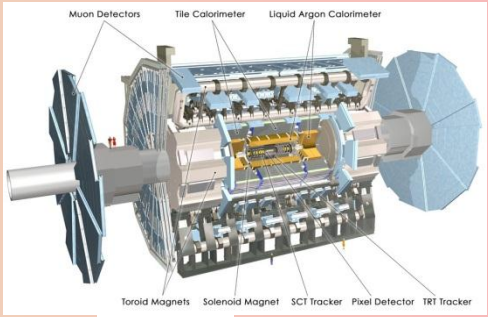


First image obtained with a TSV processed hybrid pixel detector (flat field corrected)

Particle detectors for ATLAS experiment (CERN)

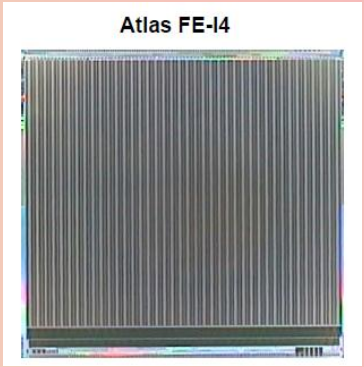
Atlas detector





CERN Glasgow university

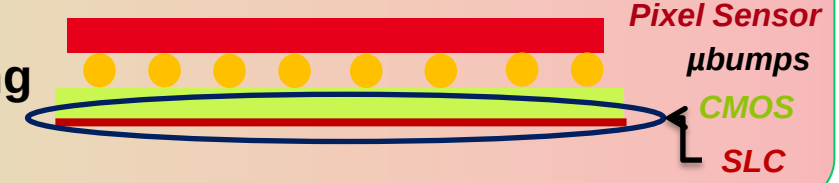
- **Particle detectors for ATLAS experiment (CERN)**
  - Realization of 60 µm fine pitch Cu pillars
  - Stress management of ultra large & thin ASIC Read-out circuits (20x20 mm2)



FEI4 size: 20 x 18.9 mm2

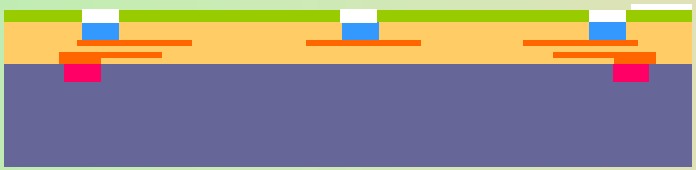
- **Develop an alternative wafer level back-side process, called Stress Layer Compensation (SLC), that compensates for the CTE mismatch of the ROIC CMOS front-side stack**

Stress compensation layer applied on thinned wafer backside

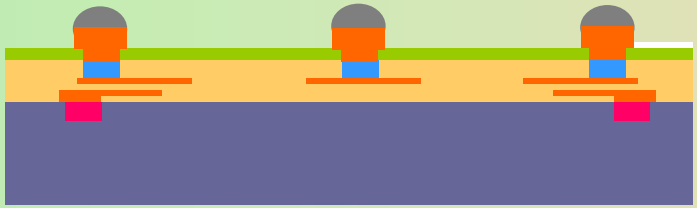


- **Compensation effect needs to be dynamically effective with temperature ranging from ambient to solder reflow (260° C)**

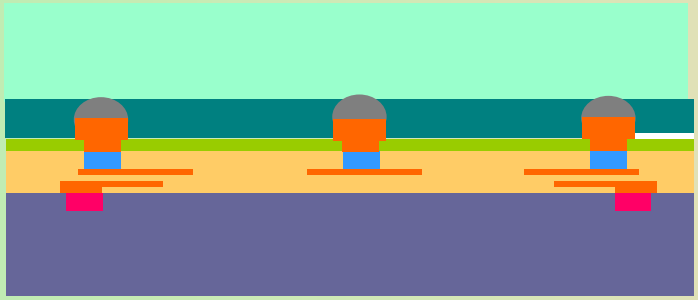
PROCESS FLOW FOR µBUMP FORMATION (FRONT SIDE) AND SLC (BACK SIDE) OF FEI4 CHIP



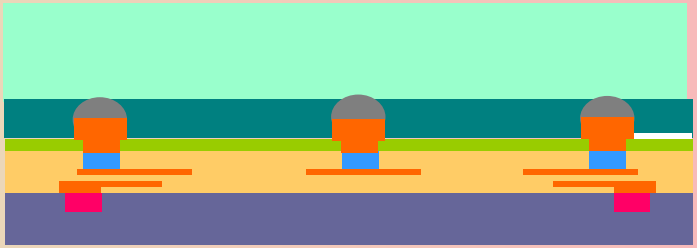
Incoming wafers



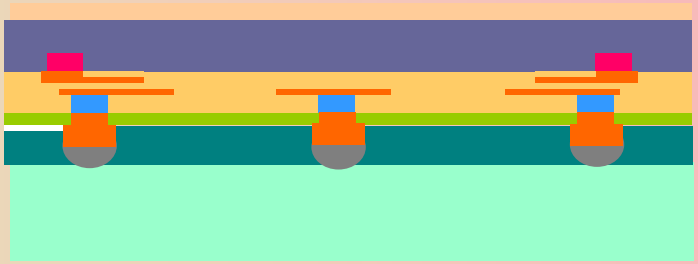
Front side µbumps



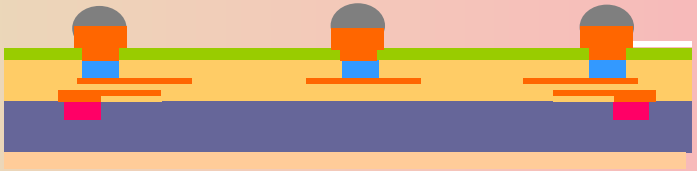
Temporary bonding



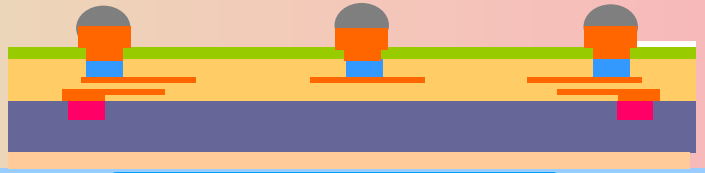
Thinning to 100µm



Stress compensation layer



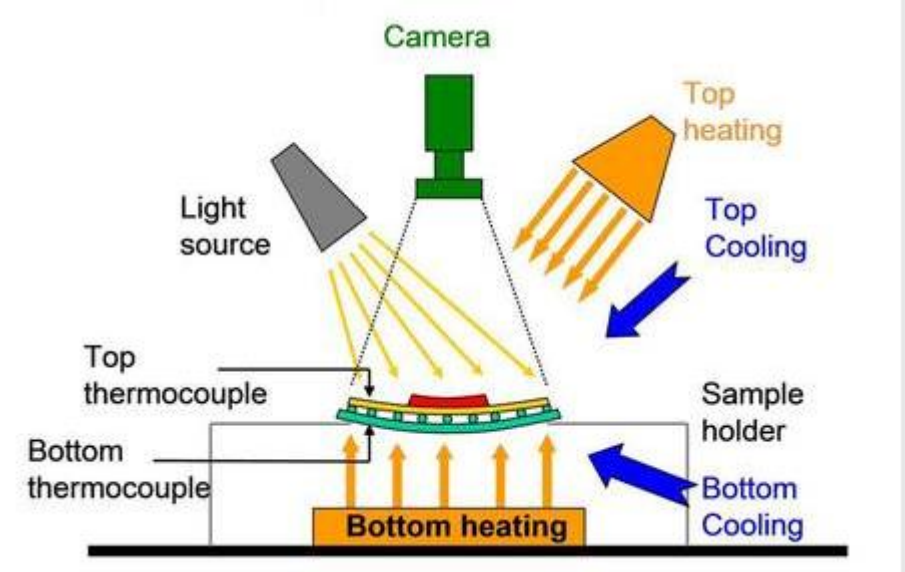
Debonding



Taping & delivering

TOPOGRAPHY AND DEFORMATION MEASUREMENT (T.D.M.) UNDER THERMO-MECHANICAL LOAD

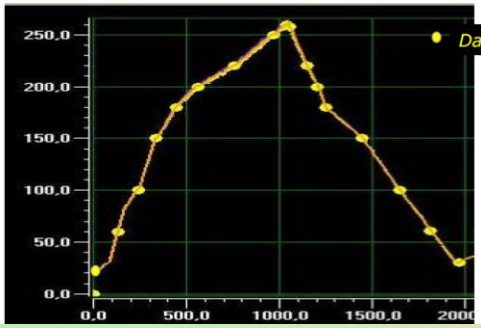
- Full-field/fast acquisition mode of the optical deformation of the sample dies under thermal load.
- Temperature of the sample is imposed with infrared heating on top and bottom sides of the samples.
- The out of plane resolution of the optics is ±3 µm and in-plane (x, y) detection ability is $dl/l = 5 \times 10^{-5}$.

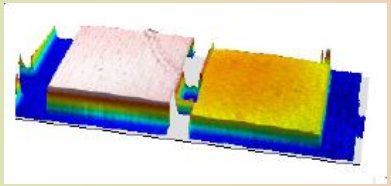


Thermal profile

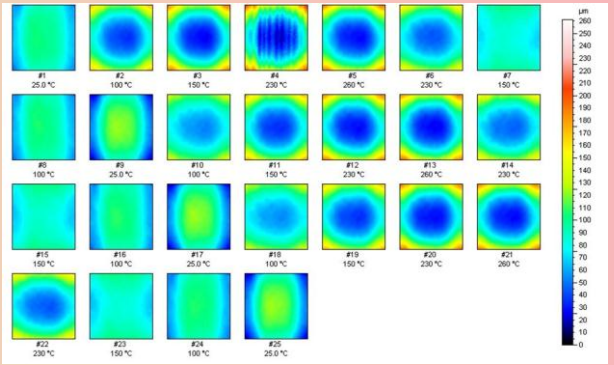
2 successive reflow profiles were lead. Each sample has undergone the same reflow profile (the chip where measured with 4 in the system).

The thermal profile was chosen to fit previous measurements conditions. But with TDM it is also possible to follow Jedec reflow (eg. with 3°C/s ramp-up).





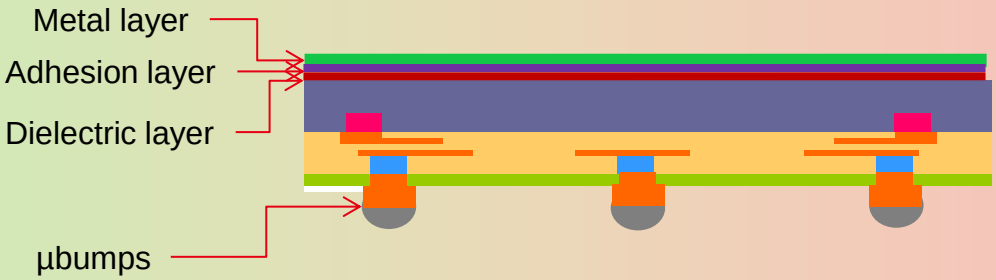
3D plot of the FE4 chip deformation at different temperatures



Profiles at subsequent temperature step

STRESS COMPENSATION LAYER RESULTS ON FEI4 CHIP

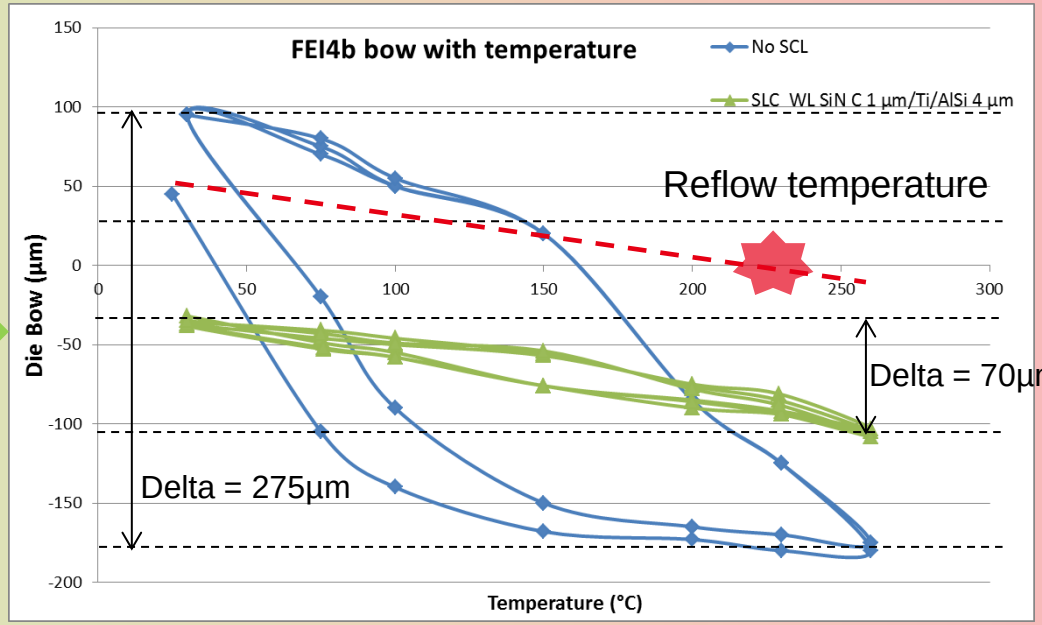
Wafer level technology modules processed on FEI4 ROIC wafers



FEI4b deformation during temperature excursion corresponding to solder reflow

Simulation with 4 µm of SiN = Ideal results

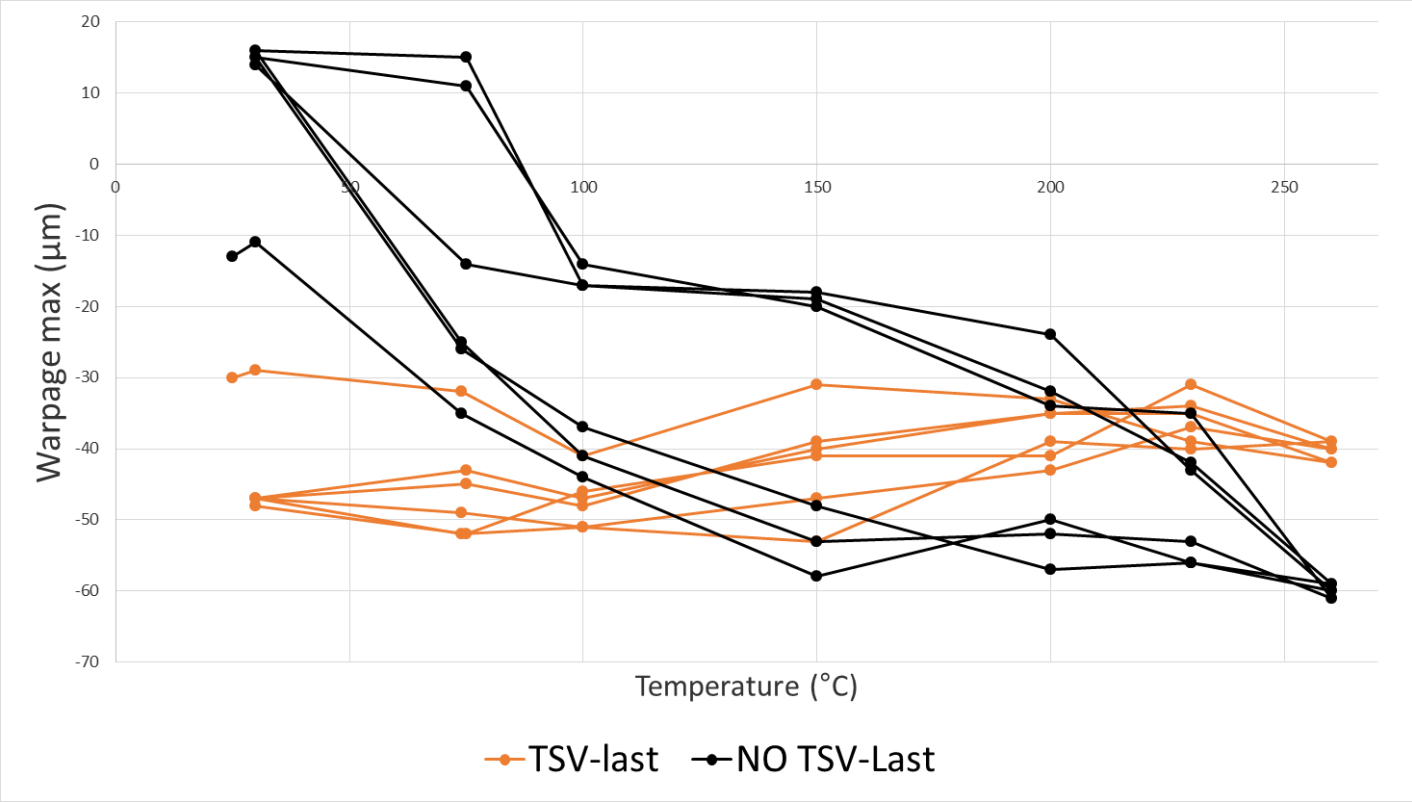
Last and best results obtained SiN C 1µm/AlSi 4 µm



➔ Already 4X reduction of bow amplitude with SCL

TSV-LAST TECHNOLOGY ON 120µM THIN MEDIPIX RX CHIP

Medipix RX has the same front side thick BEOL than FEI4
Note : medipix die is smaller size (14x18 mm) than fei4 (20x20 mm)



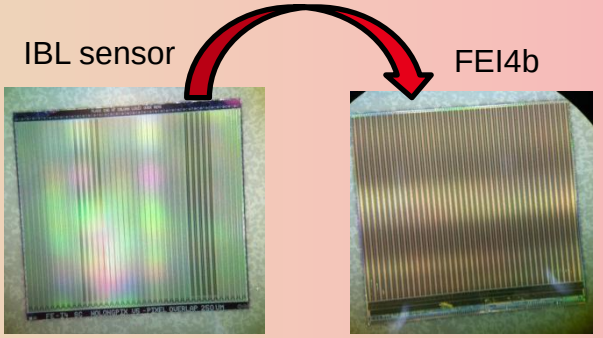
➔ TSV-last techno acts as a very promising stress compensation layer

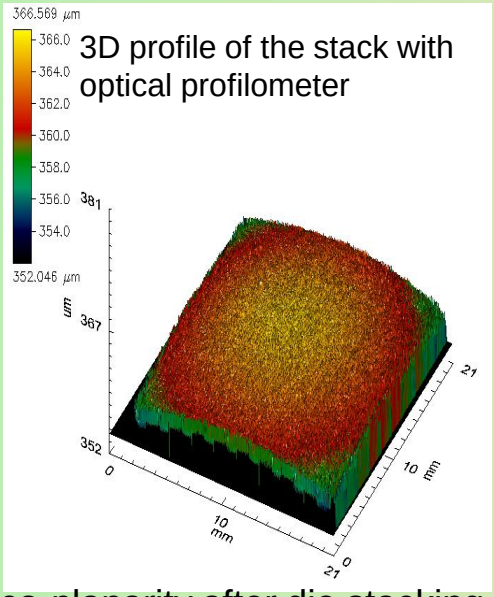
(Offset value still an issue which needs to be worked out working on dielectric materials or other compressive layer)

FEI4/SENSOR CHIP FLIP CHIP STACKING AT LETI

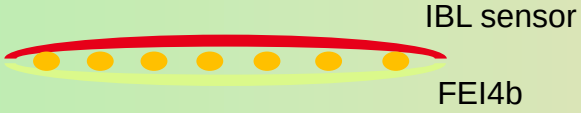
- FEI4 functional chips with micro-bumps, thickness = 280 µm
- IBL functional chips with UBM Ti/Ni/Ag pads, thickness = 280 µm

Flip chip technology:
- Flux dipping of bottom die (FEI4)
- Pick and Place with high precision automated equipment (SET150)
- In Situ soldering by thermo-compression

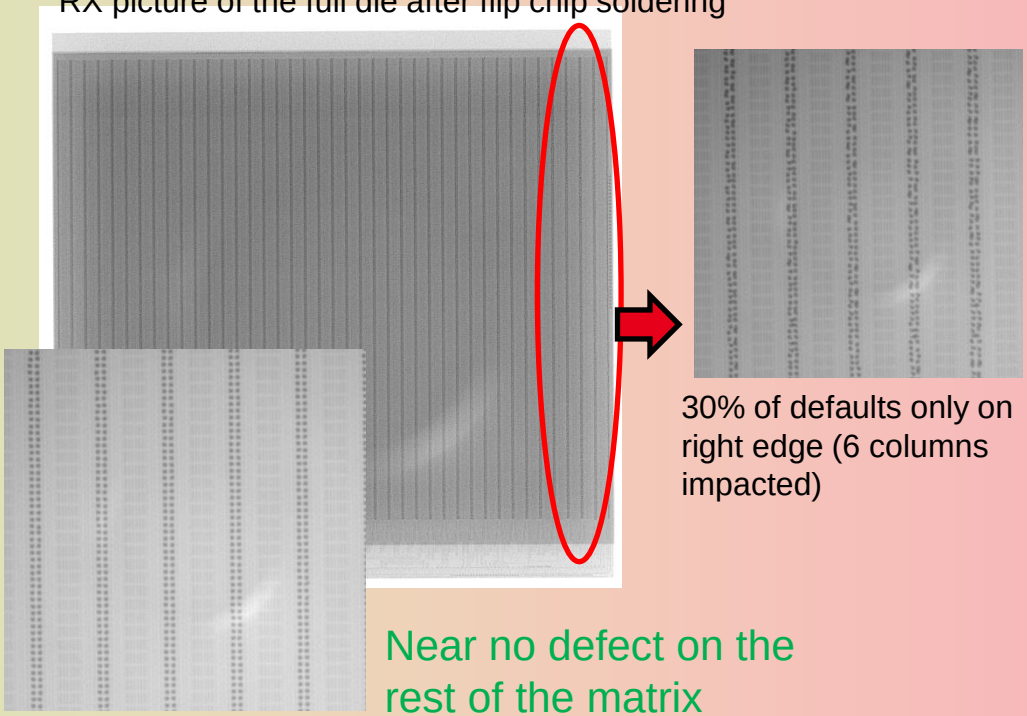




co-planarity after die stacking ~ 6 µm



RX picture of the full die after flip chip soldering



30% of defaults only on right edge (6 columns impacted)

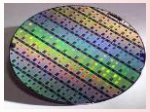
Near no defect on the rest of the matrix

➔ Functional test are ongoing at LAL

OPEN3D PLATFORM PARTNERING WITH CMP: WORK FLOW OFFER

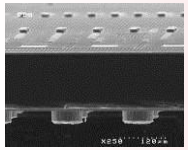
Wafer fabrication in foundry

Wafer reception at LETI

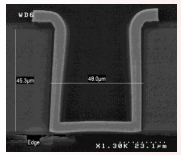


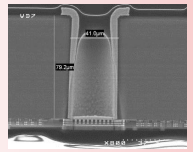
LETI
3D Technology implementation

Interconnections



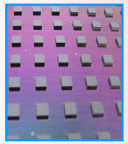
TSV



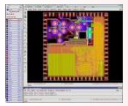


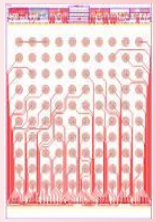
Metallization

Components stacking



Design & Layout & DRC

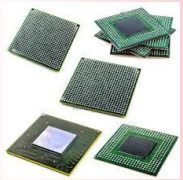




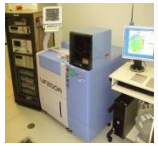
CMP MPW wafer service

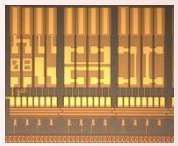
- Customer interface
- 3D modules identification
- order form

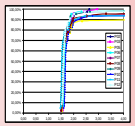
Dicing & Packaging

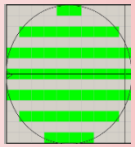


3D Electrical Tests









- **Continuous developments in 3D technology field involve:**
  - High density and fine pitch interconnections
  - Low temperature interco
  - Reliability for critical applications (automotive, aerospace, medical)
  - Thermo-mechanical constraints, stress management

- **Image sensor has long been a key driver for 3D and will continue to be, we see a lot of demands in this domain of applications**

- **CEA-Leti can provide a broad and mature 3D technology portfolio:**
  - µbumping and solder interface CMOS post-processing
  - Flip chip stacking D2D and D2W
  - TSV-last
  - MPW is now open for 3D technologies provided by Leti