Control Loop Design for Two-Stage DC–DC Converters With Low Voltage/High Current Output

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***Abstract*—This paper presents a general analysis framework for control loop design of two-stage converters. The results yield a thorough explanation of various loop design approaches. A three-loop method to extend the system bandwidth is proposed. The new control design algorithm is applied to a 48 V/3.3 V two-stage converter. Experiments verify the effectiveness of the control loop design approach.**

***Index Terms*—Control loop, dc–dc converter, multi-loop method, two-stage converter.**

I. Introduction

TWO-STAGE dc–dc converter topologies have recently begun to receive interest in high input voltage, low voltage/high current output dc–dc conversion [1]–[9]. In general, the two-stage topologies [1]–[6] for these applications have a buck converter as the first stage, which regulates output voltage. The second converter is an isolated converter, which operates with 50% duty cycle like a "dc transformer" to step down the voltage, as Fig. 1 shows. The second stage converter can be either a forward, push-pull, half-bridge, or full-bridge converter (as shown in Fig. 2).

These topologies have several benefits: Secondary synchronous rectification (SR) can be optimized. That is, since transformer secondary voltage is minimized, SRs with low $R_{\rm dson}$ can be used to improve the efficiency [1]–[7]. Thus, secondary side leakage induced oscillations [10] are alleviated as a result of minimized SR voltage stress. Also, the efficiency of the isolated converter can be improved with use of low $R_{\rm dson}$ transformer switches since transformer primary voltage is reduced and regulated as constant. Furthermore, with transformer winding voltage, a simple and high efficiency self-driven SR can also be implemented [1]–[7]. Although the buck stage adds in extra losses, the overall efficiency could still be higher than its single-stage counterpart [1]. Additionally, the main inductor L_1 on high voltage side has less ripple current and associated ac losses. So it is more feasible to design a small L_1 to carry a bi-directional current, allowing ZVS for buck switches to reduce the switching losses. Also, housekeeping power supply can be taken directly from the transformer since transformer voltage is regulated.

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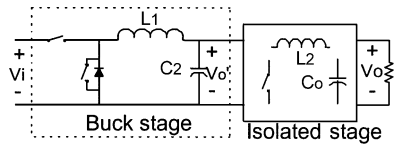

Fig. 1. Two-stage dc–dc converter.

However, two-stage converters have associated disadvantages too. Besides the extra cost, space, and losses brought by the additional switches, control design becomes more difficult. Unlike cascaded converters where the control loops are implemented in each converter separately, a two-stage converter typically attempts to regulate voltage with one PWM chip. The two stages are viewed as one system. Therefore, the pole-characteristic (Appendix I) of a two-stage converter is ideally modeled as a fourth-order system with two system resonances. As a result, the overall system bandwidth is usually kept conservatively low to assure no interaction with the resonant poles. Such a design significantly limits the transient response and degrades the dynamic regulation. It is worth mentioning that there is also an interesting cascaded solution where a buck stage is followed by the asymmetrical half-bridge converter [5]. In this approach both stages have their own feedback loops taken from V_o' and V_o, respectively, which allows wide bandwidth design while maintaining efficient synchronous rectification because of no dead-time operation of asymmetrical half-bridge converter. However, this paper does not consider this special class of converters.

There has been significant research on multi-loop control methods to increase the system bandwidth for conventional single-stage converters [11]–[15]. However, they are not directly applicable to two-stage converters. In fact, there has been little published work on high performance control loop design for two-stage converters to date until recently. Some nonlinear multi-loop control algorithms have been proposed [16]–[18] for general classes of power converters modeled by fourth order system. These methods rely on differential geometry, and therefore have not seen widespread applications [16], [17]. The control design is still a problem that impedes the application of two-stage topologies in fast transient dc–dc conversion, and this is a topic explained in the most recent work [19], [20]. Specifically, [19] and [20] suggested that including inner current loop feedback significantly extends the outer voltage loop gain crossover frequency higher than conventional approaches. This paper will identify several open issues in the implementation of linear control algorithms for two-stage converters. For example, how many ways are available to

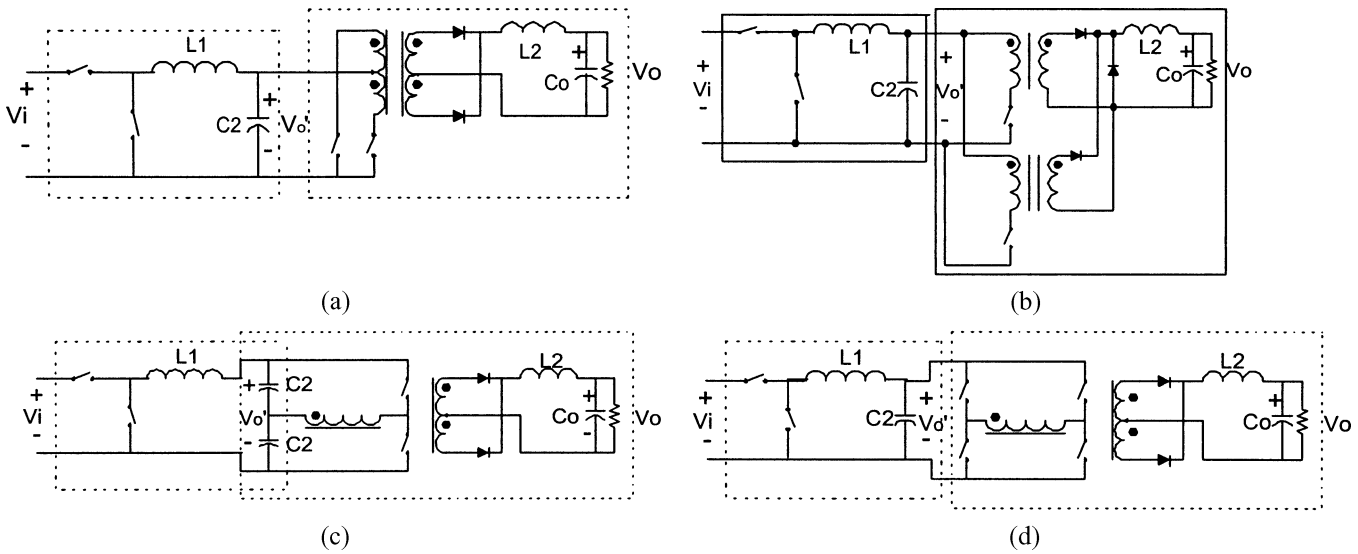

Fig. 2. Various two-stage topologies for low voltage and high current output applications: (a) buck + push-pull, (b) buck + forward, (c) buck + half-bridge, and (d) buck + full-bridge.

implement the control loops? What are the criteria for each control loop design? When should multi-loop control be used? How should each loop be implemented? This paper investigates control loop design strategies for two-stage converters and begins to answer the above questions.

The outline of this paper is as follows.

1) The small signal average model of two-stage topologies is first analyzed in Section II. New design recommendations for the power train are presented, which (for the first time) take into consideration control loop performance criteria.
2) Various control schemes for two-stage converters are examined and comparisons of their advantages and disadvantages are given in Section III. Such a discussion has been lacking in the literature and should be useful to the practicing engineer. Clear and simple guidance on how to design control loops for two-stage converters is presented.
3) In Section IV a simple two-loop design algorithm is presented. Its benefits and bandwidth limitations (below the first resonant frequency) are discussed.
4) In Section V, a main contribution of the paper is presented: A new, general three-loop design algorithm is proposed to facilitate the loop design of two-stage converters and to achieve a system bandwidth beyond the first resonant frequency. This high bandwidth had not yet been previously reported with the traditional control loop design. The proposed method uses the inner current loop (average current loop) with the compensator in the feedback path. The algorithm is applicable to most two-stage topologies.

Experimental verification of the proposed controllers is presented in Section V. Conclusions are given in Section VI. The Appendix presents necessary small signal transfer functions for reference. It also presents the technical justifications of the proposed control algorithms.

II. Modeling and Analysis of Two-Stage Topologies

Since two-stage converters regulate the output of the buck stage in PWM and convert a constant dc voltage to the output through an equivalent "dc transformer," they can be described with the same small signal model as Fig. 3 shows.

Since R'_{L2} has a strong damping effect for the two-stage topologies [2], it is neglected in the following analysis for the worst case scenario. Because the transformer operates with 50% duty cycle, the magnetizing inductance has limited effect on the small signal behavior [5] and is also neglected.

The resulting control-to-output transfer function (Appendix I) exhibits a fourth order system with two pairs of complex conjugate poles, which results in two system resonances. A zero caused by $R'_{\rm ESR}$ is assumed to be located between the two resonant frequencies. As a result, the phase shift extends up to -270° after the second resonance, as Fig. 4 shows. Since typical compensators normally add maximum phase up to 180°, the maximum achievable system bandwidth is restricted by the second resonant frequency (unless sophisticated compensators are used).

Analysis shows that the first resonant frequency (f_{r1}) is mainly determined by L_1, C_o and C_2, while the second resonant frequency (f_{r2}) is mainly determined by L_2, C_2 and C_o. The notch frequency $(f_{\rm notch})$ is mainly dependent on L_2 and C_o. So, from the aspect of power stage design, in order to help extend the closed-loop bandwidth, L_2, C_2 and C_o should be designed to move the second resonant frequency as high as possible [2]. Further, as shown later in this paper, the farther away that f_{r2} and $f_{\rm notch}$ are from f_{r1}, the larger the system bandwidth can be.

A typical two-stage converter should be designed so that $f_{r2} \geq 5f_{r1}$ and $f_{\rm notch} \geq 4f_{r1}$. This separation of frequencies between f_{r1} and f_{r2}, f_{r1} and $f_{\rm notch}$ is vital for high bandwidth control system design (as shown in Section V). Thus, we always assume in this paper that $f_{r2} \geq 5f_{r1}$ and $f_{\rm notch} \geq 4f_{r1}$. This leads to the power train design recommendation: L_2 should be designed as small as possible (limited by the least value required for suppressing the transient current overshooting). L_1 is designed to be larger than L_2, but it should not be too big. This keeps f_{r1} high enough and does not violate $f_{r2} \geq 5f_{r1}$ and $f_{\rm notch} \geq 4f_{r1}$. Although it is preferred that C_2 is bigger

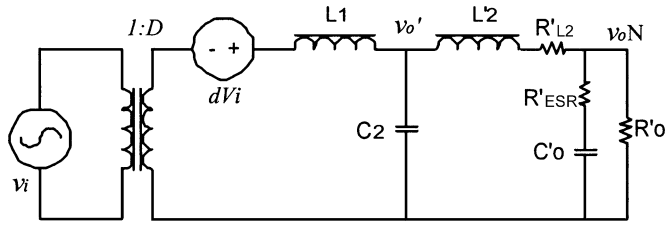

Fig. 3. Small signal equivalent model of two-stage topologies ($L_2' = L_2/N^2$, $C_o' = C_o/N^2$, $R_o' = R_oN^2$, $R_{ESR}' = R_{ESR}N^2$, $R_{L2}' = R_{L2}N^2$).

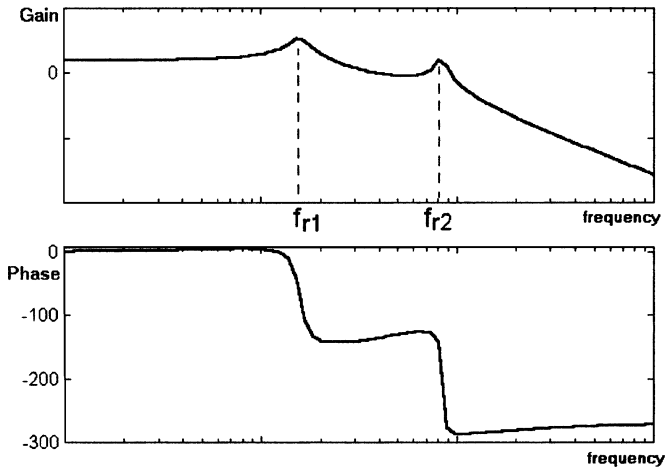

Fig. 4. Open-loop transfer functions v_o/d.

than C_o', C_2 should be also kept as small as possible to keep f_{r1} high. Section V presents mathematical formulas that specifically relate f_{r1}, f_{r2} and f_{notch} to L_1, L_2, C_2, and C_o'.

III. General Control Loop Design for the Two-Stage Converters

This section begins with an overview of the different possible control approaches. The advantages and disadvantages of each control approach are discussed. Technical justification of the limitations in each control method is also presented. These summaries and discussions should prove useful to the practicing engineer when deciding which control approach to adopt for their two-stage converter, and have been lacking in the literature.

Two possible control approaches are realistic, although numerous others are theoretically possible. First, there is a two-voltage-loop approach, as shown in Fig. 6(c). This approach is simple and regulates the transformer voltage as well as the output voltage. Because constant transformer voltage is maintained, housekeeping is simple since it can be taken directly from the transformer. Perhaps more importantly, though, is that there is no deadtime and self-driven SR can be efficiently implemented on the secondary side. A simple step-by-step control design algorithm is given for the two-voltage-loop approach in Section IV.

However, the two-voltage-loop control scheme has bandwidth limited by the first resonant frequency. Hence, this control design may not be suitable for applications that require fast transient response. An alternate control approach that adds an I_{L1} current loop is presented in Section V. This scheme eliminates the effects of the first resonant pole, and as a result, has wider bandwidth that is no longer limited by the first resonant frequency. Because the approach requires three loops, as shown in Fig. 6(e), it becomes more complicated to theoretically understand. However, it is still simple for the practicing engineer to implement: a step-by-step design procedure is presented, and is (we believe) only a little more difficult to implement than the two-loop approach. The benefits of the approach are that it maintains all the advantages of the two-voltage-loop control scheme but has faster response speed due to the wide bandwidth (see Tables I and II).

A. General Discussions of Control Schemes

Since there are four state variables in the two-stage converter, control loops can generally be constructed with one loop, two loops or three loops according to the specific requirements as Fig. 6(a)–(e) shows. However, the features of these approaches have not been thoroughly investigated. (Note that this paper only discusses average current feedback. Peak current control will be investigated in future papers.)

Table III summarizes the advantages and disadvantages of various control loop approaches. Technical explanations of the conclusions given in Table III are given below.

B. Discussions on Control Schemes in Fig. 6

1) Control Schemes Without V_o' Loop [Fig. 6(a) and (b)]: These approaches are less desirable since a primary advantage of two-stage converters is that the transformer voltage is regulated. Without constant V_o', housekeeping cannot be taken directly from the transformer and there is deadtime. This causes a drop in efficiency if direct self-driven SR is utilized.

2) Two Voltage Loops, Fig. 6(c): Since V_o' is kept constant, the transformer voltage can be directly taken to drive the synchronous rectifiers and provide housekeeping power supply. This is a reasonable approach, but it is difficult to extend loop gain crossover frequencies (of either voltage loop) beyond f_{r1}. This is easily understood for conventional (PI, lag, or K-factor controllers), but is also true for even more sophisticated controllers (PI+lead, lag-lead, etc.).

Traditional PI, lag or K-factor controllers: These controllers always have phase angle less than zero. Since the first system resonance at $G_{P1}G_{P2}$ causes an abrupt phase roll-off down to -180° (see Figs. 4 and 5), in order for the phase margin to be sufficient, the crossover frequency of the two loop gains must be less than f_{r1} or else the system is not stable. In fact, to assure stability from possible modeling inaccuracies it is common that the crossover frequency of each of the voltage loops be smaller than $0.1f_{r1} \sim 0.3f_{r1}$. Despite this limitation, the two-voltage loop approach with these conventional controllers is still a reasonable approach, especially when speed of response (bandwidth) is not vital. Their benefit is design simplicity.

3) Two Voltage Loops + i_{L2} Loop, Fig. 6(d): For this approach, the V_o' loop must be designed in the same way as in the preceding scheme. The typical resulting $v_{o'r}$-to-i_{L2} open-loop transfer function (with V_o' loop closed) is shown in Fig. 7. From Fig. 7, it can be found that the phase quickly drops to -180° at f_{r1} and -360° at f_{r2}. Hence, for the similar reasons as mentioned before for the two voltage loop control method, conventional compensators remain unable to add sufficient phase

TABLE I
DEFINITIONS OF THE SYMBOLS AND VARIABLES IN FIG. 3 AND SUBSEQUENT SECTIONS

L'_2	L_2 reflected to the primary side	C'_o	C_o reflected to the primary side
R'_{L2}	R_{L2} reflected to the primary side	R_{L2}	The total series resistance of the secondary side windings and output inductor
R'_{ESR}	R_{ESR} reflected to the primary side	R_{ESR}	The equivalent series resistance of the output capacitor
R'_o	R_o reflected to the primary side	N	Turns ratio of the transformer

TABLE II
DEFINITIONS OF THE TRANSFER FUNCTIONS AND SYMBOLS

G_P	d-to-v_o transfer function	G_{P4}	i_{L2}-to-v_o transfer function
G_{P1}	d-to-i_{L1} transfer function	G_{CVo},$G_{CVo'}$,G_{CIL1},G_{CIL2}	Compensators of V_o loop, V_o' loop, i_{L1} loop, i_{L2} loop
G_{P2}	i_{L1}-to-v_o' transfer function	K_{Vo}, $K_{Vo'}$,K_{IL1}, K_{IL2}	Scaling factors of v_o, v'_o, i_{L1} and i_{L2}
G_{P3}	v_o'-to-i_{L2} transfer function	T_X	Loop gain of x loop
H_X	Closed-loop transfer function of x loop	Φ_{mx}	Phase margin of loop gain T_X

TABLE III
COMPARISON OF THE ADVANTAGES AND DISADVANTAGES OF VARIOUS LOOP IMPLEMENTATIONS

	Advantages	Disadvantages
Single V_o voltage loop	The simplest design	Slow transient response, inefficient self-driven synchronous rectification, no simple house-keeping power supply
V_o loop + i_{L1} loop	Fast transient response	Inefficient self-driven synchronous rectification, No simple house-keeping power supply
V_o loop + V_o' loop	Self-driven synchronous rectification, Simple house-keeping power supply	Slow transient response
V_o loop + V_o' loop + i_{L2} loop	Self-driven synchronous rectification, Simple house-keeping power supply	Slow transient response, complicated design
V_o loop + V_o' loop + i_{L1} loop	Fast transient response, Self-driven synchronous rectification, Simple house-keeping power supply	Complicated design

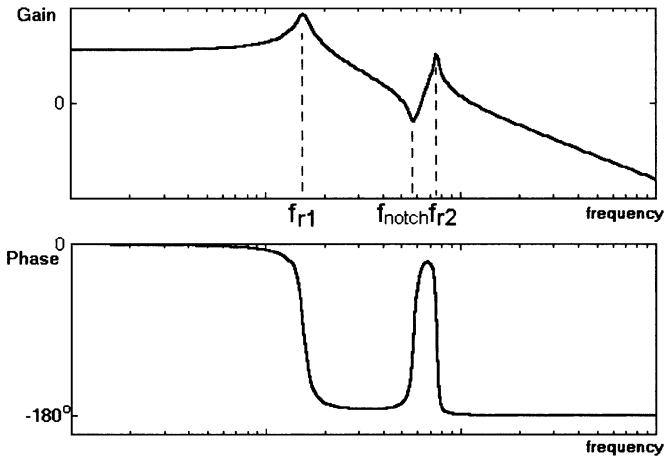

Fig. 5. Open-loop transfer functions v'_o/d.

at f_{r1} to allow the crossover frequency above f_{r1}. The achievable crossover frequency of the V_o loop, therefore, still remains below $0.1f_r$.

4) Two Voltage Loops + i_{L1} Loop, Fig. 6(e): Introducing an i_{L1} loop with the V'_o loop [Fig. 6(e)] can effectively eliminate the resonance at f_{r1}. If the inner current loop can be designed to satisfy certain loop gain conditions, the crossover frequency of the outer voltage loop can be extended above the resonant frequency f_{r1}. This is due to the elimination of the first system resonance in the inner closed-loop transfer function. Technical explanation of this fact is presented in Section V.

IV. TWO-VOLTAGE-LOOP CONTROL DESIGN

This section presents a specific two voltage loop control design algorithms for two-stage converters, as in Fig. 6(c). Technical justifications of the formulas are given in Appendix II. The below design algorithm gives the following.

1) Inner loop gain $T_{Vo'} = K_{Vo'}G_{CVo'}G_{P1}G_{P2}$ to have a phase margin of approximately 90° and a crossover frequency of $f_{CVo'} \approx 0.1f_{r1}$ at the maximum input voltage. A Type-1 controller is selected for $G_{CVo'}$ to guarantee V'_o is regulated.
2) Outer loop gain, $T_{Vo} = K_{Vo}G_{CVo}T_{Vo'}G_{P3}G_{P4}$, to have an arbitrary phase margin of $\phi_{\rm mvo}$ and a crossover frequency of $f_{CVo} = 0.1f_{r1} = f_{CVo'}$.

Proposed controller

Step1) Inner loop: Let $G_{CVo'} = A_1/s$, where $A_1 = \omega_{CVo'}/K_{Vo'}V_{i\max}$. $V_{i\max}$ is the maximum input voltage and $\omega_{CVo'} = 2\pi(0.1f_{r1})$.

Step2) Outer loop: Using the K-factor approach [21], specifically, let $G_{CVo} = A_2(s+\omega_z)/s(s+\omega_p)$. Suppose it is desired to have phase margin $\phi_{\rm mvo}$ ($\phi_{\rm mvo} > 45°$)

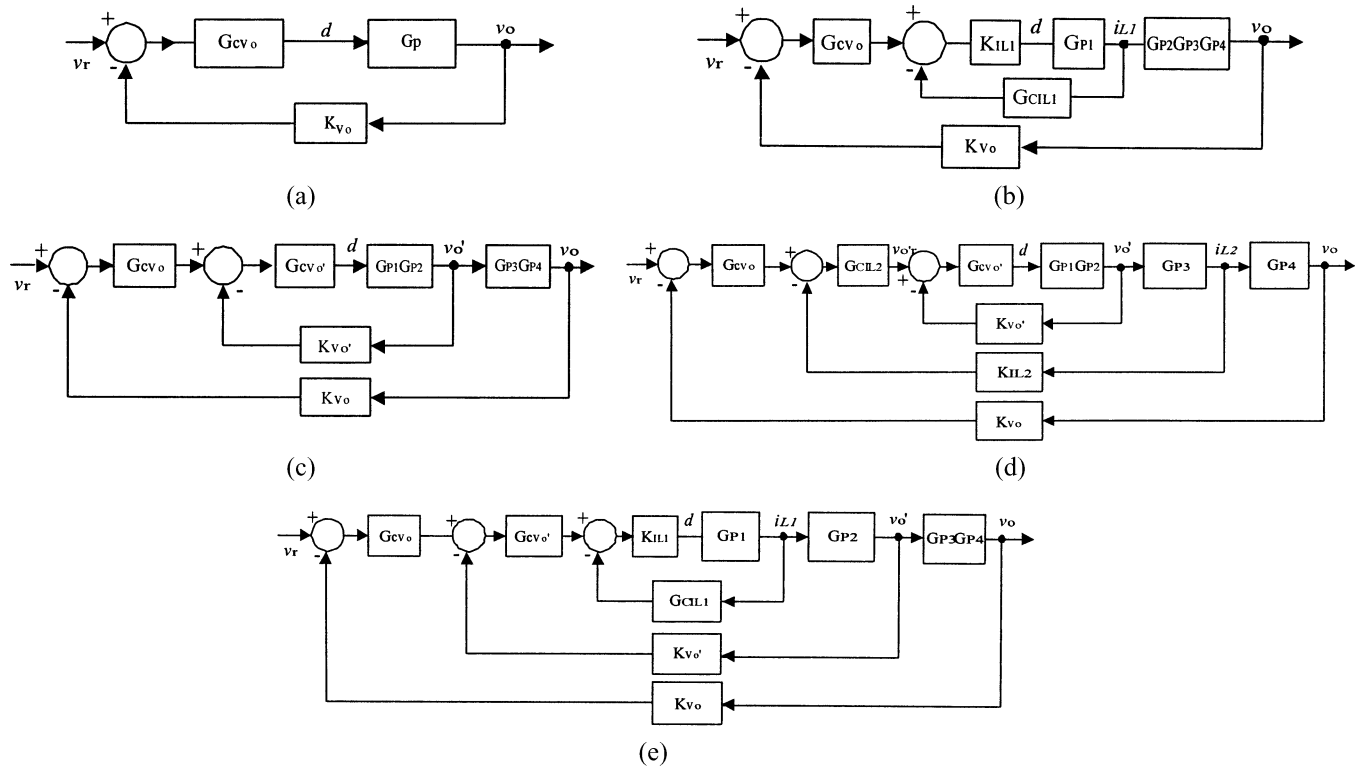

Fig. 6. Control schemes for two-stage converters: (a) single voltage loop control, (b) control structure of V_o voltage loop control + i_{L1} current loop, (c) control structure with two voltage loops, (d) control structure with two voltage loops and one i_{L2} loop, and (e) control structure with two voltage loops and one i_{L1} loop.

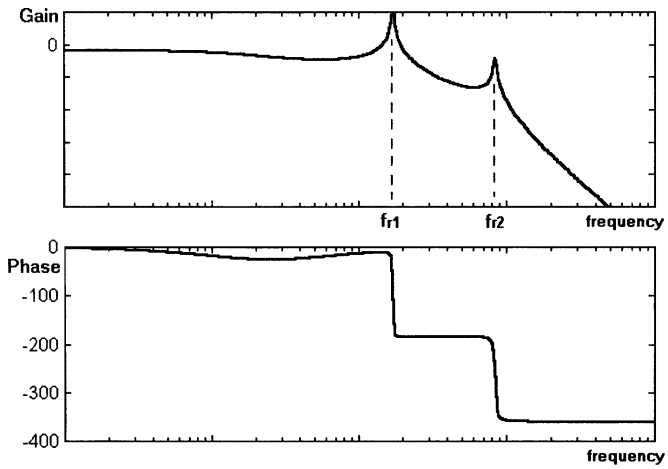

Fig. 7. Bode plot of i_{L2} open-loop transfer function with V_o' loop closed.

at the crossover frequency. Then parameters of G_{CVo} can be selected as

$$\omega_z = \frac{\omega_{CVo}}{M}, \quad \omega_p = M\omega_{CVo}, \quad A_2 = \frac{K_{vo'}\omega_{CVo}MN}{K_{vo}}$$

$$\text{where } M = \tan\left(25^\circ + \frac{\phi_{\text{mvo}}}{2}\right), \quad \omega_{CVo} = 2\pi(0.1f_{r1}).$$

The previous formulas should achieve a phase margin approximately equal to ϕ_{mvo}, perhaps a little larger. Furthermore, it is important to notice that all controller parameters depend on easily obtainable parameters that are known beforehand by the designer. In fact, the design of the proposed controllers does not require precise knowledge of capacitor and inductor values. Thus, the controller is robust to modeling errors and imprecise knowledge of resonant frequencies. As long as the crossover frequencies are sufficiently below ω_{r1}, the controllers will regulate properly. Of course, the disadvantage is its low outer voltage loop crossover frequency.

V. Three-Loop Design (Two Voltage Loops + I_{L1} Loop)

Obviously, the system resonance limits the bandwidth of the voltage loops to be less than ω_{r1} in the two-loop design procedure ($\omega_{CVo} \approx 0.1\omega_{r1}$) above. A general method to eliminate the effect of the first resonance on the outer voltage loop gain is proposed as below. (To our knowledge this is the first reported control method for two-stage converters that has this capability).

Section V-A presents the step-by-step design algorithm for the controllers. Formulas are presented to calculate the controller parameters (gains, locations of poles and zeros, etc.). Although the formulas are nonlinear, they are algebraic and in terms of known quantities. Hence, it is relatively simple for a designer to build the proposed linear three-loop controller. Technical justification/derivation of the formulas is quite complicated: details are presented in Appendix III, so as not to detract from the practicality of the result. However, Section V-B provides a discussion of the basic principles that the control design is based upon. Depending on the knowledge of the designer, these basic concepts can be utilized and adapted to design other three-loop controllers that do not exactly follow our proposed step-by-step design procedures.

A. Three-Loop Design Algorithm

Let f_{notch}, f_{r1}, and f_{r2} be as in Figs. 4 and 5, and define $\omega_x = 2\pi f_x$. In the following algorithm, let ω_{P2} the single real pole of the third-order plant G_{P2} (see Appendix I). The following controller design algorithm for Fig. 6(e) guarantees the following for all operating conditions.

1) i_{L1} current loop gain has phase margin greater than ϕ_{mIL1} and crossover frequency in the range of $\omega_{\text{CIL1}} > 5\omega_{r1}$. ($i_{L1}$ current loop gain $\equiv T_{\text{IL1}} = K_{\text{IL1}}G_{\text{CIL1}}G_{P1}$)
2) V_o' inner voltage loop gain has phase margin greater than $\phi_{\text{mvo}'}$. Its crossover frequency can be arbitrarily set provided that $\omega_{CVo'} \le 0.2\omega_{r1}$. ($V_o'$ inner voltage loop gain $\equiv T_{Vo'} = K_{Vo'}G_{CVo'}G_{P2}H_{IL1C}$; H_{IL1C} is i_{L1} closed-loop transfer function defined in Fig. 8.)
3) V_o outer voltage loop gain has phase margin greater than ϕ_{mvo}. Its crossover frequency can be arbitrarily set in the range of $\omega_{r1} < \omega_{CVo} < (0.3 \sim 0.4)\omega_{\text{notch}}$. ($V_o$ outer voltage loop gain $\equiv T_{Vo} = K_{Vo}G_{CVo}H_{Vo'C}G_{P3}G_{P4}$, $H_{Vo'C}$ is V_o' closed-loop transfer function defined in Fig. 9.)

The phase margins ϕ_{mIL1}, $\phi_{\text{mvo}'}$, and ϕ_{mvo} are selected by the designer as described as follows.

Further, in order to further simplify the engineering design, a few system frequencies are also presented for typical two-stage converter

$$\omega_{r1} \approx \frac{1}{\sqrt{L_1(C_2 + C_o')}}, \quad \omega_{r2} = \frac{1}{\sqrt{\frac{L_2'C_o'C_2}{(C_o'+C_2)}}}$$
$$\omega_{P2} \approx \frac{1}{R_o'(C_o' + C_2)}, \quad \omega_{notch} = \frac{1}{\sqrt{L_2'C_o'}}. \tag{1}$$

Proposed Controller

Step1) *Current loop compensator*, G_{CIL1}, *in* Fig. 6(e):

The current loop compensator is designed as $G_{CIL1} = K_1(s+\omega_{z1})/(s+\omega_{p1})$, where K_1, ω_{p1}, and ω_{z1} can be determined as

$$\omega_{p1} \approx \frac{1}{[R_{\text{omax}}'(C_2 + C_o')]} \tag{2}$$

$$K_1 \ge \frac{10\sqrt{2}R_{o\,\max}'}{K_{IL1}V_{i\,\min}\sqrt{1+\left(\frac{\omega_{z1}}{\omega_{p1}}\right)^2}} \tag{3}$$

$$\omega_{z1} = \frac{1.5\omega_{r1}[\omega_{p1} - 1.5\omega_{r1}\tan(-125^\circ + \phi_{mIL1})]}{\omega_{p1}\tan(-125^\circ + \phi_{mIL1}) + 1.5\omega_{r1}}$$
where phase margin $\phi_{mIL1} \ge 75^\circ$. (4)

Also, the switching current ripple attenuation [11] should be satisfied too

$$|G_{CIL1}(j2\pi f_s)| = K_1 \le \frac{V_s(1-D_{\max})}{\Delta I_{L1}}$$
(V_s is the oscillator ramp p – p voltage.
ΔI_{L1} is the ripple current). (5)

Step2) *Inner voltage loop compensator*, $G_{CVo'}$, in Fig. 6(e):

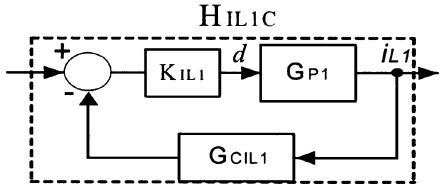

Fig. 8. Control block diagram for the i_{L1} current loop.

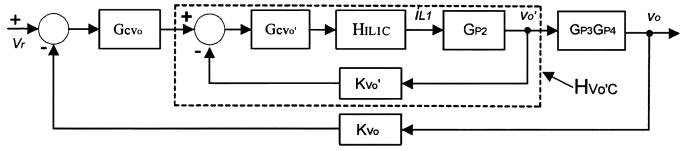

Fig. 9. Control block diagram for the inner voltage loop design.

The inner voltage loop compensator is designed as $G_{CVo'} = K_2(s+\omega_{z2})/s$, where K_2 and ω_{z2} are determined as

$$\omega_{z2} = \frac{\omega_{CVo'}}{\tan\left[-90^\circ + \phi_{\text{mvo}'} + \tan^{-1}\left(\frac{\omega_{CVo'}}{\omega_{z1}}\right)\right]} \tag{6}$$

$$K_2 \approx \frac{K_1(C_2 + C_o')\sqrt{\omega_{CVo'}^2 + \omega_{z1}^2}}{K_{Vo'}\sqrt{1+\left(\frac{\omega_{z2}}{\omega_{CVo'}}\right)^2}} \tag{7}$$

The phase margin should be selected as $\phi_{\text{mvo}'} \ge 90^\circ (< 180^\circ)$. To secure the second resonant peak is well below zero dB, $\omega_{CVo'} \le \omega_{z2}/3.21$ should also be satisfied.

Finally, sufficient switching ripple and noise attenuation should also be secured by checking if $|K_{IL1}K_{Vo'}G_{CVo'}| < (0.1 \sim 0.2)V_s/\Delta V_o'$ at f_s.

Step3) *Outer voltage loop compensator*, G_{CVo}, in Fig. 6(e):

The outer loop compensator is designed as $G_{CVo} = K_3(s+\omega_{z3})/s(s+\omega_{p3})$, where K_3, ω_{z3}, ω_{p3} are determined as

$$\omega_{z3} \approx \frac{\omega_{CVo}}{\tan[\phi_{\text{mvo}} + 35^\circ + \angle G_{\text{CIL1}}(j\omega_{CVo}) - \angle G_{CVo'}(j\omega_{CVo})]} \tag{8}$$

$$K_3 \approx \frac{K_1 N\sqrt{2}\omega_{CVo}(C_2 + C_o')\sqrt{\omega_{CVo}^2 + \omega_{z1}^2}}{K_2K_{Vo}\sqrt{1+\left(\frac{\omega_{z2}}{\omega_{CVo}}\right)^2}\sqrt{1+\left(\frac{\omega_{z3}}{\omega_{CVo}}\right)^2}} \tag{9}$$

$$\omega_{p3} = \omega_{CVo} \tag{10}$$

where ω_{CVo} is the desired crossover frequency set in the range, and ϕ_{mvo} is the phase margin of outer voltage loop.

Finally, sufficient switching ripple and noise attenuation should also be secured by checking if $|K_{Vo}K_{IL1}G_{CVo'}G_{CVo}| < (0.1 \sim 0.2)V_s/\Delta V_o$ at f_s.

Remark: It is important to note that all the controller formulas (2)–(10) are in terms of known quantities. Although the formulas are nonlinear, they are algebraic and easy to calculate. Once they are calculated, they uniquely specify all the required

controller gains, pole locations, and zero locations needed to implement the three linear controllers. Thus, it is now possible for a designer to extend the outer voltage loop gain crossover frequency beyond ω_{r1}. A disadvantage of the approach may be its reliance and sensitivity to the estimates of ω_{r1}, ω_{r2}, ω_{p2}, and ω_{notch}, as given in (1). It may also be possible, though, to measure these quantities directly, once the power circuit has been built.

B. General Explanation of Proposed Three-Loop Controller

Appendix III presents specific technical justification for the three-loop controllers presented in Section V-A previously. Although the derivation of the formulas is complicated, the general strategy for controller design can be understood easily by the practicing engineer.

1) i_{L1} *current loop*: The inner i_{L1} loop is first designed for Fig. 8. The single real pole of the third order plant G_{P2} is at ω_{P2}. Thus G_{P2} generally takes the form of $G_{P2} = K(s^2 + b_1 s + b_0)/((s + \omega_{P2})(s^2 + a_1 s + a_0))$ (see Appendix I), which has a pair of conjugate zeros and a pair of conjugate poles corresponding to $f_{\rm notch}$ and f_{r2}, respectively. The controller $G_{\rm CIL1}$ is selected as a first order, lag compensator with a pole at ω_{P1}. The gain and zero of $G_{\rm CIL1}$ are chosen so that: 1) there is sufficient phase margin and 2) the magnitude of loop gain $|K_{\rm IL1}G_{\rm CIL1}G_{P1}| \geq 10$ in the vicinity of ω_{r1}. The first condition guarantees the relative stability of the system. The second condition eliminates the resonance of G_{P1} at ω_{r1}. That is, selecting $G_{\rm CIL1}$ in this way allows the i_{L1} closed-loop transfer function $H_{\rm IL1C}$ in Fig. 8 to be approximated by $1/G_{\rm CIL1}$ in the range of $\omega_{P2} \leq \omega \leq \omega_{\rm notch}$, since $|H_{IL1C}| \equiv |K_{IL1}G_{P1}/(1 + K_{IL1}G_{P1}G_{CIL1})| \approx 1/|G_{CIL1}|$ and $\angle H_{IL1C} \approx -\angle G_{CIL1}$ when $|K_{\rm IL1}G_{\rm CIL1}G_{P1}| \geq 10$. Therefore, the first resonance at f_{r1} is effectively eliminated.

2) V_o' *loop*: The V_o' loop is now designed for Fig. 9. Using the above i_{L1} loop controller, the resulting V_o' open-loop transfer function $H_{\rm IL1C}G_{P2}$ can be approximated as $G_{P2}/G_{\rm CIL1}$ when $\omega_{P2} \leq \omega < \omega_{\rm notch}$. Notice that there is a pole-zero cancellation at ω_{P2}, since $G_{\rm CIL1}$ is selected to have a pole at the single pole location of G_{P2}. This produces a constant magnitude and improved phase angle of $H_{\rm IL1C}G_{P2}$ from ω_{P2} up to $\omega_{\rm notch}$, making the design of $G_{CVo'}$ simple. A Type-1 controller (integration) is used. From the above discussions on the i_{L1} current loop, the loop gain of the V_o' loop can be approximated as $T_{\rm Vo'} \approx K_{Vo'}G_{CVo'}G_{P2}/G_{\rm CIL1}$ in the frequency range of $\omega_{P2} \leq \omega < \omega_{\rm notch}$. And thus, controller $G_{CVo'}$ is selected so that there is high phase margin for this approximation of $T_{Vo'}$. The crossover frequency can be arbitrarily selected at any frequency between ω_{P2} and $\omega_{\rm notch}$. However, the algorithm simplifies greatly when $\omega_{CVo'} \leq 0.2\omega_{r1}$. Since the speed of the inner voltage loop is not the ultimate design goal (the speed of the outer loop is), the proposed controller forces $\omega_{CVo'} \leq 0.2\omega_{r1}$.

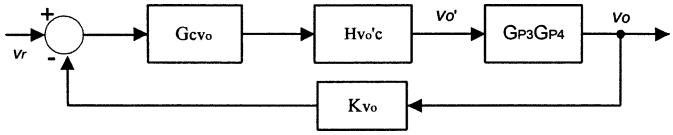

Fig. 10. Control block diagram for outer voltage loop design.

3) V_o *loop*: Using the above design procedure, the resulting V_o' closed-loop transfer function $H_{Vo'C}$ in Fig. 10 will not exhibit noticeable resonance at ω_{r1}, and therefore, neither will the resulting V_o open-loop transfer function $H_{Vo'C}G_{P3}G_{P4}$. However, $H_{Vo'C}G_{P3}G_{P4}$ still exhibits resonance at the second resonant frequency ω_{r2}. So the crossover frequency, ω_{CVo}, of the final V_o loop must be selected to be less than ω_{r2}, but it can be greater than ω_{r1}. The controller G_{CVo} should be a Type-1 controller so that steady state error is zero. The controller should also keep sufficient phase margin (greater than 45°). Finally, there should be sufficient roll-off in the loop gain at high frequencies to assure noise rejection above the switching frequency f_s.

VI. Design Example and Experimental Implementation

Following the step-by-step design procedure in Section V, three control loops are designed for a 36–75 V input, 3.3 V output two-stage converter with 30 A output current. The buck stage switches at 270 kHz with isolated stage switching at 135 kHz. Transformer turns ratio is 7.78. $L_1 = 13\ \mu H$, $L_2' = 2.5\ \mu H$, $C_2 = 4.67\ \mu f$, and $C_o = 185\ \mu f$. The relevant frequencies are found as: $f_{r1} = 13.9$ kHz, $f_{r2} = 74.5$ kHz, $f_{P1} = 1$ kHz, and $f_{\rm notch} = 56$ kHz, and are typical of commercial two-stage converters.

Using the step-by-step design procedures for the three-loop algorithm presented in Section V, three compensators are designed. Based on: $\phi_{\rm mIL1} = 75°$, $V_{i\,\rm min}/R'_{o\,\rm max} = 1.8$, $R'_{o\,\rm max} = 19.8\ \Omega$, and $\Delta i_{L1} = 1.5\ A$, $V_s = 2\ V$ for noise attenuation, the current loop compensator is designed by using (2)–(4). Choosing $f_{CVo'} = 2$ kHz, $\phi_{\rm mvo'} = 94°$, the inner voltage loop compensator is designed by using (6) and (7). Choosing $f_{CVo} = 20$ kHz, $\phi_{\rm mvo} = 45°$, $K_{Vo'} = 0.085$ the outer voltage loop compensator is designed by using and (8)–(10).

Three compensators are shown as follows (after minor adjustment for practical component values)

$$K_{IL1}G_{CIL1} = \frac{0.288(s + 1.7 \times 10^5)}{s + 6.28 \times 10^3} \tag{11}$$

$$K_{Vo'}G_{CVo'} = \frac{0.029(s + 8.9 \times 10^4)}{s} \tag{12}$$

$$K_{Vo}G_{CVo} = \frac{7.56 \times 10^5(s + 4.2 \times 10^4)}{s(s + 1.25 \times 10^5)}. \tag{13}$$

Then the compensators are implemented with experimental circuits. The loop gains are measured and compared with the simulated results in Figs. 11 and 12. The crossover frequency of the outer voltage loop is achieved at 20 kHz, which is greater

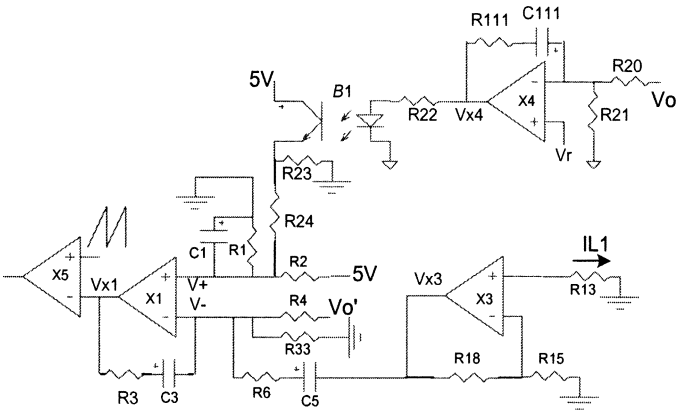

Fig. 11. Compensation circuits for the three loops.

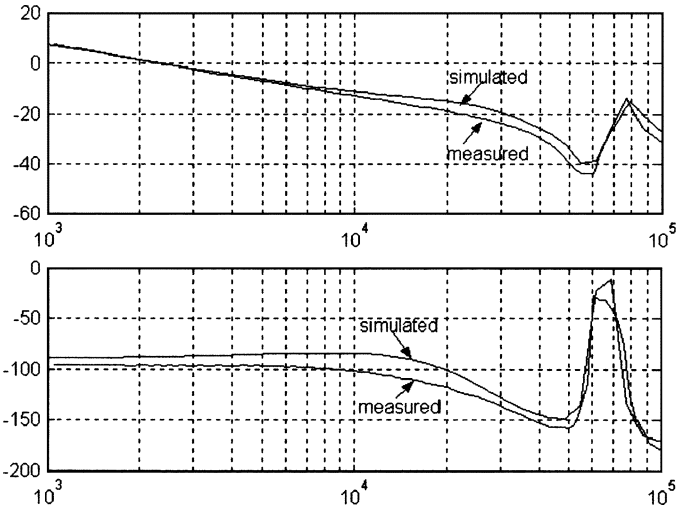

Fig. 12. Inner voltage loop gain.

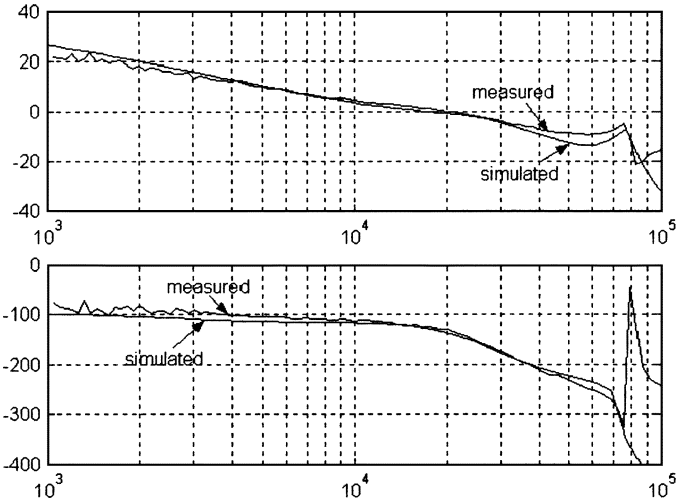

Fig. 13. Outer voltage loop gain.

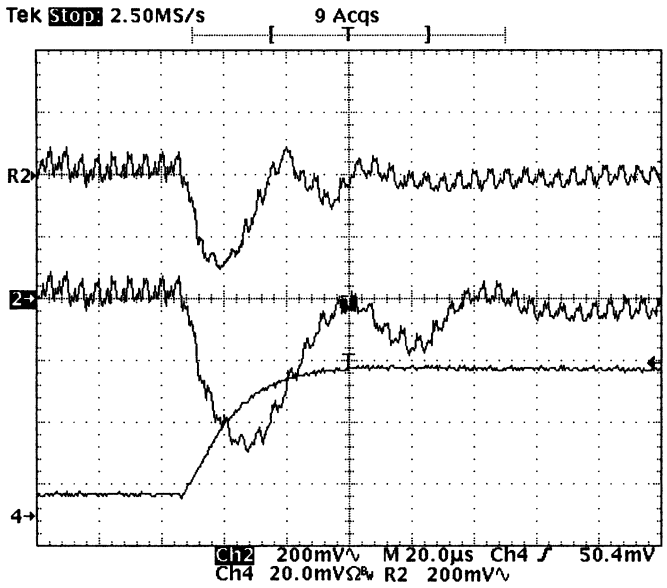

Fig. 14. Output voltage step-load response, Ch2: V_o (with two voltage loops), 0.2 V/div; R2, V_o (with three loops, 0.2 V/div); Ch4: I_o, 10 A/Div.

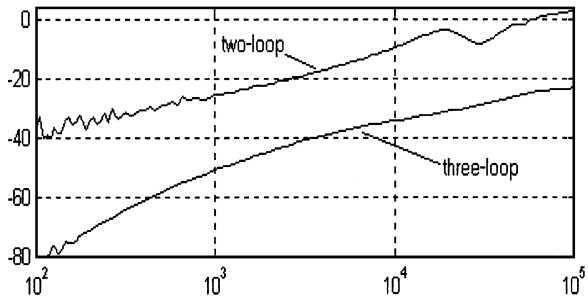

Fig. 15. Experimental closed-loop output impedance ($\mathrm{Vi} = 48$ V).

than f_{r1}. This had not been previously reported for two-stage converters.

Also note in Figs. 12 and 13 that, as designed, the first system resonance has been effectively removed by the controllers. The second resonance still exists, however. The discrepancies in Fig. 13 of gain and phase between the measured and simulated loop gains from 80 to 100 kHz are caused by the high frequency characteristic of the opto-coupler used in the loop. Fortunately, it does not affect the stability of the loop gain. In general, it can be concluded that the simulated design results verify the experimental results. To further verify the transient response improvement, the step-load response of output voltage was also experimentally measured for both the two voltage loop control (Section IV) and the three-loop control. It can be seen from Fig. 14 that 2% settling time to the load disturbance is reduced from 84 to 50 μs when proposed three-loop controller is used. The closed-loop output impedance using the three-loop controller is also shown in Fig. 15, and compared to when using two-voltage-loop control. The output impedance is reduced in both low frequency and high frequency range. We remark that the actual analytic calculation and design of performance transfer functions, such as output impedance and audiosusceptibilty, when three-loop controllers are used is a separate topic in itself. However, from the experimental converter, the three-loop control methodology achieves fast step-load response for two-stage dc–dc converters. This is a consequence of the high bandwidth design.

VII. Conclusion

This paper discusses the control design of two-stage topologies for high voltage input, low voltage/large current output applications. Due to the presence of two resonant frequencies, two-stage converters exhibit fourth-order small signal transfer functions, making compensation loop design relatively challenging. This paper presents a generalized analysis of various multi-loop control designs for two-stage converters. A main contribution of our work, however, is that a new, specific three-loop design algorithm is presented that is able to achieve outer voltage loop crossover frequency beyond the first resonant frequency. This high bandwidth had not previously been reported in the literature for two-stage converters. The outer voltage loop crossover frequency, however, is still limited by the second resonant frequency. Simulations and experiments further illustrate the effectiveness of the proposed multi-loop design.

Appendix I

See the equation at the bottom of the page.

Appendix II
Technical Justification of Proposed Controller for Two-Voltage-Loop Scheme

Since the open-loop transfer function v_o'/d (see Appendix I) satisfies $v_o'/d \approx V_i$ for $0 \le \omega \le 0.1\omega_{r1}$, the inner loop $T_{Vo'} = K_{Vo'}G_{CVo'}G_{P1}G_{P2} \approx K_{Vo'}G_{CVo'}V_i$ ($V_i = V_{i\max}$ for the worst case). Then A_1 can be solved from $|T_{Vo'}(j\omega_{CVo'})| = 1$ ($\omega_{CVo'} = 0.1\omega_{r1}$) at the maximum input voltage. The phase margin is 90°. The actual crossover frequency of inner voltage loop is $\omega_{CVo'} = 0.1(V_i/V_{i\max})\omega_{r1}$.

Since the inner voltage closed-loop transfer function $H_{Vo'C} = G_{CVo'}G_{P1}G_{P2}/(1 + K_{Vo'}G_{CVo'}G_{P1}G_{P2}) \approx 1/K_{Vo'}$ for $0 < \omega \le 0.1\omega_{r1}$, and $H_{Vo'C}(j\omega_{CVo'}) \approx$

$$\frac{v_o}{d} = \frac{V_i R_o'(1+sC_o'R_{ESR}')}{N} \Big/ \left\{s^4 L_1L_2'C_2C_o'(R_o'+R_{ESR}') + s^3(L_1L_2'C_2 + L_1C_2C_o'R_o'R_{ESR}') + s^2[L_2'C_o'(R_o'+R_{ESR}') + L_1C_2R_o' + L_1C_o'(R_o'+R_{ESR}')] + s(L_1+L_2'+R_o'C_o'R_{ESR}') + R_o'\right\}$$

$$\frac{v_o'}{d} = G_{P1}G_{P2} = V_i\left[s^2L_2'C_o'(R_o'+R_{ESR}') + s(L_2'+C_o'R_o'R_{ESR}') + R_o'\right] \Big/ \left\{s^4 L_1L_2'C_2C_o'(R_o'+R_{ESR}') + s^3(L_1L_2'C_2 + L_1C_2C_o'R_o'R_{ESR}') + s^2[L_2'C_o'(R_o'+R_{ESR}') + L_1C_2R_o' + L_1C_o'(R_o'+R_{ESR}')] + s(L_1+L_2'+R_o'C_o'R_{ESR}') + R_o'\right\}$$

$$G_{P1} = \frac{i_{L1}}{d} = V_i\left\{s^3L_2'C_o'C_2(R_o'+R_{ESR}') + s^2(L_2'C_2 + C_2C_o'R_o'R_{ESR}') + s[C_o'(R_o'+R_{ESR}') + C_2R_o'] + 1\right\} \Big/ \left\{s^4 L_1L_2'C_2C_o'(R_o'+R_{ESR}') + s^3(L_1L_2'C_2 + L_1C_2C_o'R_o'R_{ESR}') + s^2[L_2'C_o'(R_o'+R_{ESR}') + L_1C_2R_o' + L_1C_o'(R_o'+R_{ESR}')] + s(L_1+L_2'+R_o'C_o'R_{ESR}') + R_o'\right\}$$

$$G_{P2} = \frac{v_o'}{i_{L1}} = \frac{s^2L_2'C_o'(R_o'+R_{ESR}') + s(L_2'+C_o'R_o'R_{ESR}') + R_o'}{s^3L_2'C_o'C_2(R_o'+R_{ESR}') + s^2(L_2'C_2 + C_2C_o'R_o'R_{ESR}') + s[C_o'(R_o'+R_{ESR}') + C_2R_o'] + 1}$$

$$G_{P3} = \frac{i_{L2}}{v_o'} = \frac{1+sC_o'(R_o'+R_{ESR}')}{s^2L_2'C_o'(R_o'+R_{ESR}') + s(L_2'+C_o'R_o'R_{ESR}') + R_o'}$$

$$G_{P4} = \frac{v_o}{i_{L2}} = \frac{\frac{R_o'(1+sC_o'R_{ESR}')}{N}}{1+sC_o'(R_o'+R_{ESR}')}$$

$$G_{p3}G_{p4} = \frac{v_o}{v_o'} = \frac{\frac{R_o'\left(1+sC_o'R_{ESR}'\right)}{N}}{s^2L_2'C_o'(R_o'+R_{ESR}') + s(L_2'+C_o'R_o'R_{ESR}') + R_o'}$$

$(1/K_{Vo'}\angle -90°)/(1+1\angle -90°) = 1/\sqrt{2}K_{Vo'}\angle -45°$, the inner voltage closed loop transfer function can be approximated by $H_{Vo'C}(s) \approx 1/K_{Vo'}/((s/\omega_{CVo'})+1)$ $(s=j\omega)$ for $0<\omega\le 0.1\omega_{r1}$. In addition, for $0<\omega\le 0.1\omega_{r1}$, $G_{P3}G_{P4}(j\omega) \approx 1/N$. This is because the two poles of $G_{P3}G_{P4}$ are at $\omega_{\text{notch}} = 2\pi f_{\text{notch}}$ and the zero of $G_{P3}G_{P4}$ is assumed between $2\pi f_{r1}$ and $2\pi f_{r2}$. Referring to Fig. 6(c), the outer voltage loop gain with inner voltage loop closed is given as $K_{Vo}G_{CVo}H_{Vo'C}G_{P3}G_{P4}$. Thus, with the above approximations, the outer voltage loop gain becomes $T_{Vo'}(s) \approx K_{Vo}G_{CVo}/(NK_{Vo'}[(s/\omega_{CVo'})+1])$.

Using the above approximations, K-factor design G_{CVo} [12] can be applied to the loop gain $K_{Vo}G_{CVo}/(NK_{Vo'}[(s/\omega_{CVo'})+1])$, where $0.1(V_{i\min}/V_{i\max})\omega_{r1} < \omega_{CVo'} < 0.1\omega_{r1}$. For the worst case, when $V_i = V_{i\max}$, $\omega_{CVo'} = 0.1\omega_{r1}$ should be used in controller design. The formulas are obtained from standard K-factor controller formulas in [21], under the specific condition that $H_{Vo'C}(j\omega_{CVo'}) = 1/\sqrt{2}K_{Vo'}\angle -45°$ (in order to keep the answer conservative, an angle of $-50°$ is used in the K-factor formulas instead of $-45°$ as the angle of $H_{Vo'C}(j\omega_{CVo})$).

Appendix III
Technical Justification of Proposed Controller for Three-Loop Control Scheme

A. Inner Current Loop Compensator, $G_{CIL1} = K_1(s+\omega_{z1})/(s+\omega_{p1})$

Following the general design method, a pole is placed at ω_{P1}. To keep the current loop stable, a zero is added to compensate the phase lag caused by the pole.

In general, $\omega_{\text{CIL1}} > 5\omega_{r1}$. From phase or gain condition at ω_{CIL1}, it can be found that $\omega_{z1} < 3.43\omega_{r1}$. With such a controller, the worst phase lag normally occurs around $1.5\omega_{r1}$. The phase margin is therefore evaluated for this worst case. The phase condition can be determined as

$$\angle T_{IL1}(j1.5\omega_{r1}) = -180° + \phi_{mIL1(\omega st)}, \text{ where}$$
$$\phi_{\text{mIL1}(\omega\text{st})} \ge 45°, \phi_{\text{mIL1}(\omega\text{st})} \text{ is the phase margin at } 1.5\omega_{r1}.$$

On the other hand, the phase angle difference between $1.5\omega_{r1}$ and ω_{CIL1} can be found as

$$\begin{aligned}&\angle T_{IL1}(j\omega_{CIL1}) - \angle T_{IL1}(j1.5\omega_{r1})\\ &\quad\ge \angle G_{CIL1}(j\omega_{CIL1}) - \angle G_{CIL1}(j1.5\omega_{r1})\\ &\quad= \tan^{-1}\left(\frac{\omega_{CIL1}-1.5\omega_{r1}}{\omega_{z1}+\frac{1.5\omega_{CIL1}\omega_{r1}}{\omega_{z1}}}\right)\\ &\qquad- \tan^{-1}\left(\frac{\omega_{CIl1}-1.5\omega_{r1}}{\omega_{p1}+\frac{1.5\omega_{CIL1}\omega_{r1}}{\omega_{p1}}}\right) > 30°\end{aligned}$$

So $\phi_{\text{mIL1}} \ge \phi_{\text{mIL1}(\omega\text{st})} + 30°$. Also, since $\angle T_{IL1}(j1.5\omega_{r1}) \approx \angle G_{CIL1}(j1.5\omega_{r1}) - 85°$, phase condition is reduced to

$$\angle G_{CIL1}(j1.5\omega_{r1}) = -125° + \phi_{mIL1}, \text{ where}$$
$$\angle G_{CIL1}(j1.5\omega_{r1}) = \tan^{-1}\left(\frac{1.5\omega_{r1}}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{1.5\omega_{r1}}{\omega_{p1}}\right)$$

ω_{z1} is then solved as (using formula $\tan(A-B) = (\tan A - \tan B)/(1+\tan A\tan B)$)

$$\omega_{z1} = \frac{1.5\omega_{r1}\left[\omega_{p1} - 1.5\omega_{r1}\tan(-125°+\phi_{mIL1})\right]}{\omega_{p1}\tan(-125°+\phi_{mIL1}) + 1.5\omega_{r1}}. \quad \text{(A1)}$$

To make sure the resonance of G_{P1} is removed, let $|T_{IL1}(j\omega_{r1})| = |K_{IL1}G_{CIL1}G_{P1}(j\omega_{r1})| \ge 10$.

Since G_{P1} has a single zero $(=\omega_{P1})$ before ω_{r1} (see G_{P1} and G_{P2} in Appendix I and Fig. 16), $|T_{IL1}(j\omega_{p1})| = |K_{IL1}G_{CIL1}G_{P1}(j\omega_{p1})| \ge 10$ guarantees $|T_{IL1}(j\omega_{r1})| = |K_{IL1}G_{CIL1}G_{P1}(j\omega_{r1})| \ge 10$, which implies $|T_{IL1}(j\omega_{p1})| = K_{IL1}K_1\sqrt{(\omega_{p1}^2+\omega_{z1}^2)/2\omega_{p1}^2}|G_{P1}(j\omega_{p1})| \ge 10$.

This leads to

$$K_1 \ge \frac{10\sqrt{2}}{K_{IL1}\sqrt{1+\left(\frac{\omega_{z1}}{\omega_{p1}}\right)^2}\cdot|G_{P1}(j\omega_{p1})|}. \quad \text{(A2)}$$

Since $|G_{P1}(j\omega_{p1})| \ge V_{i\min}/R'_{o\max}$, K_1 can be further simplified as

$$K_1 \ge \frac{10\sqrt{2}R'_{o\max}}{K_{IL1}V_{i\min}\sqrt{1+\left(\frac{\omega_{z1}}{\omega_{p1}}\right)^2}}. \quad \text{(A3)}$$

The switching current ripple attenuation should be also satisfied

$$|G_{CIL1}(j2\pi f_s)| = K_1 \le \frac{V_s(1-D_{\max})}{\Delta I_{L1}}. \quad \text{(A4)}$$

So K_1 should be chosen within

$$\left[\frac{10\sqrt{2}R'_{o\max}}{K_{IL1}V_{i\min}\sqrt{1+\left(\frac{\omega_{z1}}{\omega_{p1}}\right)^2}}, \frac{V_s(1-D_{\max})}{\Delta I_{L1}}\right].$$

Let $K_{1\min} = 10\sqrt{2}R'_{o\max}/K_{IL1}V_{i\min}\sqrt{1+(\omega_{z1}/\omega_{p1})^2}$, and define $\omega_{\max}$ to be the frequency where $|T_{\text{IL1}}(j\omega_{\max})| = 10$, and $|T_{\text{IL1}}.(j\omega)| < 10$ when $\omega > \omega_{\max}$. It can be shown that $\omega_{\max}$ is always greater than ω_{r1}, and $\omega_{\max}$ is at minimum when $K_1 = K_{1\min}$.

B. Inner Voltage Loop Compensator, $G_{CVo'} = K_2(s+\omega_{z2})/s$

From Fig. 9, the inner voltage loop gain is given by $T_{Vo'} = K_{Vo'}H_{\text{IL1}C}G_{CVo'}G_{P2}$. By the design procedure of Step 1, $H_{IL1C}(j\omega) = K_{IL1}G_{P1}/(1+K_{IL1}G_{P1}G_{CIL1}) \approx 1/G_{CIL1}(j\omega)$ for $0\le\omega\le\omega_{CVo'}$, since $\omega_{CVo'} \le \omega_{r1}$ and $|K_{\text{IL1}}G_{P1}(j\omega)G_{\text{CIL1}}(j\omega)| \ge 10$ for $0\le\omega\le\omega_{r1}$.

Phase Condition:

$$\begin{aligned}\angle H_{Vo'C}(j\omega_{CVo'}) &= \angle G_{CVo'}(j\omega_{CVo'}) - \angle G_{\text{CIL1}}(j\omega_{CVo'})\\ &\quad + \angle G_{P2}(j\omega_{CVo'})\\ &= -180° + \phi_{\text{mvo'}}. \quad \text{(A5)}\end{aligned}$$

The transfer function G_{P2} has two complex zeros at $\omega_{\text{notch}}(\gg\omega_{CVo'})$, two complex poles near $\omega_{r2}(\gg\omega_{CVo'})$, and a pole at ω_{P2} that is close to $\omega_{CVo'}$. Therefore, for

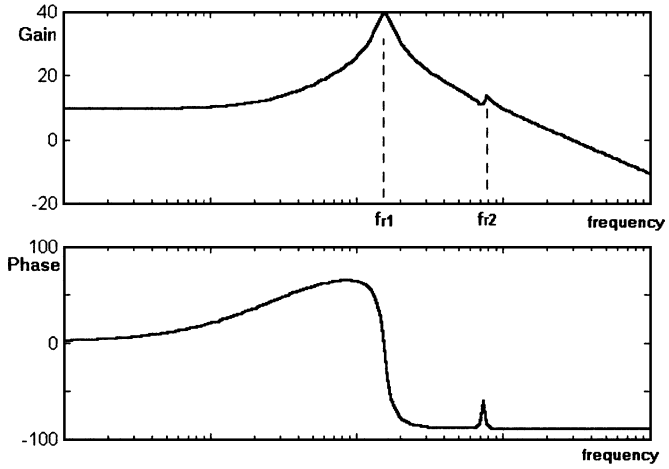

Fig. 16. Bode plot of G_{P1}.

$0 \le \omega \le \omega_{CVo'}$, the phase of G_{P2} satisfies $\angle G_{P2}(j\omega_{CVo'}) = -\tan^{-1}(\omega_{CVo'}/\omega_{P2})$. Thus, (A5) becomes

$$\left\{\tan^{-1}\left(\frac{\omega_{CVo'}}{\omega_{z2}}\right)-90^\circ\right\}-\left\{\tan^{-1}\left(\frac{\omega_{CVo'}}{\omega_{z1}}\right)-\tan^{-1}\left(\frac{\omega_{CVo'}}{\omega_{P1}}\right)\right\} + \left\{-\tan^{-1}\left(\frac{\omega_{CVo'}}{p_2}\right)\right\} = -180^\circ + \phi_{\text{mvo}'}. \quad \text{(A6)}$$

Since $\omega_{P1} = \omega_{P2}$ in the worst operating condition, we assume $\tan^{-1}(\omega_{CVo'}/\omega_{P1}) - \tan^{-1}(\omega_{CVo'}/\omega_{P2}) = 0$. Therefore, $\tan^{-1}(\omega_{CVo'}/\omega_{z2}) = -180^\circ + \phi_{\text{mvo}'} + 90^\circ - 0^\circ + \tan^{-1}(\omega_{CVo'}/\omega_{z1})$, which directly leads to the formula for ω_{z2} given in (5).

Gain Condition: By definition of crossover frequency, $|T_{Vo'}(j\omega_{CVo'})| = |K_{Vo'}G_{CVo'}H_{IL1C}G_{P2}(j\omega_{CVo'})| = |K_{Vo'}G_{CVo'}G_{P2}/G_{CIL1}(j\omega_{CVo'})| = 1$. As previously discussed, since $\omega_{\text{notch}} \gg \omega_{P2}$ and $\omega_{\text{notch}} \gg \omega_{CVo'}$, $|G_{P2}(j\omega)| \approx |R'_o/((j\omega/\omega_{P2}) + 1)|$. Therefore, $|G_{P2}(j\omega_{CVo'})| \approx R'_o\omega_{P2}/\sqrt{\omega^2_{CVo'} + \omega^2_{P2}}$, and so using $|G_{CVo'}(j\omega_{CVo'})| = K_2\sqrt{1 + (\omega^2_{z2}/\omega^2_{CVo'})^2}$, leads to

$$K_2 \approx \frac{K_1\,(C_2 + C'_o)\,\sqrt{\omega^2_{CVo'} + \omega^2_{z1}}}{K_{Vo'}\sqrt{1 + \left(\frac{\omega_{z2}}{\omega_{CVo'}}\right)^2}}. \quad \text{(A7)}$$

C. Outer Voltage Loop Compensator, $G_{CVo} = K_3(s + \omega_{z3})/s(s + \omega_{p3})$

By design, $\omega_{CVo} \gg \omega_{CVo'}$. Therefore, $H_{Vo'c}(j\omega_{CVo}) = H_{IL1C}G_{P2}G_{CVo'}/(1 + K_{Vo'}H_{IL1C}G_{P2}G_{CVo'}) \approx H_{IL1C}G_{P2}G_{CVo'}(j\omega_{CVo})$, since $K_{Vo'}H_{IL1C}G_{P2}G_{CVo'}(j\omega_{CVo}) \ll 1$. Thus, the loop gain of the outer voltage loop at ω_{CVo} is

$$\begin{aligned} T_{Vo}(j\omega_{CVo}) &= K_{Vo}G_{CVo}H_{Vo'C}G_{P3}G_{P4}(j\omega_{CVo}) \\ &\approx K_{Vo}G_{CVo}\{H_{IL1C}G_{P2}G_{CVo'}\} \\ &\quad \times G_{P3}G_{P4}(j\omega_{CVo}). \end{aligned} \quad \text{(A8)}$$

Phase Margin Condition: Using (A8), phase margin ϕ_{mvo} for the outer voltage loop satisfies $\angle T_{Vo}(j\omega_{CVo}) = -180^\circ + \phi_{mvo} = \angle G_{CVo}(j\omega_{CVo}) + \angle H_{IL1C}G_{P2}G_{CVo'}(j\omega_{CVo}) + \angle G_{P3}G_{P4}(j\omega_{CVo})$

By design of the current loop, $H_{IL1C} \approx 1/G_{CIL1}(j\omega_{CVo})$, since $|T_{IL1}(j\omega_{CVo})| \ge 10$. Also, $G_{P3}G_{P4}$ has poles at $\omega_{r2}(> \omega_{\text{notch}})$. Since $\omega_{CVo} < \omega_{r2/3}$, $\angle G_{P3}G_{P4}(j\omega_{CVo}) \approx 0^\circ$. Therefore

$$\begin{aligned} \angle T_{Vo}(j\omega_{CVo}) &\approx \angle G_{CVo}(j\omega_{CVo}) + \angle G_{CVo'}(j\omega_{CVo}) \\ &\quad + \angle G_{P2}(j\omega_{CVo}) - \angle G_{CIL1}(j\omega_{CVo}) \\ &= -180^\circ + \phi_{mvo}. \end{aligned} \quad \text{(A9)}$$

This leads to (A10) shown at the bottom of the page.

Since $\omega_{P2} \ll \omega_{CVo}$, $\angle G_{P2}(j\omega_{CVo}) \ge -80^\circ$, this leads to (A11) shown at the bottom of the page.

Gain Condition:

$$|T_{Vo}(j\omega_{CVo})| = |K_{Vo}G_{CVo}H_{Vo'C}G_{P3}G_{P4}(j\omega_{CVo})| = 1. \quad \text{(A12)}$$

Since $|T_{\text{IL1}}(j\omega_{CVo})| \ge 10$, with $\omega_{r1} \le \omega_{CVo} \le \min[\omega_{\max}, 0.4\omega_{\text{notch}}]$

$$\begin{aligned} |H_{Vo'C}(j\omega_{CVo})| &\approx |H_{IL1C}G_{P2}G_{CVo'}(j\omega_{CVo})| \\ &\approx \left|\frac{G_{P2}}{G_{CIL1}}G_{CVo'}(j\omega_{CVo})\right| \end{aligned}.$$

Referring to the formulas for ω_{P2} and ω_{notch}, $\omega_{P2} \le 0.1\omega_{\text{notch}}$ for the typical two-stage converters. Since $\omega_{CVo} \le 0.4\omega_{\text{notch}}$, G_{P2} can be approximated by a reduced order single pole system at ω_{CVo}

$$G_{P2}(j\omega_{CVo}) \approx \frac{R'_o\omega_{P2}}{j\omega_{CVo} + \omega_{P2}},$$

$$\text{which leads to} \quad |G_{P2}(j\omega_{CVo})| = \frac{R'_o\omega_{P2}}{\sqrt{\omega^2_{CVo} + \omega^2_{P2}}}$$

also, $|G_{CIL1}(j\omega_{CVo})| \approx K_1\sqrt{\omega^2_{CVo} + \omega^2_{z1}}/\sqrt{\omega^2_{CVo} + \omega^2_{p1}}$, and $\sqrt{\omega^2_{CVo} + \omega^2_{p1}} \approx \sqrt{\omega^2_{CVo} + \omega^2_{P2}}$.

$$\omega_{z3} \approx \frac{\omega_{CVo}}{\tan\left[-90^\circ + \phi_{\text{mvo}} + \tan^{-1}\left(\frac{\omega_{CVo}}{\omega_{P3}}\right) + \angle G_{\text{CIL1}}(j\omega_{CVo}) - \angle G_{P2}(j\omega_{CVo}) - \angle G_{CVo'}(j\omega_{CVo})\right]} \quad \text{(A10)}$$

$$\omega_{z3} \approx \frac{\omega_{CVo}}{\tan\left[\phi_{\text{mvo}} + \tan^{-1}\left(\frac{\omega_{CVo}}{\omega_{P3}}\right) + \angle G_{\text{CIL1}}(j\omega_{CVo}) - \angle G_{CVo'}(j\omega_{CVo}) - 10^\circ\right]} \quad \text{(A11)}$$

Therefore

$$|H_{Vo'C}(j\omega_{CVo})| \approx \frac{R'_o\omega_{P2}}{K_1\sqrt{\omega_{CVo}^2+\omega_{z1}^2}}\,|G_{CVo'}(j\omega_{CVo})|\,. \tag{A13}$$

Since $\omega_{CVo} \le 0.4\omega_{\rm notch}$, $|G_{P3}G_{P4}(j\omega_{CVo})| \approx 1/N$. So, (A14) can be rewritten as

$$\begin{aligned}1 &= |T_{Vo}(j\omega_{CVo})| \\ &\approx \frac{K_{Vo}R'_o\omega_{P2}}{K_1N\sqrt{\omega_{CVo}^2+\omega_{z1}^2}}\,|G_{CVo}G_{CVo'}(j\omega_{CVo})| \\ &= \frac{K_{Vo}K_2K_3R'_o\omega_{P2}}{K_1N\omega_{CVo}\sqrt{\omega_{CVo}^2+\omega_{z1}^2}} \\ &\quad\times\sqrt{\left[1+\left(\frac{\omega_{z2}}{\omega_{CVo}}\right)^2\right]}\sqrt{\left[\frac{1+\left(\frac{\omega_{z3}}{\omega_{CVo}}\right)^2}{1+\left(\frac{\omega_{p3}}{\omega_{CVo}}\right)^2}\right]}\end{aligned}$$

which leads to

$$K_3 \approx \frac{K_1N\sqrt{\omega_{CVo}^2+\omega_{p3}^2}\sqrt{\omega_{CVo}^2+\omega_{z1}^2}}{K_2K_{Vo}R'_o\omega_{P2}\sqrt{1+\left(\frac{\omega_{z2}}{\omega_{CVo}}\right)^2}\sqrt{1+\left(\frac{\omega_{z3}}{\omega_{CVo}}\right)^2}}. \tag{A14}$$

Letting $\omega_{P3} = \omega_{CVo}$, $\omega_{P2} \approx 1/R'_o(C'_o + C_2)$, K_3 given in (8) can be derived.

Then, ω_{z3} can be further simplified as

$$\omega_{z3} \approx \frac{\omega_{CVo}}{\tan\left[\phi_{\rm mvo} + 35^\circ + \angle G_{\rm CIL1}(j\omega_{CVo}) - \angle G_{CVo'}(j\omega_{CVo})\right]}. \tag{A15}$$

Remark: It can be shown that by letting $\omega_{P3} = \omega_{CVo}$, the gain margin of the controller $\ge$10 dB at ω_{r2}. That is, the second resonant peak of loop gain (T_{Vo}) is always ≤ -10 dB.

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