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DIGITAL SYSTEMS LABORATORY

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ABSTRACT

Necessary and sufficient conditions are given for the existence of static and dynamic hazards in combinational circuits that undergo multiple input changes. These theorems are applied in the analysis of modules, such as the wye module, that have been proposed for asynchronous systems. We show that unless internal module delays are strictly less than delays between modules, incorrect operation can occur due to hazards in module implementations.

Index Terms – Asynchronous networks, hazards, delays, modular systems

TABLE OF CONTENTS

LIST OF FIGURES

INTRODUCTION

We examine the operation of asynchronous systems, systems in which there is no periodic synchronizing signal that limits system input changes to specific instants in time. We consider systems consisting of modules interconnected by lines carrying binary, level signals, The modules themselves will be asynchronous combinational circuits. It has been proposed [1,2] that asynchronous systems be built by choosing modules from a fixed, pre-defined set of module types. We consider the implementation of some of these modules. It is usually assumed and in fact desired that asynchronous systems be insensitive to the magnitudes of delays in the system.

We will examine the transient output behavior of the module circuits for certain changes of input variables. We will be interested in input changes where one or more variables change simultaneously. If the circuit output can change more than once in response to such an input change, the circuit is said to contain a hazard [3]. The extra output changes due to hazards result in stray logic pulses that may cause other portions of the asynchronous to operate improperly.

To illustrate the difficulties caused by hazards, consider the asynchronous system shown in Fig. 1. This system consists of four modules, one source module, two sink modules, and a wye module. These module types have been proposed by Altman and Lo [l]. The source module produces as output the inverse of its input. The sink module simply

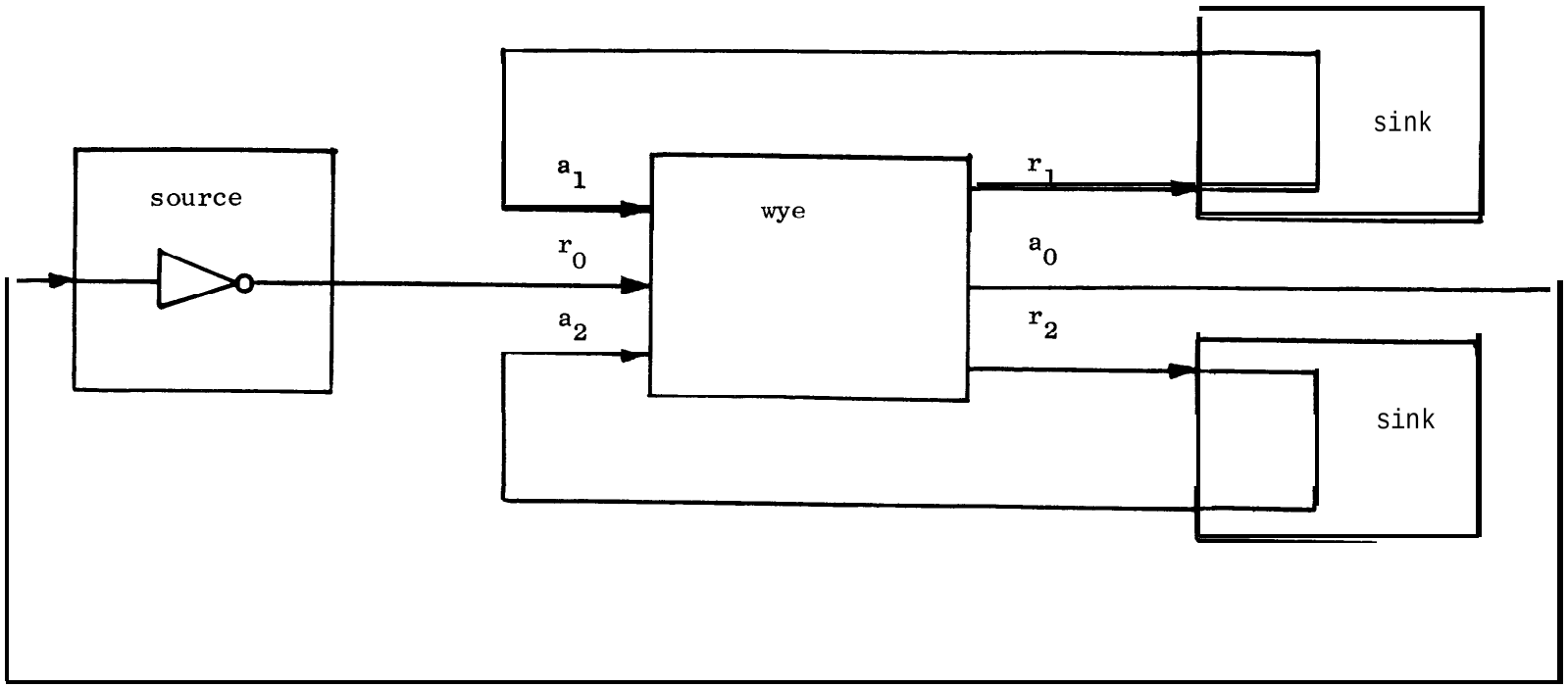


Fig. 1. An example of an asynchronous system.

transmits its input value as its output. The wye module is intended to function as follows. An input request to the wye module is either a 0 - 1 or 1 - 0 input change on line r_0. When the wye module receives such a request it initiates identical requests on lines r_1 and r_2. That is, a change in the logic level of line r_0 causes the wye module to change the logic level of lines rl and r_2. The wye module now waits until it recognizes changes on lines a_1 and a_2 which acknowledge that the requests initiated by the wye module have been received. After recognizing the acknowledge signals on lines a_1 and a_2, the wye module produces an acknowledge signal on line a_0. A 0 - 1 request on line r_0 results in 0 - 1 acknowledge transistions on lines a_0, a_1, and a_2. Similarly, 1 - 0 requests result in 1 - 0 acknowledge transitions. A Karnaugh map and circuit implementation of the wye module are shown in Fig. 2 and Fig. 3, respectively.

We have just described the intended operation of the wye module. However, due to delays in the system, it may not always operate this way. If delays internal to the wye module are greater than delays in the circuits that generate acknowledge transitions on lines a_1 and a_2, the wye module may see input changes on lines a_1 and a_2 before it has completely responded to a change on line r_0. These input changes may cause the asynchronous system to operate incorrectly as follows. Assume that all lines in the system shown in Fig. 1 are initially 0. Let the source

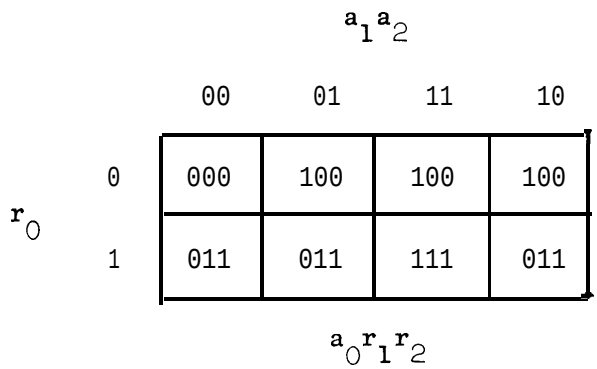
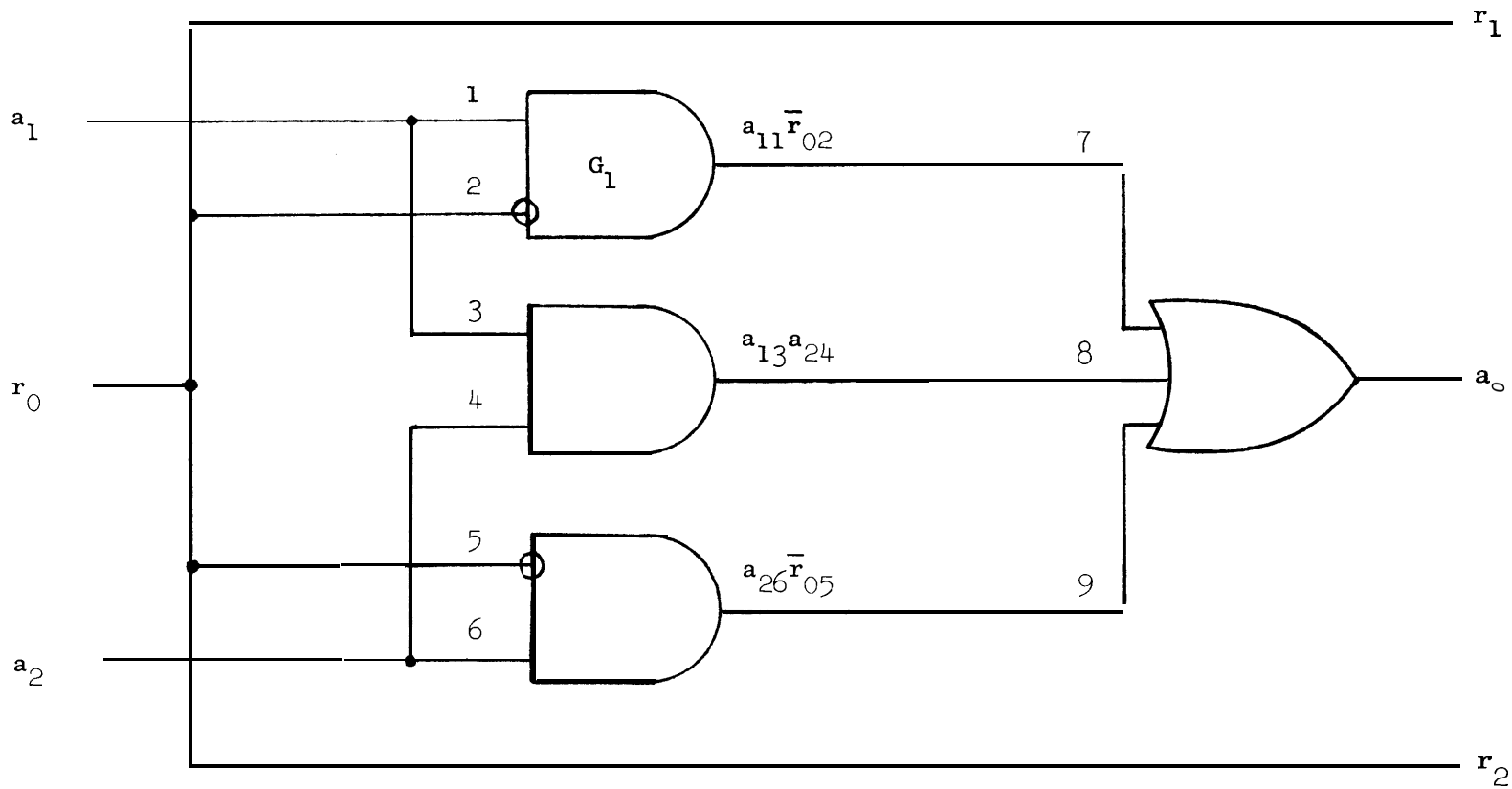


Fig. 2. Karnaugh map for the wye module.



Transient output function for $a_0 = a_{117}\bar{r}_{027} + a_{138}a_{248} + a_{269}\bar{r}_{059}$

Fig. 3. Circuit diagram for the wye module.

module before the 1 on r_0 has propagated through the inverter on the input to gate G_1, then gate Gl will change its output to 1. This will cause a_0 to change to 1, signaling the source module that the wye module is ready for another request on line r_0. In fact, the wye module is not ready for another signal on r_0 because the sink module connected to line r_2 has not signaled its completion yet. This is an example of the incorrect operation that a hazard can cause.

This example shows that delays in an asynchronous system can be very important. We now turn to the problem of characterizing the effects of delays on system operation. A notation is presented that shows the effect of delays on the output of a combinational circuit. Then theorems are given that characterize the conditions that cause a circuit to contain a hazard. Finally, the system of Fig. 1 is analyzed for hazards.

DELAYS AND OUTPUTS OF COMBINATIONAL CIRCUITS

In this section we present a method due to McCluskey [3, Ch. 7] for producing a functional description of a combinational circuit output that accounts for the effects of all possible delays in that circuit. Delays may be present in circuit gates and lines. These delays are assumed to change the time of arrival of a signal but not its amplitude. The magnitude of a delay is assumed to be finite but unbounded. Several delays in series have a cumulative effect. The total delay, from the time an input changes to the time its effects are noted at the output, is the sum of the delays along its path to the output. A single input variable may have several paths that it can follow to the output. A direction of propagation and a delay is associated with each line in a circuit. Delays are not explicitly associated with gates or inverters. The delay in a gate or inverter merely adds to the delay present in its input lines, so it is lumped in with the line delays.

To account for delay effects, each different delay path a variable may encounter in propagation to the output of a combinational network must be identified and a unique literal for the variable generated for each path. To accomplish this, the lines in the network are numbered as shown in Fig. 3 for the wye module circuit. Each number i represents a delay d_i present in that line. The transient output function of the network is computed by appending the line number to the subscript of each variable in the expression for the logic function associated with a network

line. Thus the transient output function for output a_0 of the wye module circuit in Fig. 3 is: $a_0 = a_{117}\bar{r}_{027} + a_{138}a_{248} + a_{269}\bar{r}_{059}$.

If the transient output function is written in sum of products form, the literals in each product term form a P set of the network. When the transient output function is written in product of sums form, the literals in each of the sum terms form an S set of the network. The P sets for the wye module network of Fig. 3 are $\{a_{117}, \bar{r}_{027}\}$, $\{a_{138}, a_{248}\}$, and $\{a_{269}, \bar{r}_{059}\}$. The P set is formally defined as follows [4, p.20]. A P set of a network is a set of subscripted literals $\{x_i,\ldots,y_{jk}\}$ if and only if (1) the signal represented by x_i being equal to 1 at time $t - d_i$ and . . . and the signal represented by y_{jk} being equal to 1 at time $t - d_j - d_k$ will cause the output signal to be 1 at time t, and (2) any one of these signals being 0 will cause the output signal to be equal to 0. The definition of an S set is dual to this P set definition and is obtained by replacing P set by S set and interchanging 0's and l's in the P set definition. P sets and S sets are useful in analyzing combinational circuits for the presence of hazards.

DETECTION OF HAZARDS

Before describing techniques for detecting hazards in combinational circuits, a more precise description of circuit input and output behavior is required. The initial input state of a circuit is a binary vector that describes the logic level of the network input prior to an input change. A circuit with inputs a, b, and c and a starting input state of (101) would have a=l, b=0, and c=l. The final input state is the binary vector that

describes the input levels after an input change is completed. An input change may also be called an input transition. An input variable is assumed to change only once during a transition. Those variables that are constant are nonchange variables. Literals may also be designated as change or nonchange type. If a single input variable changes, it is called a single input change. If more than one variable changes at a time, then it is called a multiple input change.

Hazards can be characterized by the output response they cause. A combinational circuit is said to contain a static 1 hazard for a transition between initial input state A and final input state B if the network output for input states A and B is 1, and it is possible for a momentary 0 output to occur during or after the input transition. A network contains a static 0 hazard for a transition between initial input state A and final input state B if the circuit output for input states A and B is 0, and it is possible for a momentary 1 output to occur. A circuit is said to contain a dynamic hazard for the transition from initial input state A to final input state B if A produces a 0 output, B produces a 1 output, and it is possible for a momentary 1 - 0 output sequence to occur during the input transition. It is also a dynamic hazard if A produces the 1 output, B produces the 0 output, and there is a momentary 0 - 1 output sequence.

We now state and prove two theorems that characterize conditions for which a combinational circuit contains a static or dynamic hazard. The theorems require that the P or S sets be formed for the circuit. In these proofs a P set is said to cover an input state if all literals in the P set equal 1 for that input state. An S set is said to cover an input state if all the literals of the S set are equal to 0 for that input state.

Theorem 1: A circuit contains a static 0 (1) hazard for the transition from initial input state A to final input state B if and only if:

1. Both input states produce 0 (1) outputs.
2. There is a P (S) set of the network whose nonchanging literals all have the value 1 (0).

Proof:

a. First we show sufficiency. Condition 1 insures that the initial and final output values are correct for a static hazard, We need only show it is possible for a momentary 1 (0) output to occur. A 1 (0) output occurs if all the changing literals of the P (S) set are 1 (0) at some instant. This happens if all changes from 0 (1) to 1 (0) precede all changes from 1 (0) to 0 (1). Since the delay associated with each literal is arbitrary, the circuit contains a hazard.

b. Next we show necessity. Assume a static 0 (1) hazard exists. The initial input state and final input state must produce 0 (1) outputs, so condition 1 is necessary. For the momentary 1 (0) output to occur, there must exist a P (S) set of the circuit whose literals are all 1 (0) some time during the transition. Since the nonchanging literals have the same value before and after the transition, if they are to be 1 (0) at any point in the transition, they must always be 1 (0). Therefore condition 2 is necessary also.

Theorem 2: A circuit contains a dynamic hazard for the transition from initial input state A to final input state B if and only if:

1. A and B produce different network outputs.
2. One of the following two conditions hold:
   A. In the case input state A yields a 0 output, there must exist a P set, call it K_1, whose nonchanging literals are all 1 and that does not cover B. In addition, there can be no P set that covers B whose literals under input state A are a subset of the 0 literals of K_1 for input state A.
   B. If the output for A is 1, there must exist a P set K_0 whose nonchanging literals are all 1 and which does not cover A. In addition, there can be no P set that covers A whose literals for input state B are a subset of the 0 literals of K_0 under input state B.

Proof:

a. First we show sufficiency. Consider conditions 1 and 2A. Condition 2A sets the initial output to 0. If only those literals that are 0 in K_1 are allowed to change to 1, the output will become 1. Now if all the literals that will be 0 for input state B are allowed to change to 0, the output will become 0. This follows since each of the P sets that cover B contain at least one literal not in K_1 that was 0 in input state A. The P sets that do not cover B are all 0 since all the literals that are 0 under input state B have changed to 0. Condition 1 guarantees a 1 final output. Conditions 1 and 2A are sufficient to cause a dynamic hazard in the case the initial output is 0.

In the case the initial output is 1, condition 2B applies. If every literal that is 0 under input state B and is contained in a P set that covers A but is not in K_0 changes to 0, the output will become 0. This follows because all the P sets that formerly had no 0 literals now each have at least one. If all the literals that will be 1 under input state B change to 1, all of K_0's literals will be 1, making the circuit output 1. Condition 1 forces a 0 final output. Therefore conditions 1 and 2B are sufficient to cause a dynamic hazard in the case the initial output is 1.

b. Next we show necessity. Assume the circuit contains a dynamic hazard and produces a O-l-O-1 output sequence for the input transition A to B. The initial O-1-0 output sequence requires that there be a P set, call it K_1, that turns on, then off again. K_1 may not cover B, else the output would not go to 0 following the initial 1. Those P sets that cover B may not have any of their literals that are 0 under input state A be a subset of K_1's literals that are 0 under input state A. If this condition were violated, the output would remain 1 after the first 0 to 1 output change. Finally, if the output for input state B is to be 1, then condition 1 is necessary. In the case the output for initial state A is 0, conditions 1 and 2A are necessary. Now assume the network produces a 1-0-1-O output for the input transition A to B. The second 1 in the output sequence indicates that there is a P set, call it K_0, that does not cover input state A. K_0 must not cover A, else the second 1 in the output sequence would not be possible. Those P sets that cover A may not have any of their literals that are 0 under input state A be a subset of K_0's

literals that are 0 under input state a. If this condition were violated the output would remain 0 after the first 1 to 0 output change. Thus conditions 1 and 2B are necessary for a 1-0-1-0 output sequence.

Theorem 2 can also be stated in terms of S sets.

Theorem 2A: A circuit contains a dynamic hazard for the transition from initial state A to final input state B if and only if:

1. A and B produce different network outputs.
2. One of the following two conditions holds:
   A. In the case input state A yields a 0 output, there must exist an S set, call it K_1, whose nonchanging literals are all 0 and that does not cover A. In addition, there can be no S set that covers A whose 1 literals for input state B are a subset of the 1 literals of K_1 for input state B.
   B. If the output for A is 1, there must exist an S set, K_0, whose nonchanging literals are all 0 and which does not cover B. In addition, there can be no S set that covers B whose 1 literals for input state A are a subset of the 1 literals of K_0 for input state A.

The proof is analogous to the proof for Theorem 2. In the next section we will see an example of the use of Theorem 2.

These theorems are related to the work of several others. McCluskey [3] gives theorems that characterize conditions for single input change static and dynamic hazards. Eichelberger [5] has characterized conditions for multiple input change static hazards. Unger [6] has stated theorems that characterize conditions for multiple input change static and dynamic hazards.

Unger's theorems differ from those given here in their statement of the theorem conditions and also in their proof.

ANALYSIS OF ASYNCHRONOUS SYSTEMS

We can now apply the theoretical results of the previous section in the analysis of asynchronous systems composed of modules realized as combinational networks. To illustrate the method we will consider a hazard analysis for the a_0 output of the wye module circuit of Fig. 3 when used in the asynchronous system shown in Fig. 1.

In Fig. 4 we show the input transitions predicted for the wye module by its design specification. By checking the conditions of Theorems 1 and 2 with the P sets for the circuit of Fig. 3, it can be verified that the circuit is free from both static and dynamic hazards for all these input transitions.

In Fig. 5 we show the additional input transitions that will be seen by the wye module circuit after a change in input variable r_0 from 0 to 1 if delays internal to the wye module are greater than delays in propagation between modules. We consider first the input change $r_0a_1a_2$: 000-110. The P set $\{a_{117}, \bar{r}_{027}\}$ satisfies condition 2 of Theorem 1 so the wye module contains a static 0 hazard for this transition. For the change $r_0a_1a_2$: 000-111, the initial and final output values for a, are 0 and 1 respectively so the circuit must be checked for a dynamic hazard. Two of the P sets satisfy the conditions of Theorem 2. They are $\{a_{117}, \bar{r}_{027}\}$ and $\{a_{269}, \bar{r}_{059}\}$. Thus the wye module circuit contains a dynamic hazard for this input change. There are additional

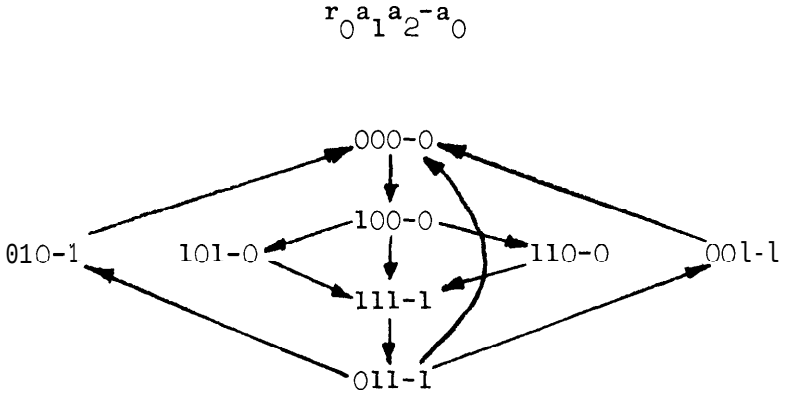


Fig. 4. Input transitions permitted by the wye module design specification.

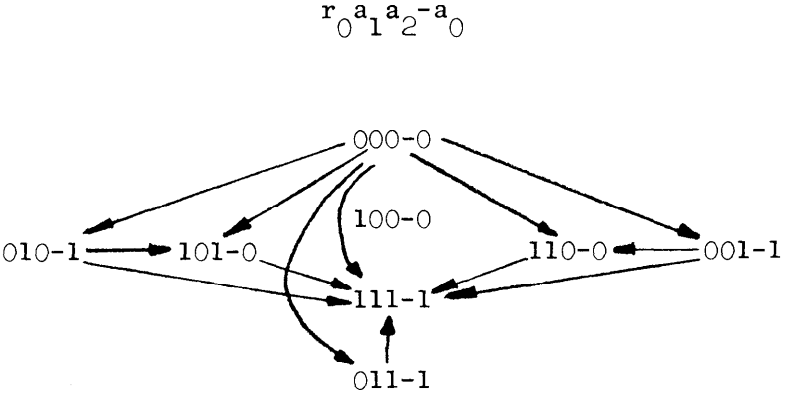


Fig. 5. Additional wye module input transitions if delays internal to wye module are greater than delays between modules for input transition r_0: 0-1.

hazards for the transitions of Fig. 5 and also several hazards when r_0 changes from 1 to 0.

It might be expected that these hazards result from the particular two-level, and-or logic used to implement the wye module function. In fact, as long as the relative magnitudes of all system delays are arbitrary, any circuit that implements the wye module will contain hazards. This is due to the fact that the Karnaugh map (Fig. 2) for the wye module contains function hazards [5,6] which are inherent in the function being realized and cannot be removed by the addition of logic gates to a network.

The hazard outputs for the wye module do not occur if the module sees only the originally specified input changes. In the case of the wye module this means that delay elements, which implement fixed, lumped delays, must be inserted in the system realization. These delay elements must be inserted in the output lines r_1 and r_2 and must have values greater than all stray delays present in the wye module that could affect propagation of changes in r_0 to output a_0. We emphasize these delay elements are necessary if the wye module is to operate as specified.

We have examined other modules that have been proposed for asynchronous systems and found that the junction, trigger, and union modules also contain hazards for certain input changes. As found in our examination of the wye module, these are function hazards inherent in the module definitions; however, the hazards only occur if internal delays are greater than delays between modules.

CONCLUSIONS

Asynchronous systems are intended to be insensitive to the relative magnitudes of delays present in the system. By means of a hazard analysis, we have shown that, unless delays are carefully controlled, asynchronous systems can function incorrectly. One general delay requirement appears to be that delays internal to a system module must be strictly less than delays present between modules. This requirement has been pointed out previously by Unger [6, p. 121]; however, it appears to have been ignored in the literature discussing the implementation of asynchronous systems [1].

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