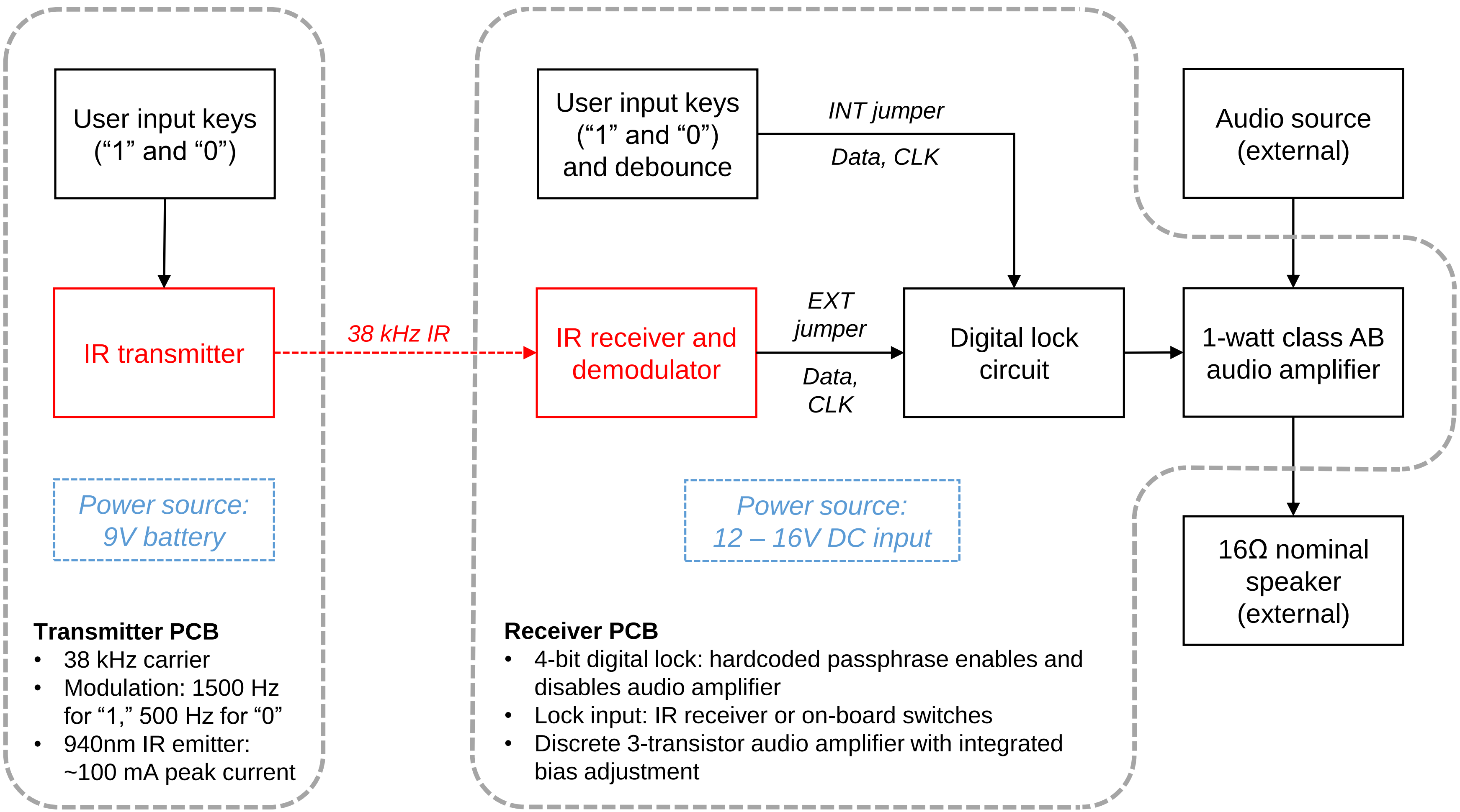
Lecture 5

Design project analysis and course conclusion

Graphics used with permission from AspenCore (http://electronics-tutorials.ws)

Block diagram



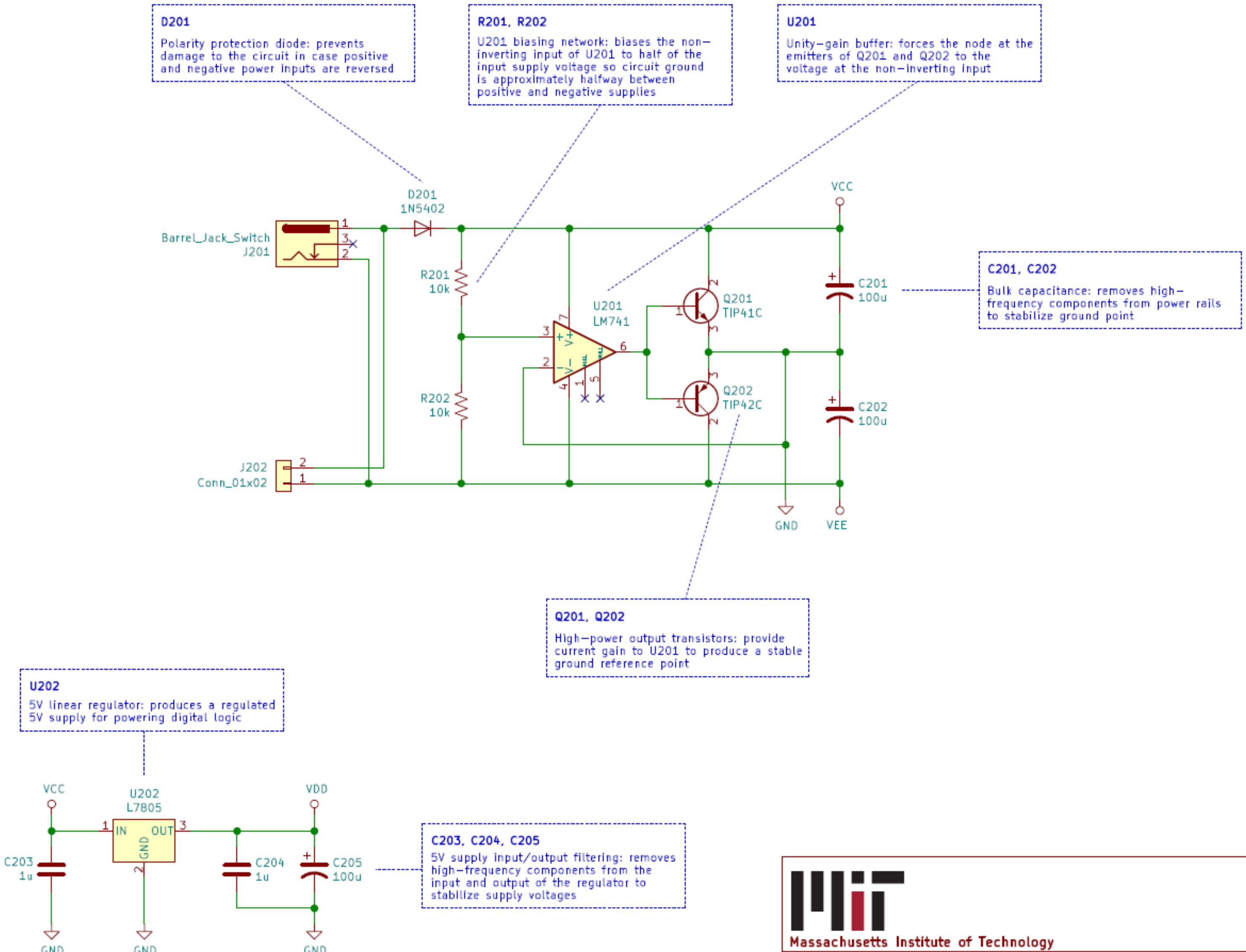
Transmitter PCB
- 38 kHz carrier
- Modulation: 1500 Hz for "1," 500 Hz for "0"
- 940nm IR emitter: ~100 mA peak current

Receiver PCB
- 4-bit digital lock: hardcoded passphrase enables and disables audio amplifier
- Lock input: IR receiver or on-board switches
- Discrete 3-transistor audio amplifier with integrated bias adjustment

Agenda

1. Power supply
2. Digital lock
3. Audio amplifier
4. IR receiver
5. Course conclusion

Power supply



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Sheet: /Power/
File: power.sch

Title: 6.117 Final Project: Receiver

Size: USLetter	Date: 1/15/2020	Rev: A.0.1
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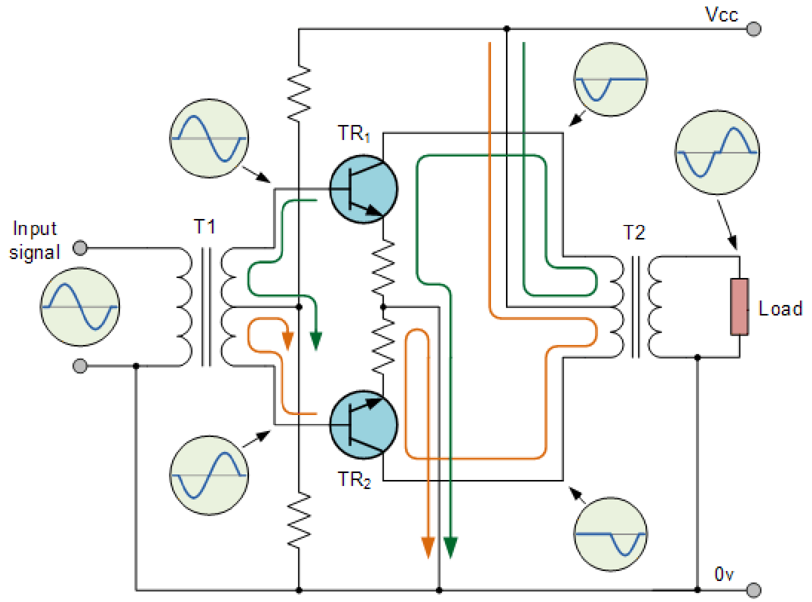
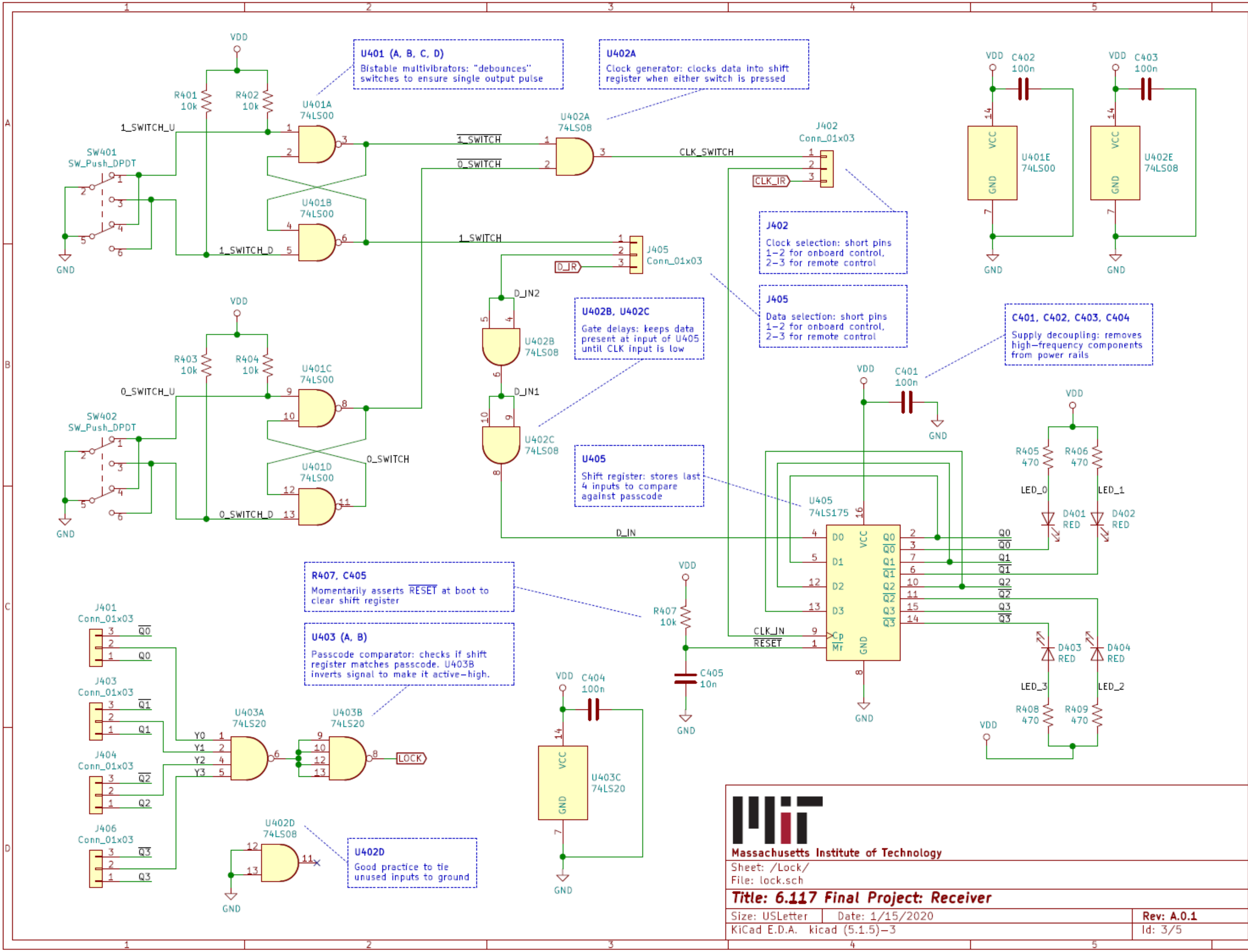
Push-pull output stage

- Basically just a Class B amplifier operating at DC
- Uses **feedback** into op-amp to compensate for the voltage drop (V_{BE}) induced by the BJTs
- Net current into/out of GND net causes op-amp to adjust midpoint



Digital lock


U401 (A, B, C, D)
Bistable multivibrators: "debounces" switches to ensure single output pulse
U402A
Clock generator: clocks data into shift register when either switch is pressed
J402
Clock selection: short pins 1–2 for onboard control, 2–3 for remote control
J405
Data selection: short pins 1–2 for onboard control, 2–3 for remote control
U402B, U402C
Gate delays: keeps data present at input of U405 until CLK input is low
C401, C402, C403, C404
Supply decoupling: removes high–frequency components from power rails
U405
Shift register: stores last 4 inputs to compare against passcode
R407, C405
Momentarily asserts RESET at boot to clear shift register
U403 (A, B)
Passcode comparator: checks if shift register matches passcode. U403B inverts signal to make it active–high.
U402D
Good practice to tie unused inputs to ground
VDD
GND
R401 10k
R402 10k
R403 10k
R404 10k
SW401 SW_Push_DPDT
SW402 SW_Push_DPDT
1_SWITCH_U
1_SWITCH_D
0_SWITCH_U
0_SWITCH_D
1_SWITCH
0_SWITCH
U401A 74LS00
U401B 74LS00
U401C 74LS00
U401D 74LS00
U402A 74LS08
U402B 74LS08
U402C 74LS08
U402D 74LS08
CLK_SWITCH
J402 Conn_01x03
CLK_IR
J405 Conn_01x03
D_IR
D_IN2
D_IN1
D_IN
U401E 74LS00
U402E 74LS00
C402 100n
C403 100n
C401 100n
C404 100n
VCC
U405 74LS175
D0
D1
D2
D3
Cp
Mr
Q0
Q1
Q2
Q3
CLK_IN
RESET
R407 10k
C405 10n
R405 470
R406 470
R408 470
R409 470
LED_0
LED_1
LED_2
LED_3
D401 RED
D402 RED
D403 RED
D404 RED
J401 Conn_01x03
J403 Conn_01x03
J404 Conn_01x03
J406 Conn_01x03
Y0
Y1
Y2
Y3
U403A 74LS20
U403B 74LS20
U403C 74LS20
LOCK
Massachusetts Institute of Technology
Sheet: /Lock/
File: lock.sch
Title: 6.117 Final Project: Receiver
Size: USLetter
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Rev: A.0.1
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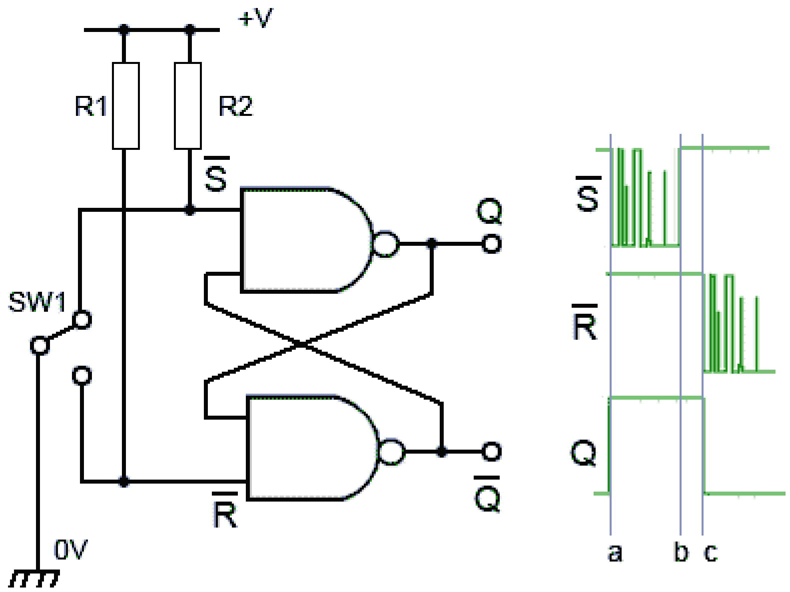
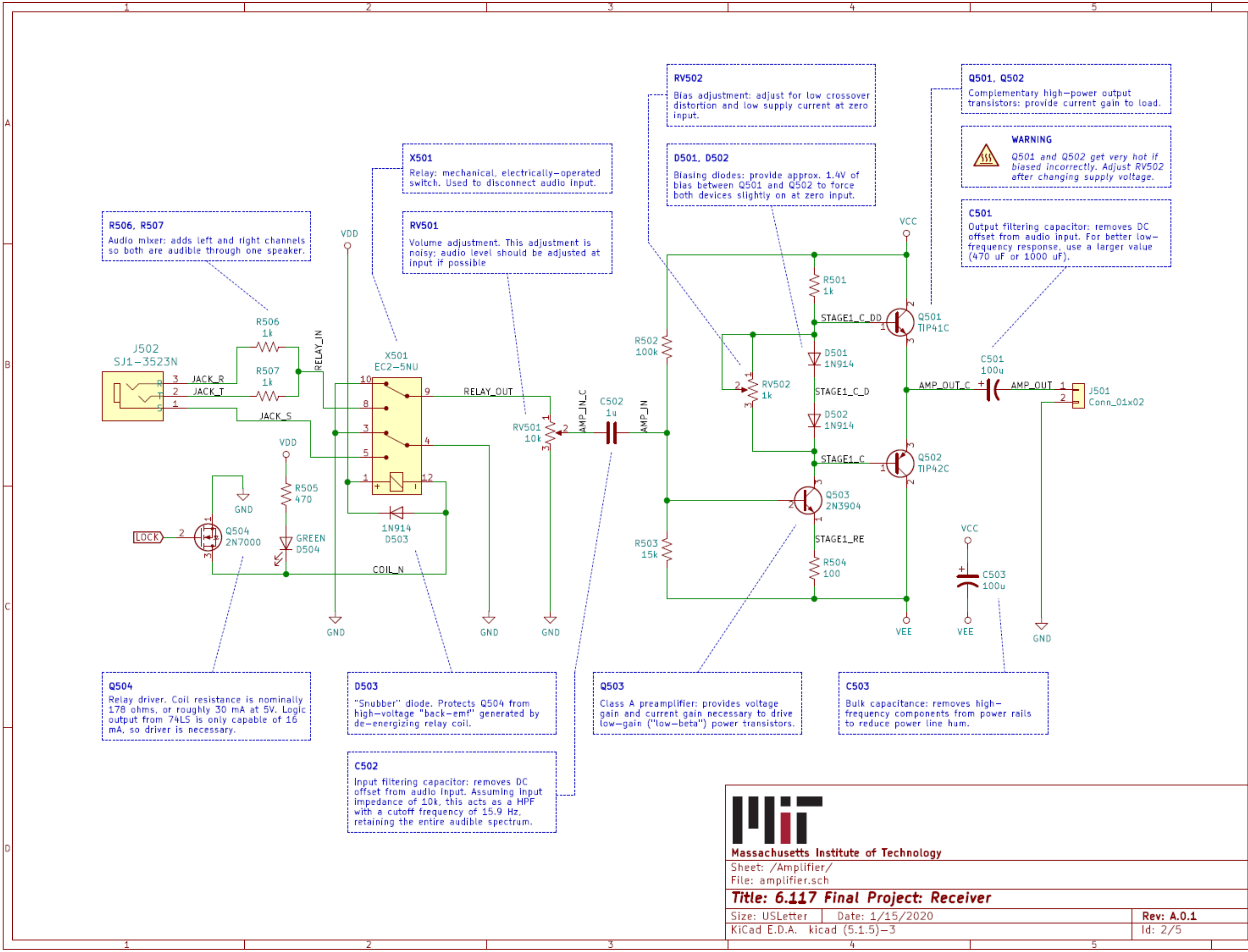
Switch debouncing

- **Bouncing** causes a contact to generate multiple electrical pulses when a connection is made or broken
- Can use a **dual-pole** switch and SR flip-flop to eliminate



Audio amplifier


R506, R507
Audio mixer: adds left and right channels so both are audible through one speaker.
X501
Relay: mechanical, electrically-operated switch. Used to disconnect audio input.
RV501
Volume adjustment. This adjustment is noisy; audio level should be adjusted at input if possible
RV502
Bias adjustment: adjust for low crossover distortion and low supply current at zero input.
D501, D502
Biasing diodes: provide approx. 1.4V of bias between Q501 and Q502 to force both devices slightly on at zero input.
Q501, Q502
Complementary high-power output transistors: provide current gain to load.
WARNING
Q501 and Q502 get very hot if biased incorrectly. Adjust RV502 after changing supply voltage.
C501
Output filtering capacitor: removes DC offset from audio input. For better low-frequency response, use a larger value (470 uF or 1000 uF).
J502
SJ1-3523N
R506
1k
R507
1k
JACK_R
JACK_T
JACK_S
RELAY_IN
VDD
X501
EC2-5NU
RELAY_OUT
RV501
10k
AMP_IN_C
C502
1u
AMP_IN
R502
100k
R501
1k
STAGE1_C_DD
Q501
TIP41C
D501
1N914
RV502
1k
STAGE1_C_D
D502
1N914
STAGE1_C
Q502
TIP42C
VCC
AMP_OUT_C
C501
100u
AMP_OUT
J501
Conn_01x02
GND
R505
470
GREEN
D504
LOCK
Q504
2N7000
1N914
D503
COIL_N
Q503
2N3904
R503
15k
STAGE1_RE
R504
100
VEE
C503
100u
Q504
Relay driver. Coil resistance is nominally 178 ohms, or roughly 30 mA at 5V. Logic output from 74LS is only capable of 16 mA, so driver is necessary.
D503
"Snubber" diode. Protects Q504 from high-voltage "back-emf" generated by de-energizing relay coil.
Q503
Class A preamplifier: provides voltage gain and current gain necessary to drive low-gain ("low-beta") power transistors.
C503
Bulk capacitance: removes high-frequency components from power rails to reduce power line hum.
C502
Input filtering capacitor: removes DC offset from audio input. Assuming input impedance of 10k, this acts as a HPF with a cutoff frequency of 15.9 Hz, retaining the entire audible spectrum.
Massachusetts Institute of Technology
Sheet: /Amplifier/
File: amplifier.sch
Title: 6.117 Final Project: Receiver
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2N3904

"Absolute maximum" ratings: Values outside these ranges will cause permanent damage to the device

Maximum voltages: Limited by power supply (V_{CEO}, V_{CBO}) or input range (V_{EBO})

Maximum current: Limited by load impedance

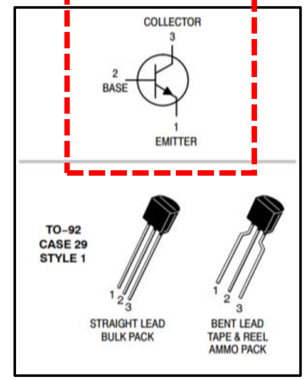
Gain-bandwidth product: Defines maximum gain in an amplifier

Small-signal gain: Ratio of collector current to base current

Pin diagram: Pinning for 2N3904 is like "ABC" (actually EBC)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	60	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C



SMALL–SIGNAL CHARACTERISTICS

Current – Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903 2N3904	f_T	250 300	– –	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{ie}	1.0 1.0	8.0 10	k Ω
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	X 10^{-4}
Small–Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{fe}	50 100	200 400	–
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903 2N3904	NF	– –	6.0 5.0	dB

Source: https://www.onsemi.com/pub/Collateral/2N3903-D.PDF

TIP41, TIP42

Collector-emitter voltage: Capable of switching high voltages

Packaging: Collector electrically connected to case

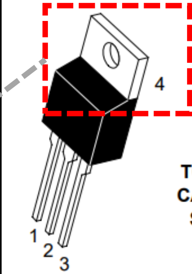
Collector current: Capable of driving high-current loads

Power dissipation: Capable of dissipating much more power than small-signal devices (2N3904)

DC current gain: Much lower current gain than small-signal devices

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CEO}	40 60 80 100	Vdc
Collector−Base Voltage	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CB}	40 60 80 100	Vdc
Emitter−Base Voltage		V_{EB}	5.0	Vdc
Collector Current−	Continuous Peak	I_C	6.0 10	Adc
Base Current		I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C		P_D	65 0.52	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2.0 0.016	W W/°C
Unclamped Inductive Load Energy (Note 1)		E	62.5	mJ
Operating and Storage Junction, Temperature Range		T_J, T_{stg}	−65 to +150	°C



TO−220AB CASE 221A STYLE 1

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 30 mAdc, I_B = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	40 60 80 100	− − − −	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	I_{CEO}	− −	0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	− − − −	400 400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	− 75	−
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	2.0	Vdc

Source: http://www.farnell.com/datasheets/40034.pdf

Audio amplifier analysis

D1, D2
Output biasing diodes: Biases Q2 and Q3 slightly on to eliminate crossover distortion

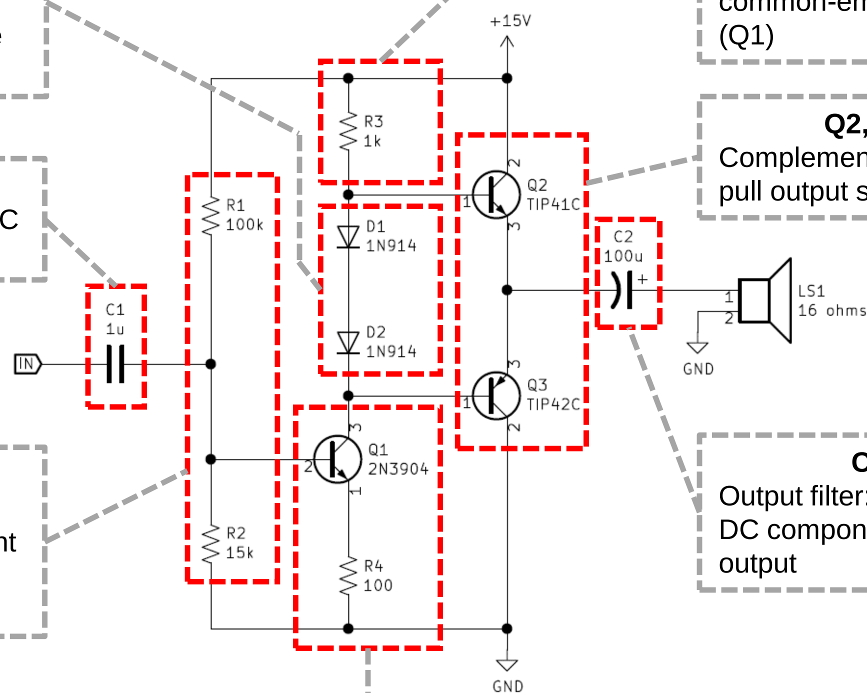
C1
Input filter: removes DC component from input

R1, R2
Q1 biasing network: sets the operating point for common-emitter (Class A) stage

R3
Sets voltage gain of common-emitter stage (Q1)

Q2, Q3
Complementary push-pull output stage

C2
Output filter: removes DC component from output



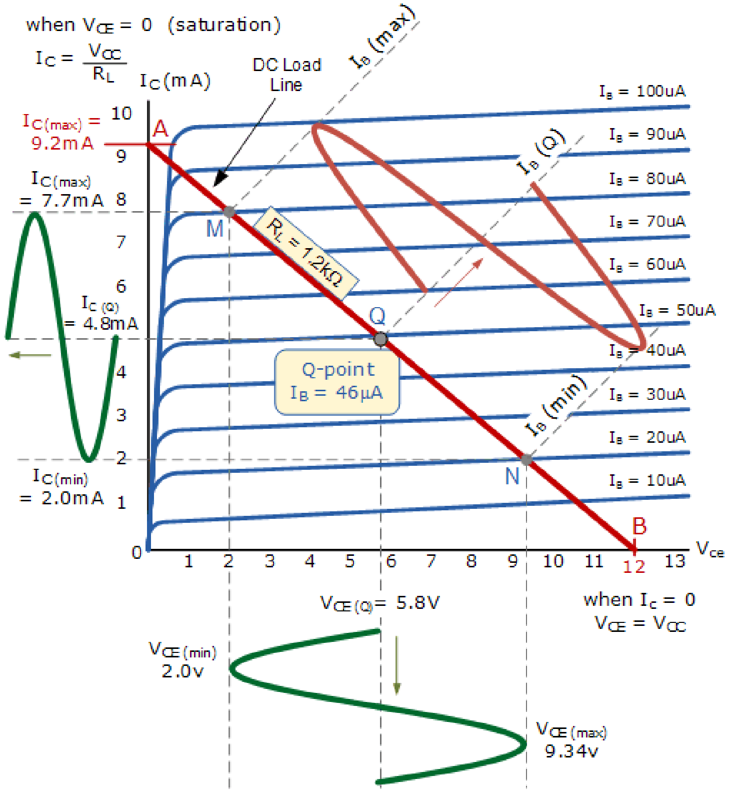
Q1
Common-emitter amplification stage: Provides current gain for driving output power transistors (Q2 and Q3)

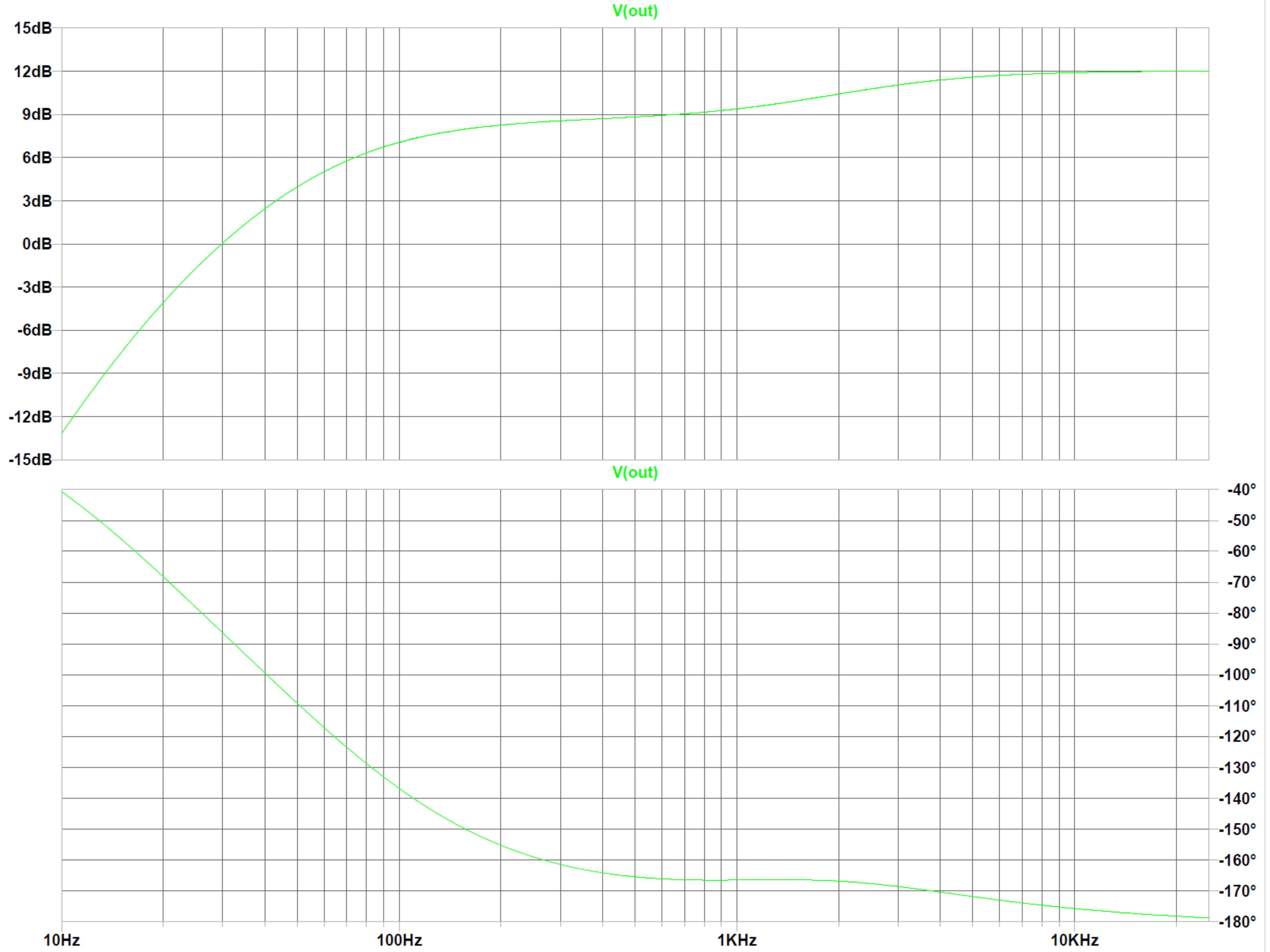
Preamplifier biasing

- **Goal:** provide voltage and current gain for output stage
- **Biasing** accomplished with voltage divider

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$\text{Voltage Gain} = \frac{V_{out}}{V_{in}} = \frac{\Delta V_L}{\Delta V_B} = -\frac{R_L}{R_E}$$





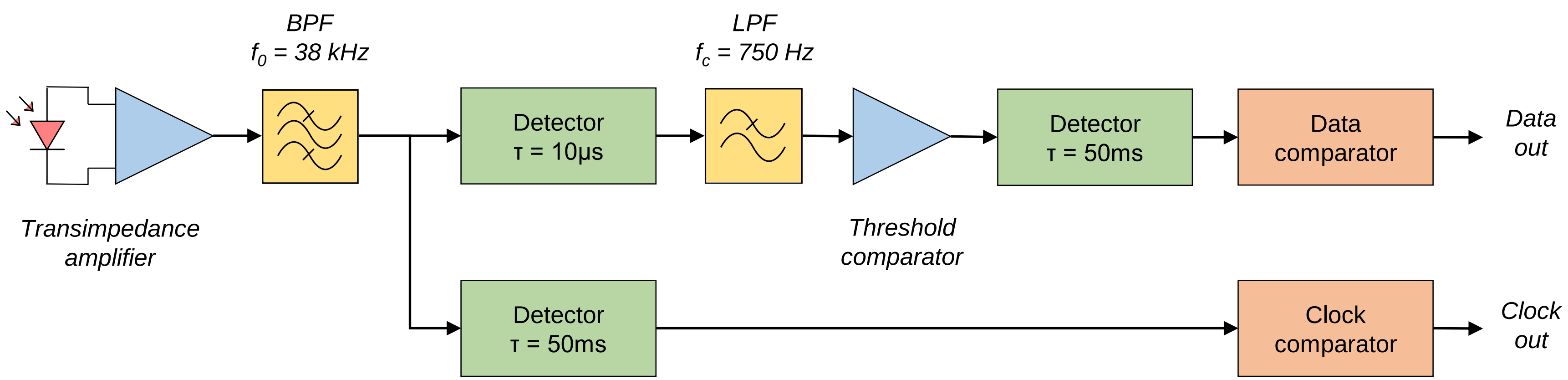
V(out)
15dB
12dB
9dB
6dB
3dB
0dB
-3dB
-6dB
-9dB
-12dB
-15dB
V(out)
-40°
-50°
-60°
-70°
-80°
-90°
-100°
-110°
-120°
-130°
-140°
-150°
-160°
-170°
-180°
10Hz
100Hz
1KHz
10KHz

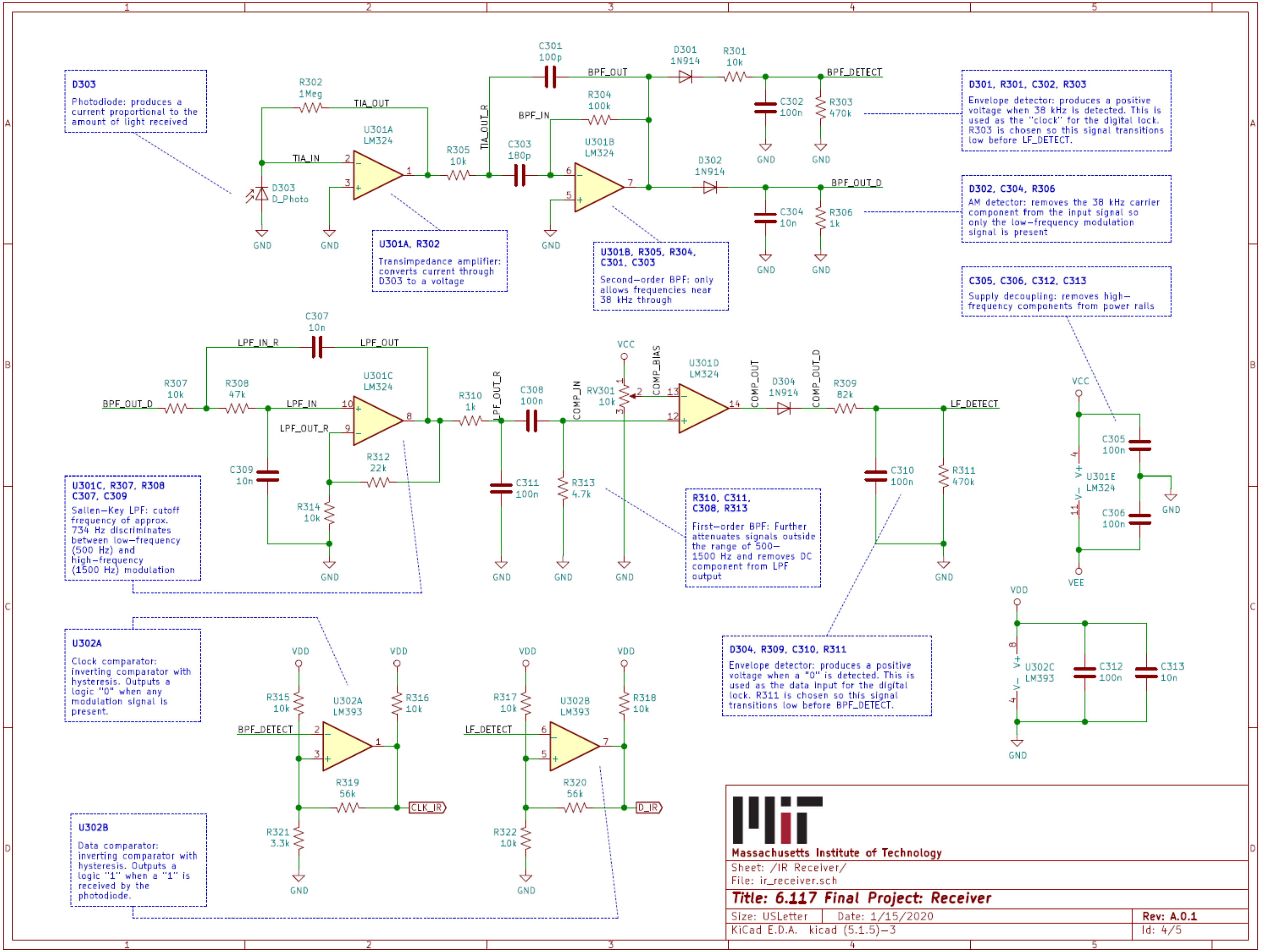
IR receiver

Receiver architecture

- **Goal:** Produce data and clock signals for digital lock
- Need to demodulate the incoming IR signal

IR receiver block diagram (from Lab 4 handout)




D303
Photodiode: produces a current proportional to the amount of light received
U301A, R302
Transimpedance amplifier: converts current through D303 to a voltage
U301B, R305, R304, C301, C303
Second−order BPF: only allows frequencies near 38 kHz through
D301, R301, C302, R303
Envelope detector: produces a positive voltage when 38 kHz is detected. This is used as the "clock" for the digital lock. R303 is chosen so this signal transitions low before LF_DETECT.
D302, C304, R306
AM detector: removes the 38 kHz carrier component from the input signal so only the low−frequency modulation signal is present
C305, C306, C312, C313
Supply decoupling: removes high−frequency components from power rails
U301C, R307, R308 C307, C309
Sallen−Key LPF: cutoff frequency of approx. 734 Hz discriminates between low−frequency (500 Hz) and high−frequency (1500 Hz) modulation
R310, C311, C308, R313
First−order BPF: Further attenuates signals outside the range of 500−1500 Hz and removes DC component from LPF output
D304, R309, C310, R311
Envelope detector: produces a positive voltage when a "0" is detected. This is used as the data input for the digital lock. R311 is chosen so this signal transitions low before BPF_DETECT.
U302A
Clock comparator: inverting comparator with hysteresis. Outputs a logic "0" when any modulation signal is present.
U302B
Data comparator: inverting comparator with hysteresis. Outputs a logic "1" when a "1" is received by the photodiode.
TIA_IN
TIA_OUT
TIA_OUT_R
BPF_IN
BPF_OUT
BPF_DETECT
BPF_OUT_D
LPF_IN_R
LPF_IN
LPF_OUT
LPF_OUT_R
COMP_IN
COMP_BIAS
COMP_OUT
COMP_OUT_D
LF_DETECT
CLK_IR
D_IR
R302 1Meg
U301A LM324
R305 10k
C303 180p
C301 100p
R304 100k
U301B LM324
D301 1N914
R301 10k
C302 100n
R303 470k
D302 1N914
C304 10n
R306 1k
D303 D_Photo
C307 10n
R307 10k
R308 47k
U301C LM324
C309 10n
R312 22k
R314 10k
R310 1k
C308 100n
C311 100n
R313 4.7k
RV301 10k
U301D LM324
D304 1N914
R309 82k
C310 100n
R311 470k
C305 100n
C306 100n
U301E LM324
U302C LM393
C312 100n
C313 10n
R315 10k
U302A LM393
R316 10k
R319 56k
R321 3.3k
R317 10k
U302B LM393
R318 10k
R320 56k
R322 10k
VCC
VEE
VDD
GND
Massachusetts Institute of Technology
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File: ir_receiver.sch
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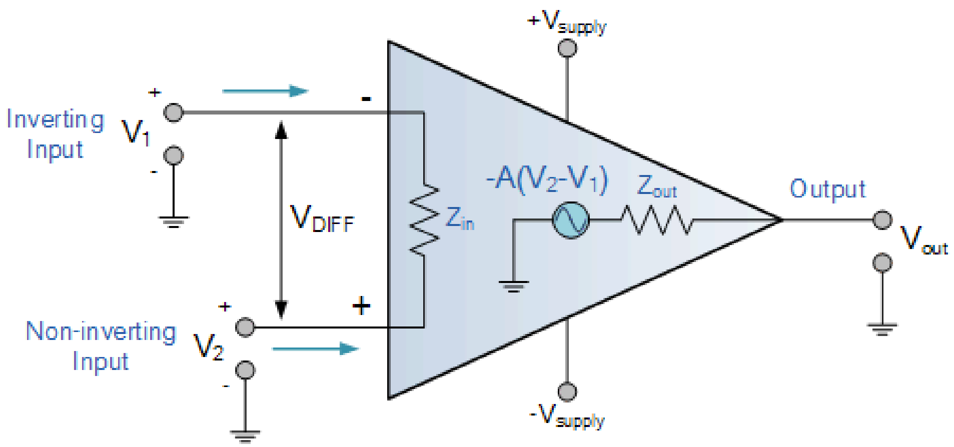
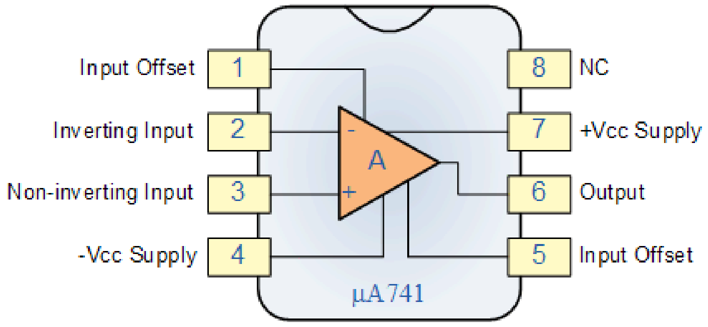
Operational amplifiers

- **Operational amplifier (op-amp):** Amplifies the difference between two voltages
- "Operational": can be used for arithmetic operations (addition, subtraction, multiplication by a constant)
- Many common circuits can be enhanced with op-amps

Op-amp equivalent circuit



uA741 / LM741 pinout diagram



Ideal op-amp properties

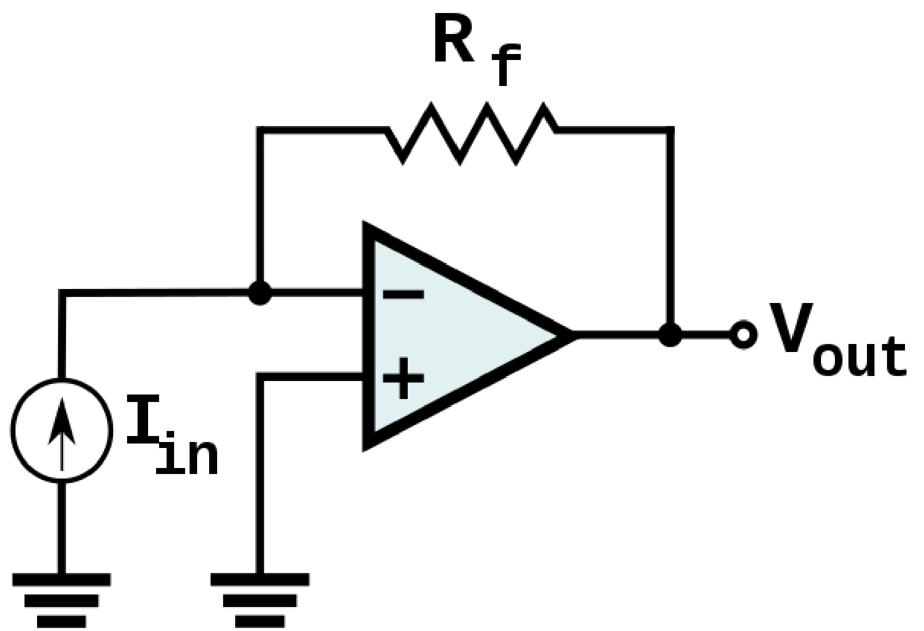
Two “golden rules”[1] of op-amps:

1. In a **closed loop** the output attempts to do whatever is necessary to make the voltage difference between the inputs zero.
2. The inputs draw no current.

[1] Horowitz, Paul; Hill, Winfield (1989). *The Art of Electronics.*

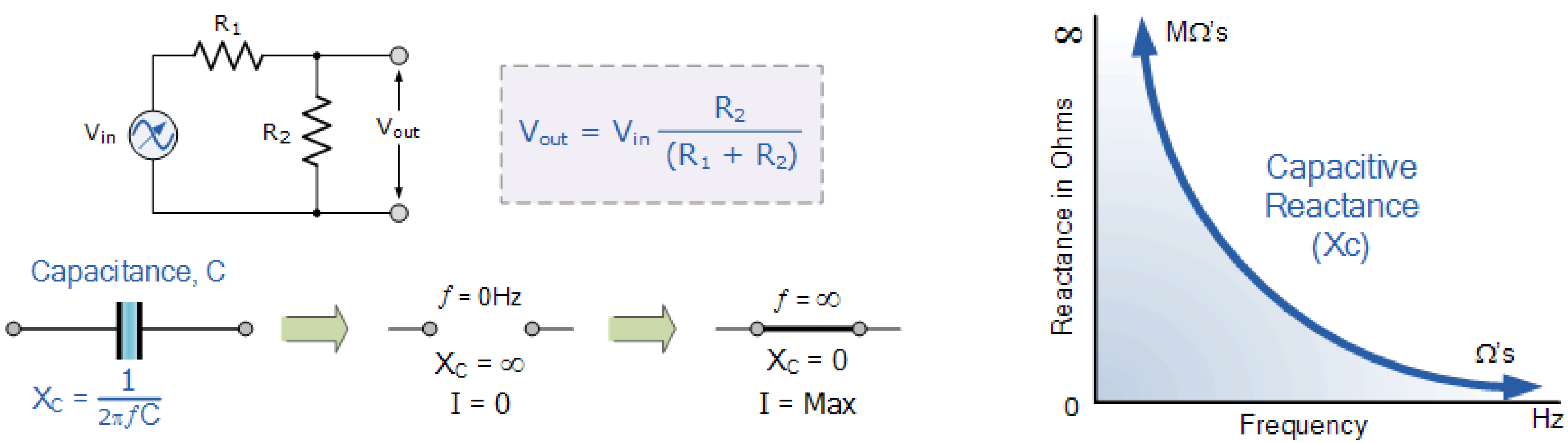
Transimpedance amplifier

- **Transimpedance amplifier:** Converts current to voltage
- Used with photodiode to produce a light-varying voltage



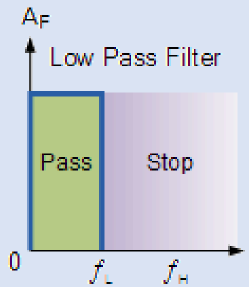
Filtering

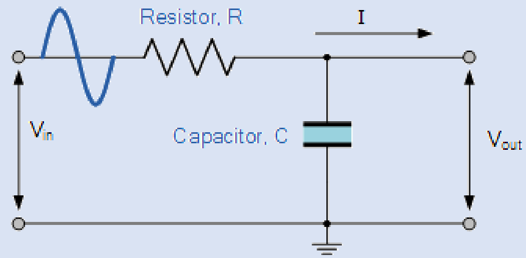
- **Filter:** Circuit whose response depends on the frequency of the input
- **Reactance:** “Effective resistance” of a capacitor, varies inversely with frequency
- Can construct a voltage divider using a capacitor as a “resistor” to exploit this property



Types of filters

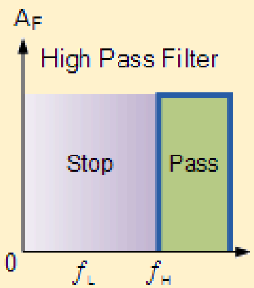
LPF

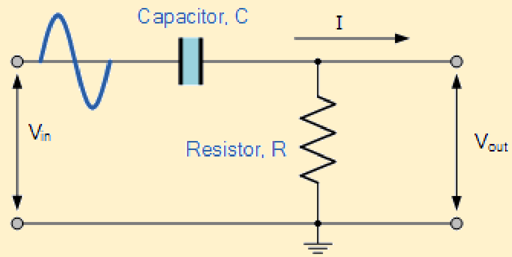




$$f_c = \frac{1}{2\pi RC} Hz$$

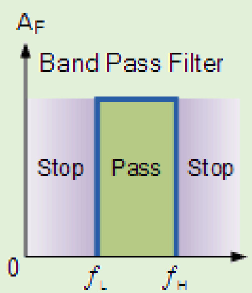
HPF

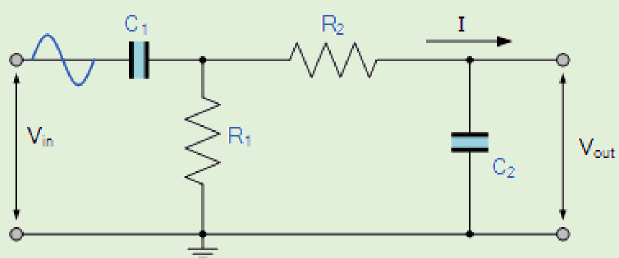




$$f_c = \frac{1}{2\pi RC} Hz$$

BPF





$$f_H = \frac{1}{2\pi R_1 C_1} Hz$$

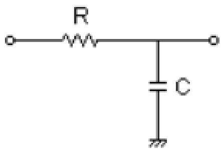
$$f_L = \frac{1}{2\pi R_2 C_2} Hz$$

Transfer functions

- **Transfer function:** Ratio of output to input voltage
- Can be derived with voltage divider analogy

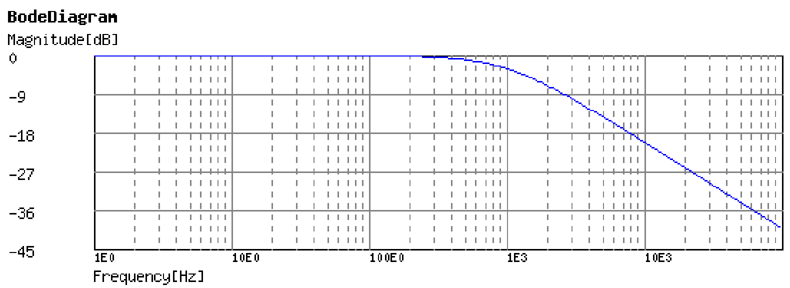
Low-pass filter (LPF)

Vin(s)→



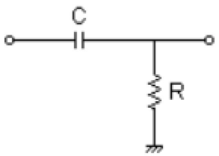
→Vout(s)

$$\frac{Vout(s)}{Vin(s)} = \frac{\frac{1}{CR}}{s + \frac{1}{CR}} \qquad fc = \frac{1}{2\pi RC}$$



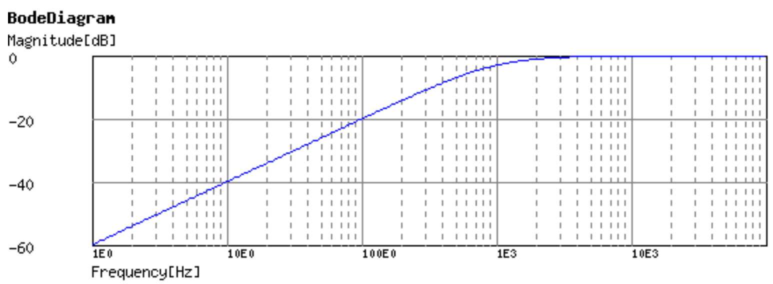
High-pass filter (HPF)

Vin(s)→

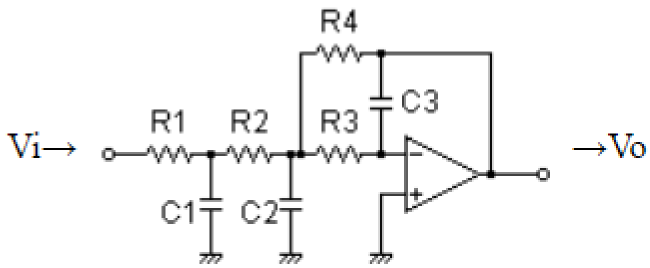


→Vout(s)

$$\frac{Vout(s)}{Vin(s)} = \frac{s}{s + \frac{1}{CR}} \qquad fc = \frac{1}{2\pi RC}$$



Transfer functions

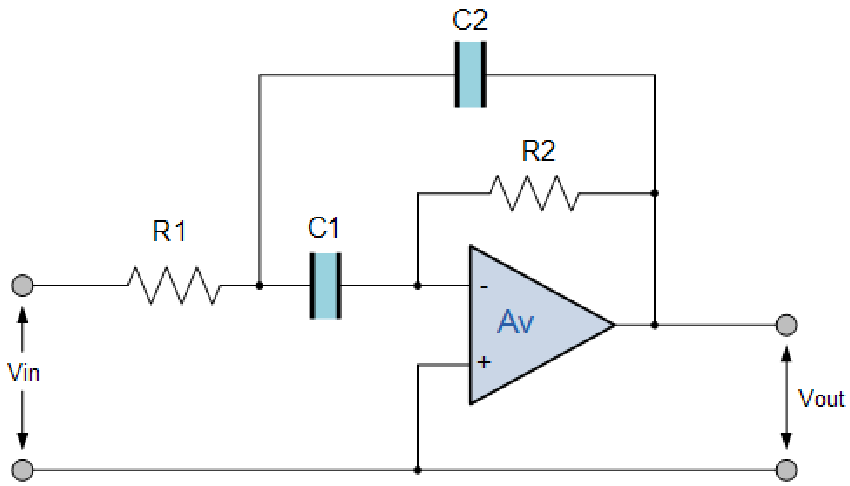


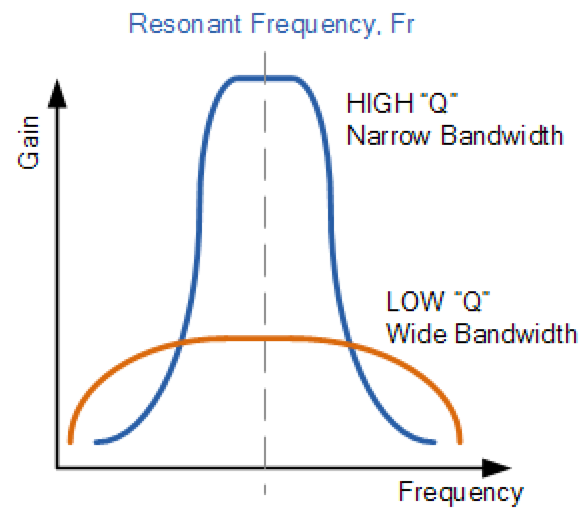
$$\frac{vo}{vi} = \frac{-\dfrac{1}{C1C2C3R1R2R3}}{s^3 + s^2\left(\dfrac{1}{C1R1} + \dfrac{1}{C1R2} + \dfrac{1}{C2R2} + \dfrac{1}{C2R3} + \dfrac{1}{C2R4}\right) + s\left(\dfrac{1}{C1C2R1R2} + \dfrac{1}{C1C2R1R3} + \dfrac{1}{C1C2R2R3} + \dfrac{1}{C1C2R2R4} + \dfrac{1}{C1C2R1R4} + \dfrac{1}{C2C3R3R4}\right) + \dfrac{R1 + R2}{C1C2C3R1R2R3R4}}$$

Equivalent block diagram:

$$Vi(s) \rightarrow \boxed{\frac{2\pi fc1}{s+2\pi fc1}} \rightarrow \boxed{\frac{(2\pi fc2)^2}{s^2+2\zeta(2\pi fc2)s+(2\pi fc2)^2}} \rightarrow Vo(s)$$

“Infinite-gain” BPF





$$f_r = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \qquad Q_{BP} = \frac{f_r}{BW_{(3dB)}} = \frac{1}{2}\sqrt{\frac{R_2}{R_1}}$$

$$\text{Maximum Gain, } (Av) = -\frac{R_2}{2R_1} = -2Q^2$$

Infinite-gain BPF

Center frequency

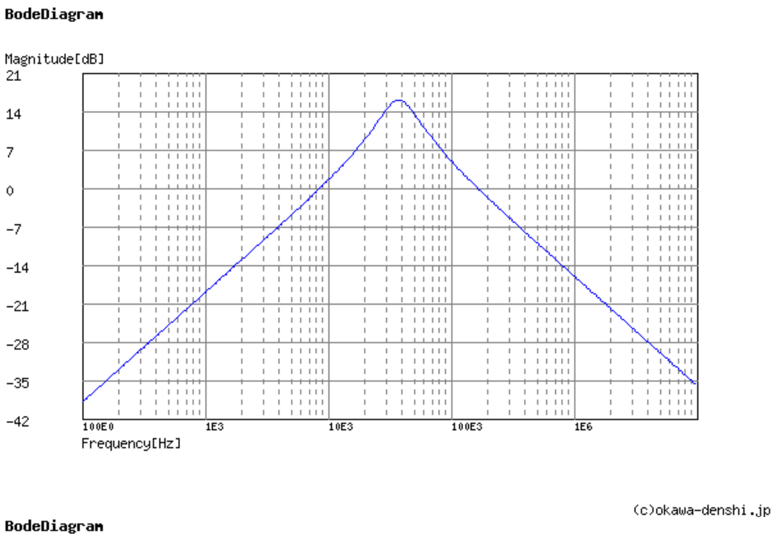
f_0 = 37513.36740531 [Hz]

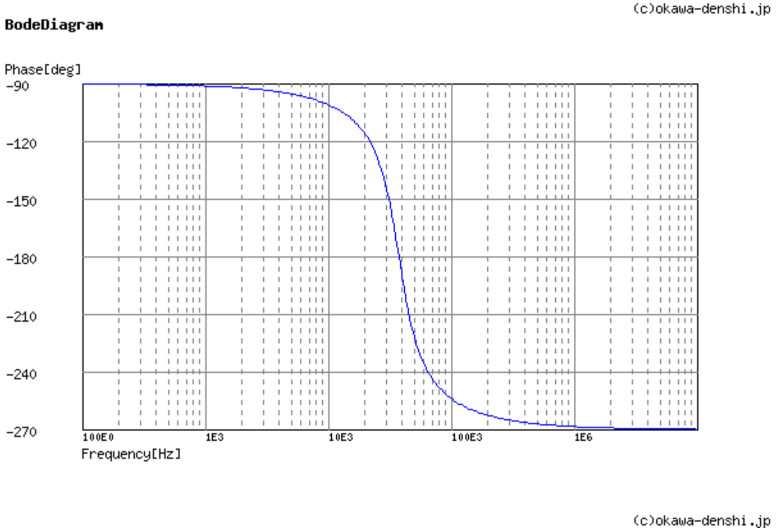
Gain at f_0

G_{pk} = -6.4285714285714 [times]
(16.162289475222) [dB]

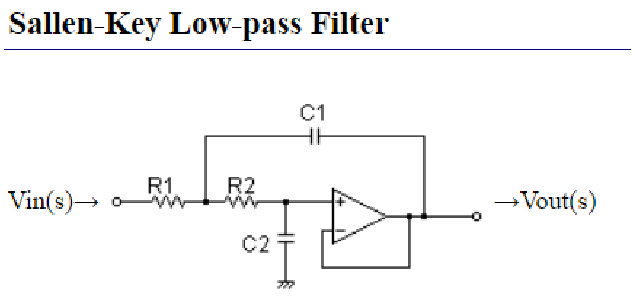
Quality factor

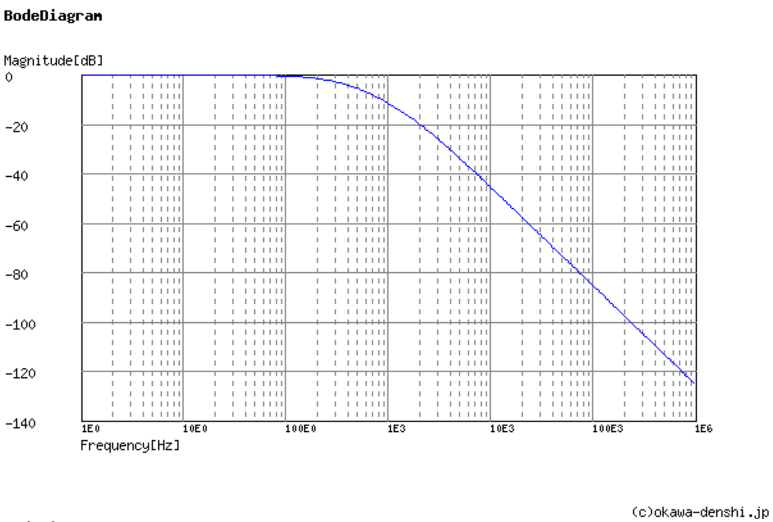
Q = 1.5152363929535





Sallen-Key LPF



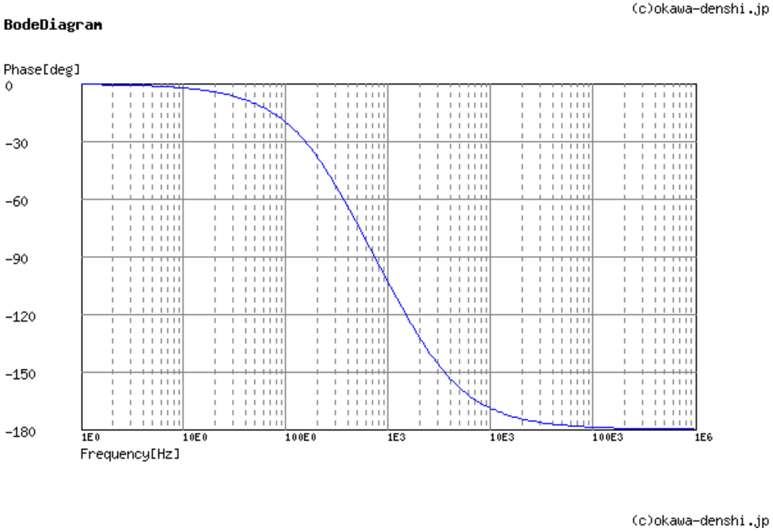


Cut-off frequency

fc = 734.12700957167[Hz]

Quality factor

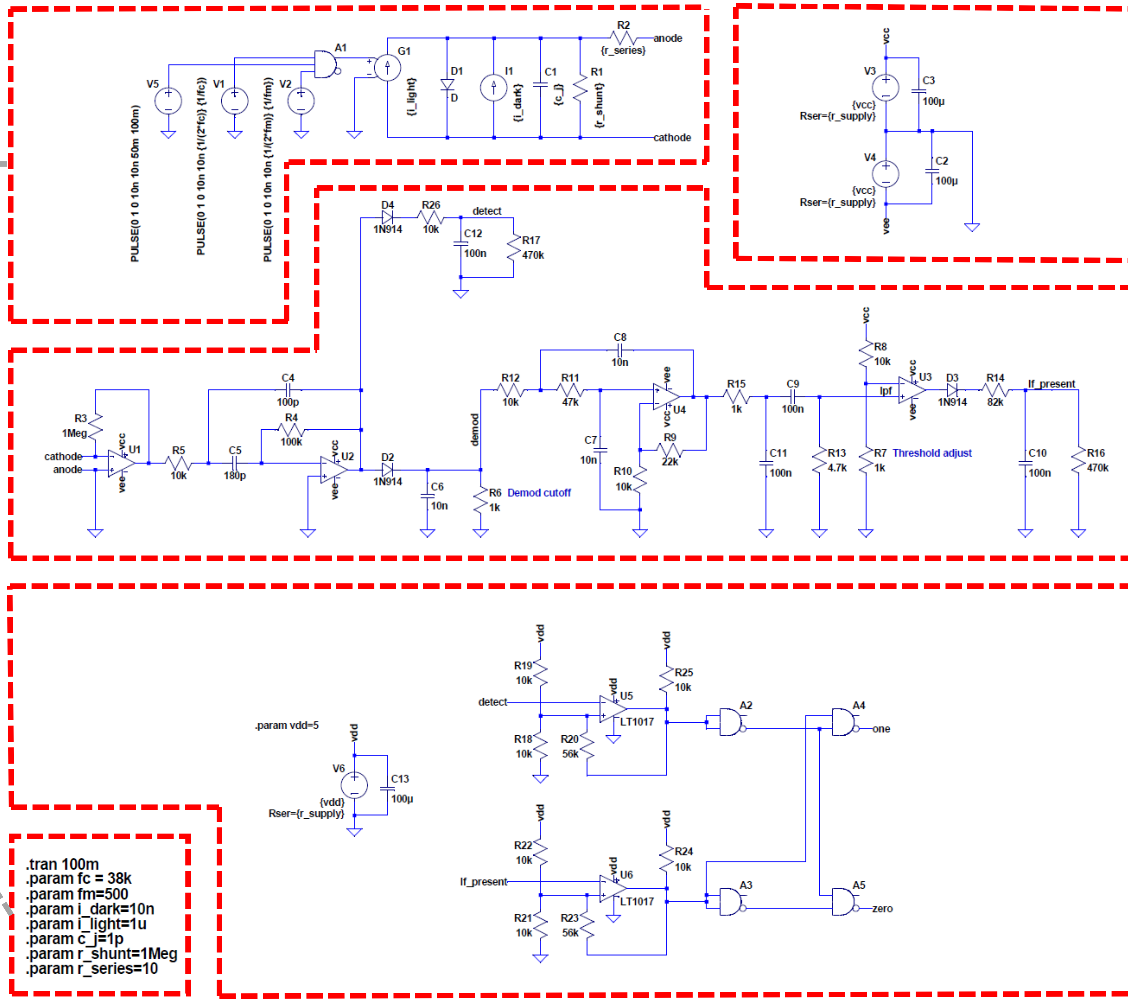
Q = 0.38034181383647



LTSpice model

Photodiode model: Models parasitic resistance and capacitance

Power supply model: Models series resistance and bulk capacitance



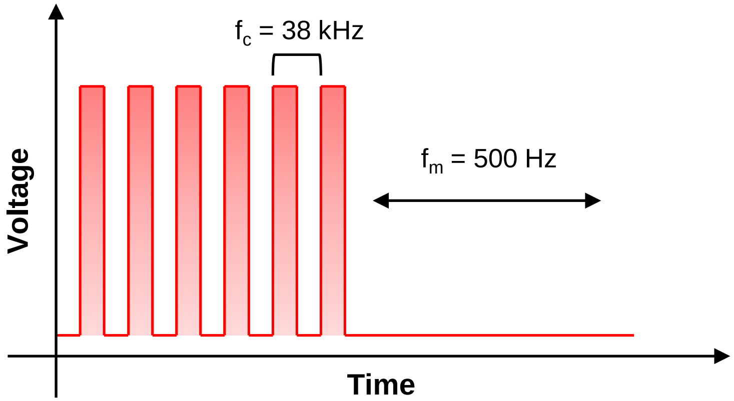
Receiver model: Constructed as on PCB

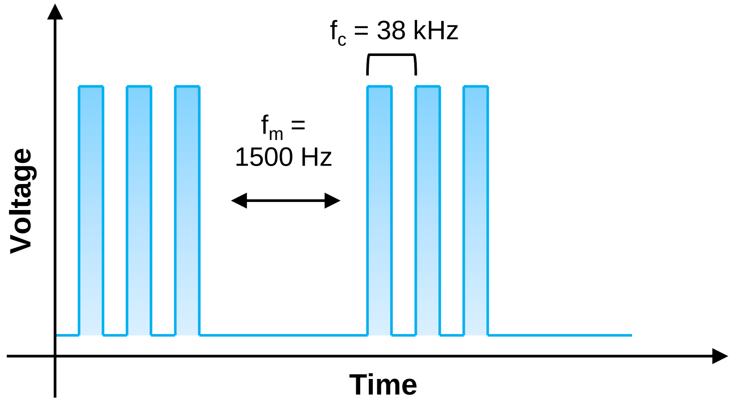
Simulation directives: Assign values to model parameters (supply voltage, modulation frequency, etc.)

Comparator section: Contains AND gates to produce readable simulations

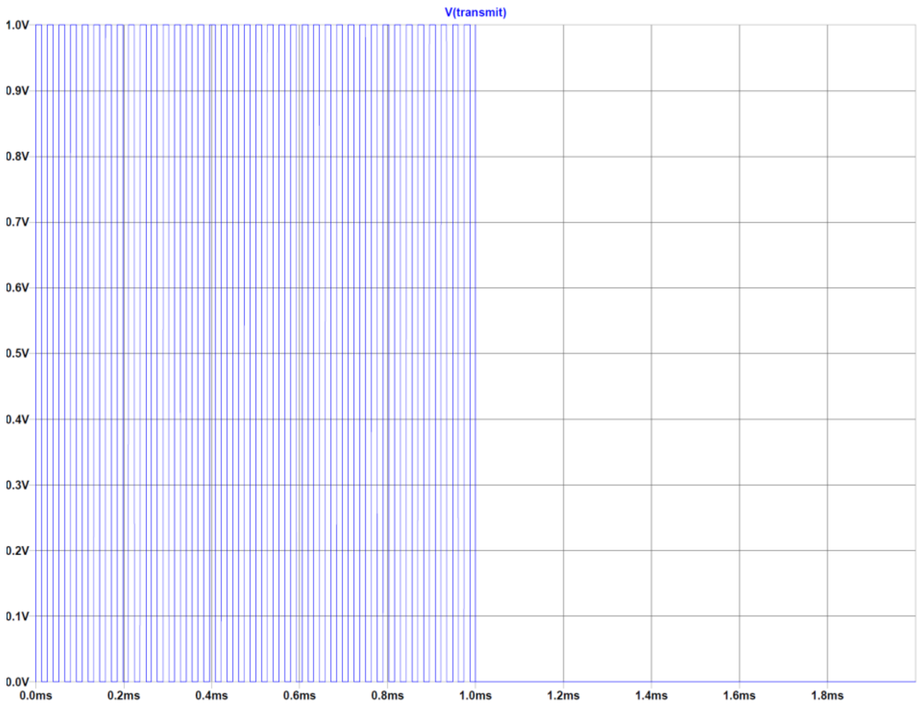
Modulation scheme (not to scale)

- **Amplitude shift keying (ASK):** Changes in amplitude of carrier represent binary data
- **Modulate** with 500 Hz for 0, 1500 Hz for 1





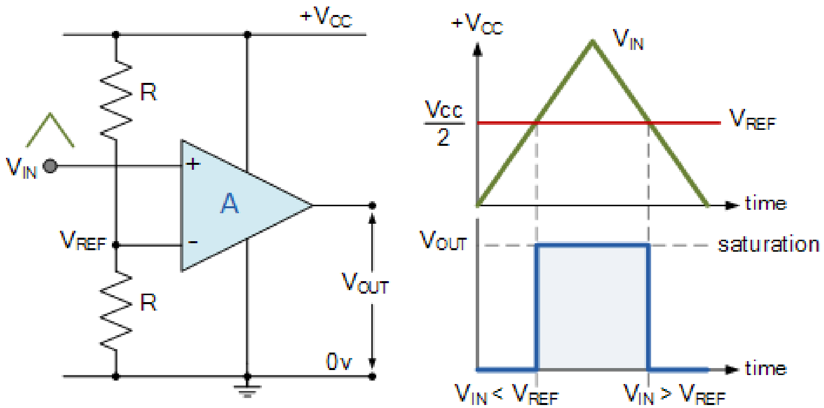
Modulation scheme (to scale)



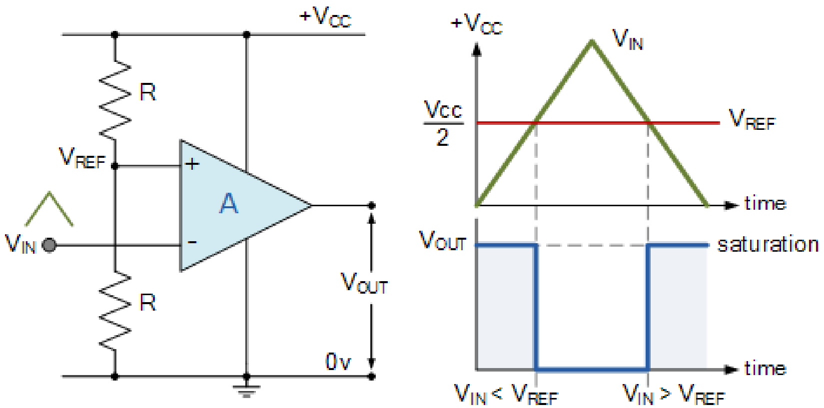
Comparator

- **Comparator:** Compares input voltage (V_{IN}) with reference voltage (V_{REF})
- Exploits “infinite” gain to produce **binary output**
- Most op-amps cannot operate **rail-to-rail**

Non-inverting comparator circuit

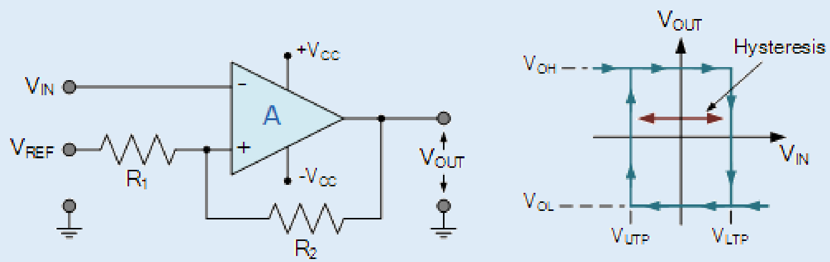


Inverting comparator circuit

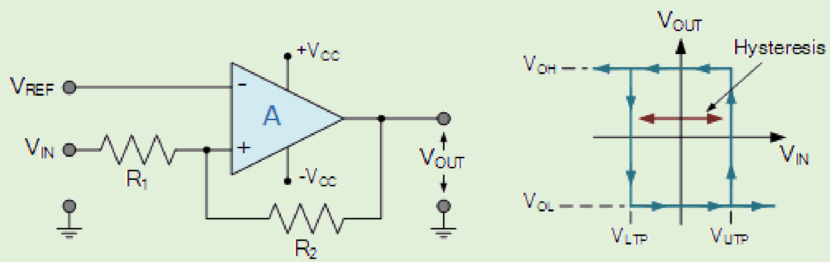


Comparator with hysteresis

- **Hysteresis:** Removes noise from comparator output
- Creates upper and lower "trip points" (V_{UTP} and V_{LTP})
- Amount of hysteresis determined by R_1 and R_2



Inverting comparator with hysteresis



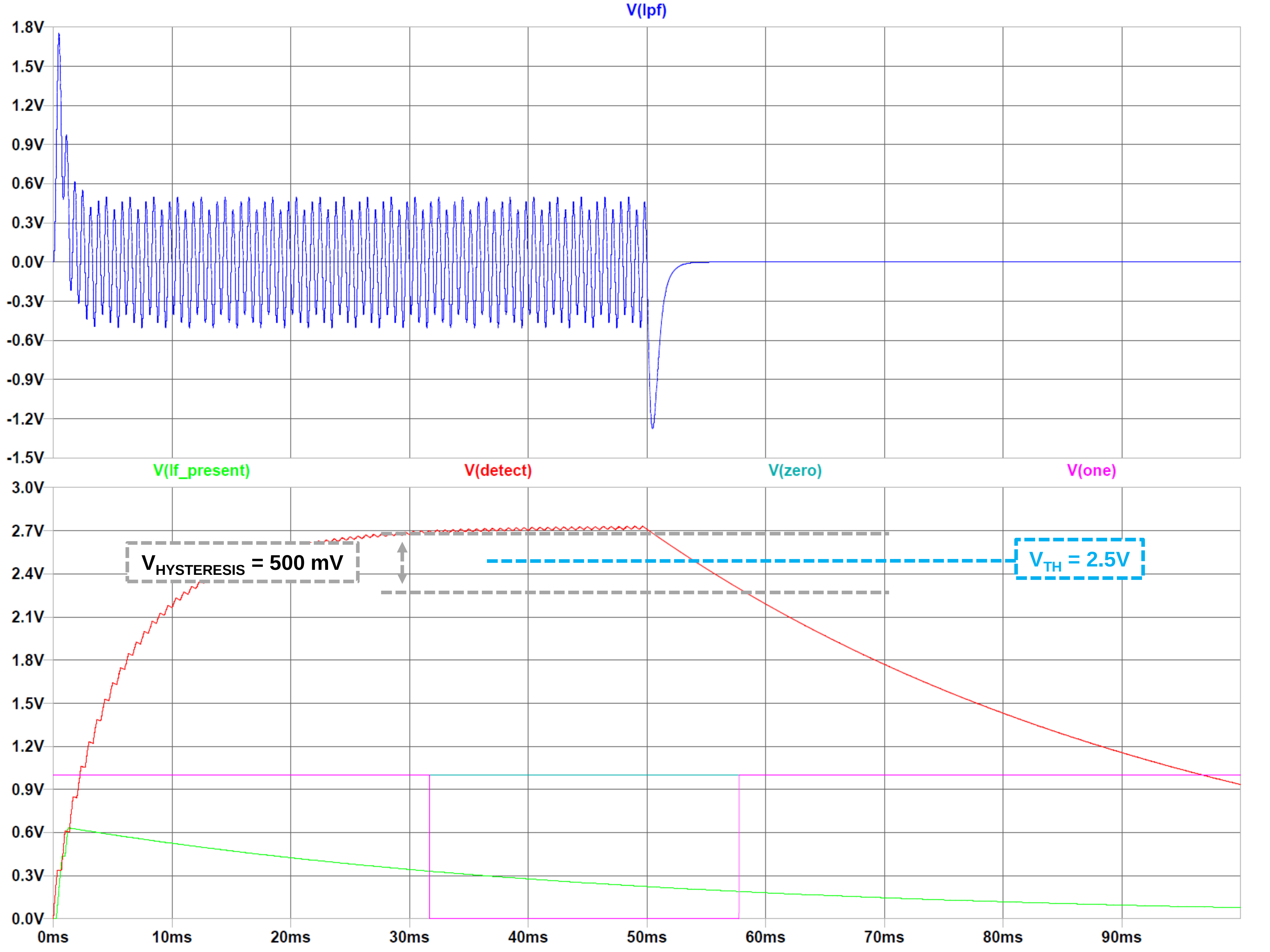
Non-inverting comparator with hysteresis

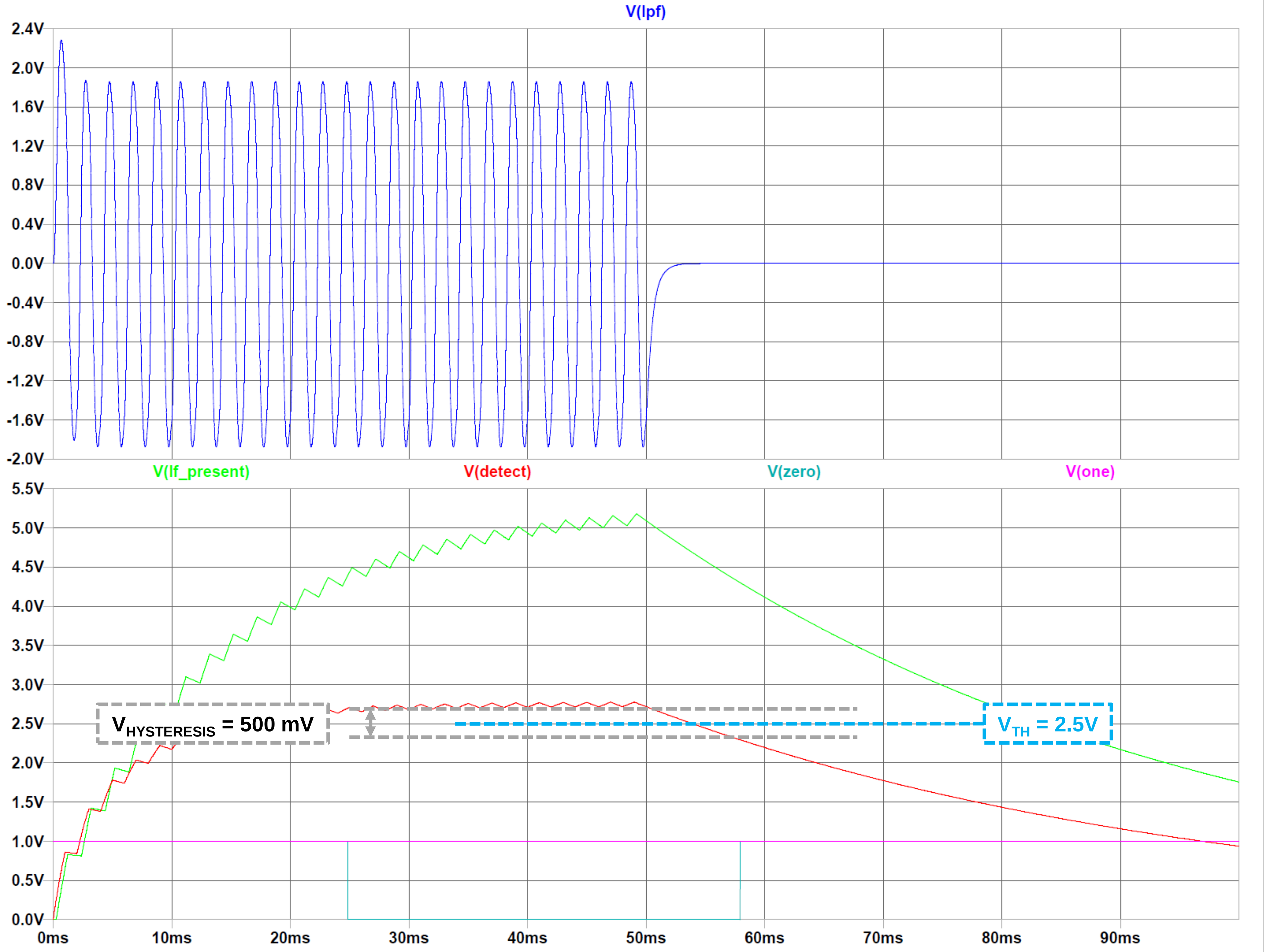
$$\beta = \frac{R_1}{R_1 + R_2}$$

$$V_{HYSTERESIS} = V_{UTP} - V_{LTP}$$

$$V_{HYSTERESIS} = +\beta Vcc - (-\beta Vcc)$$

$$\therefore V_{HYSTERESIS} = 2\beta Vcc$$


V(lpf)
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
-0.3V
-0.6V
-0.9V
-1.2V
-1.5V
V(lf_present)
V(detect)
V(zero)
V(one)
3.0V
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
V_HYSTERESIS = 500 mV
V_TH = 2.5V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
90ms



V(lpf)
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
V(lf_present)
V(detect)
V(zero)
V(one)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V_HYSTERESIS = 500 mV
V_TH = 2.5V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
90ms

Course conclusion

Related courses

Intro

- 6.002 (Circuits and Electronics)
- 6.003 (Signals and Systems)
- 6.004 (Computation Structures)

Lab (advanced)

- 6.101 (Analog Electronics Laboratory)
- 6.111 (Digital Electronics Laboratory)
- *6.131 (Power Electronics Laboratory)*

Wrapping up

Please complete subject evaluations

In particular,

- Were the labs too long/too short?
- Should the lectures focus more or less on theory?

EE Careers and Experience Panel

Friday, 1 – 3pm in 4-231