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# 8-Bit 250-MS/s ADC Based on SAR Architecture with Novel Comparator at 70 nm Technology Node

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**Abstract**

The data converters are prerequisite for digital processing of analog signals. SAR ADC is preferred for their good balance between speed, area and power considerations. In this paper, we proposed a novel comparator design based on double tail architecture for an 8-bit successive approximation register analog-to-digital converter. We implemented 8 bit analog-to-digital converter contains a Successive Approximation register , Ring counter , SR-Latch, R2R Ladder type digital-to-analog convertor and a proposed novel comparator. The circuit is simulated using Predictive Technology model 70nm Technology using Tanner EDA tool. The average INL and DNL are less than 1 LSB and 1 LSB, respectively. At the sample rate of 250 MHz (2GHz clock Freq) and supply voltage of 1.2 V, the ADC consumed about 1.3 mW. The analog-to-digital converter using proposed comparator deign consumes less power and thus can be used in portable device.


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*Keywords:* SAR; ADC; Comparator; INL; DNL

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## 1. Introduction

Analog to digital convertor and digital to analog converters are the link between analog real world and digital world of data processing. In Analog world signal processing is limited by SNR, in Digital world number of bits plays the similar role. This implies larger the number of bits in ADC/DAC better will be SNR in Analog domain; similarly the bandwidth is governed by sampling speed. Highest frequency that can be reliably fed to system from continues world, cannot be greater than half of sampling frequency. Due to recent advances in technology the digital processing ability has grown tremendously, processors are available that can work with 64 bit data and operating at GHz clock frequency. In such scenario ADCs are becoming the bottleneck due to complexity of the process. This leads to trade-off between speed, area, power and accuracy. There are a number of architectures available based on these tradeoffs, for example flash type ADC can deliver output code at more than 5 Giga sample/sec [1] but resolution is less and needs large area and power, Sigma delta ADCs on the other hand gives accurate results at the cost of speed. Successive Approximation Register ADC is one such architecture. This architecture has many advantages and balanced performance thus amongst available ADC architectures SAR is suited for low power and low voltage design [2]. One of the main advantages of this architecture is that only comparator and DAC needs analog designing considerations and all other components are in digital domain.

The SAR ADCs have excellent power efficiency [3].Emerging electronic systems need a good balance between speed power and area. Though the scaling of MOSFET enhances area speed and power performance, but the performance pattern remains similar i.e. Flash ADCs will be faster than sigma delta ADCs at same technology node.

The ADC market for medium- to high-resolution ADCs majorly uses Successive-Approximation-Register (SAR) analog-to-digital converters. Many SAR ADCs have been reported that can deliver more than 100 MSPS sampling rates with 8 to 18 bits of resolution. The SAR architecture allows for high-performance, low-power ADCs to be packaged in small form factors for today's demanding applications [4].

In this paper a novel design for comparator is proposed in SAR ADC Architecture. Organization of this paper is as follows: Section 2 describes the previous work related to different SAR ADC. Section 3 discusses individual blocks of ADC. Section 4 presents the simulation results followed by the conclusion in section 5.

## 2. Related Work

Several SAR ADCs have been reported recently. A 40MS/s Pipelined SAR ADC [5] is discussed the ADC is in 65nm Technology with supply voltage of 1V and has a 8.9 bit ENOB. This ADC uses binary weighted capacitor DAC. The architecture also uses a CMFB opamp. The total power consumption is reported to be 1.2mW and half of this power was consumed by the opamp alone. 9-bit SAR ADC with 150 MS/s using hybrid architecture [6] of flash and SAR. Flash was used to generate MSBs and SAR architecture was used for generate 6-LSBs This ADC has a power consumption of 1.53mW at 1.2V supply. A 9 bit 100MS/s ADC without track and hold the ADC [7] is implemented in 45nm technology with 1V power supply. A dynamic comparator is used in this ADC. The DNL and INL are mentioned to be 0.94 and 0.66 LSB respectively.

## 3. ADC Architecture

The architecture of a successive approximation analog to digital convertor is shown in Fig 1(a). The comparator is heart of the convertor as comparators performance matrices governs many of the performance matrices of ADC. The comparator compares the analog input provided by Sample and hold circuit with the DAC output. The SAR register generates the next guess according to input provided by comparator. This guess is in digital world and is converted to analog domain using a

digital to analog convertor which is provided to comparator.

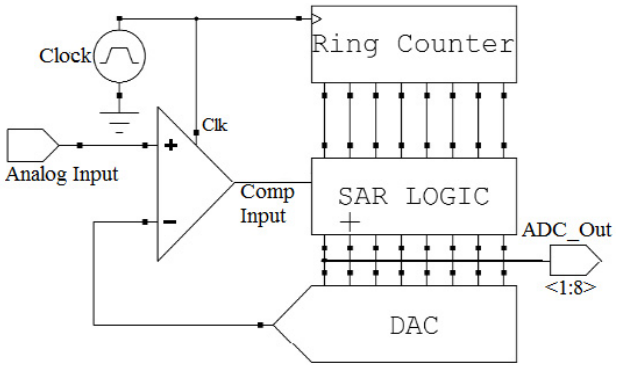
The working algorithm is discussed in brief here. Every clock cycle one bit of Successive Approximation Register is set to high as a guess. The DAC generates the analog equivalent of this code. The analog value is compared against analog input from real world, if the guessed value is smaller than current analog value then this guess is valid and maintained, else if guess evaluates larger than the analog input value then the latest guessed bit is discarded and the bit is set back to low. This process goes on for each bit sequentially, starting from MSB to LSB. Thus taking 'n' clock cycles for n-Bit ADC.

### *3.1. Ring Counter*

The ring counter is realized using eight D-flip-flops connected in series to form a shift register. The output of last flip flop is fed back to input of first bit. The D-flip-flop used in ring counter is realized using two D latches in master slave configuration as shown in Fig 1(b). The D Latch is realized using 2:1 Multiplexer using CMOS logic as shown in Fig 2(a). The multiplexer logic is modified to incorporate preset or clear logic. The CMOS implementation is shown in Fig 3(a). As in CMOS Logic we get the complemented output of the function being implemented, an inverter is placed to get back un-inverted output. This inverter is in D to Q path and decreases the speed of operation. It can be observed that the data coming is inverted twice from $D_{in}$ of master to Q out of slave latch. Thus to reduce the critical path the inverter within MUX is placed such that it is removed from the critical path as shown in Fig 1(a). The data entering the slave is complement of Din and it is complemented back again at slave latch. This reduces the Clock to Q delay and helps keeping width of MOSFETs small otherwise large MOSFETs are required to improve upon speed.

### *3.2. Successive Approximation Register (SAR)*

A SR Latch is used to obtain the $n^{th}$ bit. The latch is used instead of flip flop as flip flop would have introduced one clock latency if used synchronously and also the master slave configuration means extra space in layout. The logic one of the ring counter is used to set high the current bit under consideration. The block diagram for one bit of SAR logic is shown in Fig 2(b). The output of latch is Set if corresponding Ring counter bit turns high. This new bit turned on is the new guess of SAR. Simultaneously it is also required to reset output of previously set bit if it was wrong guess which is indicated by Comparator output. If comparator output goes high this indicates that output of DAC has exceeded input analog value. The problem here is that if all the SR Latches are connected to comparator output then all the SR latches will respond to this comparator signal. Thus to ensure that only previous bit is reset the comparator output is ANDed with Ring counter output of next bit (n+1 bit) before feeding to reset i.e. only previous SR Latch whose response is current comparator output, responds to reset.



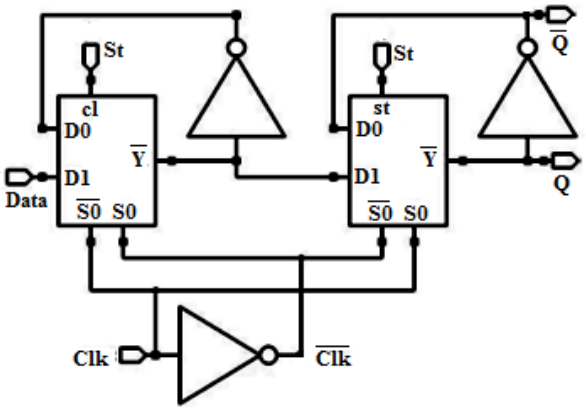



Fig. 1: (a) SAR Architecture (b) Realization of D flip flop with reduced critical path delay

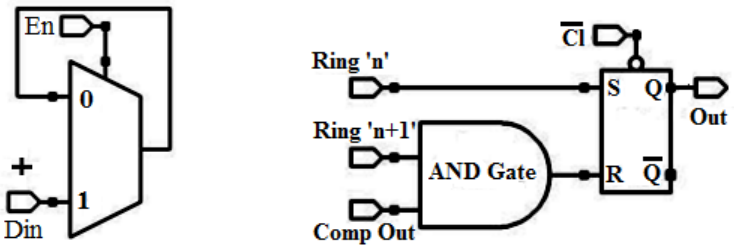



Fig. 2: (a) D latch using 2:1 MUX (b) SAR Logic using SR Latch

### *3.3. Comparator*

The Comparator is one of the most important blocks of any ADC. In fact it can be said that comparators are the fundamental Analog to digital converters generating one bit of digital data. Rest of the circuits just converts this one bit digital information to required N-bit data. Many comparator architectures have been reported to be used for ADC like latched comparator, dynamic comparator, double tail comparator. Double tail architecture is considered good for attaining a high speed of operation at low supply voltage [8], as it has lower the number of cascode transistors. The positive feedback latch is isolated from input by the preamplifier stage and thus provides low kickback noise [9]. Transition of comparator node is shown in Fig. 5(a).

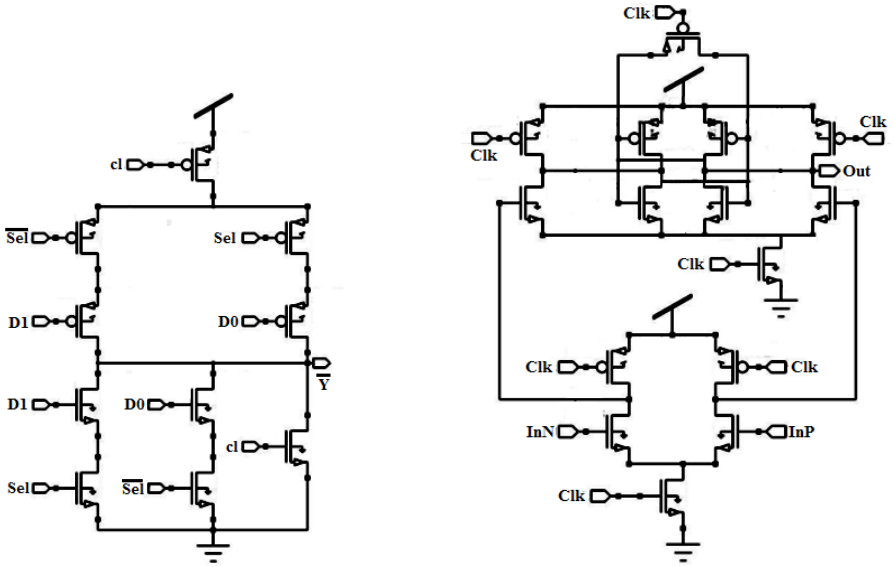



Fig. 3: (a) 2:1 MUX for D-latch with clear signal (b) Comparator used in the ADC

A novel comparator architecture based on double tail architecture is proposed. The comparator takes 184ps to resolve 2mv input voltage difference and operates at 2GHz clock frequency. The resolution is good enough for 8bit ADC working at 0.6 volts operating range (1.2Volts power supply). The comparator is shown in Fig. 3(b). The comparator output is used to Reset All SR Latch in SAR Logic thus it needs to have large fan-out. The comparator output is strengthened using an inverter chain.

### *3.4. Digital to Analog Converter*

Many DAC architectures are available to convert a digital signal to analog domain, each having its own pros and cons i.e. current steering, charge scaling, voltage division [10] for this work R2R Ladder architecture is used for digital to analog convertor due to its simple architecture[11]. The R2R Ladder has two flavors current mode R2R ladder and voltage mode R2R ladder. Voltage mode R2R is preferred in this work as it don't need a operational amplifier at output stage [12], also input impedance in voltage mode vary, but output impedance is constant and equal to 'R' of R-2R ladder[13]. This helps handling kickback noise of comparator. A resistor of value 'R' is placed at the analog input terminal of comparator. The kickback currents are almost same in both inputs. The resistance seen by both terminals is equal and thus has same kickback voltages jerks. Due to differential nature of comparator effect of this noise is very much reduced.

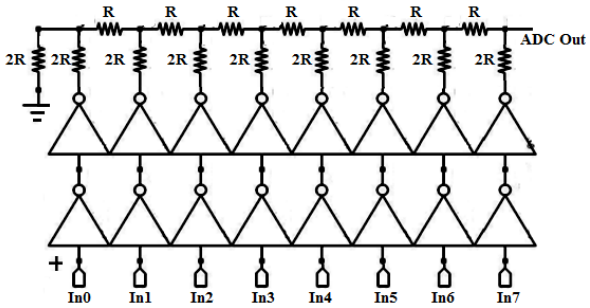



Fig. 4: R-2R Ladder DAC used in ADC

Implementation of R-2R Ladder is as shown in Fig 4. R of R-2R ladder is set to 50KΩ. The R2R

ladder is driven by a large Inverter so that it should be able to drive large currents needed to drive resistive load and to minimize output resistance shown by inverter which may add to resistance mismatch [11]. To drive this large inverter chain with ratio e (= 2.71) is used.

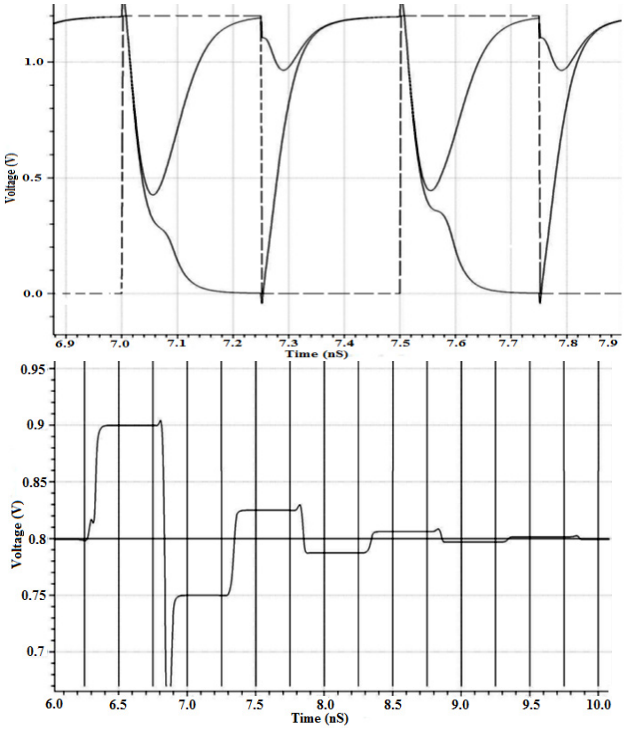



Fig. 5: (a) Transition of comparator nodes (b) Output of DAC during a conversion

## 4. Simulation Results

The SAR ADC was simulated using PTMs (Predictive Technology Model) 70nm Technology model file. The power supply of 1.2 Volts is provided. A single clock of 2GHz is used to drive ring counter and comparator. The time period of one conversion thus is 4ns for 8bit ADC this infers a conversion rate of 250 Mega samples per sec. The conversion cycle is shown in Fig 5(b). The output of DAC is plotted with time on x axis for a given input voltage (a Dummy DAC was placed in parallel to DAC in loop, so that kickback noise can be avoided in graph). The power Consumption of the ADC was noted to be 1.3mW.

### *4.1 Histogram Test*

The standardized ramp histogram test [14] was used to find dynamic non linearity (DNL) and Integral non linearity (INL). A staircase signal with step size 100μV was given as input over a range of 0.6V to 1.2V. The number of samples generating each code was noted. The histogram plot for DNL is as shown in Fig 6(a). INL is computed by integrating DNL and is plotted in Fig 6(b). Both INL and DNL can be observed to be less than 1 LSB.

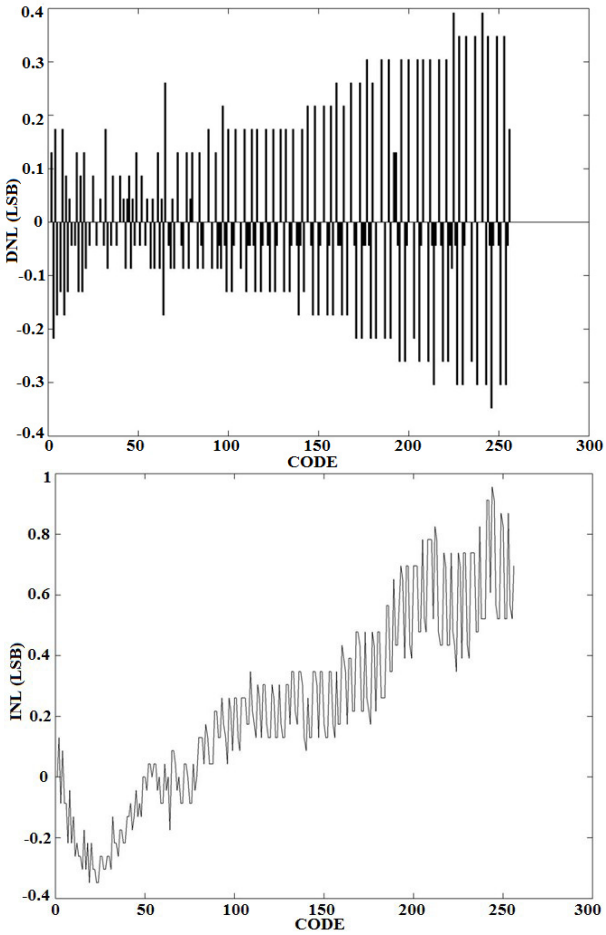



Fig. 6: (a) Histogram for DNL (b) INL graph obtained by integration of DNL

Table 1. Comparison to state of art works and specification summary

| Specification (Unit) | [5] | [6] | [7] | This Work |
|---|---|---|---|---|
| Supply Voltage (Volts) | 1.1 | 1.2 | 1 | 1.2 |
| Sampling Rate (MS/s) | 40 | 150 | 100 | 250 |
| Power Consumption (mW) | 1.21 | 1.53 | 6.1 | 1.3 |
| FOM (fJ/Conv.-step) | 65 | 24.7 | -- | 20.3 |
| Architecture | SAR | Flash + SAR | SAR | SAR |
| Resolution (Bit) | 9 | 9 | 9 | 8 |
| INL (LSB) | -- | 0.48 | 0.66 | 0.9 |
| DNL (LSB) | -- | 0.48 | 0.94 | 0.4 |
| Process technology | 65 nm | 90 nm | 45 nm | 70 nm |

## 5. Conclusion

A 8-bit 250 MS/Sec Successive Approximation Resister ADC with a novel comparator is presented. The proposed ADC draws a small power of 1.3mW at 1.2 volts supply and 2GHz clock frequency. The proposed comparator which is a variant of double tail comparator works effectively at low supply voltage of 1.2 volts due to less stacking of MOSFET and generates low kickback noise attained 8 bit precision.

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