A 2.4-GHz Monolithic Fractional-N Frequency Synthesizer With Robust Phase-Switching Prescaler and Loop Capacitance Multiplier

Keliu Shu, *Student Member, IEEE*, Edgar Sánchez-Sinencio, *Fellow, IEEE*, José Silva-Martínez, *Senior Member, IEEE*, and Sherif H. K. Embabi, *Senior Member, IEEE*

***Abstract*—The design of a 2.4-GHz fully integrated ΣΔ fractional-N frequency synthesizer in 0.35-μm CMOS process is presented. The design focuses on the prescaler and the loop filter, which are often the speed and the integration bottlenecks of the phase-locked loop (PLL), respectively. A 1.5-V 3-mW inherently glitch-free phase-switching prescaler is proposed. It is based on eight lower frequency 45°-spaced phases and a reversed phase-switching sequence. The large integrating capacitor in the loop filter was integrated on chip via a simple capacitance multiplier that saves silicon area, consumes only 0.2 mW, and introduces negligible noise. The synthesizer has a 9.4% frequency tuning range from 2.23 to 2.45 GHz. It dissipates 16 mW and takes an active area of 0.35 mm^2 excluding the 0.5-mm^2 digital ΣΔ modulator.**

***Index Terms*—Capacitance multiplier, CMOS, fractional-N, frequency synthesizer, loop filter, phase-switching prescaler, phase-locked loop (PLL), sigma–delta (ΣΔ).**

I. Introduction

THE phase-locked loop (PLL)-based frequency synthesizer (PLL-FS), shown in Fig. 1, is a critical component for frequency translation and channel selection in wireless transceivers. A fully integrated frequency synthesizer in CMOS is preferable because of its low cost, reliability, and small printed circuit board area. There are two highlights of the proposed frequency synthesizer, namely, an enhanced low-power inherently glitch-free phase-switching prescaler and an area- and power-efficient integratable loop filter based on a capacitance multiplier.

Since the on-chip *LC* oscillator can operate at very high frequencies, the prescaler becomes the speed bottleneck of the high-frequency PLL designed in CMOS technology. Usually, the prescaler consumes lots of power and takes a significant chip area, and its operating frequency is limited by the CMOS technology [1]–[4]. The conventional prescaler uses a ÷4/5 (or ÷3/4, ÷2/3, etc.) synchronous counter as its input stage. The three (or two) flip-flops (FFs) in this input stage are clocked by the voltage-controlled oscillator (VCO) output, and are usually power hungry [1]–[6]. Furthermore, compared with the asynchronous ÷2 frequency divider, this synchronous stage often can only operate at a much lower input frequency.

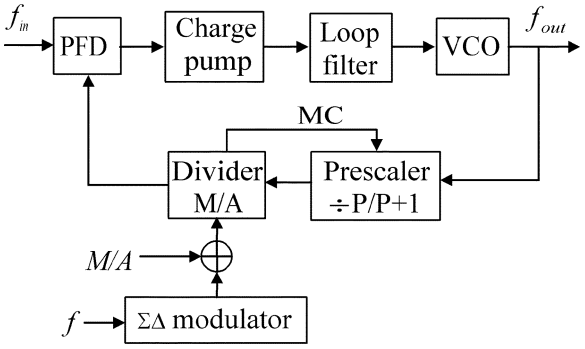

Fig. 1. ΣΔ fractional-N frequency synthesizer.

The existing phase-switching prescaler [7]–[10] generates four 90°-spaced phases using two stages of ÷2 divider in cascade. Then it uses a 4-to-1 multiplexer (MUX) to switch from one phase to the next phase lagging 90°. This architecture exploits the toggling speed of a flip-flop or even an analog ÷2 frequency divider, and thus, it can work much faster than the conventional prescaler based on the synchronous counter. However, the main drawback of this approach is the potential glitches, which can cause the following counter to miscount. Various significant efforts have been made in the literature to remove the glitches [7]–[10]. Unfortunately, these glitch-removing techniques either involve substantial power and/or reduce the maximum operating speed. Furthermore, the phase-switching operation is still not robust enough with these existing glitch-removing techniques.

In this paper, an enhanced low-power and inherently glitch-free phase-switching prescaler is proposed. We judiciously arranged the phase-switching sequence in the prescaler to avoid glitches. Furthermore, the phase-switching is made between eight 45°-spaced phases. The resulting architecture both reduces power consumption and improves circuit robustness.

The loop filter is a barrier in fully integrating the narrow-band PLL because of its large integrating capacitor. To make the loop capacitance as small as possible while keeping the same loop bandwidth, designers increase the loop resistance and reduce the charge-pump current. However, there are practical limitations for both the loop resistance and the charge-pump current.

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K. Shu, E. Sánchez-Sinencio, and J. Silva-Martínez are with the Analog and Mixed-Signal Center, Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: sanchez@ee.tamu.edu).

S. H. K. Embabi is with Texas Instruments Incorporated, Dallas, TX 75243 USA.

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Thermal noise in the large resistor modulates the VCO control voltage and generates phase noise, and the charge-pump noise increases when the current decreases.

The dual-path topology has been a popular solution to this problem [11]–[15]. It equivalently scales down the large integrating and zero-generating capacitance by the scaling factor of the dual charge-pump currents. Besides increased noise and power due to active devices, the charge pump of the integration path is still working with a very small current and contributes significant noise. Also, the delay mismatch of the dual charge pumps may change the loop filter parameters. Furthermore, for the implementations in [12]–[14], the voltage decay of the low-pass path causes undesirable ripples on the VCO control voltage.

To overcome the constraints of the dual-path topology, a novel loop filter solution is proposed in this work. A capacitance multiplier [16] based on current techniques is used to reduce the capacitance by a large factor, and make it easily integratable within a small area.

Section II explains the architecture of the frequency synthesizer. The designs of the proposed prescaler and loop filter are covered in Sections III and IV, respectively. Section V addresses the implementation of the other building blocks of the frequency synthesizer. Experimental results are presented in Section VI. Finally, conclusions are drawn in Section VII.

II. Synthesizer Architecture

The synthesizer is based on the $\Sigma\Delta$ fractional-N PLL architecture [17], [18]. The block diagram of the $\Sigma\Delta$ fractional-N frequency synthesizer is illustrated in Fig. 1. It consists of a phase-frequency detector (PFD), a charge pump, a loop filter, a VCO, a dual-modulus prescaler, and a programmable divider. In this monolithic design, the VCO was integrated with on-chip spiral inductors, and the on-chip loop filter was implemented by means of a capacitance multiplier. A dual-modulus prescaler (divide ratio P or $P+1$) and a programmable pulse-swallowing divider are used in this scheme. A feedback from the divider is for the prescaler's modulus control (MC). M and A are programmable integers and f is a programmable fraction. The nominal frequency divide ratio is $N = M \cdot P + A + f$.

III. Enhanced Phase-Switching Prescaler

To overcome the disadvantages of the existing phase-switching prescaler mentioned in Section I, an enhanced inherently glitch-free phase-switching prescaler, as shown in Fig. 2, is suggested in this design. One additional divide-by-2 stage is added to further divide down the input signal before phase switching occurs. This stage consists of two master–slave FFs in parallel to generate eight 45°-spaced phases, $p0$–$p7$. The spacing in time domain remains to be one prescaler's input cycle. Since the frequency of input phases is reduced by half (from $f_{\rm in}/4$ to $f_{\rm in}/8$), signal-level amplification is no longer needed, and the 8-to-1 MUX can be implemented with standard digital cells instead of current-mode logic gates to save power. Furthermore, the robustness of the phase-switching operation is improved due to the relaxed timing requirement.

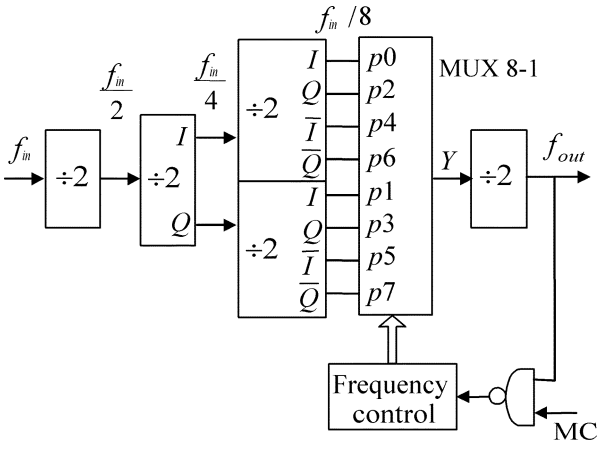

Fig. 2. Proposed enhanced phase-switching prescaler.

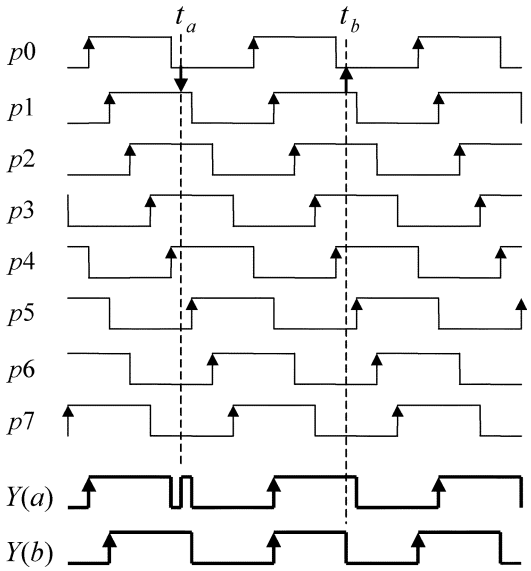

Fig. 3. Inherently glitch-free phase-switching.

One problem associated with using two divide-by-2 FFs working in parallel is that the eight output waveforms, $p0$–$p7$, can be either of two possible patterns. Although the phase relationship of the four outputs of each FF is fixed, the combination of the eight outputs has two and only two possible patterns. It depends on the initial status of the two FFs and the beginning order of their clock signals. One pattern is that shown in Fig. 3. Compared with this pattern, the phases of odd-numbered signals are changed by 180°, that is, the phases are exchanged in signal pairs $(p1, p5)$ and $(p3, p7)$ in the other pattern.

Fig. 3 illustrates how we change the switching sequence to obtain an inherently glitch-free phase-switching which yields the MUX output $Y(b)$. It effectively swallows a cycle, that is, the instantaneous divide ratio is increased by one, when switching occurs in the conventional sequence. The main problem with this conventional switching scheme is the potential glitches at the MUX output. As shown in Fig. 3, if the switching from $p0$ to $p1$ occurs at instant t_a where $p0$ and $p1$ have different logic levels, there will be an unwanted glitch at the MUX output $Y(a)$. However, if the switching is reversed from $p1$ to $p0$, that is, the instantaneous divide ratio is decreased by one, there will be no

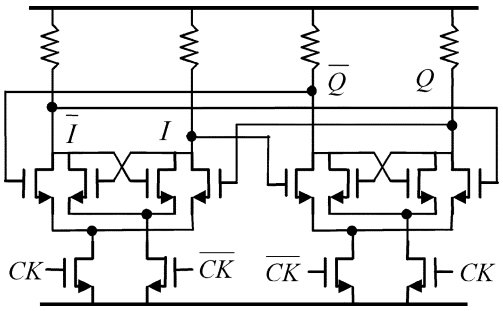

Fig. 4. SCL flip-flop configured as divide-by-2.

glitches in the MUX output whenever the switching occurs. The difference can be seen in Fig. 3 where the switching from $p1$ to $p0$ occurs at instant t_b and the MUX output $Y(b)$ is glitch-free although $p0$ and $p1$ have different logic levels at this time instant. Since the enhanced phase-switching architecture is inherently glitch free, no power-hungry retiming or synchronization circuit is needed for the switching control and the robustness of the switching operation is guaranteed. The division ratio of the prescaler is 15/16. When the MC input is high, one switching occurs during the prescaler's output cycle, and the instantaneous division ratio of the prescaler is 15. Otherwise, no switching occurs and the division ratio is 16.

To deal with the two possible phase patterns, the phase relationship between $p0$ and $p1$ is detected to self-adjust the switching sequence. If $p0$ leads $p1$ by 45°, the phase switching will occur in the following sequence: $p0 \rightarrow p7 \rightarrow p6 \rightarrow \cdots \rightarrow p0$. If $p0$ leads $p1$ by 225°, the switching sequence is $p0 \rightarrow p3 \rightarrow p6 \rightarrow p1 \rightarrow p4 \rightarrow p7 \rightarrow p2 \rightarrow p5 \rightarrow p0$.

The schematic of the high-speed master–slave FF configured as a ÷2 divider is illustrated in Fig. 4. It uses source-coupled logic (SCL) without tail current. Thus, it can toggle at a very high frequency with low power supply. The input ÷2 divider determines the prescaler's maximum operating frequency as well as its input sensitivity.

IV. Loop Filter With Capacitance Multiplier

A. Characteristics of the Third-Order Loop Filter

A third-order passive loop filter for the charge-pump PLL is shown in Fig. 5. There are three capacitors and two resistors. C_1 produces the first pole at the origin for the type-II PLL. This is the largest capacitor, hence, it is a key integration bottleneck of the PLL. C_1 and R_1 are used to generate a zero for loop stability. C_2 is used to smooth the control voltage ripples and to generate the second pole. R_3 and C_3 are used to generate the third pole to further suppress reference spurs and the high-frequency phase noise in the $\Sigma\Delta$ PLL.

The transimpedance of this loop filter is

$$Z(s) = \frac{V_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{1}{s} \cdot \frac{\frac{1+s\tau_1}{C_1+C_2+C_3}}{1 + s\frac{C_1\tau_3+C_2(\tau_1+\tau_3)+C_3\tau_1}{C_1+C_2+C_3} + s^2\tau_1\tau_3\frac{C_2}{C_1+C_2+C_3}} \tag{1}$$

where $\tau_1 = R_1C_1$ and $\tau_3 = R_3C_3$.

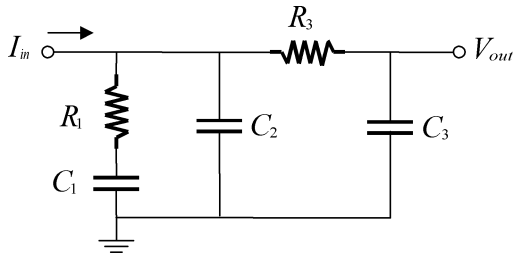

Fig. 5. Third-order passive loop filter for charge-pump PLL.

In the filter, there are three poles and one finite zero. The locations of the poles and zero can be approximated for the case of $C_1 \gg C_2$, C_3, and $R_1 > R_3$ as

$$\omega_{p1} = 0 \tag{2}$$

$$\omega_{p2} \approx \frac{1}{R_1(C_2+C_3)} \tag{3}$$

$$\omega_{p3} \approx \frac{1}{\frac{R_3C_2C_3}{(C_2+C_3)}} \tag{4}$$

and

$$\omega_z = \frac{1}{R_1C_1}. \tag{5}$$

One additional pole at the origin in the PLL comes from the VCO. The PLL −3-dB bandwidth $\omega_{-3\,\text{dB}}$, which is equal to its open-loop unity gain ω_u, must be placed somewhere between ω_z and ω_{p2} to obtain a reasonable phase margin for the PLL loop stability. Assuming that $\omega_u = \sqrt{\omega_z\omega_{p2}}$ and $\omega_{p3} \gg \omega_u$, then the phase margin yields

$$\phi_m \approx \arctan\left(\sqrt{\frac{\omega_{p2}}{\omega_z}}\right) - \arctan\left(\sqrt{\frac{\omega_z}{\omega_{p2}}}\right). \tag{6}$$

For example, if ω_{p2} is 16 (or 9) times of ω_z, then ϕ_m is 62° (or 53°).

B. On-Chip Loop Filter With Capacitance Multiplier

In this paper, the loop filter values are $R_1 = 10$ kΩ, $C_1 = 160$ pF, $C_2 = 10$ pF, $R_3 = 1$ kΩ, and $C_3 = 10$ pF. With PLL loop bandwidth of about 250 kHz, calculations using (1)–(6) show that the PLL loop phase margin is about 51°. To overcome the disadvantages of the dual-path topology, the capacitance scaling technique [16] is employed in the design of the third-order on-chip loop filter. In TSMC 0.35-μm CMOS process, the 160-pF poly-to-poly capacitor C_1 would occupy about 0.2 mm^2 of die area. To reduce its area, it was built with a capacitor $C_i = 10$ pF scaled up by a factor of 16, as shown in Fig. 6. To minimize the current leakage at node A, cascode current mirrors with long-channel transistors are used. The equivalent small-signal admittance at the input terminal is

$$y_{\text{in}} = \frac{i_{\text{in}}}{v_{\text{in}}} = g_{oA} + s\left[C_{p2} + (M+1)C_i\frac{1+s\frac{C_{p1}}{(M+1)g_{m1}}}{1+s\frac{C_i+C_{p1}}{g_{m1}}}\right]. \tag{7}$$

C_{p1} and C_{p2} are parasitic capacitors at node A and B, respectively. Usually, $C_{p1} \ll C_i$ and $C_{p2} \ll C_{p1}$ because C_{p1} includes the large parasitic capacitance between the bottom plate

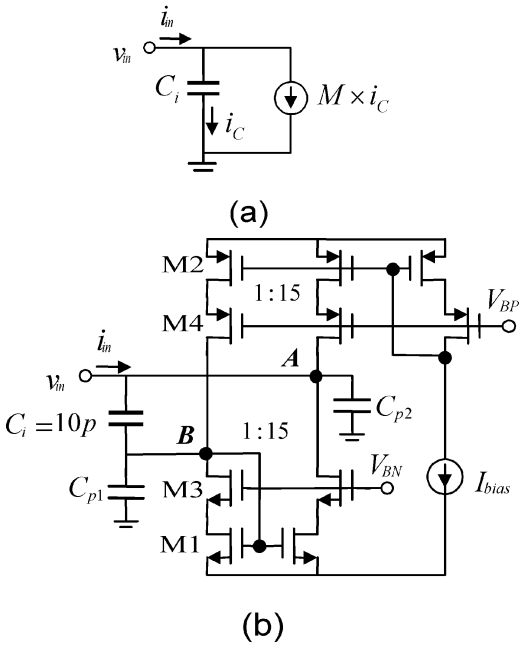

Fig. 6. Capacitance multiplier. (a) Principle. (b) Circuit implementation.

of poly–poly capacitor C_i and ground. g_{m1} is the transconductance of transistor M1, and g_{oA} is the overall conductance at node A. $M = 15$ is the current gain of the current mirror (or current amplifier). Fig. 7 shows the simulated frequency responses of y_{in} in comparison with an ideal 160-pF capacitor. The three corner frequencies of y_{in} are

$$\omega_{c1} = \frac{g_{oA}}{C_{p2} + (M+1)C_i} \approx \frac{g_{oA}}{C_1} \tag{8}$$

$$\omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(M+1)g_{m1}}{C_1} \tag{9}$$

and

$$\omega_{c3} = \frac{(M+1)g_{m1}}{C_{p1}}. \tag{10}$$

ω_{c1} and ω_{c3} are poles while ω_{c2} is a zero. y_{in} can be approximated in the four frequency ranges separated by the above three corner frequencies as follows.

1) At very low frequencies, i.e., $\omega < \omega_{c1}$, $y_{\text{in}} \approx g_{oA}$.
2) In the frequency range of $\omega_{c1} < \omega < \omega_{c2}$, $y_{\text{in}} \approx s(C_{p2} + (M+1)\,C_i) \approx SC_1$, which is the intended capacitance.
3) In the frequency range of $\omega_{c2} < \omega < \omega_{c3}$, $y_{\text{in}} \approx sC_{p2} + ((M+1)\,C_i/(C_i + C_{p1}))\,g_{m1} \approx (M+1)\,g_{m1}$.
4) At very high frequencies, i.e., $\omega > \omega_{c3}$, $y_{\text{in}} \approx s\,(C_{p2} + C_iC_{p1}/(C_i + C_{p1})) \approx sC_{p1}$.

The following two constraints on the corner frequencies of the scaled capacitance are imposed for this application. 1) To minimize the current leakage, a small value of g_{oA} is needed to make ω_{c1} as low as possible. Also, the current mismatch between the top and bottom current sources at node A must be minimized. 2) To keep the PLL's phase margin unchanged, it is desirable that the second corner frequency ω_{c2} should be much larger than the zero of the loop filter ω_z, i.e., $\omega_{c2} \gg \omega_z$.

The first requirement can be met by using cascode current mirrors with long-channel transistors, but the second requirement may not be satisfied in some cases. Therefore, we need to investigate the impact on the loop filter's frequency response when $\omega_{c2} \gg \omega_z$ is not satisfied.

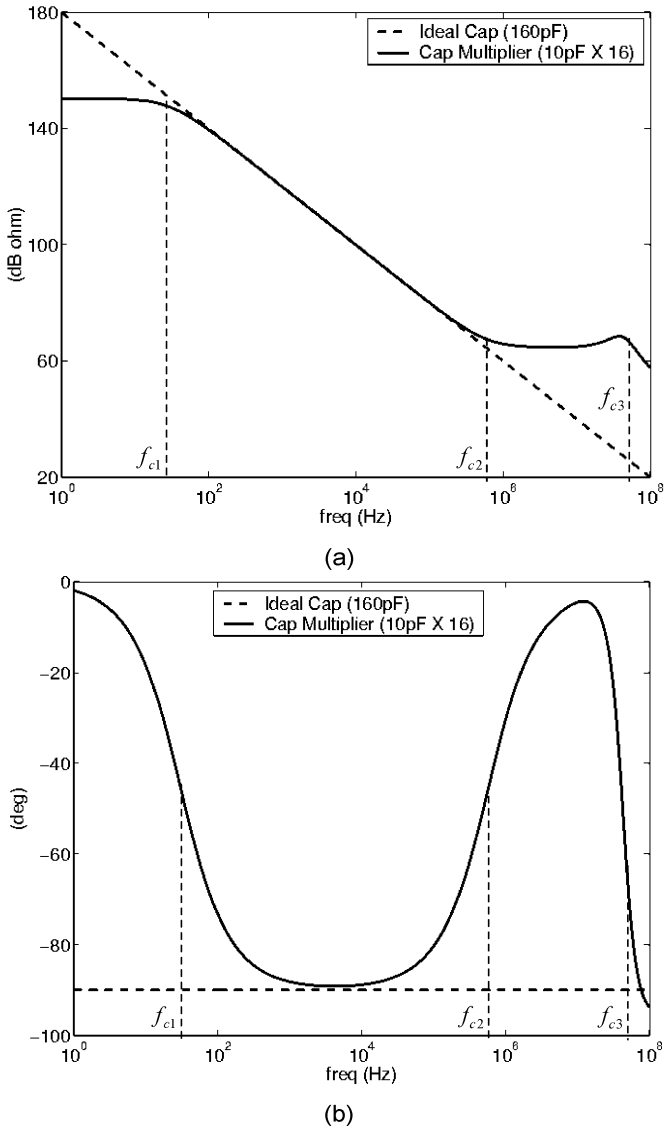

Fig. 7. Frequency response of capacitance multiplier impedance. (a) Magnitude. (b) Phase.

In the frequency range of $\omega_{c1} < \omega < \omega_{c3}$, from (7), we have

$$y_{\text{in}} \approx \frac{s(M+1)C_i}{1 + s\frac{C_i}{g_{m1}}} = \frac{1}{\frac{1}{sC_1} + \frac{1}{(M+1)g_{m1}}}. \tag{11}$$

Thus, in this frequency range, the capacitance multiplier is equivalent to the desired capacitance C_1 in series with a resistance of $[(M+1)g_{m1}]^{-1}$ value. Since R_1 is in series with the capacitance multiplier, then the overall resistance is increased and the zero of the loop filter becomes

$$\omega_z' = \frac{1}{\left(R_1 + \frac{1}{(M+1)g_{m1}}\right)C_1} = \frac{\omega_z}{1 + \frac{1}{(M+1)g_{m1}R_1}}. \tag{12}$$

If $[(M+1)g_{m1}]^{-1}$ is less than 20% of R_1, that is

$$g_{m1} \geq \frac{5}{(M+1)R_1} \tag{13}$$

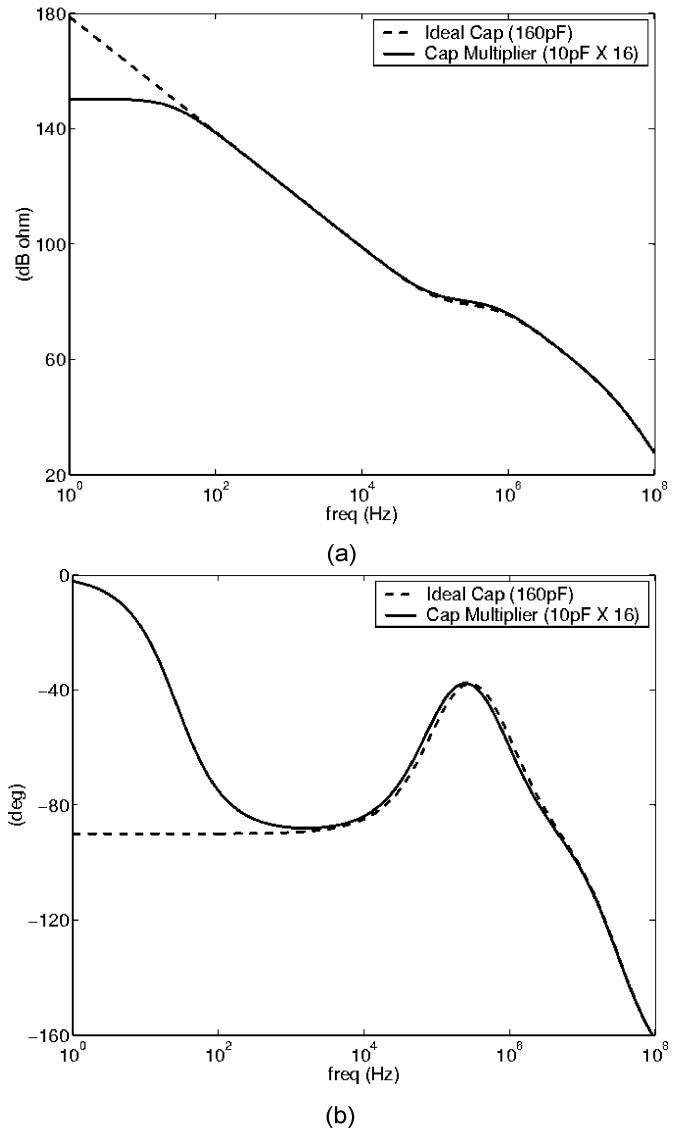

Fig. 8. Simulated loop filter transimpedance. (a) Magnitude. (b) Phase.

it can be neglected. Otherwise, we need to reduce the resistance of R_1 by the amount of $[(M+1)g_{m1}]^{-1}$ to keep the zero frequency unchanged. This imposes that $[(M+1)g_{m1}]^{-1}$ should never be greater than R_1. The simulated frequency responses of this loop filter with scaled and nonscaled capacitors, respectively, are shown in Fig. 8. It indicates that the resistance at node A $(= 1/g_{oA})$ is around 30 MΩ, which is large enough to make the current leakage negligible, and one can say that the capacitance multiplier emulates a large grounded capacitance very well in this application.

Finally, we must check the noise introduced by the capacitance multiplier to make sure that it is negligible in comparison with other noise sources in the frequency synthesizer. We consider the phase noise caused by the capacitance multiplier at 1-MHz offset because the phase noise requirement around 1 MHz is the most stringent for most of the wireless applications. Since the thermal noise dominates at 1 MHz, a simple way is to compare the equivalent noise resistance of the capacitance multiplier with R_1. From Fig. 7(a) and the analysis made

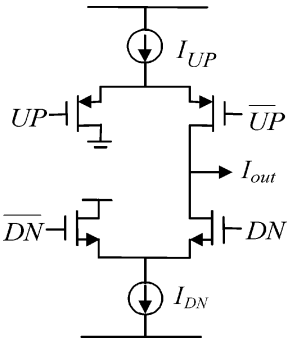

Fig. 9. Simplified schematic of the charge pump.

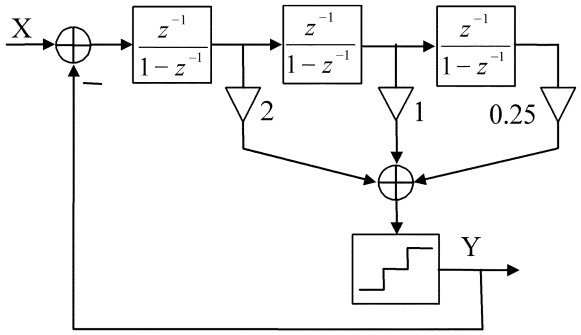

Fig. 10. Third-order single-stage digital ΣΔ modulator.

before, we know that the admittance of the capacitance multiplier at 1 MHz is approximately $(M+1)g_{m1}$. Neglecting the minimized noise of the bias, the voltage noise density of the capacitance multiplier is approximately given by

$$v_n^2 = \frac{8kT}{3(M+1)g_{m1}}\left(\frac{1+g_{m2}}{g_{m1}}\right). \tag{14}$$

The transconductance of transistor M2, g_{m2}, can be less than g_{m1} for noise optimization, but let us consider the case $g_{m2} \approx g_{m1}$, then (14) yields

$$v_n^2 = \frac{16kT}{3(M+1)g_{m1}}. \tag{15}$$

Therefore, the thermal noise produced by the capacitance multiplier is equivalent to the one generated by a resistance of $4/(3(M+1)g_{m1})$ value. To make the noise contribution from capacitance multiplier at 1 MHz negligible, we need to satisfy, i.e.

$$g_{m1} \geq \frac{4}{3(M+1)} \cdot \frac{1}{R_1}. \tag{16}$$

As far as the noise contribution from R_1 [12] is negligible for a certain application, the noise contributed by the capacitance multiplier is also negligible.

In our design, the sizes (in micrometers) of transistors M1–M4 are 12/2, 6/3, 12/3, and 12/3, respectively. The dc current of this branch is 5 μA. $g_{m1} \approx 0.1$ mA/V, which is large enough to satisfy the conditions in (13) and (16). This capacitance multiplier consumes only 0.2 mW including its bias circuitry.

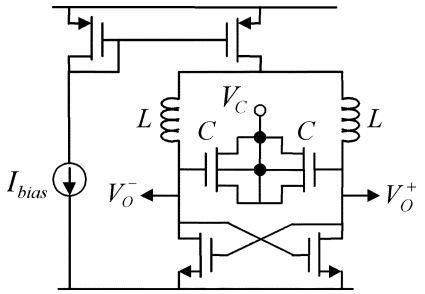

Fig. 11. Schematic of the *LC* VCO.

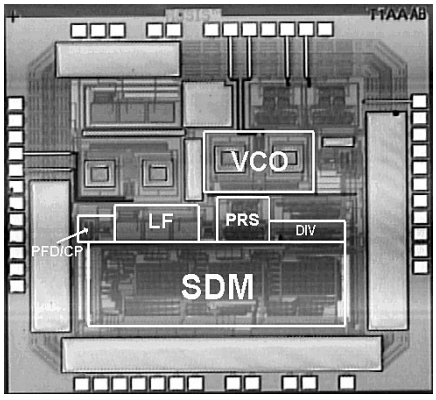

Fig. 12. Chip microphotograph of PLL-FS.

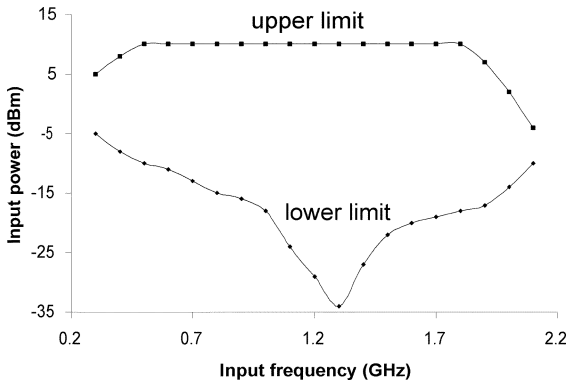

Fig. 13. Prescaler input sensitivity over frequency ($V_{\rm DD} = 1.5$ V).

V. Other Building Blocks of the Frequency Synthesizer

A. Phase-Frequency Detector (PFD) and Charge Pump

A commonly used dead-zone-free PFD similar to the one in [12] is used in this paper. Usually, we use an inverter to generate reverse signals $\overline{UP}$ and $\overline{DN}$ from UP and DN, respectively. With a 2-V single supply, a typical inverter delay is 0.3 ns. To improve the linearity of the PFD and charge pump, we should align UP and DN with their reverse signals as well as possible. The standard exclusive-or (XOR) based on transmission gates is used to reach this goal in our design. For example, $UP \oplus 0 = UP$ and $UP \oplus 1 = \overline{UP}$. The XOR gates are simplified since one of its inputs is tied to either 1 or 0. Simulation results show that the timing misalignment between UP (or DN) and $\overline{UP}$ (or $\overline{DN}$) is reduced to less than 50 ps. The charge pump in this paper is shown in Fig. 9. Since the reference frequency of this fractional-N synthesizer is high, the reference spur is not a concern. Since the turn-on time of the charge pump is only about 1 ns in the locked state, fast and symmetrical transient response of the charge pump is preferred for good linearity.

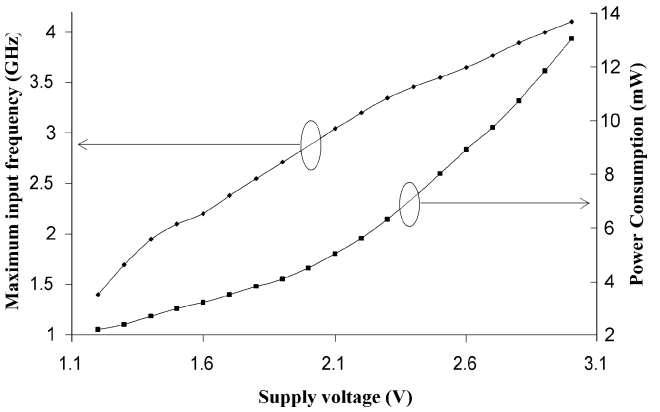

Fig. 14. Prescaler maximum input frequency and power consumption versus supply voltage.

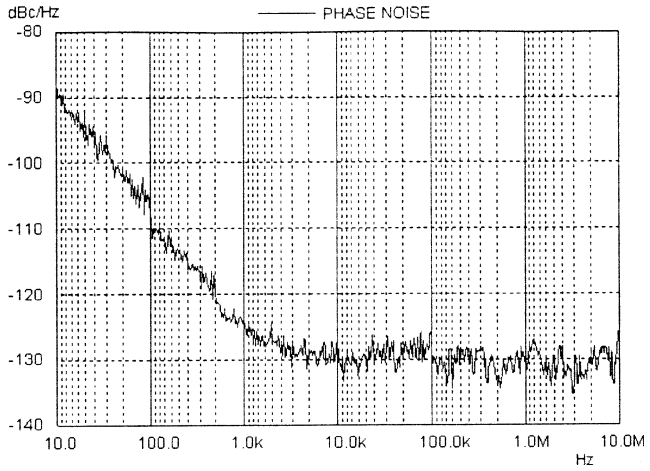

Fig. 15. Measured prescaler residual phase noise.

B. Digital $\Sigma\Delta$ Modulator (SDM)

A third-order single-stage $\Sigma\Delta$ modulator used in the frequency synthesizer of Fig. 1 is implemented as shown in Fig. 10. It is a modified version of the one reported in [18]. A delay is added for each integrator (accumulator) to increase the maximum operating speed of the modulator. The quantizer has three levels: 0, 1, and 2, which is the minimum number of quantization levels that makes the stable dc input cover the fractional range from 0.5 to 1.5. To reduce the circuit complexity and increase the operating speed of the adder before the quantizer, its three inputs are truncated. Compared with other topologies studied in [19], this one has less spread phase error at the PFD introduced by the $\Sigma\Delta$ modulator, and it reduces the phase noise associated with the charge pump and the folding of phase noise due to PLL nonlinearities.

C. VCO

The schematic of the *LC* VCO used in this paper is shown in Fig. 11. On-chip spiral inductors with patterned ground shields are built with the top metal layer. The quality factor Q value

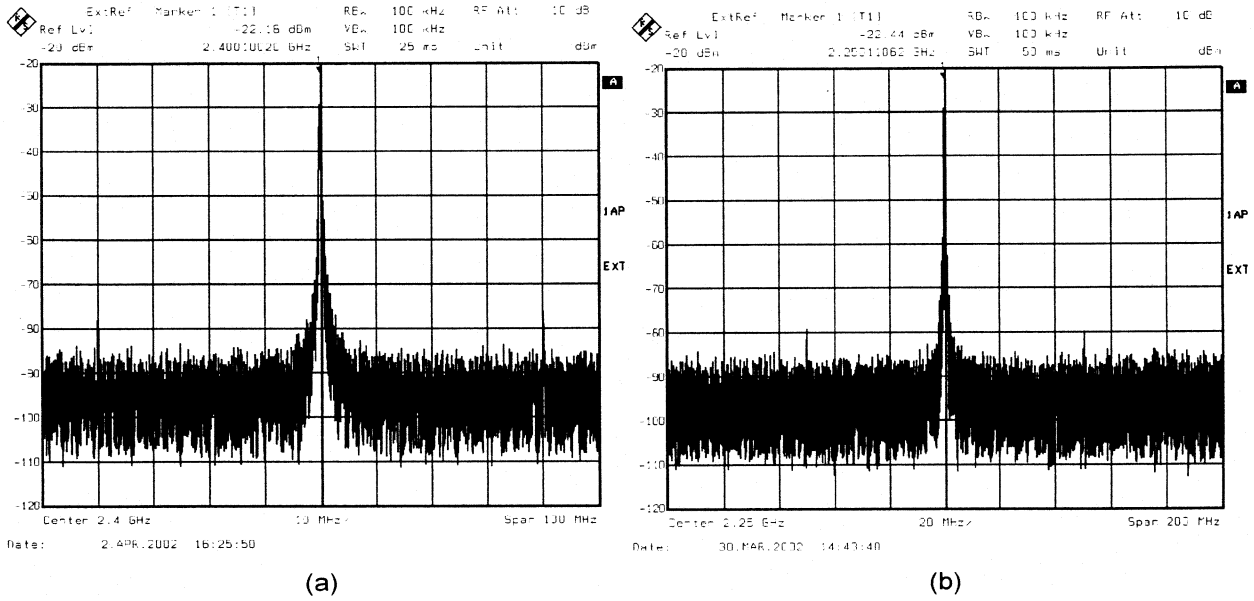

Fig. 16. Measured PLL-FS output power spectrum with: (a) $f_{\rm ref} = 40$ MHz and (b) $f_{\rm ref} = 50$ MHz.

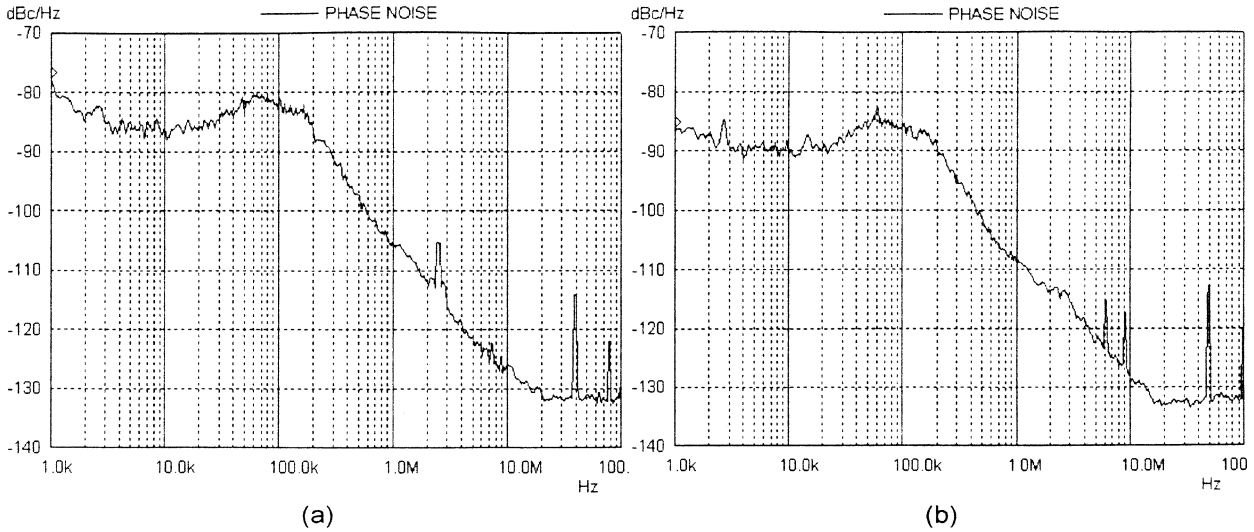

Fig. 17. Measured PLL-FS phase noise with: (a) $f_{\rm ref} = 40$ MHz and (b) $f_{\rm ref} = 50$ MHz.

of the spiral inductors is only around two. To cover the center frequency variation, the VCO tuning range, through V_c, is designed to be wide (around 10%) in this work. Since the dc level of the VCO output matches that of the prescaler input, the VCO drives the prescaler directly in this PLL. The VCO needs to draw a large current (more than 4 mA) to generate enough output swing. It is the main power-consuming building block in the whole PLL system and the on-chip spiral inductors (about 2 nH each) occupy a large chip area.

VI. Experimental Results

The chip was fabricated in TSMC 0.35-μm double-poly four-metal CMOS technology through MOSIS. Each building block is encircled by double guard rings to minimize the substrate noise. Fig. 12 shows the microphotograph of the whole chip, which includes the monolithic PLL and some standalone blocks for testing. The monolithic PLL has an area of 0.85 mm^2 (100%) out of which the digital $\Sigma\Delta$ modulator, the VCO, the loop filter, and the prescaler occupy 0.5 mm^2 (58.8%), 0.15 mm^2 (17.7%), 0.05 mm^2 (5.9%), and 0.04 mm^2 (4.7%), respectively. The VCO and the prescaler draw 6 and 2 mA from a 1.5-V supply, respectively, and other blocks draw 2 mA from a 2-V supply in total, whereby the whole PLL system consumes 16 mW. Compared with the 18-mW dual-path loop filter in [12], the proposed loop filter with capacitance multiplier consumes only 0.2 mW.

The performances of the standalone prescaler were measured. Fig. 13 shows the input sensitivity versus frequency with supply voltage of 1.5 V. The maximum input power (the upper trace in Fig. 13) is limited to 10 dBm by the signal generator. The self-oscillating frequency of the prescaler is around 1.316 GHz in the absence of an input ac signal. The maximum operating frequency and the corresponding power consumption increases with supply voltage, and this is shown in Fig. 14. The prescaler works up to 4.1 GHz with 3.0-V power supply. The measured residual phase noise of the prescaler with a 2.0-GHz input and

divide ratio of 15 is shown in Fig. 15. The phase noise at 1.0-kHz offset is -124 dBc/Hz. It is worthwhile to mention that the frequency synthesizer designed in 0.25-μm CMOS in [3] failed to work beyond 2.41 GHz due to limitations of the conventional prescaler.

The power spectrum and phase noise of the PLL-FS output were measured by using the Rohde & Schwarz FSEB30 spectrum analyzer. They are shown in Figs. 16 and 17, respectively. Reference spurs of -55 and -57 dBc are observed with reference frequencies of 40 and 50 MHz, respectively, in Fig. 16. The frequency synthesizer output tuning range is 9.4%, from 2.23 to 2.45 GHz. The PLL loop bandwidth is 250 kHz. The phase noise levels at 10-MHz offset are -126 and -128 dBc/Hz with the reference frequency of 40 and 50 MHz, respectively, which is mainly limited by the low-quality inductor. The spurs caused by the nonideal 45° spacing [e.g., at 6.25 MHz in Fig. 17(b)] in the phase-switching prescaler are negligible. Based on the low-power and robust phase-switching prescaler and loop capacitance multiplier, the proposed topology saves considerable power and area while improving the circuit robustness.

VII. Conclusion

A monolithic 2.4-GHz $\Sigma\Delta$ fractional-N frequency synthesizer is designed in 0.35-μm CMOS technology. New approaches have been made to tackle the speed bottleneck (the prescaler) and integration bottleneck (the loop filter) of the PLL-based frequency synthesizer. An enhanced inherently glitch-free phase-switching prescaler is proposed. It is robust and power and area efficient. Capacitance scaling is deployed to integrate a large capacitor of the loop filter within small die area. This technique avoids the constraints of the dual-path topology [11]–[15], and it can emulate capacitors of hundreds of picofarads easily integratable on chip. The PLL operates with 1.5 V (analog), 2.0 V (digital), and consumes 16 mW. Measurement results verified the feasibility and robustness of the enhanced phase-switching prescaler and the practicality of the loop capacitance multiplier.

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Keliu Shu (S'99) was born in Anhui, China. He received the B.Sc. and M.Sc. degrees in electrical engineering from Fudan University, Shanghai, China, in 1995 and 1998, respectively. He has been a Research Assistant working toward the Ph.D. degree in the Analog and Mixed-Signal Center, Texas A&M University, College Station, since 1998.

He was involved in military training at Dalian Military Academy during the 1990–1991 academic year. In the summer of 1995 and the 1996–1997 academic year, he worked on IC design in Zhuhai, China. In the summer and fall of 2000, he worked on PLL design as a Co-op Student at Texas Instruments Incorporated, Dallas, TX. His research interests include analog/RF and mixed-signal circuits design.

Edgar Sánchez-Sinencio (M'74–SM'83–F'92) was born in Mexico City, Mexico. He received a Professional degree in communications and electronic engineering from the National Polytechnic Institute of Mexico, Mexico City, in 1966, the M.S.E.E. degree from Stanford University, Stanford, CA, in 1970, and the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1973.

In 1974, he held an industrial Postdoctoral position with the Central Research Laboratories, Nippon Electric Company, Ltd., Kawasaki, Japan. From 1976 to 1983, he was the Head of the Department of Electronics at the Instituto Nacional de Astrofísica, Optica y Electrónica (INAOE), Puebla, Mexico. He is currently the TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center, Texas A&M University, College Station. He is a coauthor of the book *Switched Capacitor Circuits* (New York: Van Nostrand-Reinhold, 1984), and co-editor of the book *Low Voltage/Low-Power Integrated Circuits and Systems* (New York: IEEE Press, 1999). His current research interests are in the area of RF-communication circuits and analog and mixed-mode circuit design.

Dr. Sánchez-Sinencio was an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS from 1985 to 1987, and an Associate Editor for the IEEE TRANSACTIONS ON NEURAL NETWORKS. He was the General Chairman of the 1983 26th Midwest Symposium on Circuits and Systems. He is the former Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is a former President of the IEEE Circuits and Systems (CAS) Technical Committee on Analog Signal Processing. He is a former IEEE CAS Vice President–Publications. He was the IEEE Circuits and Systems Society Representative to the Solid-State Circuits Society (2000–2002), and is currently a member of the IEEE Solid-State Circuits Award Committee. In November 1995, he was awarded an *Honoris Causa* Doctorate by the National Institute for Astrophysics, Optics and Electronics, Mexico, the first honorary degree awarded for Microelectronic Circuit Design contributions. He received the 1995 Guillemin-Cauer Award for his work on cellular networks. He was the corecipient of the 1997 Darlington Award for his work on high-frequency filters. He received the Circuits and Systems Society Golden Jubilee Medal in 1999.

José Silva-Martínez (SM'98) was born in Tecamachalco, Puebla, Mexico. He received the B.S. degree in electronics from the Universidad Autónoma de Puebla in 1979, the M.Sc. degree from the Instituto Nacional de Astrofísica Optica y Electrónica (INAOE), Puebla, in 1981, and the Ph.D. degree from the Katholieke Univesiteit Leuven, Belgium, in 1992.

From 1981 to 1983, he was with the Electrical Engineering Department, INAOE, where he was involved with switched-capacitor circuit design. In 1983, he joined the Department of Electrical Engineering, Universidad Autónoma de Puebla, where he remained until 1993. He was a cofounder of the graduate program on optoelectronics in 1992. From 1985 to 1986, he was a Visiting Scholar in the Department of Electrical Engineering, Texas A&M University, College Station. In 1993, he rejoined the Electronics Department, INAOE, and from May 1995 to December 1998, was the Head of the Electronics Department. He was a cofounder of the Ph.D. program in electronics in 1993. He is currently with the Analog and Mixed Signal Center, Department of Electrical Engineering, Texas A&M University, where he is an Associate Professor. His current field of research is in the design and fabrication of integrated circuits for communication and biomedical applications.

Dr. Silva-Martínez served as IEEE Circuits and Systems (CAS) Society Vice President, Region 9, from 1997 to 1998, and as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1997 to 1998 and from May 2002 to the present. He was the main organizer of the 1998 and 1999 International IEEE CAS Tour in Region 9, and was Chairman of the International Workshop on Mixed-Mode IC Design and Applications from 1997 to 1999. He is the inaugural holder of the TI Professorship I in Analog Engineering, Texas A&M University. He was a corecipient of the 1990 European Solid-State Circuits Conference Best Paper Award.

Sherif H. K. Embabi (S'87–M'91–SM'98) received the B.Sc. and M.Sc. degrees in electronics and communications from Cairo University, Cairo, Egypt, in 1983 and 1986, respectively, and the Ph.D. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1991.

In 1991, he joined Texas A&M University, College Station, as an Assistant Professor of electrical engineering, and became an Associate Professor in 1997. In 1999, he joined the RF Design Group, Texas Instruments Incorporated, Dallas, TX, as a Member of Technical Staff. He has coauthored one book and over 40 technical journal and conference papers. He is currently working on highly integrated transceivers for cellular applications. His areas of interest include RF circuits and systems.

Dr. Embabi received the National Science Foundation Research Initiation Award in 1994. He served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING between 1995 and 1997.