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A 3-input all magnetic full adder with misalignment-free clocking mechanism

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The clocking field misalignment is a critical issue for the application of Magnetic Quantum-dot Cellular Automata (MQCA). Recent work demonstrates a novel architecture to address this issue—by progressively tuning the shape anisotropy, we could enforce a misalignment-free signal propagation and logic operation. In this paper, we propose a novel architecture of a 3-input full adder based on the 45°-clocking field mechanism. The effectiveness of this design is confirmed through both simulation and experiments. Our work paves the way for the application of MQCA logic. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4974109]

I. INTRODUCTION

The concept of Magnetic Quantum-dot Cellular Automata[1] (MQCA, also referred to as Nanomagnet Logic, or NML) has attracted people's attention due to many advantages over conventional Si CMOS technology, such as low heat dissipation, non-volatility, and high integration density. The basic idea of MQCA is to process information and perform Boolean logic operations, via nearest-neighbor dipole coupling, in logic gates comprised of specific arrangements of nanoscale magnetic elements. These gates require a clocking field to bring the elements to their "NULL" state along the hard axis.[1,2] However, a field misalignment of even $\pm 1°$ would lead to incorrect logic operation 75% of the time, making MQCA logic practically challenging.[1] To address this issue, many approaches have been tested to enhance the stability characteristics by uniformly tuning the nanomagnet shape,[3–6] i.e., introducing a sub-stable state along the hard axis.[3] Although these designs facilitate signal propagation to some extent, they all rely on a highly accurate clocking field alignment.

Recent demonstration of a novel architecture to progressively tune the shape anisotropy by shortening the long axis of elements enforces misalignment-free signal propagation[7] and logic operation[8] by using a 45° clocking field: a reversal clocking field 45° off the hard axis with progressively reduced amplitude. The clocking mechanism could enhance the misalignment tolerance, resulting in robust signal propagation and logic operation. Both basic structures of *nanomagnet arrays* and *majority gates* (OR function) were demonstrated.

Further development of MQCA logic requires more complicated functions, such as a full adder, for integration with electrical circuit and pipelined logic of data flow.[9] A binary full adder works to add up binary numbers and accounts for values carried in and out.[10] Although it is straightforward to design such a MQCA full adder based on blocks of *nanomagnet arrays* and *majority gates*, there are few experimental attempts to fabricate and test them due to the misalignment issue.[10–12] For example, error of wrong data-flow directionality occurs under traditional clocking field.[11] Thus, it is of interest to redesign a full adder that is robust against misalignment in clocking.

Here, we propose a novel architecture of the 3-input full adder based on the 45°-clocking field mechanism; the field alters between 0° and 45° off the *x*-axis to separate input writing and logic operation. This alternated clocking mechanism facilitates stable logic operations. Moreover, it intrinsically favors unidirectional signal flow and hence requires only 1/3 the number of elements compared to a traditional full adder design.[11] The effectiveness of this design is confirmed through both micromagnetic simulation, using the commercially available LLG software,[13,14] and experimental demonstration combining electron-beam lithography (EBL) and magnetic force microscopy (MFM).

II. LOGIC AND ALGORITHM

There are two basic architectures in MQCA logic: (a) *linear nanomagnet array* where the signal propagates and (b) *majority gate* for logic operation. For a *nanomagnet array*, the dipole field between adjacent elements would facilitate antiferromagnetic (AF) coupling, suggesting an $\uparrow|\downarrow$ alternation of magnetization in the chain. If we define $\uparrow|\downarrow$ as 1 | 0, then the same signal occurs in every other element within the array. Different from the Coulomb-coupled quantum cellular automata (QCA),[10] where an inverter is required, a MQCA *linear nanomagnet array* can achieve the NOT function by simply adding another AF-coupled element into the linear chain. Complementing the above, *majority gates* perform 3-input logic operations; the output is determined by voting among all 3 adjacent elements through the competing dipole field on the center one. Fixing the magnetic state of one input driver as pre-programmable, we could transfer the *majority gates* into 2-input AND/OR gates. Again, an additional AF-coupled element can bring up logic

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functions of NAND/NOR. In short, all five basic binary logic functions of NOT/AND/OR/NAND/NOR can be physically realized by the two basic MQCA architectures—*linear nanomagnet array* and *majority gate*.

A full adder can be designed and fabricated based purely on the above two architectural elements. A full adder[10] has three inputs of one-bit numbers, often written as A, B, and C_i. Both A and B are operands while C_i serves as a carry-in. There are two outputs, C_o and S, as shown in Table I.

A full adder can be expressed using AND (•), OR (+), and NOT (NOT of A is represented by $\bar{A}$) logic functions as

$$\begin{cases} C_o = A \bullet B + B \bullet C_i + A \bullet C_i & (1) \\ S = A \bullet B \bullet C_i + \bar{A} \bullet \bar{B} \bullet C_i + \bar{A} \bullet B \bullet \overline{C_i} + A \bullet \bar{B} \bullet \overline{C_i} & (2) \end{cases}$$

To express this function within 3-input MQCA majority gates,[9] a compact algorithm can be achieved if we define the 3-input voting function as

$$M(A, B, C_i) = A \bullet B + B \bullet C_i + A \bullet C_i \quad (3)$$

The M-function, (3), is compatible with the 2-input logic, in that the AND/OR function can be achieved by fixing the preprogrammable element, C_i, as

$$\begin{cases} A \bullet B = M(A, B, C_i = 0) & (4) \\ A + B = M(A, B, C_i = 1) & (5) \end{cases}$$

It is worth mentioning that the NOT function also applies to the new algorithm. Thus, much higher efficiency can be achieved as we could concisely rewrite the full adder with the M-function as:

$$\begin{cases} C_o = M(A, B, C_i) & (6) \\ S = M(\overline{M(A, B, C_i)}, M(A, B, \overline{C_i}), C) & (7) \end{cases}$$

Such an architecture, intrinsically requiring only three 3-input majority gates, is shown in Fig. 2(a).

III. EXPERIMENTAL DETAILS

Experimentally, we used *e*-beam lithography (EBL) with Polymethyl-methacrylate (PMMA)/LOR 1A (MicroChem Corp., Newton, MA) bilayer resist for pre-patterning. Selective wet-etching of the LOR 1A underlayer by TMAH helped introduce the undercut profile, which facilitates clean lift-off and prevents sidewall deposition. A magnetic layer 20 nm-thick Fe, with a 3 nm-thick Au cap, was deposited using a home-built ultra-high-vacuum ion beam sputtering system (UHV-IBS) with base pressure better than 5×10^{-8} Torr.[15] The magnetic configuration at remnant state was investigated by scanning electron microscopy (SEM) and magnetic force microscopy (MFM) using 15 nm-thick CoCr coated low moment probes with a lift height of 50 nm.

TABLE I. Truthvalue chart of a 3-input full adder.

Inputs	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C_i	0	0	0	0	1	1	1	1
Outputs	C_o	0	0	0	1	0	1	1	1
	S	0	1	1	0	1	0	0	1

IV. MICROMAGNETIC MODELING AND SIMULATION

Micromagnetic modeling was carried out using a commercial LLG simulation[13,16] package. Following parameters were used: saturation magnetization, $M_s = 1000$ emu/cm^3, exchange stiffness constant, $A = 2.1$ μerg/cm, and magnetocrystalline anisotropy, $K_{mc} = 0$, for the polycrystalline structure of the nanomagnet array. The 3-D model was meshed into discretized cells of $2.5 \times 2.5 \times 20$ nm^3 in size. The areal dimensional size equals the iron exchange coupling length of 2.5 nm. Thus, the magnetization gradient is small enough to consider that the magnetization, M, is uniform within each individual cell. On the other hand, only one layer along the z-axis was assumed as the thickness of each cell was set to be $t = 20$ nm, because magnetic phenomena, such as magnetic switching, took place mostly in the x-y direction. This method has been proved practical by experiments.[13,16]

V. RESULTS AND DISCUSSIONS

Our full-adder design requires switching of the clocking field between two axes oriented at 45° with respect to each other; thus, it is of interest to study the angular sensitivity of nano-elements to the switching field. We first simulated the magnetic reversal of a single element of characteristic size of $100 \times 300 \times 20$ nm^3, predefined with a uniaxial shape anisotropy due to the aspect ratio of 1:3. As predicted by the Stoner-Wohlfarth model,[17] the switching field, H_{sw}, would be minimized when the field is applied 45° off the hard axis. Correspondingly, the angular sensitivity of H_{sw}, representing the misalignment tolerance, $dH_{sw}/d\theta$, should equal zero. To test this idea, we carried out the angular (θ) dependence of the θ-sensitivity of H_{sw}, $dH_{sw}/d\theta$ from 1° to 45° off the hard axis with an angular step of 3° and magnetic field step of 1 Oe. The value of $dH_{sw}/d\theta$ represents the misalignment tolerance; hence, a lower $dH_{sw}/d\theta$ indicates more stable magnetic switching against field misalignment and is practically more favorable. As shown in Fig. 1, the misalignment sensitivity, $dH_{sw}/d\theta$, reduces from 176 Oe/° to 0.2 Oe/°, when the field direction changes from 1° to 45° off the hard axis, suggesting a totally different switching behavior when the clocking field alters between 0° and 45° along the hard axis. This makes possible the separation between *input writing* and *logic operation*, as will be discussed below.

Based on the M-function, (3), using 3-input majority gates, we demonstrate the design of a full adder using only three majority gates, as shown in Fig. 2(a). Next, the schematic design of the full adder was realized relying on the 45° clocking mechanism [Fig. 2(b)]. The clocking field is switched between 0° and 45° off the x-axis in order to alternate between *input writing* and *logic operation*. The full adder is composed of (I) a writing part of input drivers (A, B, C_i) with hard axis aligned 45° with respect to the x-axis and (II) an operation part of three 3-input majority gates with output elements of (C_o & S).

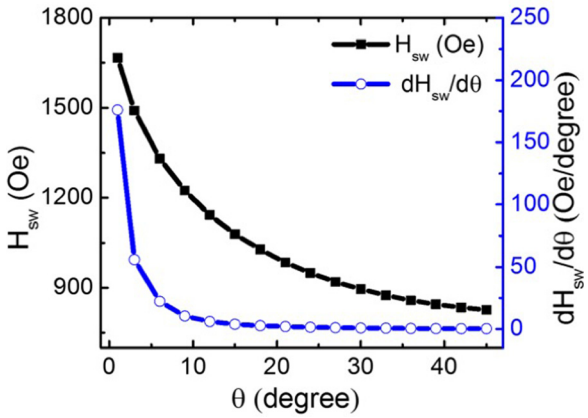

FIG. 1. Angular dependence of the switching field (H_{sw}) for an Fe single domain element with the aspect ratio of 1:3 (x:y) and its first derivative ($dH_{sw}/d\theta$).

First for the *input writing* part, different drivers (A, B, and C_i) were programed independently. Their aspect ratio and correspondingly the shape anisotropy are different, ensuring them to be switched selectively by tuning the field amplitude; larger aspect ratio requires a larger writing field. Then, for the *logic operation*, the field was turned to 45°-off the x-axis, in order to maximize the misalignment tolerance for majority gates. It is worth mentioning that our full adder intrinsically ensures unidirectional signal propagation by design; signal backflow is prohibited because input elements have a higher energy barrier than the output ones.

We use four different input combinations (A, B, and C_i) as schematically demonstrated in Fig. 2(c). In scenario (I), for example, all input elements are aligned to the right direction (either upper-right or lower-right), thus we have (A, B, C_i) equals (1,1,1). Correspondingly, we have both output elements (C_o & S). pointing down as (1,1). In scenario (II), only the input driver A is pointing rightward, while both B and C_i are pointing either upper-left or lower-left, indicating an input combination of (1,0,0). As a result, the output turns out to be (0,1). Similar to that, inputs of (0,1,1) and (0,0,0) lead

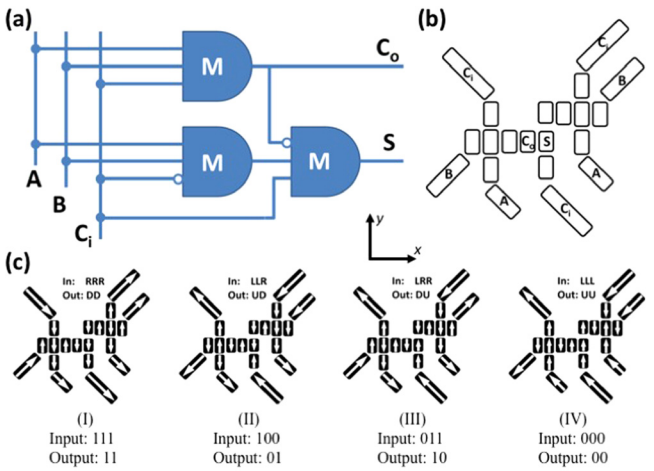

FIG. 2. (a) Design architecture of a full adder based on three 3-input majority gates; (b) schematic design of the full adder relying on the 45° clocking mechanism; (c) demonstrations of the correct output (with down/up as 1/0) based on the input (with right/left as 1/0).

to outputs of (1,0) and (0,0), respectively. In summary, the input drivers are defined by the clocking field and recorded by their final magnetic direction—where right (either upper-right or lower-right) indicates 1 and left (either upper-left or lower-left) indicates 0, and output is recorded as 1 when the magnetic moment is pointing downward for both C_o and S in Fig. 2(c).

To test this configuration, we simulated a full adder with input (1,1,1). Instead of presetting the input drives (A,B,C_i) along the positive x-axis (either ↘ or ↗ magnetic direction), for the *input writing*, we redirected the field along the negative y-axis (either ↙ or ↘ magnetic direction) in order to optimize the system thermal efficiency. Here, the identical output, (1,1), would be the expected. In addition, this *input writing* redirection is advantageous in spreading out the heat dissipation generated by the clocking current. In other words, in this specific scenario, it reduces the overall duty cycle for the x-axis field generated by the y-axis copper lead.[18] As a matter of fact, continuous signal processing usually gives pulse currents in ~GHz frequency and $\sim 10^6$ A/cm^2 current density[19] in the copper leads. Such a redirection will reduce the use and hence the heat dissipation on the heavily used y-axis copper lead by using the x-axis copper lead instead.

Figure 3(a) shows the magnetic field applied to the unit. At the beginning, a field of 1000 Oe along the y-axis was applied to preset the input drivers. Next for the operation, reversal fields with amplitudes of 620 Oe and 502 Oe were applied 45° off the x-axis. At each field cycle, only elements with lower shape anisotropy can reverse the magnetization direction until they reach the stable position after which they will remain unchanged at lowering clocking field. The inset of Fig. 3(a) shows the simulated magnetic configuration after each clocking cycle. Stage 3 (S3) corresponds to the final stage when the clocking field was removed and demonstrates the correct output. To further test the effect of a misaligned clocking field, an angular variation of ±1.5° was carried out and led to the same output, suggesting a robust design with high misalignment tolerance.

Next, we fabricated Fe nanomagnet arrays consistent with the full-adder design. The SEM image of the full adder is shown in the inset of Fig. 3(a). A continuous magnetostatic reversal field, the same as in simulation [Fig. 3(a)], was applied. The magnetic state after the input writing (I) and the logic operation (II) was recorded and corresponds to S1 and S3, respectively [Fig. 3(b)]. The magnetic state of each element was inferred from their white/black contrast in the MFM image. Assuming the magnetization direction points from white to black, we observed the correct output, (1,1), results from the input of (1,1,1). In summary, the 45° clocking mechanism was demonstrated to facilitate a robust full adder.

Finally, we would like to discuss the practical application of this full adder design using the 45° clocking mechanism. It has several advantages over the conventional designs. First, it enhances the tolerance against field misalignment to a practical level due to the intrinsic angular insensitivity in a specific angle, 45° off the hard axis. Therefore, reliable performance could be expected. Second, it requires smaller clocking field, about 50% in amplitude, to

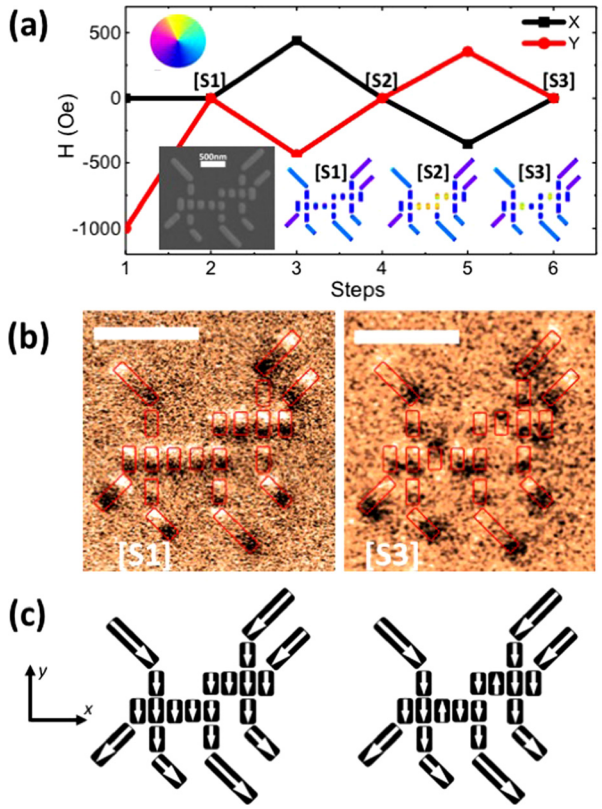

FIG. 3. (a) Reversal field used in the simulation for the full adder operation and (inset) corresponding magnetization states and color wheel representing the magnetization direction; (b) MFM images of the stage 1 [S1] and stage 3 [S3] for a 20 nm-thick Fe sample fabricated by electron-beam lithography, with the scale bar representing 1 μm; (Inset of (a)) SEM image of the lithographically fabricated sample. Magnetic field amplitude in (a): step1–1000 Oe; step 3–620 Oe; step 5–502 Oe. All magnets are in width of 100 nm, with the gap between adjacent elements kept the same at 50 nm. The lengths of the *logic operation* magnets are tuned to 250 nm, 200 nm, 175 nm, 162.5 nm, and 150 nm, respectively, to ensure the unidirectional signal flow.

reverse the nanomagnets. In practice, this clocking field is generated by a current through a copper wire beneath the logic surface. Thus, a reduction of current density[18] in scale of $\sim 10^6$ A/cm^2 would help further optimize the heat dissipation and elongate the device lifetime. Third, such a design requires much fewer elements, about 1/3 compared with conventional design,[11] indicating higher integration density and less fabrication processes. More than that, the progressive tuning of element shape anisotropy guarantees unidirectional signal flow. It prevents fault signal introduced by either data back-flow or random ambient noise. Moreover, this unidirectional signal flow renders the systematic designs and blocking builds of MQCA more reliable.

Admittedly, the reversal field mechanism requires multiple clocking cycles for the signal to propagate. However, it only brings extra steps to the scale of N, which is the number of required reversals for the local clocking units, typically 3 or 4. As reported, the switching occurs below 1 ns, suggesting GHz clocking frequency.[19] Thus, the influence on the circuit speed will be very limited.

The integration of MQCA logic with current CMOS technology requires a robust reading/writing system, which has been designed based on MTJ[20] and spin-transfer torque,[21] where the magnetic state of the individual element is electrically measured.[22] On the other hand, employment of the spin hall effect has been reported to deliver a spin torque for clocking.[23] For example, the magnetization of CoFeB elements has been reported to align to their NULL state by a current through the underlying Ta wire.[24] The current required is much smaller than that from a copper wire. All these mechanisms make it feasible to integrate the MQCA device into the CMOS circuits.

VI. CONCLUSION

In summary, practical application of MQCA logic requires a robust clocking mechanism with low error rate. Our full adder design with 45° clocking field enables unidirectional signal flow and correct output. It is also advantageous in lower heat dissipation and higher integration density. Thus, this misalignment-free full adder using the 45° clocking mechanism paves way for the application of MQCA.

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