A Case Study on the Power Quality Issues in the Hospitality Sector

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Abstract: This paper analyzes various power quality problems that occur in a famous hotel (a hospitality sector). Pollutions such as harmonics are generated due to the luxurious facilities offered in hotels generally. Such problems are caused by the systems as well as other loads connected to the system. Due to the various power quality problems, the equipment connected to the system get affected. A case study is done in a hotel and the various power quality problems have been studied. Data are taken on primary side of the transformer, power panel supply of chiller unit, air humidity unit, lift unit and lighting supply unit, and are analyzed. Further, the power flow and harmonic load flow on the hotel model are studied through ETAP power station package. The harmonic load flow is then used for the designing of a single tuned filter using iteration method to reduce the current THD and avoid the penalty imposed by the utilities.

Key words: power quality, harmonic analysis, single tuned filter, total harmonic distortion

Abbreviations:

AHU: Air handling unit

TOB: Total observation blossom THD: Total harmonic distortion TDD: Total demand distortion VFD: Variable frequency drive PCC: Point of common coupling PFC: Power factor correction UPS: Uninterrupted power supply

P.F.: Power Factor
LT: Low Tension
DG: Diesel Generator
SSB: Station Supply Board
CFL: Compact Fluorescents Lamp

HV: High Voltage

I. INTRODUCTION

In hotels, various power quality problems arise due to the improvement of facilities like UPS and lift operation. Problems such as harmonics and voltage imbalances in hotel industry affect the grid system.

Nowadays, many countries impose penalty on industries

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Paper submitted to the International Conference on Power Systems Transients (IPST2013) in Vancouver, Canada July 18-20, 2013.

whose systems pollute through harmonics. Hence, assessing the power quality problems in industries becomes essential to avoid penalty and reduce damage to the equipment.

In this context, as a case study, a specific hotel industry is taken to analyze its power quality. Data have been collected from HV side of transformers, chiller unit, air humidity unit, lift unit and lighting power panel supply of the hotel. Using Fluke 1735 model and <u>Circutor</u> Spain and <u>AR5L</u> model analyzers, various power quality issues are measured and the results are provided to each department.

In the case study, the power quality problems like voltage imbalance, P.F and harmonics alone could be studied. The above power quality problems are revealed in Section II. Section III studies the simulation made through ETAP and the designing of single tuned filter to limit the harmonics.

II. POWER QUALITY ISSUES

The single line diagram of the hotel under study is shown in Fig. 1. The voltage and the current power quality issues are measured from the PCC of air handling unit, chiller unit, lift, laundry, lighting and on HV side of the transformer. A variable frequency drive is used to control the motors used for the cooling tower, AHU and lift.

A. Single line Diagram

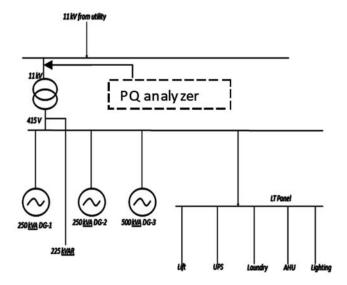


Fig. 1 Single line diagram of the hotel.

The hotel has three diesel generators with a capacity of 2×250kVA and 1×500kVA each to feed the load whenever there is any interruption of supply from the utility. 200kVAR capacitor, a permanent static capacitor, is used to maintain the power factor in addition to an AFC 225 kVAR capacitor. From the transformer, various sections like, lift, laundry, air handling units and lighting in the hotel are being fed through the LT panel. A 22kVA UPS is connected to the LT panel to feed the lighting in corridor, pantry and car parking area during the change over time from the utility supply to the DG supply during interruption.

B. Power Factor

The Electricity Board is imposing penalty whenever consumers go below 0.85lag in the power factor. Hence, the consumers have to take steps to maintain the power factor to avoid penalty. Static capacitors of capacity 200kVAR along with 225kVARAFC capacitor are used in the hotel under study to maintain the power factor.

Fig.2 and Fig.3 are the power factor spectrum measured on the HV side of the transformer by providing power quality analyzer as shown in the Fig. 1. with and without capacitors respectively. From the above power factor profile, it is evident that the facility is maintaining power factor between 0.87 and 0.98 (lagging) with capacitors. When there are no capacitors, the power factor ranges between 0.83 and 0.85 (lagging). Hence, there is no possibility of imposing the penalty due to low power factor by the utility.

C. Voltage Imbalance

The voltage imbalance is the deviation of each phase from the average voltage of all the three phases [1].

Voltage imbalance = 100×maximum deviation from averagevoltage/averagevoltage

averagevoltage/averagevoltage (1) Averagevoltage = sum of voltages of each phase/3 (2)

Normally, the motors can tolerate a voltage imbalance of 2%[1].

The voltage is measured in the three phases on the incoming side of the transformer and is shown in Fig.4.

The voltage imbalances of the facility are less than 0.7% and they are within the limit (less than 2 %).

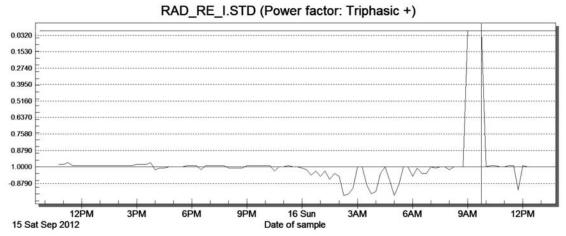


Fig. 2 Power Factor spectrum with capacitors

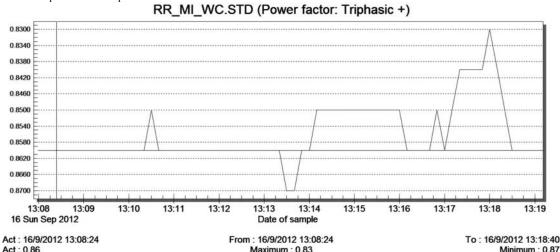


Fig. 3 Power Factor spectrum without capacitors

MULTIGRAPHIC RAD_RE_I.STD (Voltage: Phase 2 - Phase 3) RAD_RE_I.STD (Voltage: Phase 1 - Phase 2) RAD_RE_I.STD (Voltage: Phase 3 - Phase 1) 10000 8000 6000 4000 2000 3PM 6PM 16 Sun 3AM 6AM 9AM 12PM 15 Sat Sep 2012 Date of sample Selected Variable: RAD_RE_I.STD (Voltage: Phase 1 - Phase 2) Act: 15/9/2012 10:45:09 From: 15/9/2012 10:45:09 To: 16/9/2012 12:30:00

Maximum: 10800 (V)

Fig. 4 Voltage spectrum of line voltage at HV side of the facility's transformer

D. Harmonics

Act: 10200 (V)

The voltage and current harmonics are measured on the incoming side of the facility transformer and the PCC of the chiller, AHU, laundry and lift. The harmonics measured are shown in the Tables I to III.

The fault level calculated at the facility side is designed to 20,000 MVA and the maximum capacity of the facility is 650 MVA. The calculated I_{SC}/I_L is 30.8. Hence, the limits are referred to the range 20-50 in the IEEE 519-1992 standards.

Desc	11 kV Main incomer with PFC capacitors		11 kV Main incomer without PFC capacitors				
	Phase						
		R	2.00%		2.20%		
	V	Y	2.00%		2.20%		
Measured % of THD		В	1.90%		2.20%		
Measured % of 1 HD		R	9.50%		5.70%		
	I	Y	8.70%		5.30%		
		В	9.50%		5.30%		
	As per IEEE – 519, 1992, TDD%					8.00%	
	Total Voltage Distortion THD (%) for the bus voltage ≤ 69 kV					5.0%	
As per IEEE – 519	As per IEEE – 519, 1992, I _{sc} / I _L range					20 - 50	
As per IEEE – 519.			Measured %		Measured %		
permissible % of ind	lividual	Order of	of indi	ividual	of individual		
voltage & current ha	rmonic	Harmonics	Harn	onics	Harn	onics	
V	I		V	I	V	I	
3.0	7.0	3	0.567	0.711	0.281	0.596	
3.0 7.0		5	1.448	4.856	1.945	4.953	
3.0 7.0		7	0.958	7.996	0.93	3.063	
3.0			0.16	0.503	0.124	0.198	
3.0			0.344	2.21	0.418	1.316	
3.0	3.0 3.5		0.228	0.996	0.077	1.316	
3.0			0.084	0.104	0.12	0.171	
3.0	3.5	17	0.18	0.302	0.165	0.54	

From Table 1, it is found that the current THD without PFC capacitors measured is within the limits specified by IEEE, but THD measured are 9.50%, 8.7%, and 9.50% in the three phases and are beyond the limits specified by IEEE when PFC capacitors are connected. The individual 7th order harmonics alone is measured to be 7.996% and is slightly higher than the limits specified by IEEE 519-1992 standards when the capacitors are connected to the system of study. These harmonics are formed due to the resonance between the supply circuit and the capacitors connected for the improvement of the power factor [2].

Minimum: 0 (V)

The resonant frequency
$$f_r$$
 [2] is given by
$$= (MVA_{fl}/MVA_c)^{1/2}$$
where

 MVA_{fl} = three phase fault level at the consumer bus bar in MVA

 MVA_c = total capacitor output in MVA_r .

The fault level calculated is 20000MVA at the consumer bus bar and the PF correction static capacitor provided is 200KVAR and hence the resonance frequency works out to 316Hz. The harmonic order works out to be 316/50 = 6.3. This reveals that the harmonic order due to the connection of the capacitors is 7.

The harmonic currents interacting with the PF capacitors will cause equipment failure. Since, the PFC capacitors are a must to avoid the penalty to be imposed by the utility for low power factor, suitable filters are to be installed. Hence, it is essential to provide a suitable tuned filter, both to compensate the harmonics and correct the PF.

TABLE II VOLTAGE AND CURRENT HARMONICS AT INDIVIDUAL DEPARTMENTS (PART-I)

					(41K I - I	,					
Description			Chiller – Chiller – 2 (York) (Clivet)		Lighting		AHU-SSB2		AHU- TOB			
Phase		Phase	TI	ID%	TH	D%	TH	D%	TH	D%	TH	D%
		R	6.	96%	1.9	3%	2.1	2%	2.0)4%	2.1	6%
Meas	V	Y	2.	11%	1.8	2%	2.0	9%	1.8	37%	1	.95%
ured		В	2	21%	1.9	9%	2.1	6%	2.1	12%	2.2	4%
% of		R	3.60%		4.43%		11.50%		28.71%		3.22%	
THD	I	Y	3.	94%	4.67%		10.12%		25.62%		3.65%	
		В	4.	14%	4.7	2%	10.7	77%	62.	46%	3.55%	
As per	IEEE TDI	-519, 1992, 0%	8.00	0%	8.00%		8.00%		8.00%		8.00%	
Total Voltage Distortion THD (%) of individual voltage ≤ 69 kV			5.0% 5.0%		5.0%		5.0%		5.0%			
As per IEEE-519, 1992, permissible % of individual voltage & current harmonic		Order of Harmon- ics	Meas % indivi harm	of idual	% indiv	of idual	indiv	of idual	% indiv	sured o of vidual nonics	% indiv	
V	I		V	I	V	I	V	I	V	I	V	I
3.0	7.0	3	5.239	0.406	0.420	0.605	0.68	8.951	0.356	7.502	0.329	2.472
3.0	7.0	5								38.978		
3.0	7.0	7								34.226		
3.0	7.0	9	0.658	0.161	0.174	0.011	0.278	1.772	0.221	4.862	0.219	0
3.0	7.0	11								24.518		

Table II shows the current THD and individual harmonics measured in lighting panel, chiller units, AHU SSB2 and AHU TOB. The current THD measured in lighting panel, and in AHU SSB2 alone are higher than the IEEE standards. The third and fifth order current harmonics in the lighting panel are higher than the limits. In the lighting panel, a load of 40kW bulbs are connected for the lights in the corridor, car parking, etc. and 7.0 hp capacity motors are provided in the car parking for the pumping of water for cleaning purpose.

TABLE III HARMONICS MEASURED IN VARIOUS DEPARTMENTS

			(PAR	1-11)					
Description	Description			Lift		Laundry		UPS	
Phase		Phase	THD%		THD%		THD%		
R		2.14%		2.13%		1.92%			
	V	Y	2.14%		1.97%		2.17%		
Measured % of		В	2.2	29%	2.1	8%	1.85%		
THD		R	35.	31%	2.4	3%	3	0.47%	
	I	Y	52.19%		3.3	4%	31.83%		
		В	27.	50%	2.1	9%	3	2.23%	
As per IEEE-51	As per IEEE-519, 1992, TDD%		8.0		8.0		8.0		
	Total Voltage Distortion THD (%) of individual voltage ≤ 69 kV		5.0%		5.0%		5.0%		
As per IEEE-519, 1992, permissible % of individual voltage &		Order of Harmonics	% of in	easured idividual nonics	% indiv	easured of idual ionics	% of ir	easured idividual nonics	
current harmonic			V	I	V	I	V	I	
		3	0.784	8.696	0.345	1.72	0.197	7.703	
		5	1.443	43.694	1.305	1.457	1.603	22.288	
		7	1.682	26.134	1.767	2.133	1.617	13.344	
		9	0.249	4.203	0.145	0.766	0.053	4.875	
		11	0.618	12.105	0.659	0.81	0.3	10.148	
		13	0.308	7.346	0.395	0.574	0.123	8.483	

The lighting bulbs are of CFL type. The CFL bulbs are used for efficient consumption of electricity. Previously, harmonics due to the choke used in CFL have been ignored since the injection is small. But the total becomes significant [3]. In this study, the predominant harmonic is the 5th followed by the 3rd order.3rd, 5th, 7th and 11th order current harmonics and current THD in AHU SSB2 are higher than the limits specified by IEEE standards. Since the motors are driven by 6 pulses Thyristor controlled VFD and Fluorescent lights of 40kW with ballistic chokes connected in the panel, the individual harmonics 3rd, 5thand 7thand 11th and current THD

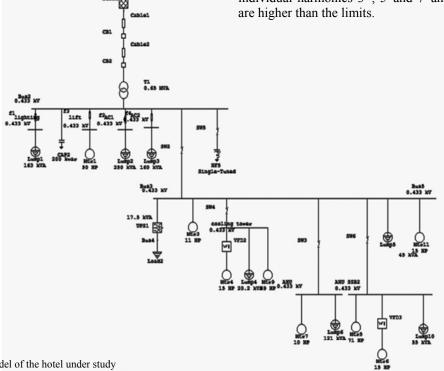


Fig. 5 Simulation Model of the hotel under study

The current THD in the lift unit and UPS and their individual harmonics 3rd, 5th, 7th, 11th and 13th are very much higher than the IEEE standards, since the motors are driven by 6 pulse Thyristor controlled VFD and Fluorescent lights for the lift and SMPS in UPS system.

Although, the individual harmonics and current THD measured in AHU SSB2 unit, lift and lighting unit are higher than the IEEE standards, the penalty would be levied to the industry through the measurement of THD on the incoming side of the transformer. The maximum current THD and individual 7th order current harmonics measured on the incoming side of the transformer are 9.50% and 7.996% respectively as per Table I which are higher than the limits.

Since, providing the filters in each unit and carrying out the maintenance, the cost will be higher than the penalty (15% of kWh) to be imposed by the utility. Hence, it is must to concentrate on the incoming side to reduce the harmonic limits, to avoid penalty and also reduce the installation cost, thus avoiding pollution in the grid. Hence, simulation is made through ETAP power station package and a suitable filter is designed.

III. SINGLE TUNED FILTER DESIGN

A. Simulation model

Non linear loads present in the hotel pollute the power supply and also leads to imposing of penalty.

Penalty is being imposed for higher value of THD by measuring the primary side of the transformer. Hence, it is necessary to provide a filter for harmonic suppression. In order to design the filter, a simulation model through ETAP [4], [5] is developed. The simulation model is shown in Fig. 5.

In the given simulation model which is based on the actual load, each department is separated from others by buses. Such a model facilitates easy analysis of the data through simulation and the comparison with the original data.

Using the simulation model, power flow and harmonic flow study was done. Using the power flow and harmonic flow study, single tuned filter[6] is designed. The impedance characteristic of the filter is shown in the Fig. 6

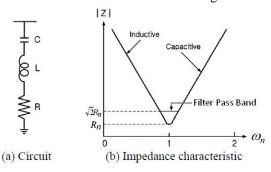


Fig. 6 Circuit and Impedance characteristic of single tuned filter.

B. Design equations for a single tuned filter

A single tuned filter which is a series RLC circuit tuned to a single harmonic frequency provides a low harmonic impedance characteristic.

Its total impedance is given by

$$Z = R_n + j(\omega L_n - 1/\omega C_n) \tag{4}$$

At a resonance frequency
$$\omega L_n = 1/\omega C_n$$
 and hence $Z = R_n$ (5)

An ideal single-tuned filter is said to be tuned to the frequency that makes its inductive and capacitive reactance equal.

Q (Quality factor) is defined as the ratio of the inductance (or capacitance) to the resistance at the resonant frequency.

i.e.,

$$Q = X_{\rm n}/R_{\rm n} \tag{6}$$

Tuned factor (δ) in relation with resonant frequency $\omega = \omega_n(1 + \delta)$ (7)

$$\delta = (\omega - \omega_{\rm n})/\omega_{\rm n} \tag{8}$$

$$\omega = \frac{1}{\sqrt{IC}} \tag{9}$$

The reactance of inductor or capacitor in ohms at the tuned frequency is

$$X_{\rm n} = \omega_{\rm n} L_{\rm n} = \frac{1}{\omega_{\rm n} c_{\rm n}} = \sqrt{\frac{L}{c}}$$
 (10)

$$Q = \frac{X_n}{R_n} \tag{11}$$

$$C_{\rm n} = \frac{1}{\omega_{\rm n} X_{\rm n}} = \frac{1}{\omega_{\rm n} R_{\rm n} Q} \tag{12}$$

$$L_{\rm n} = \frac{X_{\rm n}}{\omega_{\rm n}} = \frac{R_{\rm n}Q}{\omega_{\rm n}} \tag{13}$$

By substituting the above results, the parameters of the single tuned filter are expressed in terms of quality factor (Q) and tuned factor $(\delta)[7]$.

$$\omega L_{\rm n} = \omega_{\rm n} (1+\delta) \cdot \frac{R_{\rm n} Q}{\omega_{\rm n}} = (1+\delta) R_{\rm n} Q \tag{14}$$

$$\frac{1}{\omega C} = \frac{1}{\omega_n (1+\delta) \cdot \frac{1}{\omega_n RO}} = \frac{R_n Q}{1+\delta}$$
 (15)

$$Z = R_{\rm n} + j \left(\omega L_{\rm n} - \frac{1}{\omega C_{\rm n}} \right) = R_{\rm n} + j \left[R_{\rm n} Q \left\{ \frac{\delta(2+\delta)}{1+\delta} \right\} \right] \quad (16)$$

$$Z = R_{\rm n} \left\{ 1 + jQ\delta \left(\frac{2+\delta}{1+\delta} \right) \right\} \tag{17}$$

Or, considering that δ is relatively small as compared with unity,

$$Z = R_{\rm n}(1 + j2\delta Q) \tag{18}$$

and in terms of impedance is
$$X_n(Q^{-1} + j2\delta)$$
 (19)

$$Z \approx R_{\rm n} (1 + 4\delta^2 Q^2)^{1/2}$$
 (20)

C. Designing of single tuned filter

The power flow analysis and harmonic load flow analysis are conducted on the simulation model through ETAP. The predominant harmonic order found on the incoming side is 7th. The single tuned filter is then designed to suppress the 7th order harmonics, to maintain P.F. and to avoid penalty. The details obtained through ETAP software simulation are used for filter design. The harmonic load flow details without and with filter are given in Table IV.

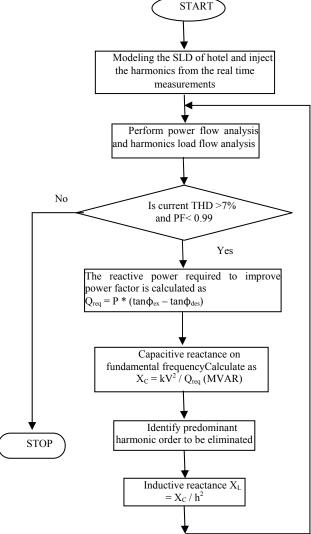


Fig. 7 Flow chart for designing single tuned filter.

TABLE IV
LOAD FLOW AND POWER FLOW WITH AND WITHOUT FILTER

Sl.no	Harmonic order	Voltage (kV)	Real power kW	•	Load kVA	p.f%	%V THD
1	7(without filter)	0.432	794	141	801	0.83	7.73
2	7(with filter)	0.433	804	130	794	1.00	4 28

The filter design is performed in an iterative manner. The flow chart shown in the Fig.7 gives the step by step procedure for the design of the single tuned filter. The design values to reduce the level of harmonics are given in Table V.

TABLE V FILTER DESIGN

	T IETER DESIGN	
Sl. no	1	2
Harmonic order	THD	7
Actual measured values in %	9.5	7.99
Simulation model (without filter) values in %	10.05	8
with filter in %	4.28	4
Capacitor value (kVAR)	131	131
Inductive reactance (ohms)	0.0243	0.0243
Q factor	80	80
limit as per IEEE	8	7

D. Simulation results

The load connected in the hotel is assumed as the current source. The simulation is carried out through the model without and with filter. The voltage waveforms on the primary side of the transformer without and with filter are given in Fig. 8 and Fig. 9. The harmonics spectrum on the primary side of the transformer without filter is shown in Fig. 10 and it is higher than the limits. The harmonics spectrum on the primary side of the transformer with filter is shown in Fig. 11 and is found within the limits.

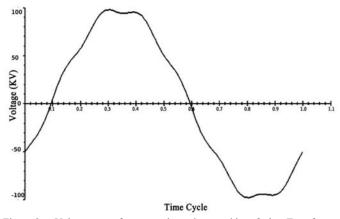


Fig. 8 Voltage waveform on the primary side of the Transformer without filter.

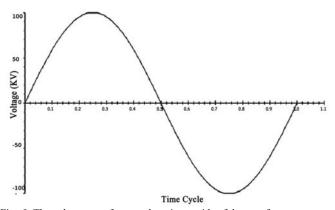


Fig. 9 The voltage waveform on the primary side of the transformer with filter.

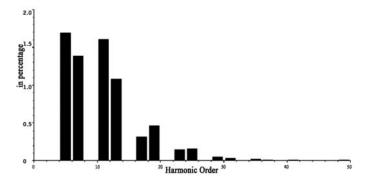


Fig. 10 The harmonic spectrum on the primary side of the transformer without filter.

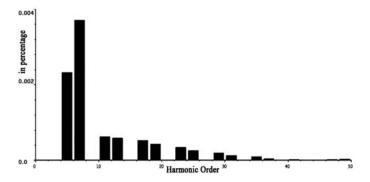


Fig.11 The harmonics spectrum on the primary side of the transformer with filter.

IV. CONCLUSION

In most of the countries, penalty is imposed when the harmonic levels are higher than the limits specified for the respective utilities. The reason for choosing a hotel for case study is that there is an enormous expansion of this sector in recent times.

In the hotel under review, except the THD and individual harmonics, all the other power quality problems are found to be well within the limits. Hence, attention is focused on the harmonics in the paper in designing the filter.

The Electricity Board has not framed any limits on the harmonics and hencelimits specified by the IEEE are followed.

In this case study, even though the individual current harmonics of order 3rd, 5th, and 7th in the panels of lift, laundry, AHU SSB2 and in UPS are higher than the limits specified by the IEEE standards, the current harmonics of order 7th alone is found to be higher on the incoming side of the transformer. Since, the utility is measured for energy billing from the incoming side of the transformer, the simulation is made through ETAP in designing the single tuned filter to suppress the 7th order harmonics and limit the THD.

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