A Compact X-Band Coplanar Waveguide Hybrid Lowpass Filter

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***Abstract*—The paper presents the design of a compact coplanar waveguide lowpass filter in the X band. The lowpass filter has a 3-dB cutoff frequency of 10 GHz. The compact size is achieved due to the use of localized surface mount capacitive loading. For the first time, the employment of localized loading capacitors for miniaturization proves to be efficient at high frequencies. The designed hybrid filter proves to have smaller size and better performance than commercially available filter with which a comparison is made.**

***Index Terms*—Coplanar waveguide technology, compact lowpass filter, miniaturization, semi-lumped, X-Band**

I. Introduction

In microwave communication systems lowpass filter is an important device that is usually employed in the design of RF systems. Planar filters are very popular because they can be fabricated using PCB technology and are appropriate for commercial applications due to their relatively simply design, compactness and low cost of fabrication.

With the advancement of applications of wireless communication systems, the development of filters has emphasized compact size and high performance. Several miniaturization techniques have been reported. The most used techniques can be classified under three categories: the use of high permittivity substrates [1]-[5], tilting, folding and meandering [6]-[7], and the use of hybrid approach [8]-[15]. The three categories are discussed in the next paragraphs.

The use of substrates with high relative dielectric permittivity (ε_r>20) is effectively reported in some researches providing a good percentage of miniaturization of around 45% [1]-[5]. However, the drawbacks of using high permittivity substrates are bandwidth reduction, high cost, and difficulty in achieving high impedances. High impedances are very important in achieving acceptable electrical characteristics.

Meandering technique, on the other hand, helps obtaining compact devices. However, the disadvantage of such a technique is the increase of circuit complexity [6]-[7]. Moreover, parasitic coupling effects of nearby elements should be accounted for while designing which can add further circuit complexity. Researchers using this technique reported miniaturization percentages around 50%.

Thirdly, the hybrid approach is heavily used due to its simplicity in design. It is achieved by loading transmission lines with lumped elements (mainly capacitors) [8]-[15]. It is usually referred to as the "semi-lumped" approach. The advantage of employing the semi-lumped approach, compared to the use of distributed approach (only transmission lines), is clearly the miniaturization. On the other hand, its advantage compared to the purely lumped approach (exclusively capacitors and inductors), is to overpass the normalized value problem. For these reasons, the semi-lumped approach is used in this work.

Authors in [8]-[9] reported that by adding lumped capacitors to a transmission line while increasing its characteristic impedance permits to reduce the physical length of the transmission line and thus overall device dimensions. The capacitors can be added either at the middle of the transmission lines [8] or at the extremities [9]. Inductors can be used instead of capacitors, but they suffer from very poor quality factor especially at high operating frequency [9].

The use of localized surface mount components (SMC) for miniaturization has been proved very effective for frequencies reaching no higher than 2-3 GHz. However, to the authors' knowledge, no studies on the possibility of using localized SMC for miniaturization at higher frequencies are done.

In this paper, a compact lowpass filter having a 3-dB cutoff frequency of 10 GHz is designed. The employed design is the coplanar waveguide technology (CPW) for its effectiveness at high frequencies.

The organization of the paper is as follows: First, in Section II, the design of a hybrid lowpass filter having a cutoff frequency around 10 GHz is presented. Fabrication and measurement results are presented and discussed in Section III. Then, a comparison of the designed filter with commercially available lowpass filter is made.

II. Hybrid Lowpass Filter Design

A. Employed Topology

Several topologies based on the use of semi-element approach have been proposed. One of the efficient topologies in reducing the size of a filter is the one proposed in [8]. The authors in [8] proposed to load

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transmission line sections at their middle by SMC capacitors. The equation giving the value of the loading capacitance in function of the transmission line parameters is available in [8]. Several lowpass filters were designed at 1 GHz, fabricated and validated. The filters show good characteristics in terms of compactness, return loss, insertion loss, shape factor (selectivity) and suppression of spurious. This topology is employed in this paper to design a lowpass filter having a 3-dB cutoff frequency of 10 GHz. However, at high frequencies SMC capacitors present parasitic effects. In the next sub-section, a model of these capacitors is suggested and validated in order to use during filter design.

B. Modeling of SMC Capacitors

At high frequencies, the parasitic effects of lumped elements (SMC capacitors here) must be taken into account. Above a certain nominal frequency to be defined later, lumped elements could introduce severe design problems. Moreover, the pads used for soldering the capacitors should be modeled for the design to be accurate.

Several models of SMC capacitors were reported by researchers [16]-[18]. In this work, the series RLC model is used. The model is inspired from different models in [16]-[18]. It is simple and efficient, as shown in Fig. 1. For each SMC capacitor, a parasitic series resistance R_s and an inductor L_s together with a shunt resistance (R_p) are used to create the model. These elements take into account the parasitic effects at high frequencies. The series inductor L_s is included to represent the conduction and displacement current densities in the metallic and dielectric parts of the capacitor that lead to a surrounding magnetic field. R_s is added to represent the dielectric and Ohmic losses in the capacitor and is usually referred to as the equivalent series resistance (ESR). The shunt resistance (R_p) represents the coupling losses between the electrodes of the capacitor. R_p has usually very large values even at high frequencies. For simplifying the model, R_p can be neglected. The measurement results will confirm the validity of the last decision.

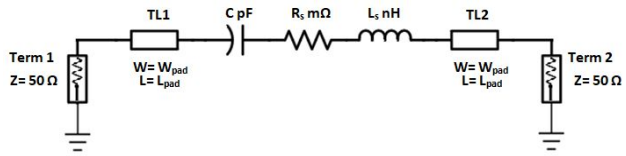


Fig. 1. Capacitor equivalent model.

As for the pads used for soldering the SMC capacitors, we propose to model them as short transmission lines. The length of the transmission lines representing the pads is kept less than $\lambda/10$. This choice is very realistic since the pads are extensions of lossy transmission lines in most cases. Neglecting the parasitic effects of the pads modifies the propagative characteristics of the EM wave and hence the design.

Fig. 1 shows the complete used parasitic model of the SMC capacitor having a nominal capacitance value C (pF). In this case, the capacitor is connected in series between an input and an output port. The model is constructed using the circuit simulator advanced design system (ADS). When simulated for its frequency response, the capacitor circuit model will exhibit a minimum impedance value at a specific frequency called the self-resonant frequency (SRF). The SRF can be analytically determined from the capacitance C and the series parasitic inductance (L_s). At the SRF, the capacitive and inductive reactance values are equal ($1/2\pi fC = 2\pi fL_s$). Capacitors behave as inductive devices at frequencies above the SRF and, as a result, cannot be employed. The model of capacitors is extracted using measurements by fitting the values of the parasitic elements R_s and L_s of Fig. 1.

For measurements, the SMC capacitor is welded at the center of a CPW transmission line between the main conductor and the ground plane as shown in Fig. 2. The used SMC capacitor has a capacitance of 0.2 pF and a case size 0603. This capacitance value is of interest for the design of the LPF in the next subsection. The used CPW transmission line has a moderate characteristic impedance of 50 Ω. These arrangements guaranty good accuracy in extracting the model. It is worth recalling that without accurate modeling, the use of the SMC capacitors will induce design imprecision.

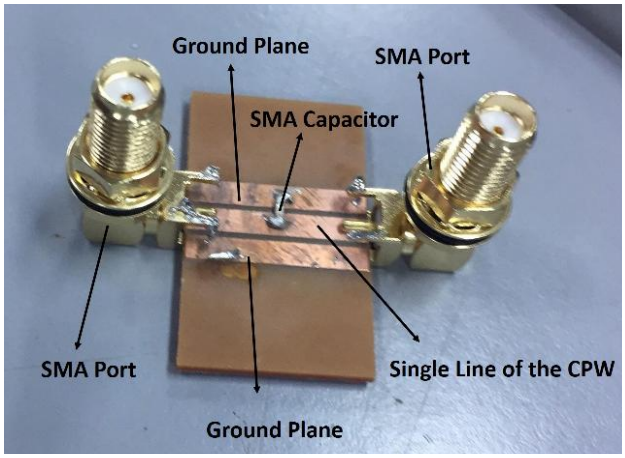


Fig. 2. Photograph of the soldered capacitor.

A TRL (thru, reflect, line) calibration was performed prior to measurements. The S-parameters of the loaded transmission line were extracted up to 13.6 GHz using the Rohde&Schwarz ZVL vector network analyzer.

The next step was to fit the measurement results to the simulation results of the model by varying the values of R_s and L_s. Fig. 3 shows a comparison of the S-parameters obtained from measurements and from model simulation. The best fit can be obtained for L_s=0.78 nH and R_s=530 mΩ. It is worth noticing that the SRF of these capacitors does not appear in the investigated frequency band. So, this type of capacitors can be used safely for targeted X-band frequency range. The same procedure is done for another capacitance value.

This value is 0.15 pF. The results of the capacitor's model optimization are shown in Fig. 4. The figure shows a comparison of the S parameters results between measurements and model simulations of the 0.15 pF SMC capacitor (case size 0603).

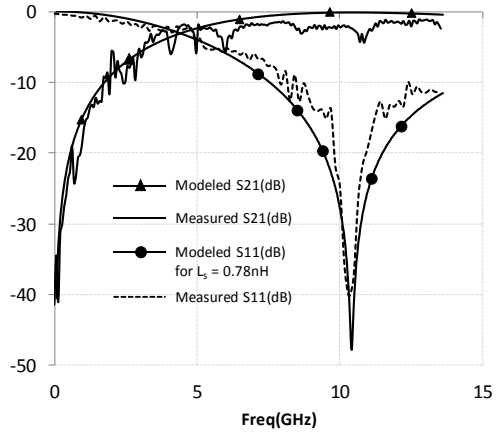


Fig. 3. Comparison of S-parameters of the 0.2 pF capacitor: Measured and modeled.

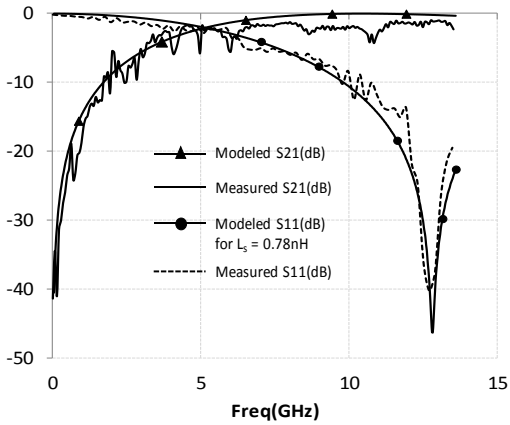


Fig. 4. Comparison of *S*-parameters of the 0.15 pF capacitor: Measured and modeled.

Again, this capacitance value is of interest for the design of the LPF in the next subsection. The obtained value of the series inductance L_s was found to be 0.78 nH and the value of the equivalent series resistance R_s is 580 mΩ. L_s has the same value as in the previous case of the 0.2 pF capacitor. This is logical because theoretically the value of L_s is defined by the case size and dimensions of the employed SMC (0603 in this case). Here again, the SRF does not appear in the band of interest. On the other hand, R_s which represents the dielectric and Ohmic losses in the capacitor (usually referred to as the equivalent series resistance ESR) depends on the value of the capacitance and defined by the fabrication accuracy of the capacitor.

C. Lowpass Filter Design

The desired filter template is of lowpass nature having a 3-dB cutoff frequency at around 10 GHz. The designed filter will be compared to commercially available filter RLPF13G09 offered by offered by RF-LAMBDA©.

For comparison reasons, the desired lowpass filter template should exhibit an insertion loss of no more than 1 dB at half the cutoff frequency f_c, and the spurious should not appear until at least double the cutoff frequency. The filter should be matched (return loss better than -10 dB within the operating passband) and have a cutoff roll selectivity higher that 50 dB/GHz. The design encompasses both distributed elements and localized ones. As the target is to operate in the X-band, the localized component is chosen to be capacitor. The reason is that capacitors have relatively higher quality factors than inductors. The idea, again, is to transfer the use of lumped SMC elements into higher frequency using appropriate design (technology and topology).

The coplanar waveguide (CPW) technology is adopted. The reason for using the CPW technology is because it has generally smaller frequency dispersion than microstrip technology especially in the case of our design where narrow transmission lines (high characteristic impedances) are required. Moreover, the presence of the ground planes from both sides of the strip in the case of CPW transmission lines avoids the use of via holes that, at relatively high operating frequencies, need to be precisely modeled. The filter is designed using Rogers RO4003® substrate having as parameters: dielectric constant ε_r=3.55, height h=813 µm, metal thickness t=35 µm and loss tangent $\tan\delta$ = 0.0027.

Fig. 5 shows an ideal schematic of the proposed filter. It is composed of six sections defining, hence, the order of the filter (sixth order). This order is sufficient to get a high roll off selectivity as required. Each elementary section is composed of two ideal transmission lines and a capacitor. The capacitor is connected at the center of the transmission lines for simplicity reasons. The parasitic model of the capacitors is not considered is this preliminary investigation.

In order to get good matching characteristics in the passband, taperization is used as shown in Fig. 5. Taperization consists of breaking the topology's periodicity by changing the characteristic of the sections at the input and at the output of the filter. Taperization is achieved in this case by varying the length of the transmission lines at the near and far end sections (θ_1, L_1) and/or varying the corresponding loading capacitance of the near and far-end sections (C_1). On the other hand, the sections at the middle have equal electrical length θ_2 (corresponding to physical length L_2) and loaded by capacitors of same capacitance value C_2. It is worth mentioning that the characteristic impedance Z_c of all transmission line sections (middle and near and far ends) have the same value. For minimal filter dimensions, it is interesting to use high characteristic impedance values.

However, due to fabrication constrains the maximum characteristic impedance that can be used for all the transmission lines is limited in this work to 120 Ohms corresponding on the considered substrate to a width (W) of 0.25 mm and a gap (G) of 1.3 mm. For ground plane uniformity, all transmission lines will have the same values for the width W and the gap G.

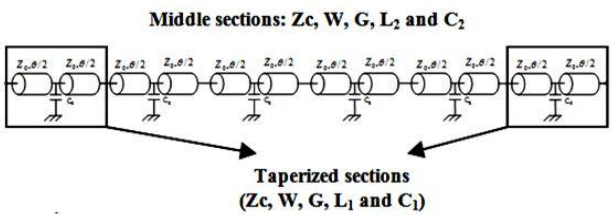


Fig. 5. Schematic of the sixth order lowpass filter.

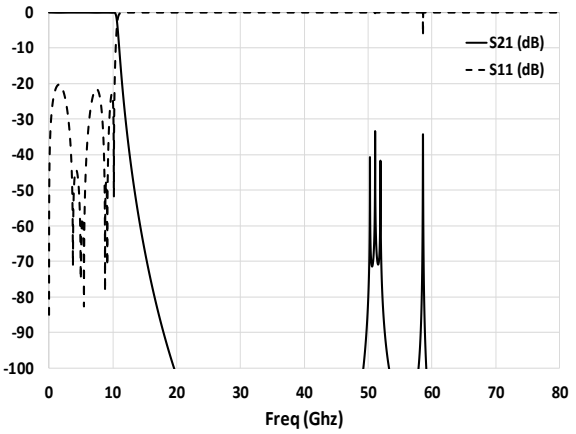


Fig. 6. Preliminary results of the return loss S11 and the insertion loss S21 in dB of the lowpass filter.

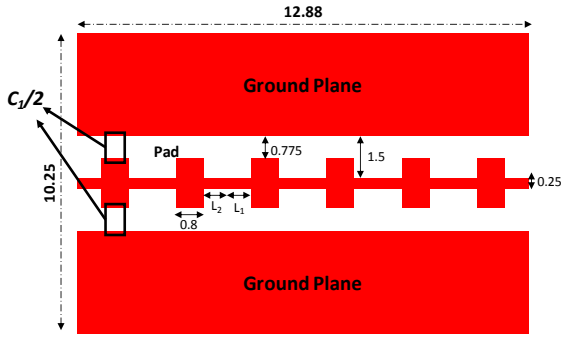


Fig. 7. Layout of the CPW lowpass filter (dimensions in mm).

Fig. 6 shows the result of the first optimization that does not take into account all fabrication constrains and different parasitic effects. The optimized values of L_1, L_2, G, W, C_1 and C_2 are 0.96 mm, 1.29 mm, 5 mm, 1.64 mm, 0.42 pF and 0.49 pF respectively.

The simulation results meet the desired template. The matching in the passband is better than 20 dB and there are no spurious in the large band response. However, these results are very optimistic since there are some important effects that should be taken into account. As discussed earlier, at high frequencies, the parasitic effects of capacitors and the pads used for soldering them must be taken into account. Moreover, the capacitance values must be normalized.

The filter is re-optimized to meet the desired template by modifying the lengths of the transmission lines and the values of C_1 and C_2. The new optimization includes the capacitors' and pads' models and all fabrication constraints. The optimization is done using the electromagnetic simulator Momentum of ADS as it yields more accurate results. The generated layout of the optimized lowpass filter is shown in Fig. 7 (dimensions in mm). For clarity, not all the capacitors are shown in the figure. Only C_1 at the near end is represented. As shown in Fig. 7 for C_1, all capacitors are divided into two connected in parallel across the main transmission line.

Doing this ensures a more balanced response and helps reducing the effect of the series parasitic elements of the capacitor. The expected advantage is lower insertion loss of the lowpass filter. The capacitors used are the same as the ones modeled in the previous section $C_1/2$= 0.15 pF (taperized sections) $C_2/2$= 0.2 pF (middle sections). The simulation results are shown in Fig. 8. The cut-off frequency is at 9.7 GHz, the return loss is -16 dB, the spurious appears at 25 GHz, and the insertion loss is 0.11 dB at half the cut-off frequency and remains less than 0.5 dB until about 9 GHz. Moreover, the filter's cutoff roll selectivity is 65.8 dB/GHz. As the desired template is met, the filter is fabricated and measured for validation.

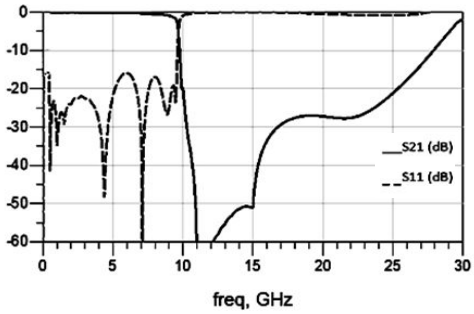
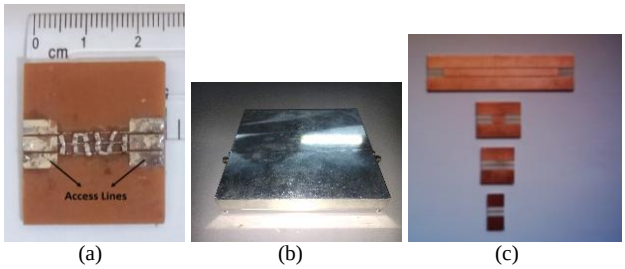


Fig. 8. Momentum Simulation Results.



(a) (b) (c)

Fig. 9. Fabricated devices: (a). the realized hybrid lowpass filter (with access lines), (b). the tested filter with packaging, (c). TRL calibration set.

III. Fabrication and Measurments

Fig. 9 shows the fabricated filter ((a) and (b)) and the TRL calibration kit necessary for measurements (c). Access lines were added at the two ports of the filter for measurement purposes. Fig. 9 (a) shows the filter without packaging. Fig. 9 (b) shows the measured filter with packaging.

Measurements were done using the ROHDE & SCHWARZ vector network analyzer up till 13.6 GHz. Fig. 10 shows that there is a good agreement between measurements and simulations.

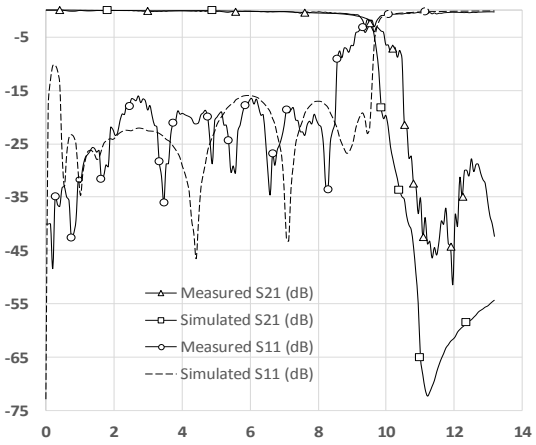


Fig. 10. Measured and simulation results of the return loss S11 and the insertion loss S21 in dB.

The results in Fig. 10 shows that SMC loading approach has potential in designing compact filters at high frequency (around 10 GHz) without deteriorating the electrical performance of the device. For that, surface mounted capacitors can be used in conjunction with coplanar waveguide technology offering, thus, very good compactness, maintained performance, and reduced cost.

For performance evaluation, the designed filter is compared with a commercially available one. The chosen filter is available among the products offered by RF-Lambda. The filter chosen is the RLPF13G09. The technology used in designing the filter is the Suspended Stripline technology. Of course, this technology is more expensive and relatively complicated. The filter is compared, as well, with other state-of-art filters [19]-[21].

TABLE I. COMPARISON BETWEEN DIFFERENT AVAILABLE FILTER AND THE FILTER DESIGNED IN THIS PAPER

Filter	[19]	[20]	[21]	RF-LAMBDA	This work
Bandpass (GHz) @ insertion loss < 1 dB	DC to 6 GHz	DC to 3.9 GHz	DC to 2.44 GHz	DC to 9 GHz	DC to 9.2 GHz
Insertion loss at 0.5 f_c	-1 dB	-0.5 dB	-0.67 dB	-1 dB	-0.11 dB
Return loss (S_{11})	-12 dB	-13 dB	-17.7 dB	NA	-17 dB
Selectivity (dB/GHz)	12	79.5	67.27	60	65.8
Spurious (S_{21}> -20 dB)	35 GHz	18 GHz	16 GHz	16 GHz	25 GHz
Dimensions: $L \times W$ (mm²) (with packaging)	22.9 × 7.5	16.8 × 7.55	17.4 × 10	26.92 × 22.09	12.88 × 10.25

Table I compares different recent filters, with the one presented in this paper. The comparison is performed in terms of bandpass (in GHz), insertion loss (in dB) at half the cutoff frequency, return loss (in dB), selectivity (in dB/GHz), spurious frequencies and physical dimensions. Comparing with RF-LAMBDA, it can be noticed that both filters have almost the same cutoff frequency. The filter designed in this work presents less insertion loss than the RF-LAMBDA filter (-0.11 dB compared to -1 dB). As for comparing with other filters published in [19]-[21], they all present higher insertion loss as well than our design. Moreover, the measured return loss (S_{11}) values show that all compared filters are matched to better than 10 dB. As for the out of band response, it is right that this work presents better response in the out band since the spurious appear at higher frequency (25 GHz for our filter compared to 16 GHz for the RF-Lambda filter, [20] and [21]). But still filter in [19] achieves higher out-of-band rejection. The proposed Lowpass filter is the smallest in size. Also it has the simplest design. Hence, the presented lowpass filter combines good electric characteristics with best compactness.

The good electrical performance of the filter and its compactness are due to the use of SMC elements. These elements have to be well modeled in order to be employed at high frequency.

IV. CONCLUSION

The design of a compact coplanar waveguide lowpass filter in the X band was presented. The lowpass filter has a 3-dB cutoff frequency of 10 GHz. The compact design makes use of localized surface mount capacitive as loading elements. Due to proper characterization, the use of surface mount capacitors proves to be efficient at high frequencies. Moreover, the use of the surface mount capacitors offers compact size and good electrical. The designed hybrid filter was compared to a commercially available filter having the same cutoff frequency. The comparison validated the efficiency of using localized surface mount components at higher frequencies.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

H. Issa is the main investigator in this work, he provided the research idea, conducted the first simulations, prepared the layouts for fabrication, conducted the measurements and characterizations, and wrote the paper. W. Diab validated the theory behind the work and conducted the simulations for the proposed design. M. Wehbi fabricated the circuits and helped with the measurements. All authors had approved the final version.

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