A Control and Measurement System for an Elevation over Azimuth Antenna Pedestal

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A dissertation submitted to the Department of Electrical Engineering,
University of Cape Town, in fulfilment of the requirements
for the degree of Bachelor of Science in Electrical Engineering.

Cape Town, October 2007

Declaration

I declare that this dissertation is my own, unaided work. It is being submitted to the Department of Electrical Engineering at the University of Cape Town in partial fulfillment of the requirements for the degree of Bachelor of Science in Engineering. It has not been submitted before for any degree or examination in any other university.

Signature of Author .....

Cape Town

22 October 2007

Abstract

This project concerns the design and implementation of a control and measurement system for an elevation over azimuth antenna on a Navy Jammer pedestal. The control system is run using LabVIEW from the parallel port of a PC, through the interfaced drive electronics. The measurement system involves acquiring data signals from the synchros on the pedestal and capturing the resulting data in a GUI based interface with a North Atlantic Industries, 76CS1 PCI S/D data acquisition card.

Acknowledgements

I would like to thank my family for their continued support throughout my undergraduate degree at the University of Cape Town. I would also like to thank my friend and colleague Arjun Radhakrishnan for his support throughout this project period.

Finally, I would like to thank Professor Inggs from the University of Cape Town for having faith in me to embark on this project. His supervision and guidance throughout this project were invaluable to me.

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Nomenclature

Azimuth—Angle in a horizontal plane, relative to a fixed reference, usually north or the longitudinal reference axis of the aircraft or satellite.

Basic Input/Output System (BIOS)—The firmware code run by a personal computer when powered on. The BIOS identifies and initiates component hardware to prepare the computer for software control.

Digital to Analogue Converter (DAC)—Electronic circuitry that converts a digital output (logic high or logic low) to and analogue representation.

Elevation—Angle in the vertical plane, relative to a fixed reference, usually the horizontal reference axis of the aircraft or satellite.

Graphical User Interface (GUI)—A user interface that allows the user to communicate with the computer through the use of icons and visual indicators.

National Instruments LabVIEW—A graphical development environment that helps create flexible and scalable deign, control and test applications.

Pedestal—The structure that supports the antenna.

Peripheral Component Interconnect (PCI)—A computer bus for attaching peripheral devices to a computer motherboard.

Pulse Width Modulation (PWM)—The modulation of the duty cycle of a signal or power source to control the amount of power sent to the load.

Rotor—The rotating armature of a motor.

Stator—The stationary part of a motor or generator in or around which the rotor revolves.

Virtual Instrument (VI)—A LabVIEW GUI based instrument that controls hardware connected to the computer.

Visual Basic (VB)—An event driven programming language and associated development environment from Microsoft. Visual Basic enables the rapid application development of GUI applications [18].

Chapter 1

Introduction

1.1 Subject of this report

This project describes the electrical engineering principles used in designing, testing and implementing a control and measurement system used on an antenna. Specifically, an elevation over azimuth position controller on a Navy EW Jammer Pedestal as shown in Figure 1.1:

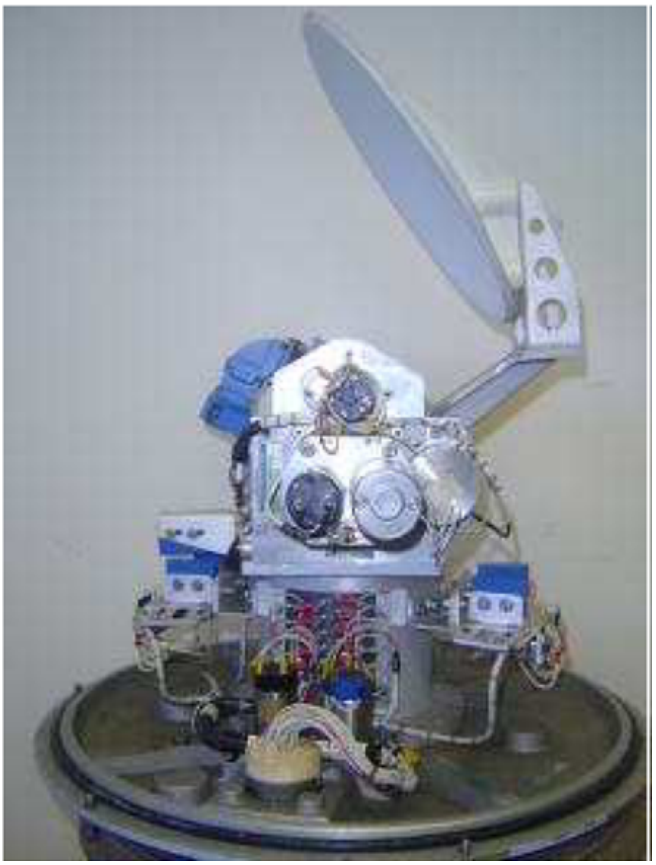

Figure 1.1: A Navy EW Jammer Pedestal

1.2 Background and Justification to Study

The Department of Electrical Engineering at the University of Cape Town has a Navy Electronic Warfare jammer pedestal for research and experimentation purposes. The pedestal uses an elevation over azimuth position configuration and uses a 28V DC supply to drive two motors of the antenna in both the vertical (elevation) and horizontal (azimuthal) axis. The pedestal has been out of commission for many years and this study proposes to investigate and refurbish the system to a working condition where the user can control and measure the antenna attributes through a computer based interface.

1.3 Project Requirements

The requirements of this project were presented as follows:

- To familiarize myself with National Instrument's LabVIEW graphical programming language.
- To write a program to control the parallel port of a standard computer using LabVIEW.
- Investigate the antenna and determine the steps required to refurbish the system to a working condition.
- Commission a 28V split power supply to drive the motors of the antenna.
- Research, design and build drive electronics to drive the motors of the antenna at different speeds from the parallel port, using LabVIEW.
- Install and configure a North Atlantic Instrument's 76CS1 PCI Synchro/resolver-to-digital (S/D) data acquisition card on a computer.
- Commission a 78 pin male, D-type connector to interface the 76CS1 with the antenna's synchros.
- Interface the 76CS1 with the synchros on the pedestal to acquire speed and angle measurements of the antenna.

1.4 Objectives of this report

The objectives of this project are three-fold. To investigate the electro-mechanical setup of the antenna and subsequently design, test and implement the drive electronics to control the antenna; to interface the S/D card with a computer and to create a graphical user interface to show the antenna attributes.

1.4.1 Methodology

In order to meet the project requirements, the following steps were taken:

- Understand the electro-mechanical components of the elevation over azimuth position controller.
- Refurbish the system to a working state
- Design a control system for the drive electronics.
- Drive the motor control system using the parallel port of a standard PC, using LabVIEW.
- Interface the antenna with a North Atlantic Industries 76CS1 S/D card together with LabVIEW, to create a simple GUI to show the attributes of the antenna (angle, speed and velocity).
- Finally to integrate the drive electronics with the S/D card GUI to control and measure the antenna attributes.

1.4.2 Deliverables

The final deliverables for the project were:

- The software used to control the bits of the parallel port.
- The hardware of the drive electronics used to control the antenna via parallel port.
- A simple GUI to display the antenna attributes once interfaced with the S/D card.
- This report entailing the background and theory behind the control and measurement system; and the related issues in designing, testing and implementing this complete system.

1.4.3 Testing

The antenna is to be controlled along the elevation and azimuth axes at different speeds, with the resulting attributes measured. The hardware and software that is designed and implemented to do this will be tested and the results obtained will be compared with those acquired from theoretical calculations.

1.5 Scope and Limitations

This project pursues the design and implementation problem in the fields of electro-mechanics and software. This project is to be undertaken over a period of twelve weeks, the pedestal itself has been out of service for many years and refurbishing it to a full working condition is presented as the major limitation.

1.6 Report Outline

An outline of the rest of the report is detailed as follows:

1.6.1 Chapter Two

Chapter two of this report discusses the background, theory and references used in completing the project. Many electrical engineering concepts were used in the design of the necessary hardware. These concepts, as well as the software used to interface the system are described here.

The background of the following key components of the project are discussed in detail in this chapter, each element described forms a core part of the entire system to be designed and implemented:

The Elevation over Azimuth Antenna Position Controller The Navy EW Jammer pedestal uses an elevation over azimuth position controller. The hardware incorporated in the position controller, which ultimately needs to be controlled is discussed.

Synchros Synchros form the heart of the measurement system in the application of this project. An overview of synchro theory is discussed, as well as how the synchro is used for velocity and angle measurement.

S/D conversion The synchros output an analogue voltage. It is the function of the Synchro/Resolver-to-Digital card to convert these analogue voltages into the corresponding angle and velocity measurements. A North Atlantic Industries 76CS1 data acquisition card was used for the S/D conversion.

LabVIEW LabVIEW is the software that was used to interface the computer with the pedestal. LabVIEW allows for easy interfacing and control because of the fundamental concept behind which it has been developed, that is, graphical programming.

The Parallel Port The parallel port was used to interface the computer with the pedestal. The bits of the parallel port are to be controlled using LabVIEW.

Once the background of the elements of the system have been presented, the electrical engineering concepts used to design and implement the final control and measurement system are then described. These concepts include:

The Power Supply The pedestal requires a $\pm$28V split power supply to operate. The theory behind the design of such a power supply is discussed.

Digital-to-Analogue Conversion In order to use the parallel port to interface the computer with the pedestal, a DAC needs to be implemented. The DAC will convert the logic signals output from the parallel port to analogue voltages that can tell the antenna what to do.

Drive Speed Control The axes of the pedestal are to be controlled at varying speeds. The electrical engineering concepts available to control the voltage applied across the motor terminals are listed and evaluated.

Safety Limits The elevation axis of the pedestal needs to have safety limits to prevent uncontrolled motion of the motor. The theory behind such a limit switch is described.

Data acquisition Once the antenna axes are moving as required, the motion needs to be measured in terms of angle and speed. The theory behind data acquisition on the 76CS1 S/D card is explained.

A clear understanding of the core components of the system is now gained. This background and theory presented gives us a basis of the system that ultimately needs to be designed, as discussed in Chapter three.

1.6.2 Chapter Three

Chapter three focuses on the design of the hardware and software required to control the antenna. The following hardware and software were designed with the theory and references of chapter two to fulfill the requirements of the project:

The Power Supply Unit The design of a $\pm$28V power supply unit (PSU) involved the commissioning of a full bridge rectifier, a centre tapped transformer and positive and negative rail voltage regulators. The PSU would be dedicated to the pedestal, running of 230V mains.

Software to control the parallel port through LabVIEW The "Parallel port read and write loop" Virtual Instrument was used to control the bits of the parallel port. The TTL output from the ports were inputs to the DAC.

Digital-to-Analogue Conversion A 3-bit DAC, with a gain stage amplifier was designed to translate the parallel port logic outputs into analogue voltages that would control the motion of the axes of the antenna.

Pulse Width Modulation A PWM based scheme was chosen to vary the voltage applied across the motor terminals. The PWM generator design was based on an operational amplifier model. The duty cycles of the output waveform could be varied from 0% to 90% using this design.

Safety Limit Switches The design of the safety limit switches involved circuitry that would prevent current flowing to the motor on the elevation axis once a limit had been reached. The motor would stay idle until a reverse polarity voltage was applied across it to drive it out of limit.

GUI for Synchro Measurement The 76CS1 VB S/D GUI was used to acquire the velocity and angle attributes of the antenna during motion.

All eight bits of the parallel port were used in the design. A block diagram of the final system to be designed is presented.

The design for the system as required is now complete. All the design specifications stated in Chapter three serve as a basis for the building and testing of the hardware and software as described in Chapter four.

1.6.3 Chapter Four

Chapter four discusses the building and testing of the hardware and software concepts as decided in chapter three. The hardware and software is tested, and the results from the associated tests are presented. The compromises made in translating the theoretical designs into viable practical circuits are discussed. Limitations encountered during testing are discussed and the resulting final system to be designed is presented.

Major limitations encountered included the failure of the motor on the elevation axis and the commissioning of a 78 pin D-type male connector to interface the S/D card with the synchros. As a result, the final system design did not incorporate the elevation axis.

Only four bits of the parallel port were now used to control the system. A block diagram of the final system designed is presented.

Table 1.1 shows the final antenna speed control measurements tabulated from testing the various user inputs from LabVIEW:

Speed	LabVIEW - DAC Input Binary State	Antenna Speed (RPM) - Azimuth
Off	000	0
Slow	001	10
Fast	111	23

Table 1.1: Final Antenna Speed Control-LabVIEW User Input and Corresponding Speed

The results obtained from testing of the system described in Chapter four leads to conclusions and further recommendations for this study, as discussed in Chapter five.

1.6.4 Chapter Five

Chapter five discusses the conclusions that are drawn based on the results of the testing of the final system as described in chapter four. The final system is discussed with respect to the initial project requirements. At the end of the twelve week period allocated to this project, the system designed is open for further research and experimentation. Recommendations as to how the elements of this project could be used as a basis for continued research and experimentation are made.

Table 1.2 shows the status in the phases of research, design and implementation reached at the end of the project period:

Project Phase	Task	Status
Research	System to be Implemented	Complete
Research	Background to Hardware	Complete
Research	Background to Software	Complete
Design	$\pm$28V PSU	Complete
Design	Parallel Port Control - LabVIEW	Complete
Design	3-Bit DAC	Complete
Design	PWM Generation	Complete
Design	Data Acquisition from Synchros	Complete
Design	Limit Switches	In Progress
Implementation	$\pm$28V PSU	Complete - Alternative Method Used
Implementation	Parallel Port Control - LabVIEW	Complete
Implementation	3-Bit DAC	Complete
Implementation	PWM Generation	Complete
Implementation	Data Acquisition from Synchros	In Progress
Implementation	Limit Switches	Not Implemented

Table 1.2: Final Project Status

By comparing the final system presented to that of which was the original requirement of this project, it can be seen that the objectives have only been partially met. This is justified by the limitations of the project, stated in Chapter four.

As a continuation of this study, one could implement a system that uses this project as a basis to design a system that can be used for set-point tracking.

In this system, the user would specify coordinates in LabVIEW. The antenna would then move along the elevation and azimuth axes to this coordinate at a user defined speed.

Implementing this system would serve as a culmination of all the elements of the current project together with the new requirements to produce a useful set-point tracking system.

Chapter 2

Background and Theory

Chapter two of this report discusses the background, theory and references used in completing the project. Many electrical engineering concepts were used in the design of the necessary hardware. These concepts, as well as the software used to interface the system are described here.

The background of the following key components of the project are discussed in detail in this chapter, each element described forms a core part of the entire system to be designed and implemented:

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2.1 Background

The background of the hardware and software used in this project are discussed in detail.

2.1.1 Elevation over Azimuth Position Controller

Antennae have many different configurations. The two axis, elevation over azimuth configuration has however been the standard architecture for many decades. In this configuration, the elevation axis is closer to the antenna than the azimuth axis, hence the name: elevation over azimuth. This design is ideally suited to many target tracking applications because a two-axis design has a minimum number of moving parts, and hence fewer modes of failure and minimal maintenance concerns[5, page 1]. A typical example of an elevation over azimuth tracking antenna is shown in Figure 2.1:

Figure 2.1: A Typical Elevation over Azimuth Tracking Antenna [5]

The elevation over azimuth configuration does however have its limitations; namely, the situation whereby the target being tracked passes directly overhead (90 degree Zenith pass). To address this limitation, several pedestal architectures have been investigated and designed, some of these include:

- Elevation over Azimuth over Tilt
- Elevation over Azimuth over Train
- Cross Elevation over Elevation over Azimuth

The discussion of these pedestal design configurations is beyond the scope of this project and will not be discussed any further.

The pedestal concerned with this report incorporates the elevation over azimuth configuration. The two axes are driven by separate motors running off a 28 volt split direct current (DC) supply.

The azimuth axis allows for a full 360^orotation of the antenna. The elevation traverses through $90^o$and has its mechanical vertical limits at $0^o$and 90^o.

2.1.2 Direct Current Brushed Motors

The pedestal is moved by two identical direct current (DC) brushed motors that operate across a voltage range of -28 V to 28 V. The motors (Vactric 15P203) have a maximum current rating of 0.95 Amps. The rated maximum speed is 5000 revolutions per minute (RPM) with a torque of 220 grams per centimeter [1].

2.1.3 Brake

The Elevation axis has a brake to prevent uncontrolled motion of the system after reaching its vertical limits. The brake is disengaged at voltages greater than 24V. The braking system was not implemented in the pedestal for the purposes of this project.

2.1.4 Synchros

A Synchro is in essence an instrument that can be connected in various ways to form shaft angle measurement and positioning systems. All synchros work on the principle of a rotating transformer. Synchros have been widely available for about 40 years as part of electromechanical servo and shaft angle positioning systems.

Synchros are cylindrical objects that resemble small AC motors with varying diameter. Synchros are classified according to their sizes. Thus, a synchro with an outer diameter of 1.051 inches would be referred to as a size 11 while a synchro with an outside diameter of 2.270 inches would be a size 23.

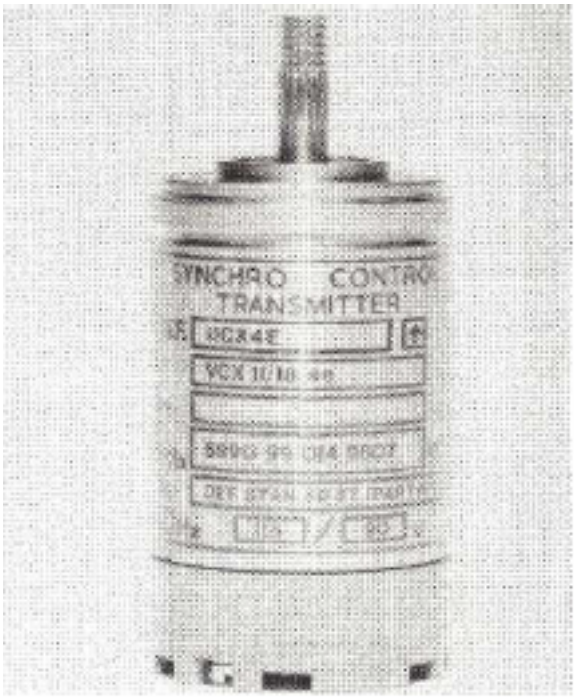

Figure 2.2: A Size 11 Synchro [2]

The Synchro can form the heart of a digital shaft angle measurement and positioning system, which in terms of reliability and cost effectiveness is unsurpassed by any other method [3].

Synchros can be divided into two types, Torque and Control Synchros.

Torque Synchros are are required when it is necessary to transmit angular information from the shaft of a synchro to the shaft of another without the need for any form of servo system. The synchros themselves handle the necessary power requirements. Torque Synchros are beyond the scope of this project and will not be discussed any further, more information on them can be found in North Atlantic Industries Synchro Conversion Handbook [2].

Synchro Control Transformers

A synchro control transformer (CT) is an angular transducer. CTs are rotating transformers that output an analogue voltage respective of the input shaft angle. A CT consists of a rotor with one winding which revolves around a stator with 3 windings in wye format, 120 degrees apart . The internal structure of a CT is shown in Figure 2.3

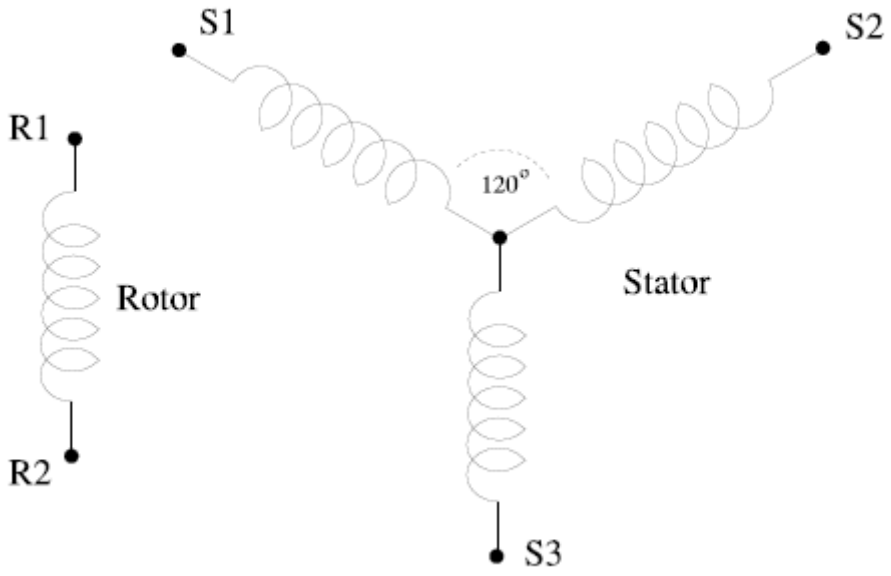

Figure 2.3: The internal structure of a Synchro Control Transformer [1]

A CT accepts input voltage across the stator terminals (synchro format voltages) as described as follows [1, 2, 3, 4]:

$$\text{S1 to S3} = \text{A sin } \omega \text{ t sin } \phi$$

$$\text{S3 to S2} = \text{A sin } \omega \text{ t sin } (\phi + 120^o)$$

$$\text{S2 to S1} = \text{A sin } \omega \text{ t sin } (\phi + 240^o)$$

where ϕ is the synchro shaft angle.

The rotor windings will then only produce a voltage across their terminals if the shaft input on the CT is not at angle ϕ. This output voltage is an error signal which can be fed into a phase sensitive detector and an error amplifier to produce a signal that will drive a motor to the correct position, and thus provide a servo control system.

Position Resolver Transmitters

The position resolver transmitter (TX) is a form of synchro (resolvers are often referred to as synchro resolvers) in which the windings on the stator and rotor are displaced mechanically at 90^o to each other instead of 120^o as in the case of synchros. The resolver therefore exploits the sinusoidal relationship between the shaft angle and the output voltage. In outward appearance, resolvers are very similar to synchros and are produced in the standard synchro frame diameters. Internally, resolvers come in many forms with a wide variety of winding configurations and transformation ratios. The simplest resolver

would have a rotor with a single winding and a stator with 2 windings at 90^o to each other. The internal structure of a TX with two rotor windings and two stator windings at $90^o$to each other is shown in Figure 2.4

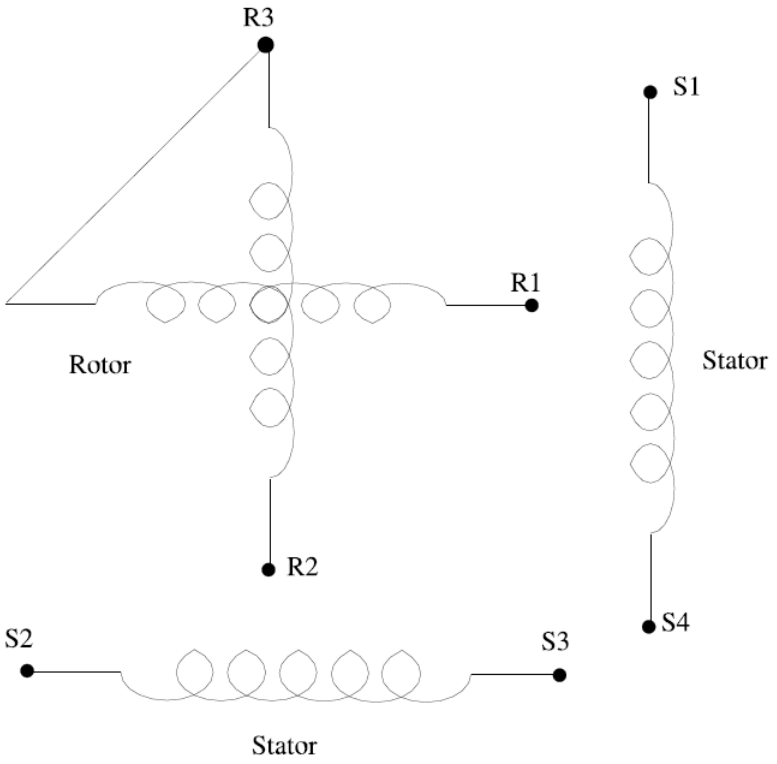

Figure 2.4: Internal Structure of a Position Resolver Transmitter [2]

The shaft angle can be calculated using a TX using two methods [1] :

1. Excitation of the rotor windings

   If an alternating current is introduced across one of the rotor windings, a voltage is induced in the stator windings. Since the stator windings are at right angles to each other, the amplitudes of the voltages induced are related by the sine of cosine of the shaft angle [1, 2]. So if the rotor is excited by the AC reference voltage:

   $$A\sin\omega t$$

   Then the voltage appearing on the stator terminals would be:

   $$\text{S1 to S3} = V\sin\omega t\sin\theta \text{ and}$$

   $$\text{S4 to S2} = V\sin\omega t\cos\theta$$

   where θ is the Resolver shaft angle

2. Excitation of the stator windings

   If the two stator windings are excited with two signals in phase quadrature to one another, the voltage on the rotor winding will have a fixed amplitude and frequency, but will have a phase that varies according to shaft angle θ

$$V_{S1-S3}=V_R \sin \omega t$$

$$V_{S2-S4}=V_R \sin \omega t + 90^o = V_R \cos \omega t$$

   The voltage induced across the rotor winding will now be:

$$V_{R1-R2}=V_R \sin \omega t + \theta$$

   As the phase of the signal across the rotor winding changes from 0^o to 360^orelative to the reference signal, it can be measured to determine the shaft angle as shown in Figure 2.5. [1]

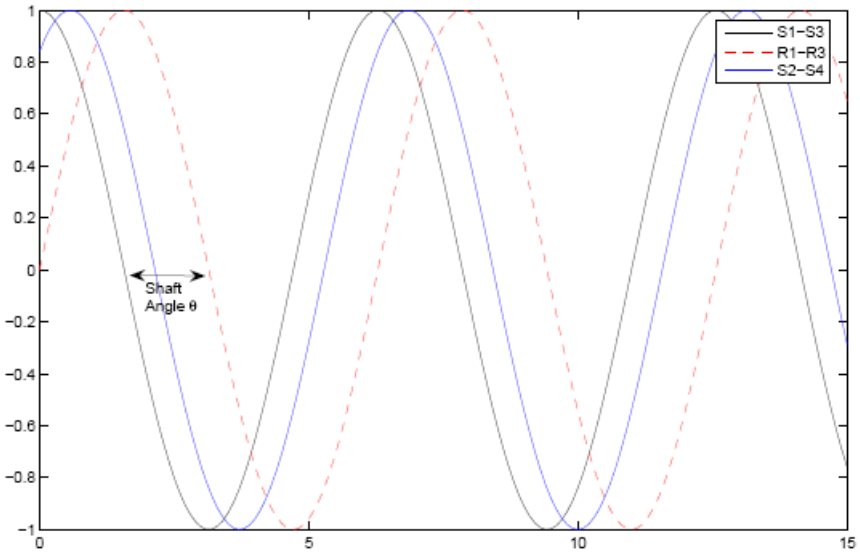

Figure 2.5: Signals on Position resolver with Stator Excitation [1]

2.1.5 The Synchro/Resolver-to-Digital Card

The University of Cape Town has a Synchro/Resolver-to-Digital (S/D) PCI card, a North Atlantic Industries PCI-76CS1 [7] as shown inf Figure 2.6. The card is in essence a data acquisition card that reads and analogue voltage from synchros or resolvers and converts it to a digital signal representing the angle and velocity measurement of the synchro/resolver (S/D function). The card also has the ability to do Digital-to-Synchro/Resolver operations whereby it writes out to the synchro/resolver (D/S function).

Figure 2.6: The North Atlantic Industries 76CS1 PCI card [7]

The 76CS1 has 8 channels for S/D conversion, and 6 channels for D/S conversion. It interfaces its inputs and outputs through a 78 pin female d-type connector.

Key features of the 76CS1 include:

- 16 bit resolution
- Power-On-Self-Test (POST)
- Self-calibrating S/D channels
- Support for 3.3V or 5V PCI bus
- Accurate digital velocity outputs
- Latch feature (read all channels simultaneously)

For a full review of all the features of the 76CS1, please refer to Appendix A.

The 76CS1 comes packaged with a Microsoft Windows support kit, as well as support for Linux distributions. This project involved measuring and simulating the synchros/resolvers in a Windows environment, as a result, the 76SC1 Linux support drivers and utilities are not discussed. The Windows support kit comes with a Visual Basic (VB) based graphical user interface (GUI) that provides a user friendly interface for measurement or simulation. Figure 2.7 shows the VB GUI for synchro/resolver measurement (S/D).

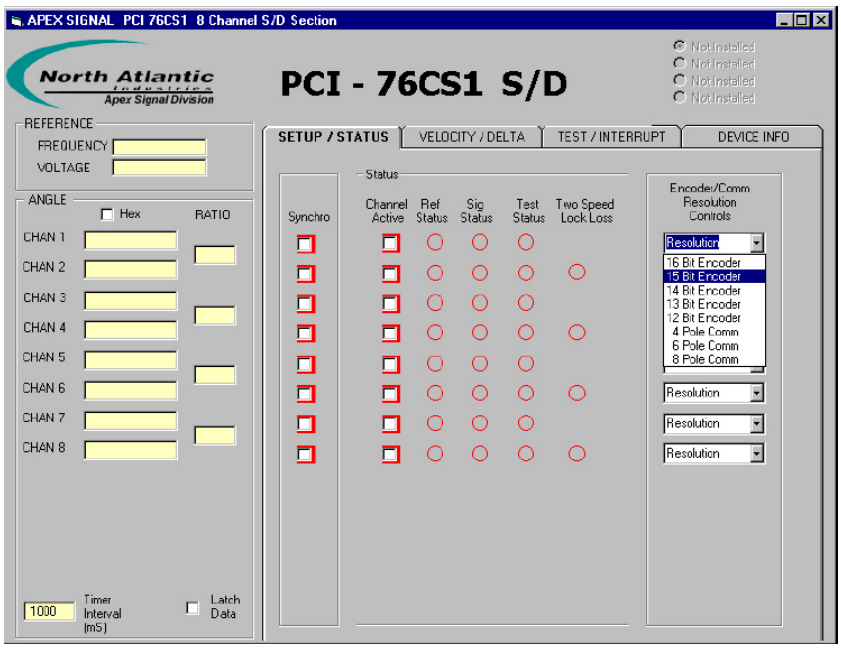

Figure 2.7: GUI for Synchro/Resolver Measurement [8]

The corresponding VB GUI for Synchro/Resolver simulation (D/S) is shown in Figure 2.8:

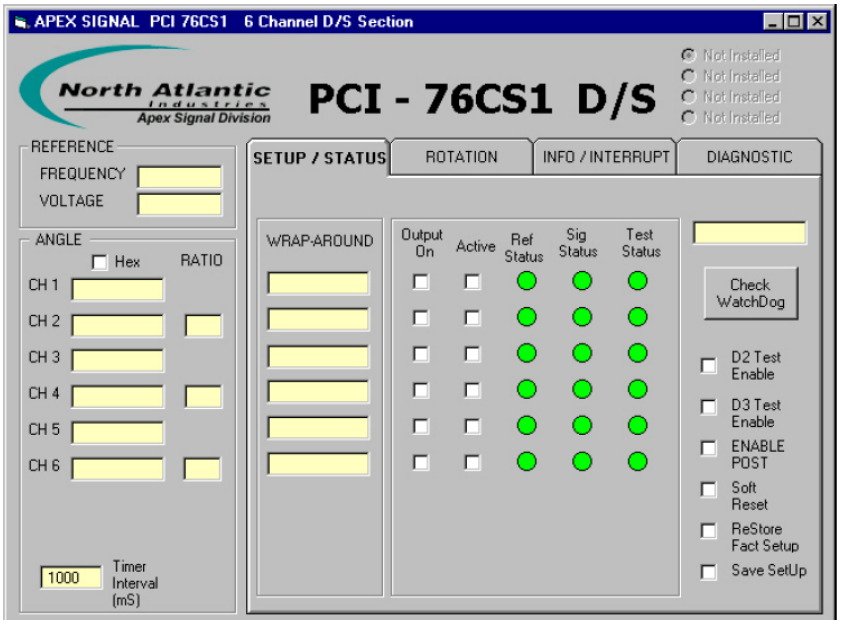

Figure 2.8: GUI for Synchro/Resolver Simulation [8]

The 76SC1 comes with support for National Instrument's LabVIEW graphical programming language (discussed in detail in section 2.1.6). The dynamic link library (dll) file of the 76CS1 (file-name: as_PCI76cs1.dll) can be examined by LabVIEW and the specific functions of the 76SC1 can be called (eg: getAngle, setLatch, getVelocity).

2.1.6 LabVIEW

In order to interface the parallel port of the computer with the drive control hardware, and ultimately, the antenna, National Instruments LabVIEW was used. LabVIEW is an acronym for: Laboratory Virtual Instrumentation Engineering Workbench.

LabVIEW is based on a graphical development environment that helps create flexible and scalable deign, control and test applications. Its applicability lies in the fact that it is a data acquisition and instrument control utility that uses graphical programming.

LabVIEW makes use of 'Virtual Instruments' or 'VIs' in which the user can create on a block diagram level; data acquisition, testing, control and measurement, analysis and output tools for both real-time and non real-time applications. LabVIEW was originally released for Apple Macintosh in 1986, after much development, National Instruments have released their latest version, version 8.5 in August 2007 with support for Unix, Linux, Mac OS and Microsoft Windows [19]. For this project, I worked with LabVIEW version 7.21 on a Microsoft Windows XP based platform.

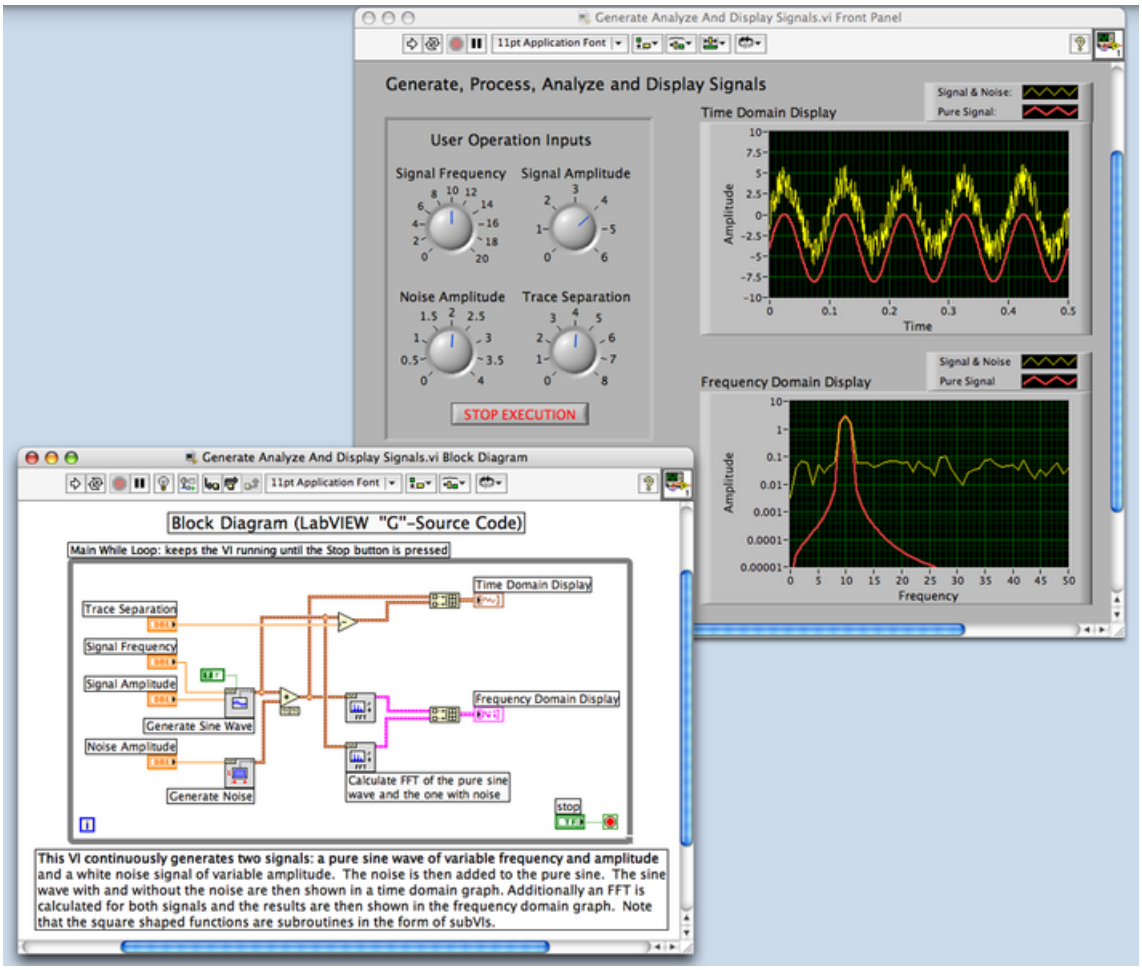

Figure 2.9: LabVIEW example showing Front Panel and Block Diagram [9]

The advantage of using graphical programming as in LabVIEW, is that it avoids the user having to go into the programming aspect of the required action. Users can place graphical representations of hardware by examining their respective hardware drivers or dynamic

link libraries (dll's). Each VI has two components: a block diagram and a front panel as shown in Figure 2.9. The front panel can be run either as a program, prompting the user for input, or as a function if it is implemented on another block diagram.

LabVIEW comes installed with many examples and on-line help is readily available with LabVIEW support groups such as LAVA – LabVIEW Advanced Virtual Architects [9].

2.1.7 The PC Parallel Port

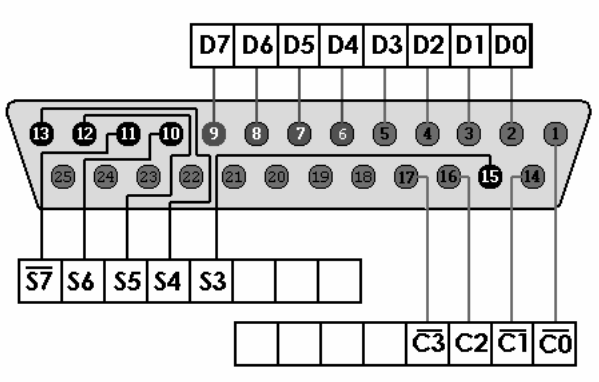

Figure 2.10: Parallel Port Pin Connections [10]

The bits of the parallel port of a standard PC are to be used to control the antenna. The parallel port has 25 lines, however only eight of these lines are available to the user. These eight lines are called the data bits, the other pins are reserved status and control bits. The pin connections of the parallel port are shown in Figure 2.10, the pin attributes are shown in Table 2.1

There are three locations in the I/O port address space at which parallel ports can be configured on computers: 0x278, 0x378 and 0x3BC. The 0x3BC address space is traditionally used on monochrome displays or printer cards and is phased out. 0x278 and 0x378 are common on newer cards (usually marked LPT1 and LPT2).

In order to write bits to the parallel port, the correct printer port must be selected first. The hexadecimal address of the local computer's parallel port can be set in the BIOS.

There are 8 bits that are available for user input. These bits, marked as Data0 to Data7 (pin2-pin9) can be asserted to generate a logic high or low. The parallel port data pins are Transistor-Transistor-Logic (TTL) outputs and generate a typical logic high of 3V-5V DC and a logic low of 0V

Pin	Signal	Direction	Register Bit	Inverted?
1	nStrobe	Out	Control-0	Yes
2	Data0	In/Out	Data-0	No
3	Data1	In/Out	Data-1	No
4	Data2	In/Out	Data-2	No
5	Data3	In/Out	Data-3	No
6	Data4	In/Out	Data-4	No
7	Data5	In/Out	Data-5	No
8	Data6	In/Out	Data-6	No
9	Data7	In/Out	Data-7	No
10	nAck	In	Status-6	No
11	Busy	In	Status-7	Yes
12	Paper Out	In	Status-5	No
13	Select	In	Status-4	No
14	Linefeed	Out	Control-1	No
15	nError	In	Status-3	No
16	nInitialize	Out	Control-2	No
17	nSelect Printer	Out	Control-3	Yes
18-25	-	-	-	-

Table 2.1: Parallel Port Pin Attributes [10]

2.2 Theory

The electrical engineering theory used in the completion of this project is discussed in detail as follows.

2.2.1 Power Supply Unit

The two DC brushed Vactric 15P203 motors on the pedestal are controlled by a 28V split power supply. The power supply must therefore have output terminals at +28V, 0V(ground) and -28V to meet the motor's full speed (5000 rpm) and torque (220 g/cm) attributes.

2.2.2 Digital to Analogue Conversion

The output from the data pins of the parallel port of the PC will ultimately drive the antenna. These outputs as explained in section 2.1.7 are TTL outputs ranging from 3V-5V. This digital output must be converted to an analogue voltage in order to drive the antenna circuitry.

A simple R-2R ladder network will be used as the digital to analogue converter (DAC) [11]. A R-2R ladder network has the advantage that only two resistor values in a repeated cascade design are required in the circuit design. Figure 2.11 shows an N-bit DAC:

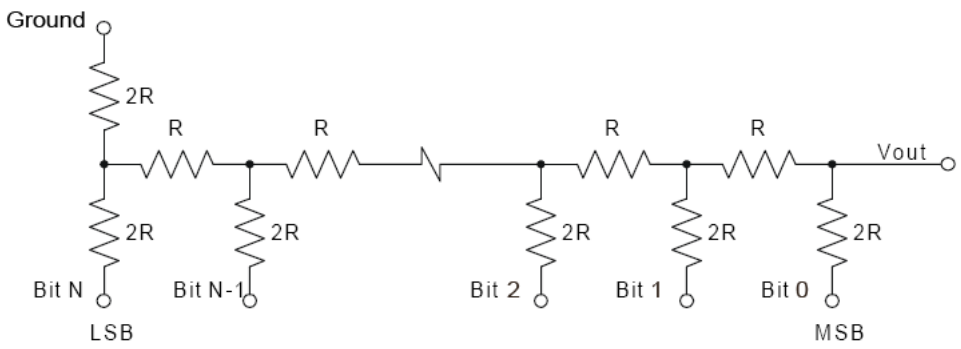

Figure 2.11: An N-bit DAC [11]

Digital information is presented to the ladder as individual bits of a digital word switched between a reference voltage (V_r) (3V-5V from parallel port) and ground.

Depending on the number and location of the bits switched to V_r or ground, Vout will vary between 0V and V_r. If all inputs are connected to ground, Vout = 0V. If all inputs are connected to V_r, the output voltage approaches V_r. If some inputs are connected to ground and some to V_r then an output voltage between 0V and V_r occurs. These inputs (bits) range from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). As the names indicate, the MSB, when activated, causes the greatest change in the output

voltage and the LSB, when activated, will cause the smallest change in the output voltage [11].

Since an R/2R ladder is a linear circuit, Vout can be calculated by applying the principle of superposition. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 0 and 2 are connected to V_r with all other inputs grounded, the output voltage is calculated by:

$$\text{Vout} = \frac{V_r}{2} + \frac{V_r}{8}$$

A general formula for calculating Vout for an N-bit DAC is given below:

$$\text{Vout} = \frac{Vr}{2^N}(S_{N-1}2^{N-1} + S_{N-2}2^{N-2} + \ldots + S_0 2^0)$$

Where the input S_N to bit N is '1' if it is connected to a voltage V_r and '0' if it is grounded. The R/2R ladder is a binary circuit. The effect of each successive bit approaching the LSB is 1/2 of the previous bit. If this sequence is extended to a ladder of infinite bits, the effect of the LSB on Vout approaches 0. Conversely, the full-scale output of the network (with all bits connected to Vr) approaches Vr [11].

2.2.3 Controlling Drive Speed

The drive speed is ultimately controlled by the torque changes induced by varying voltage levels across the the motors. In order to control the voltage applied across the motors for both elevation and azimuth, the following options were available:

- Varying the amplitude

  Whereby the amplitude of the input voltage is varied to control the torque generated across the motor.

- Varying the duty cycle

  By adjusting the duty cycle, the average output voltage would change, therefore varying torques would be applied across the motor of the antenna subsequently causing the respective axes to move at different speeds.

The chosen method for controlling the voltage across the motors was that of varying the duty cycle with a pulse width modulation (PWM) scheme. A PWM scheme would allow for simple interfacing with the DAC.

2.2.4 Data Acquisition from the 76CS1

The S/D card interfaces with the synchros/resolvers through a 78 pin D-type female configuration. There are two available configurations available to read and write to the S/D and D/S channels:

1. 8 S/D Channels with up to 4 D/S Channels

2. 6 D/S Channels with up to 4 S/D Channels

For the purposes of this project, Configuration 1 was adopted. The pin connections for Configuration 1 are shown in Table 2.2 :

S/D Channels

Pin	Ch.1 S/D	Pin	Ch.2 S/D	Pin	Ch.3 S/D	Pin	Ch.4 S/D
39	S1	18	S1	36	S1	15	S1
58	S2	76	S2	55	S2	73	S2
78	S3	57	S3	75	S3	54	S3
19	S4	37	S4	16	S4	34	S4
38	RHi	17	RHi	35	RHi	14	RHi
77	RLo	56	RLo	74	RLo	53	RLo
Pin	Ch.5 S/D	Pin	Ch.6 S/D	Pin	Ch.7 S/D	Pin	Ch.8 S/D
33	S1	12	S1	30	S1	9	S1
52	S2	70	S2	49	S2	67	S2
72	S3	51	S3	69	S3	48	S3
13	S4	31	S4	10	S4	28	S4
32	RHi	11	RHi	29	RHi	8	RHi
71	RLo	50	RLo	68	RLo	47	RLo

D/S Channels

Pin	Ch.1 D/S	Pin	Ch.2 D/S	Pin	Ch.3 D/S	Pin	Ch.4 D/S
27	S1	6	S1	24	S1	3	S1
46	S2	64	S2	43	S2	61	S2
66	S3	45	S3	63	S3	42	S3
7	S4	25	S4	4	S4	22	S4
26	RHi	5	RHi	23	RHi	2	RHi
65	RLo	44	RLo	62	RLo	41	RLo

Table 2.2: Pin connections for 76CS1 in Configuration 1: 8 S/D, 4D/S Channels [7]

With reference to Table 2.2, S1, S2, S3, S4 represent the stator connectors and RHi and RLo represent the rotor connectors on the synchros.

2.2.5 Limit Switches

The elevation axis of the elevation over azimuth antenna requires limit switches to prevent the motors from being continuously run after the antenna has reached its vertical limits defined in section 2.1.1. These protective interlocks limit the antenna movements to a safe working space. These limit switches must be designed in such a way that the current flow to the motor is stopped in the event of reaching the respective limit. The motor must then be able to drive the elevation axis in the opposite direction, out of limit, if the polarity of the supply is inverted.

A clear understanding of the core components of the system is now gained. The background and theory presented here in Chapter two gives us a basis of the system that ultimately needs to be designed, as discussed in Chapter three.

Chapter 3

Design

Chapter three focuses on the design of the hardware and software required to control the antenna. The following hardware and software were designed with the theory and references of chapter two to fulfill the requirements of the project:

- The power supply unit
- The software to control the parallel port through LabVIEW
- The digital to analogue converter
- The pulse width modulation generating circuitry
- The safety limit switches for motion along the elevation axis motion
- The graphical user interface to measure the angle and speed attributes of the synchros

A block diagram of the entire system to be designed is shown in Figure 3.1.

The system is controlled by the bits of the parallel port. All eight bits available to the user are used as shown in Table 3.1:

Bit	Function
2 (Data-0)	Direction
3 (Data-1)	Elevation
4 (Data-2)	Azimuth
5 (Data-3)	Speed
6 (Data-4)	Speed
7 (Data-5)	Speed
8 (Data-6)	Top Limit (Elevation)
9 (Data-7)	Bottom Limit (Elevation)

Table 3.1: Parallel Port Bit Usage

The specific component and part list for the hardware to be designed for the completion of the design is available in Appendix B.

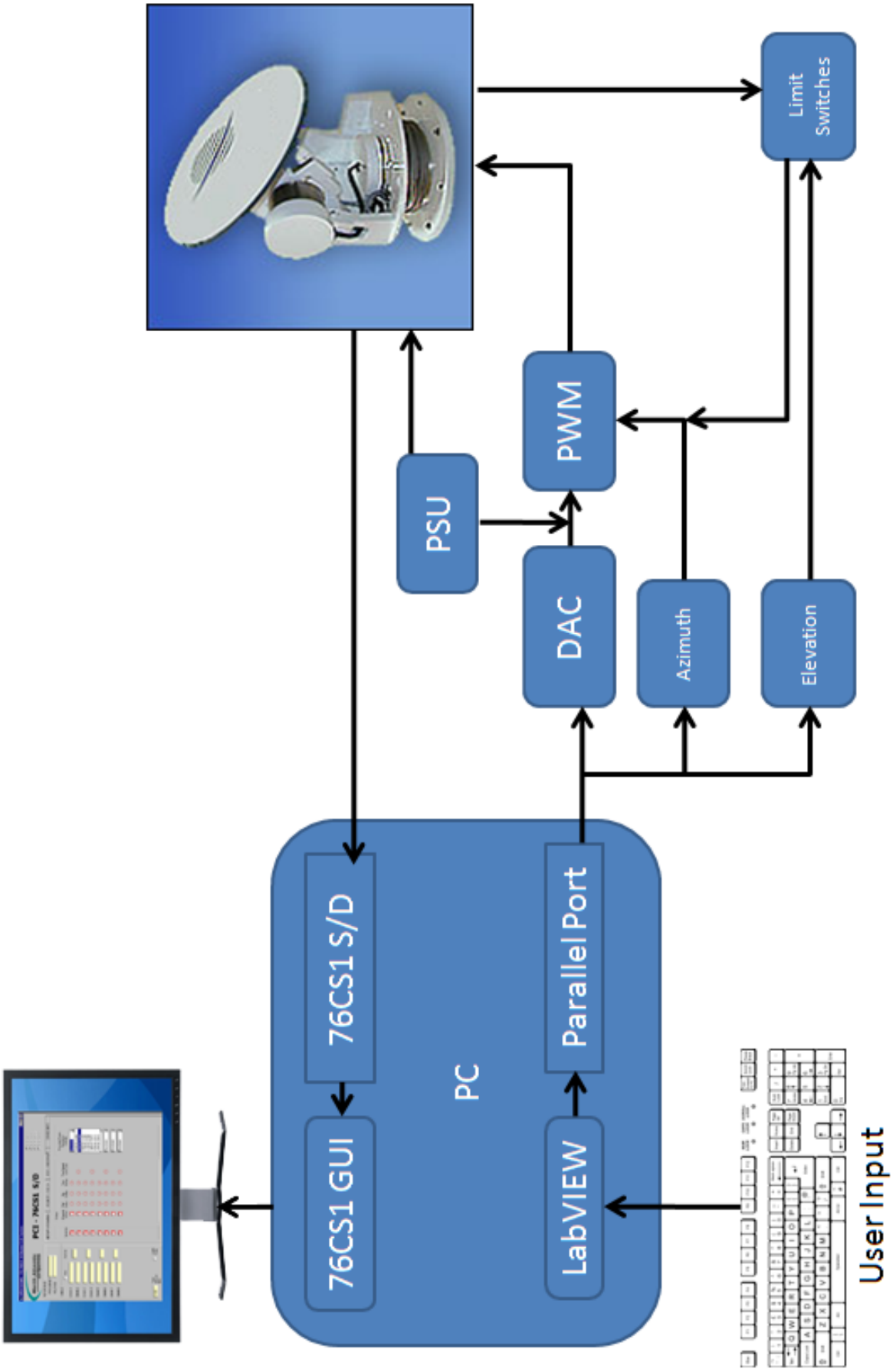

Figure 3.1: Block Diagram of Control and Measurement System to be Designed

3.1 The Power Supply Unit

The commissioning of a 28V split power supply unit (PSU) involved the commissioning of the following key components [6] :

- A 60V/1A centre tapped transformer
- Two 10000μF smoothing capacitors
- A LM317 three terminal voltage regulator (+28V)
- A LM337 three terminal voltage regulator (-28V)
- Two 1N4001 diodes (100V/1A minimum rating)

A block diagram for the PSU is shown in Figure 3.2:

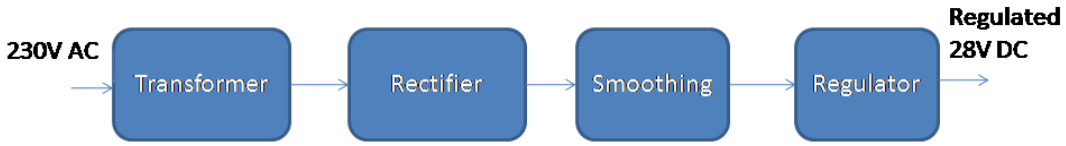

Figure 3.2: Block Diagram for PSU [6]

The complete circuit diagram of the power supply is shown in Figure 3.3:

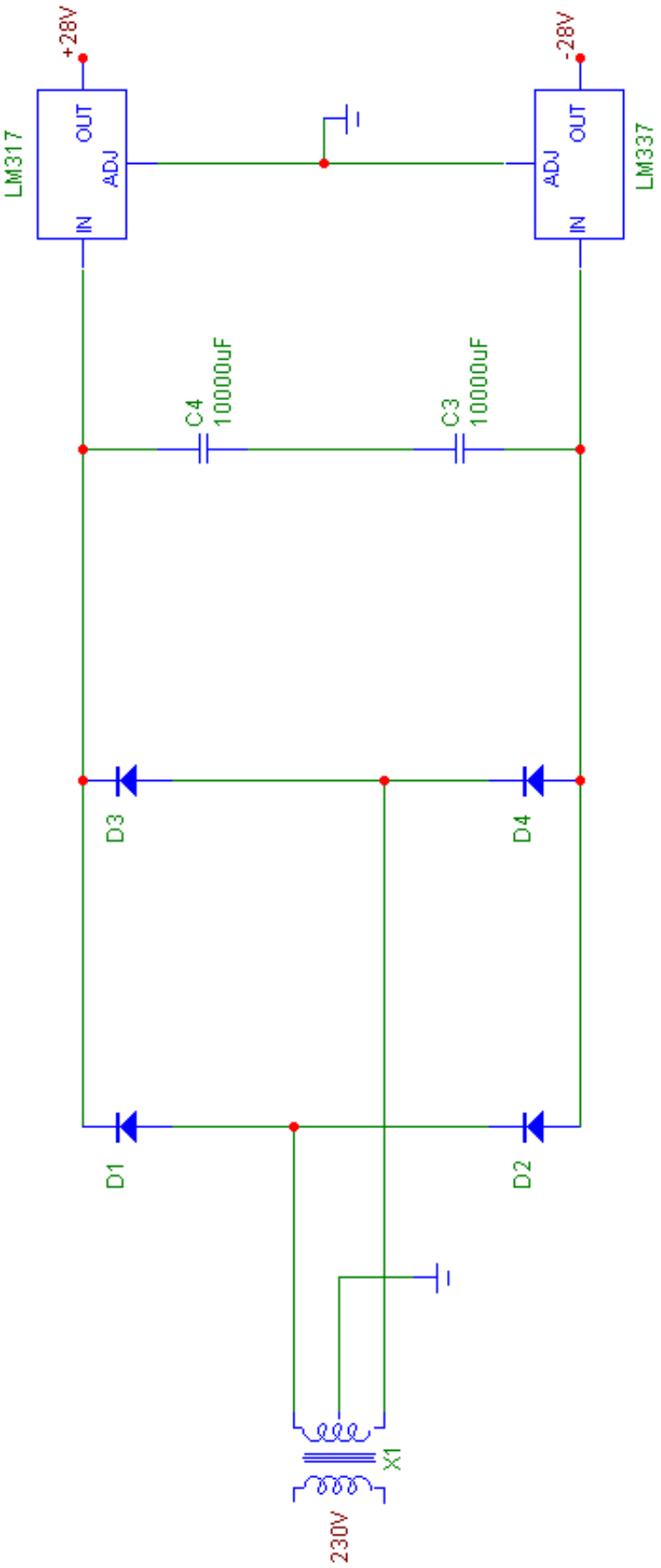

Figure 3.3: A 28V split power supply [6]

3.2 Controlling the parallel port from LabVIEW

There is an existing LabVIEW virtual instrument (VI) called the 'parallel port read and write loop'. In order to control the parallel port, the port status must be set to the Standard Parallel Port (SPP) mode. The other modes, Enhanced Parallel Port (EPP) and Extended Capabilities Mode (ECP) are not compatible with this VI. The parallel port mode can be set in the computer's basic input/output system (BIOS).

Once the base address of the local computer is determined, it can be entered into the VI input. For my test cases, the parallel port was always configured to the hexadecimal address 0x378.

Bits can be written out to the data pins of the parallel port (pins 2-9) and the subsequent read-in is also displayed. The VI allows you to change the logic status of any of the pins that have write access.

The following example shown in Figure 3.4 creates a logic high output on pin 2(Data-0) only:

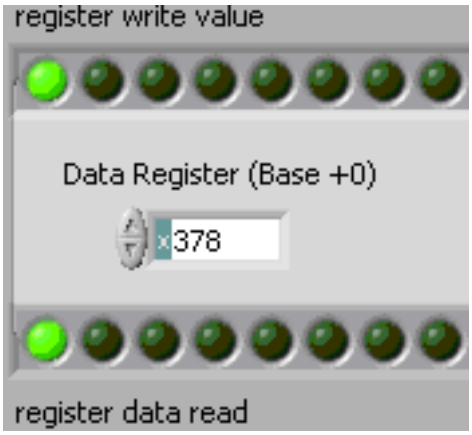

Figure 3.4: Asserting Data-0 high

The actual parallel port I/O connector status for the above example is shown in Figure 3.5. Note, in controlling the parallel port bits, we are only interested in the logic states of pin2-pin9. The logic states of the other pins are irrelevant for the purpose of this application.

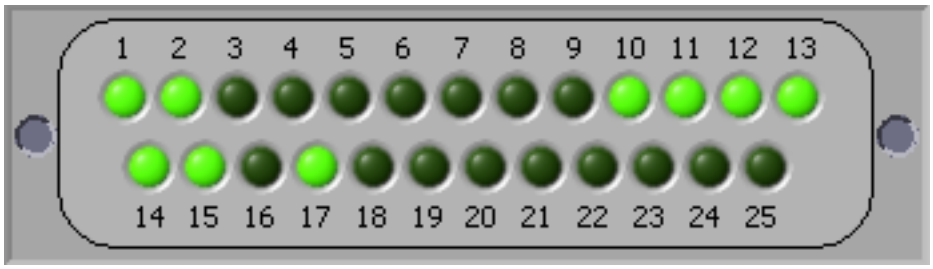

Figure 3.5: Parallel port pin status with Data-0 high

If instead, a data output is only written to pin 6 (Data-4), the necessary user input required is shown in Figure 3.6.

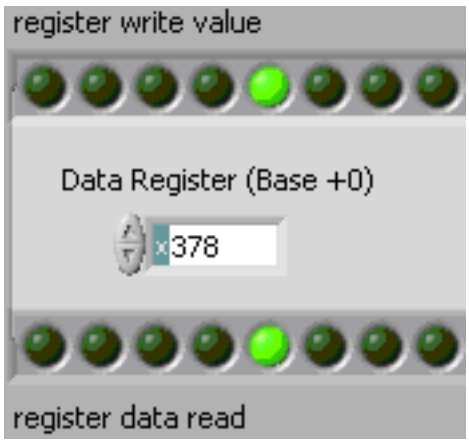

Figure 3.6: Asserting Data-4 high

The resulting parallel port pin status is shown in Figure3.7:

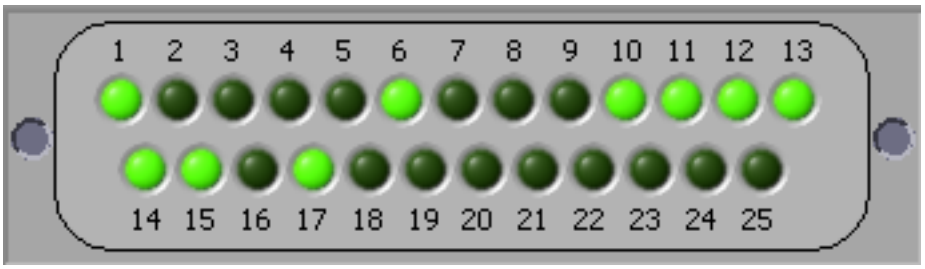

Figure 3.7: Parallel port pin status with Data-4 high

3.3 A 3-Bit Digital to Analogue Converter

The 3-bit Digital to Analogue Converter (DAC) was designed using a simple R-2R ladder network as shown in Figure 3.8 [11]. A gain amplifier was added to ensure that a logic high TTL output triggered from the parallel port is indeed detected and asserted on the subsequent drive speed control circuitry operating at $\pm$28V.

The resistor values chosen in the R-2R ladder network were arbitrary and chosen as 1MΩ and 2.2MΩ respectively.

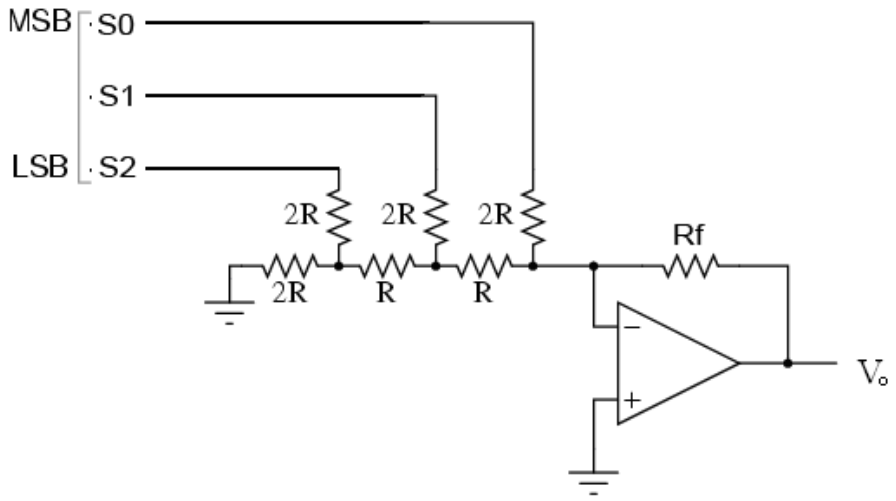

Figure 3.8: An R-2R ladder DAC with gain

The output voltage generated from this circuit is given by:

$$V_o = -\frac{R_f}{R}.V_r(S_2 2^2 + S_1 2^1 + S_0 2^0)$$

Where the input S_N to bit N is '1' if it is connected to a voltage V_r and '0' if it is grounded.

3.4 Drive Speed Control

A pulse width modulation (PWM) scheme was used to vary the voltage applied across the motors. In PWM, the power supply to the motor is switched on and off rapidly. The DC voltage is converted to a square-wave signal that alternates between 0V and the supply voltage. By adjusting the duty cycle of the signal, the average power can be varied and subsequently, the motor speed. An example of the varying duty cycles in a PWM scheme is shown in Figure 3.9 :

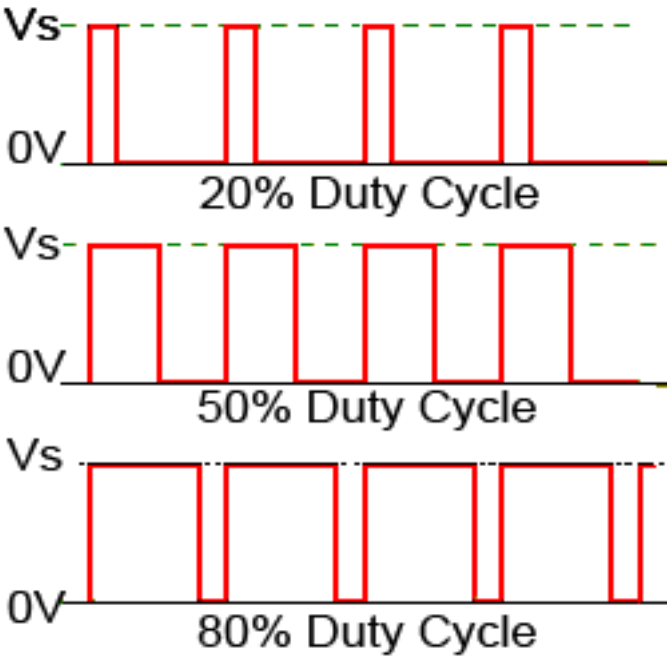

Figure 3.9: Varying duty cycles in a PWM scheme

The PWM waveform was created using an operational amplifier (op-amp) circuit. A quad op-amp integrated circuit (IC), an LM324 was used. The schematic for the PWM circuit is shown in Figure 3.10[12]:

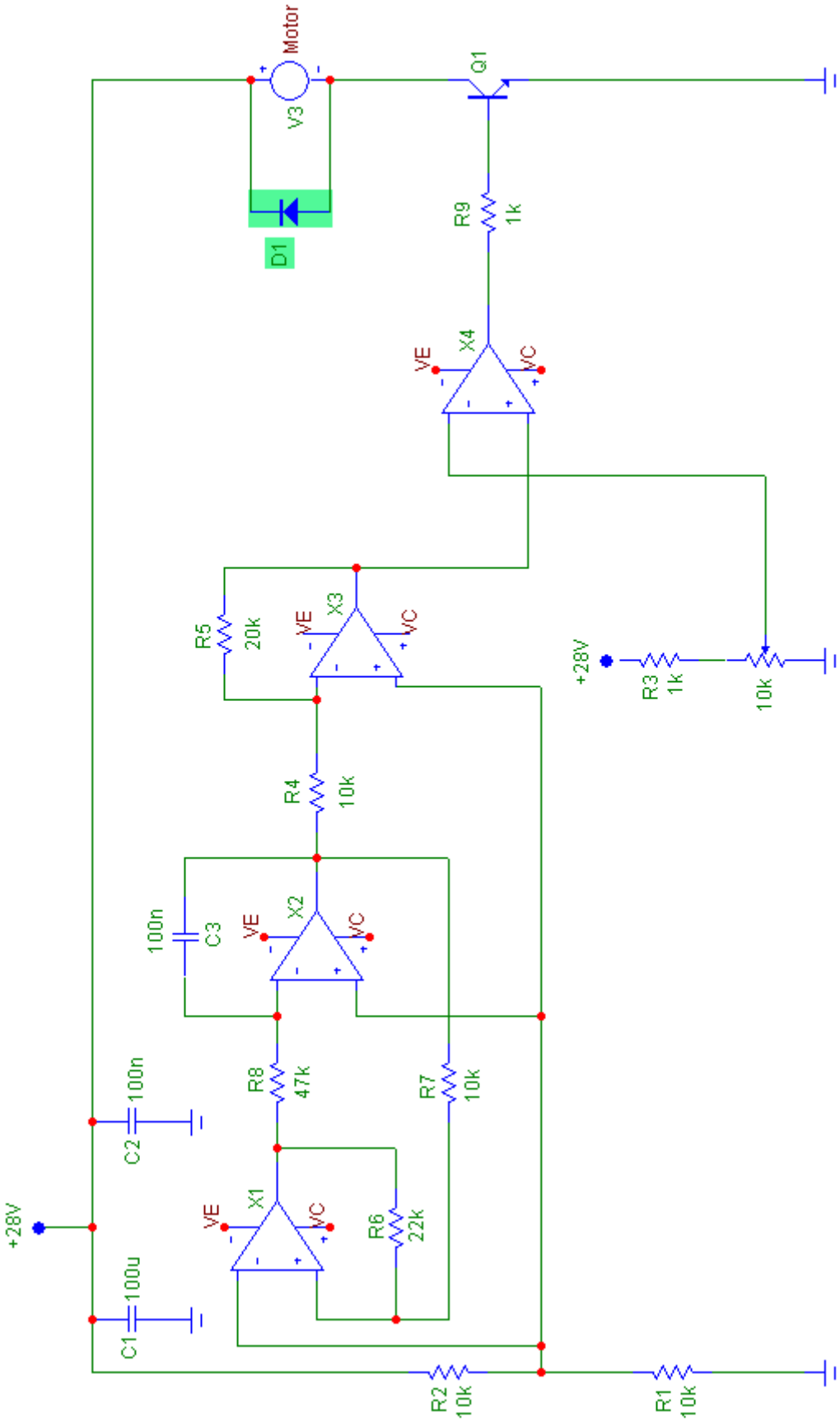

Figure 3.10: A PWM generating op-amp circuit

How the PWM circuit works [14][12]

With reference to Figures 3.10 and 3.11, the PWM signal is generated as follows:

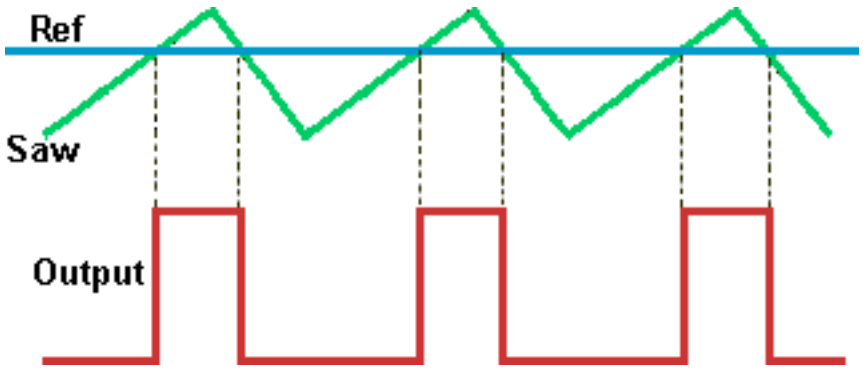

Figure 3.11: How the PWM circuit works [12]

- An oscillator is used to generate the sawtooth waveform (Saw-green line). The sawtooth waveform is generated by op-amps X1 and X2 configured as a Schmitt Trigger and Miller Integrator.
- Op-amp X3 acts as a low gain amplifier that brings the trough of the sawtooth waveform to just above 0V, and peaking at about 26V.
- A potentiometer is used to set a steady reference voltage (Ref-blue line).
- A comparator (op-amp X4) compares the sawtooth voltage with the reference voltage. When the sawtooth voltage rises above the reference voltage, the power transistor (Q1) is switched on. As it falls below the reference, it is switched off. This gives a square wave output to the motor (Output-red line).
- If the 10kΩ potentiometer is adjusted to give a higher reference voltage (thus raising the blue line), the sawtooth never reaches it, so the output is zero (0% duty cycle). With a low reference, the comparator is always on, giving full power (100% duty cycle)
- Instead of using a potentiometer to vary the motor speed, the variable DAC output voltage is integrated as an input to the operational amplifier X4 which acts as a comparator circuit. As a result, varying user inputs in LabVIEW would be used to drive the motor at different speeds.

3.5 Reading from Synchros

The pedestal has two synchros, one on the elevation axis and the other on the azimuth axis. Acquiring velocity and angle measurements from these synchros involves interfacing them with the 76CS1 card. With reference to Table 2.2, the channels that will be used

to read the data from each of the synchros are Channel 1 S/D and Channel 7 S/D for the elevation axis and the azimuth axis respectively. The choice of which channels to use is arbitrary, Channel 1 and Channel 7 were chosen because of the fact that they are the most widely spaced channels, therefore allowing easier interfacing with the 78 pin connector.

Once the channels are connected correctly, the synchro-to-digital operation takes place in the 76CS1 and the corresponding output is displayed in the 76CS1 S/D GUI (as in Figure 2.7. Channel 1 and channel 7 are ticked as active and the resulting angle and velocity readings are obtained.

3.6 Limit Switches

The limit switches are designed to prevent uncontrolled motion of the motors on the elevation axis. By using the limit switches, the elevation axis will moves between 0^o-90^o angle, safely. When the motor reaches its upper or lower limitation, the limit-switch cuts-off the motor's voltage supply. The elevation axis will then only move if a reverse polarity voltage is applied across it (to drive it out of limit) [17].

The design for the system as required is now complete. All the design specifications stated here in Chapter three serve as a basis for the building and testing of the hardware and software as described in Chapter four.

Chapter 4

Building and Testing

Chapter four discusses the building and testing of the hardware and software concepts as decided in chapter three. The hardware and software is tested, and the results from the associated tests are presented. The compromises made in translating the theoretical designs into viable practical circuits are discussed. Limitations encountered during testing are discussed and the resulting final system to be designed is presented.

4.1 A 28V Split Supply

While taking into account the practical aspects of the hardware required for the PSU, the final deliverables from this project were re-evaluated and determined to be impractical given the twelve week time limit. Commissioning the 60V/1A transformer and the $10000\mu F$ capacitors proved to be the major limitations as these components were not readily available in the department and commissioning them would require time beyond the twelve weeks allocated towards this project.

As a result, a bench power supply that was readily available within the department was used. The supply used is an EZ Digital - GP1303DU Regulated DC Power Supply that can output up to $\pm$30V. The supply has a rated maximum power output of 270VA.

The bench power supply was set to series mode and the output voltage was adjusted so as to output the required +28V, 0V and -28V leads.

4.2 The Parallel Port and LabVIEW

The parallel port bits are controlled by LabVIEW, as discussed in sections 2.1.7 and 3.2. The user has control of 8 bits of the parallel port (pin2 - pin9). Using the 'Parallel Port Read and Write Loop' VI in LabVIEW, the data outputs were tested by physically connecting a digital oscilloscope to the pins of the parallel port. The expected results were that pins 2-9 would show a logic high (5V) once asserted in LabVIEW. The results obtained however showed that on the particular computer that I was using, pins 2-9 were

not in fact asserted in the correct order. Table 4.1 shows the expected results compared to those observed.

Data Pin	Corresponding Pin (expected)	Corresponding Pin (observed)
Data-0	2	12
Data-1	3	11
Data-2	4	10
Data-3	5	9
Data-4	6	8
Data-5	7	7
Data-6	8	6
Data-7	9	5

Table 4.1: Parallel Port Outputs - Expected vs Observed

The computer BIOS was checked to make sure that the parallel port was indeed set to Standard Parallel Port (SPP) mode as required by LabVIEW for the functioning of this VI as stated in section 3.2. Although the pin numbers do not correspond to those expected, we still have control of eight bits of the parallel port which is what is required for this project. As a result, this problem was not investigated further and the pin outputs of the hardware interface were reconfigured to pins 5-12.

The expected TTL output from the parallel port as stated in section 2.1.7 was 3V-5V. The amplitude of these outputs as measured with the digital oscilloscope was 3V DC.

4.3 Integrating the DAC with the PWM controller

The DAC outputs feed directly into the PWM controller. With reference to Figure 3.10, the PWM controller was initially tested with the 10kΩ potentiometer as the input to the inverting input of operational amplifier X4.

By adjusting the potentiometer, the duty cycle also varied. Table 4.2 shows the observed duty cycles for the varying inputs to the inverting pin of operational amplifier X4.

Input Voltage (V)	% Duty Cycle Across Load
0	0
4.5	10
9	20
13.5	40
18	60
22.5	70
27	90

Table 4.2: Duty Cycles Observed for Varying Input Voltages

By integrating the DAC with the PWM controller, the potentiometer is removed and the variable voltage is obtained from the TTL 3V outputs from the parallel port (amplified

with a gain stage amplifier). For the designed 3-bit DAC, Table 4.3 shows the corresponding output voltage and duty cycle for the respective binary state:

DAC Input Binary State	Output Voltage (V)	% Duty Cycle
000	0	0
001	9.4	20
010	12	35
011	15	52
100	14	50
101	17.2	56
110	17.6	58
111	19.2	65

Table 4.3: Integrating the DAC and PWM; Duty Cycles Observed for Varying Binary States

As seen from Table 4.3, the duty cycle varies between 0% and 65%, this gives us a good range to work with in terms of speed control of the motor. The varying duty cycles result in a controllable torque across the antenna motors and consequently, a speed control system.

For the different binary states of the DAC input to the parallel port bits, the speed of rotation of the antenna along the azimuth axis was measured in revolutions per minute (rpm). The results of which are tabulated in Table 4.4:

DAC Input Binary State	Antenna Speed (RPM) - Azimuth
000	0
001	10
010	13
011	17
100	16
101	20
110	21
111	23

Table 4.4: Antenna Revolutions Along Azimuth Axis at Varying DAC Input Binary States

The objectives of this project included controlling the motion of the antenna at different speeds. From Table 4.4, three DAC input states were chosen, tabulated in Table 4.5:

Speed	DAC Input Binary State	Antenna Speed (RPM) - Azimuth
Off	000	0
Slow	001	10
Fast	111	23

Table 4.5: Final Antenna Speed Control-DAC Input and Corresponding Speed

These states can be asserted through the LabVIEW GUI.

4.4 Limitations Encountered in Testing

As discussed in section 1.5, the pedestal itself is quite old and not all the hardware components were found to be in a working order. The major limitations encountered after testing of the system were:

4.4.1 The Elevation Axis

The elevation axis of the pedestal is not in a working condition. The Vactric 15P203 motor that is used to drive the axis is burnt out. The following is a list of the hardware and software that could not be implemented as a result:

- Limit Switches

  The limit switches were designed specifically for the elevation axis, the azimuth axis is allowed to move through $360^o$and does not require positioning constraints.

- S/D Measurement

  The shaft of the synchro on the elevation axis would not be moving, as a result, when interfacing with the S/D card, Channel 7 on the 76CS1 which was allocated to the second synchro of the system will be left inactive.

4.4.2 Commissioning of a 78 pin D-type Male Connector for the S/D Card

The S/D card has a 78 pin interface and it was necessary to obtain a suitable male D-type connector in order to interface the synchros with the card. After failing to find such a connector from many hardware and component stores across South Africa, the connector was finally obtained from North Atlantic Industries in week eight of the project.

The interfacing of the synchros with the S/D card as well as the testing of the S/D GUIs and the 76CS1 LabVIEW VI could only start after the connector was obtained.

4.5 Final System Design

As a result of the limitations encountered in Section 4.4, namely the elevation axis, the final circuit block diagram of the system designed was modified from that of Figure 3.1 to the design shown in Figure 4.1:

The system is now refined to control the speed and direction of the antenna, along the azimuth axis. Table 4.6 shows how the data bits of the parallel port are used in this application:

Bit	Function
12 (Data-0)	Direction (azimuth)
11 (Data-1)	Speed
10 (Data-2)	Speed
9 (Data-3)	Speed
8 (Data-4)	Unused
7 (Data-5)	Unused
6 (Data-6)	Unused
5 (Data-7)	Unused

Table 4.6: Parallel Port Bits - Final System Design

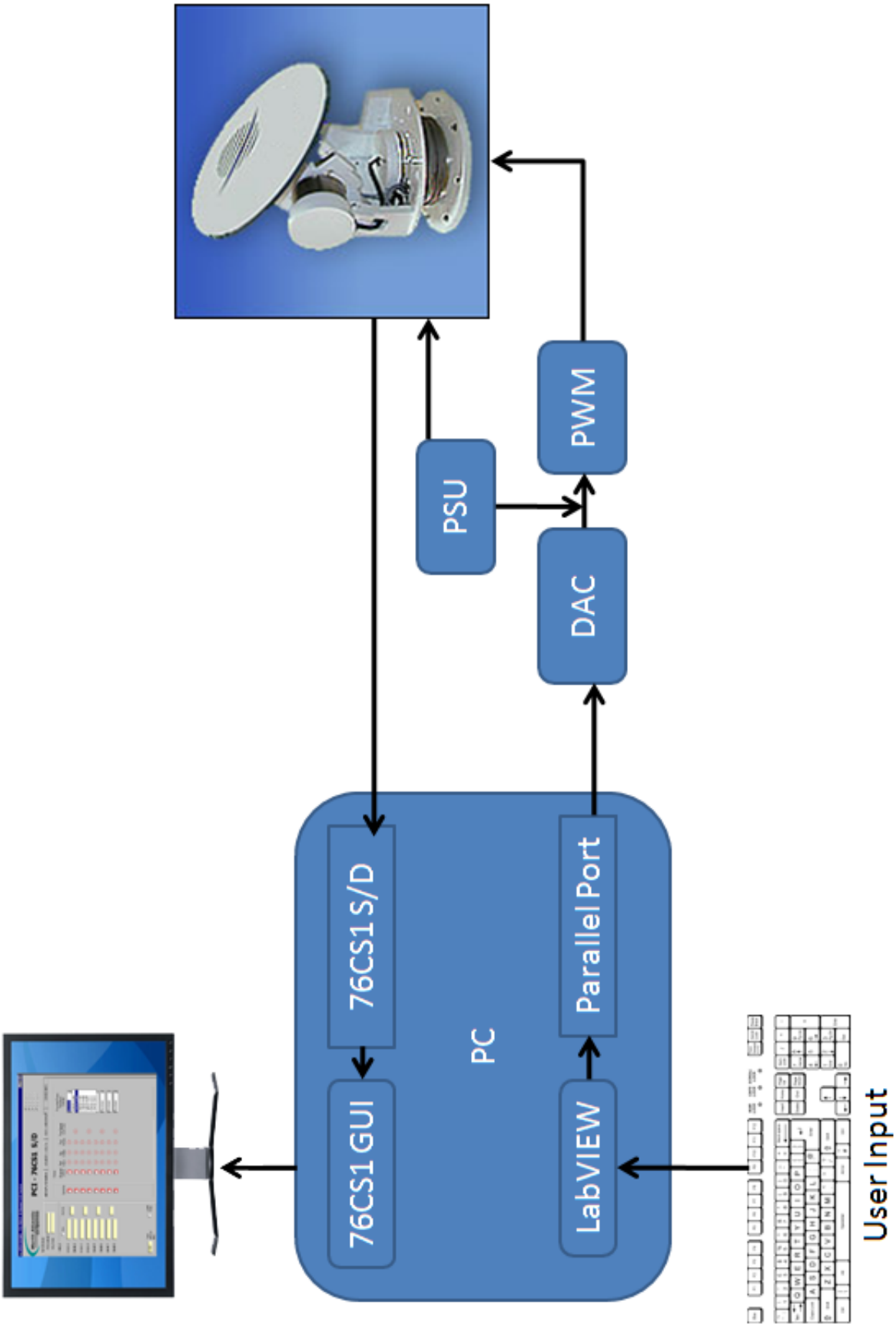

Figure 4.1: Block Diagram of the Final System

Chapter 5

Conclusions and Further Recommendations

Chapter five discusses the conclusions that are drawn based on the results of the testing of the final system as described in chapter four. The final system is discussed with respect to the initial project requirements. At the end of the twelve week period allocated to this project, the system designed is open for further research and experimentation. Recommendations as how the elements of this project could be used as a basis for continued research and experimentation are made.

5.1 Conclusions

The project status, with regards to the phases of research, design and implementation at the end of the twelve week project period is presented in Table 5.1 and discussed as follows:

System Design From the objectives presented in the user requirements, a control and measurement system was designed.

The system would ultimately control the direction, speed and axis of rotation of the antenna from a variable user input. The motion attributes (angle and velocity) would then be captured and displayed as an output to the user on a computer based interface.

Background to Hardware The hardware used in this project, namely the pedestal housing the elevation over azimuth antenna, the antenna itself and the North Atlantic Industries 76CS1 S/D card have been researched thoroughly. The theory behind the functioning of the components of the antenna hardware and the S/D card are discussed, a clear understanding of their roles in the core of the control and measurement system to be implemented has been obtained.

Project Phase	Task	Status
Research	System to be Implemented	Complete
Research	Background to Hardware	Complete
Research	Background to Software	Complete
Design	$\pm$28V PSU	Complete
Design	Parallel Port Control - LabVIEW	Complete
Design	3-Bit DAC	Complete
Design	PWM Generation	Complete
Design	Data Acquisition from Synchros	Complete
Design	Limit Switches	In Progress
Implementation	$\pm$28V PSU	Complete - Alternative Method Used
Implementation	Parallel Port Control - LabVIEW	Complete
Implementation	3-Bit DAC	Complete
Implementation	PWM Generation	Complete
Implementation	Data Acquisition from Synchros	In Progress
Implementation	Limit Switches	Not Implemented

Table 5.1: Final Project Status

Background to Software Research into how LabVIEW functions has been conducted and a clear understanding of programming with LabVIEW has been obtained. The tasks of creating VIs and utilising the existing LabVIEW VIs for the purpose of this project, have been accomplished.

The S/D card's VB GUI was examined and the functioning of it was understood and used successfully in obtaining the angle and velocity measurements of the antenna.

The Power Supply Unit The $\pm$28V PSU required for this system has been designed, with all the required hardware components noted. Due to the timing constraints of the project, this particular design was not implemented. Instead, a bench PSU that can provide the required +28V, 0V and -28V leads was used. The use of the bench PSU instead of a compact and dedicated PSU does not in anyway affect the design or implementation of the subsequent components in the control and measurement system.

The 3-Bit DAC A 3-Bit DAC for the purpose of converting the digital signal output from the parallel port (asserted by the user in LabVIEW) to an analogue voltage to ultimately control the direction and motion of the antenna has been designed and implemented. The DAC integrates with a gain stage operational amplifier and outputs to the PWM circuitry.

The PWM Generator A PWM signal was generated and varied (from the user defined DAC input) in order to control the duty cycle of the voltage applied across the motor corresponding to the azimuth axis of the antenna. The PWM scheme was implemented and configured to output duty cycles of 0%, 20% and 65% with corresponding antenna rotation speeds of 0, 10 and 23 revolutions per minute respectively.

Data Acquisition The motion attributes of the antenna (angle and velocity) were to be measured and displayed by use of the 76CS1 S/D card. The card was connected and installed on a Microsoft Windows XP based platform. A 78 pin, D-type male connector was commissioned and used to interface the synchro on the azimuth axis with channel 1 of the S/D card to obtain the antenna angle and velocity.

At the time of completion of this report, the task of interfacing the synchro with the S/D card successfully to display an output reading on the S/D VB GUI was incomplete.

Limit Switches The limit switches were required to restrict the motion of the elevation axis to within a safe working space. Due to the damaged motor on the elevation axis of the pedestal, the limit switches could not be implemented and as a result, were not designed. The underlying theory was clearly understood.

5.2 Further Recommendations

5.2.1 Achieving the Initial Project Requirements

By comparing the final system presented to that of which was the original requirement of this project, it can be seen that the objectives have only been partially met. This is justified in sections 1.5 and 4.4 where the limitations of the project have been clearly stated.

The required final system as described in the block diagram in Figure 3.1 would accomplish the following:

- Prompt the user for an input speed for the specific axis of motion (from LabVIEW).
- Move the antenna at that speed, in the desired axis (with regulated motion for the elevation axis).
- The velocity and angle of motion of the antenna would be captured by the synchro-S/D card interface and output to the screen (through the S/D card VB GUI).

In order for the complete system, as described above to be implemented, additional steps need to be taken, namely:

- The commission of a standalone PSU (using the design presented in section 3.1), dedicated to the pedestal.
- The commission and installation of a working Vactric 15P203 motor for the elevation axis.
- The design and testing of the safety limit switches to keep the elevation axis motion to within a safe working space.
- Interfacing the synchro on the elevation axis with a second S/D channel on the 76CS1 card.

5.2.2 Extensions to this Project

In addition to the work carried out to achieve the initial user requirements, further research and implementation could be carried out to extend the capabilities of the system.

Driving the Antenna to a Set-point

As an addition to the final system design, the project could be extended to drive the antenna to a set-point from a LabVIEW based GUI. In this system, the user would be prompted for an input coordinate. Based on the user input coordinate, the antenna would then move along firstly the azimuth axis, and then the elevation axis towards this coordinate. The final position of the antenna will then be compared with the angle and velocity readings attained from the S/D card to check for accuracy.

Implementing this system would serve as a culmination of all the elements of the current project together with the new requirements to produce a useful set-point tracking system.

Appendix A

76CS1 Datasheet

The detailed specifictations for the North Atlantic Industries 76CS1 S/D PCI data acquisition card are given with reference to the hardware datasheet [7]:

- 16 bit resolution
- 1 arc minute accuracy for measurement channels; 30 arc seconds accuracy for stimulus channels
- Continuous background bit testing with Reference and Signal loss detection
- Power-On Self-Test (POST)
- S/D channels are self-calibrating
- Automatically supports either 5V or 3.3V PCI bus
- 47 Hz to 10 kHz Variations available
- Encoder (A & B) plus Index Outputs with Programmable resolution-Optional
- Synchro/Resolver Programmable-Optional (Measurement side S/D)
- ON/OFF for D/S channels
- Transformer isolated
- Accurate Digital Velocity outputs
- Latch feature (read all channels simultaneously)
- Synthetic reference for S/D compensates for ±60° phase shift
- No adjustments or trimming required
- Part number, S/N, Date code, & Rev. in non-volatile memory

SPECIFICATIONS	
Resolution	16 bit (Up to 24 bit for two-speed mode)
Accuracy	±1 arc minute for single speed inputs (±1 arc minute divided by gear ratio for two-speed)
Tracking Rate	18.5 RPS for 60 Hz version; 150 RPS for 360 Hz or greater versions. (Referred to the Fine input for two-speed configuration)
Bandwidth	10 Hz for 60 Hz versions; 40 Hz for 400 Hz versions, & 100 Hz for greater than 1 kHz version. (also can be factory customized)
Input format	Synchro or Resolver
Input voltage	Resolver : 2-28 V L-L Autoranging, or 90 V L-L; Synchro : 11.8 V L-L , or 90 V L-L Resolver and Synchro are transformer isolated
Input Impedance	26 V L-L or less: 40 kΩ min. 90 V L-L: 100 kΩ min
Reference/Input	2-115 Vrms, @ 5 mA max ; Transformer isolated.
Frequency	47 Hz to 10 kHz
Encoder outputs	Either 12,13,14,15, or 16-bit resolution, (field programmable) with Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions), 13-bit is 2,048 cycles (8,192 transitions) etc. After the encoder resolution has been selected, (12-16 Bits), it will not change with varying input speeds. Differential outputs are complementary TTL (use TTL+ and dc gnd for short distances or TTL(+) and (–) in the differential mode, into differential receivers for long distance to avoid ground noise). Optional, see P/N.
Commutation outputs	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors
Phase shift	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°
Velocity, Digital	16 bit resolution; Linearity: 0.1%
Two-speed ratio	Programmable from 2 to 255.
Angle Change Alert	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt is generated. Default is disabled. Msb = 180°; Minimum differential is 0.05°. Max differential that can be programmed is 179.9°.

Table A.1: 76CS1 Measurement Channel Specifications [7]

SPECIFICATIONS	
Resolution	16 bits (.0055°)
Accuracy	30 arc seconds (.008°) at 0.3 VA; ±1 arc minute (.017°) at 1.2 VA. No load to full load
Two-Speed ratio	Programmable from 2 to 255
Rotation	Programmable Start and Stop angles. 0 rps to ±13.5 rps with a resolution of 0.15°/sec. Stepping rate is 16 bits to 3.4 rps, then is automatically reduced to 14 bits up to 13.5 rps.
Output format	Synchro or Resolver, (See part number), transformer isolated
Output voltage	2-90 VL-L
Output load	1.2 VA max./Channel. Short circuit protected (5000Ω reactive at 90 VL-L; Synchro, 90Ω reactive at 11.8 Synchro, 110 Ω reactive at 11.8 VL-L Resolver)
Regulation	5% max. No load to Full load
Reference voltage	2-26VAC, 115VAC (See part number), transformer isolated.
Reference frequency	47 Hz to 10 kHz (See part number). 47 Hz for use with external amplifiers
Reference current	1 ma max./Channel
Phase shift	5° max. between output and reference
Settling time	Less than 100 microseconds

Table A.2: 76CS1 Stimulus Channel Specifications [7]

Appendix B

Component Listing

The required components for all the hardware to be designed for this project is given below:

B.1 Power Supply Unit (PSU)

- 1 X 60V/1A centre tapped transformer
- 2 X 10000μF smoothing capacitors
- 1 X LM317 three terminal voltage regulator (+28V)
- 1 X LM337 three terminal voltage regulator (-28V)
- 2 X 1N4001 diodes (100V/1A minimum rating)

B.2 3-bit DAC with gain stage amplifier

- 4 X 2.2MΩ resistors
- 2 X 1MΩ resistors
- 1 X LM741 op-amp
- 1 X 82kΩ resistor (feedback of op-amp)
- 1 X 10kΩ resistor (inverting input of op-amp)

B.3 PWM controller

- 1 X LM324 14-pin quad op-amp
- 4 X 10kΩ resistors

- 2 X 1kΩ resistors
- 1 X 20kΩ resistor
- 1 X 22kΩ resistor
- 1 X 47kΩ resistor
- 2 X 100nF capacitors (de-coupling and feedback)
- 1 X 100μF capacitor (de-coupling)
- 1 X 10kΩ potentiometer (testing purposes only, replaced by DAC input)
- 1 X 2N2222A NPN bipolar transistor
- 1 X 1N4001 diode

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