# A Digitally Controlled Grid Connected Modular Cascaded H-bridge Multilevel Inverter

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| その他のタイトル | 電力系統に接続されたモジュラー・カスケードHブリッジ多段インバータのディジタル制御 |
| 学位授与年度 | 平成29年度 |
| 学位授与番号 | 17104甲生工第310号 |
| URL | http://hdl.handle.net/10228/00006820 |

# A Digitally Controlled Grid Connected Modular Cascaded H-bridge Multilevel Inverter

A DISSERTATION

submitted in partial fulfilment of the requirements for the degree

of

**DOCTOR OF PHILOSOPHY**

By

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**March, 2018**

# Acknowledgement

First and foremost, I would like to express special gratitude to my supervisor Prof. Tsuyoshi Hanamoto, for granting me the freedom to pursue the research ideas that have been led to completion of this dissertation. Hanamoto sensei has inspired me with his polite and brilliant suggestions for research and life. I would like to thank Hanamoto sensei most sincerely for giving me the opportunity to work under his supervision. He has been supportive and contributed immensely for successful completion of this thesis.

I sincerely thank to professors of committee, Prof. Yasunori Mitani, Prof. Ichiro Omura and Prof. Shyam S. Pandey for reading my thesis and giving me the enormous suggestions to make it more effective and concrete. I am thankful for their contribution and vast ideas to make my thesis more elaborative.

I shall extend my special thanks to my friends Ravi, Yoshino and Maehata for their support during my study in japan. These guys with in the same lab made my three years of study very enjoyable and fruitful. I also like to thank all the member of Hanamoto laboratory for planning different parties, trips, game and supporting me during my stay and research in last three years.

I also like to thank Natsumo Yoshitake for discussing and working with me as a team for the different task and to achieve different milestone in the ongoing research. His suggestion and doubts always drives me for more hard work for the relevant solutions. I shall thank Yoshitake san for helping in development of hardware prototype.

I would like to thank my all Indian friends living in Kitakyusu Japan specially Gaurav,Gyanendra, Mallikarjun, Nishanth, Nayan,Kaushal, Nishit, Atul and Vijay for their wonderful company in here. I always felt like Kitakyushu is second home because of these guys.

I would like to express my gratitude to Kyutech teaching and non-teaching staff, JSPS, KDDI foundation, FAIS for supporting my study and stay in Japan. I would like to specially thank Japanese language teachers for their experienced teaching and effort to teach Japanese language.

I also like to thank and express my gratitude to the local people of Kitakyushu, Japan for their peaceful hospitality and enjoyed playing, jogging, cycling, living in this beautiful country.

At last I would like to thank my grandparents and parents for their blessing and encouragement during my study. I also like to thanks my younger sister and brother for their time to time suggestions for maintaining my good health and interesting life throughout the academic career.

# Abstract

The issues of increasing demand of energy and limited amount of available conventional energy sources necessitates highly efficient electrical energy conversion system to control power from generation to consumer end. To achieve environment friendly and high efficiency transmission and distribution of electrical energy, power electronics technology emerges as an adequate option. Power electronics converter is used as an application of solid state devices for control and conversion of electrical power. Voltage source inverter is mainly utilized for the highly efficient electrical energy conversion within recently introduced grid codes in different renewable energy generations, industrial processes, motor drives and (hybrid) electric vehicle. Further evaluated topology of voltage source inverters evolves modular cascaded H-bridge multilevel inverter (CHMLI) which holds some advantages such as, lower switching frequency operation, less total harmonic distortion, modularity in the structure and distributed power stress on power semiconductor devices, medium voltage-high power operation.

The main focus of the work are field programmable gate array (FPGA) based digital control of CHMLI and its application to the grid.FPGA provides number of advantages such as higher performance, lower cost, and robustness of solution, DSP (digital signal processing) capabilities and solution customization.

The first chapter focusing on the energy and electricity demand and future scenario, role of power electronics, general trend in technological innovation and literature review for the presented work that includes multilevel inverters, essential role of modulation and control, power grid issues with available solutions and limitations of the currently available solutions.

In chapter 2, open loop control with phase shifted (PS) and level shifted (LS) carrier based sinusoidal pulse width modulations are implemented for CHMLI connected to linear load. Performance of PS and LS carrier based modulation is investigated using FPGA based digital control for five, seven and nine level inverter. In addition to open loop control of CHMLI, FPGA hardware-in-loop co-simulation is proposed for controller prototyping of CHMLI. Third harmonics injected PWM is used for control of CHMLI. Performance of five and seven level inverter is investigated by real time co-simulation for phase shifted and level shifted carrier based THIPWM.

In chapter 3, a novel design of LCL filter is proposed considering modified constraints of lower switching frequency operation. LCL interfaced distribution static compensator (DSTATCOM) is analyzed and three phase grid connected system model is developed in MATLAB/Simulink. LCL filter with CHMLI based system offers some adequate benefits such as reduced inductance, wider bandwidth, better ripple attenuation, less harmonics in pcc voltage. The results are demonstrated for a linear/non-linear load under unbalanced conditions, considering the voltage sag and swell in the system due to a disturbance in the load.

In chapter 4, digital multiband hysteresis current controller (HCC) is proposed for grid connected CHMLI that offers functions of close loop controller and implicit modulator. Using sinusoidal pulse width modulations with linear control techniques always possess some delays and steady state error therefore need of complex controller design arises. Digital multiband HCC is able to drive the close loop system with improved stability and possess certain easiness in implementation of digital circuitry. Experimental prototype of grid connected CHMLI is developed and controller implementation is done using Xilinx system generator based model design for FPGA.

In chapter 5, digital multiband HCC is proposed for DSTATCOM application and comparison of linear control techniques such as PI controller with LS, PS and digital multiband HCC is carried out. Leading advantages of digital multiband HCC over linear controller under load abnormalities are demonstrated.

Chapter 6, this chapter concludes the work presented in whole dissertation, summarizes the work and leads to the future possibilities in the ongoing research.

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# CHAPTER 1

# Introduction

## 1.1 Energy and Electricity

The development in social and economic life of human kind persuaded the need of energy and its management to deliver at best efficiency. We have achieved certain compatibility to use available resources by growing technology and creating man made machines. Since last 100 years the technology word evaluated for the external and internal progress of a manufacturing, transmission, and distribution.

Now we are living in real world which is a global society and where nations are increasingly independent bodies to confront for competitiveness of global demand and supply of energy sources. The world economy is expected to almost double over the next 20 years, with growth rate of averaging 3.4% per annum. Fig.1.1 shows how the energy consumption will take place according to different geographical regions: OECD (organization for economic co-operation and development) and other countries. In Fig.1.2, it is shown that present scenario of contribution of different kind of energy sources to the global energy consumption. What happens today in India and Japan, for example, affects USA and vice-versa. All the nation are facing industrial competitiveness in the marathon of global market and progress for sustainable economic position. As we know that energy prices are increasing due to limitation of conventional energy sources. Electrical energy has become one of the leading source to drive machines and so forth many industrial and domestic processes. In such a competitive environment power electronics technology with motion control is having a dominance and progressive development in the area of electrical energy conversion systems. [1]-[3].

To achieve environment friendly electrical energy generation, transmission and distribution power electronics technology emerged as an adequate option and spread to every corner of industrial, commercial, transportation, aerospace, residential, military and utility grid systems[4]-[5]. For the controlled operation and management of electrical energy it is required to control the voltage, current, power and frequency from generation to the consumer end. The commercial availability of electricity has been started particularly by the invention of induction motors then the age of solid state electronics by the invention of transistors in 1948, and commercially thyristor was

introduced in 1958[6] and processed the evolution of modern power electronics. After gradual development to the age of integrated circuits, computers, communication and robotics, now it has been reached to world of internet. Energy consumption in the world has been increased through over last six decades. During these development ages the growth in generation and consumption in proportion to cater the need of increasing population of the world, we had hardly considered their adverse effect on environment.

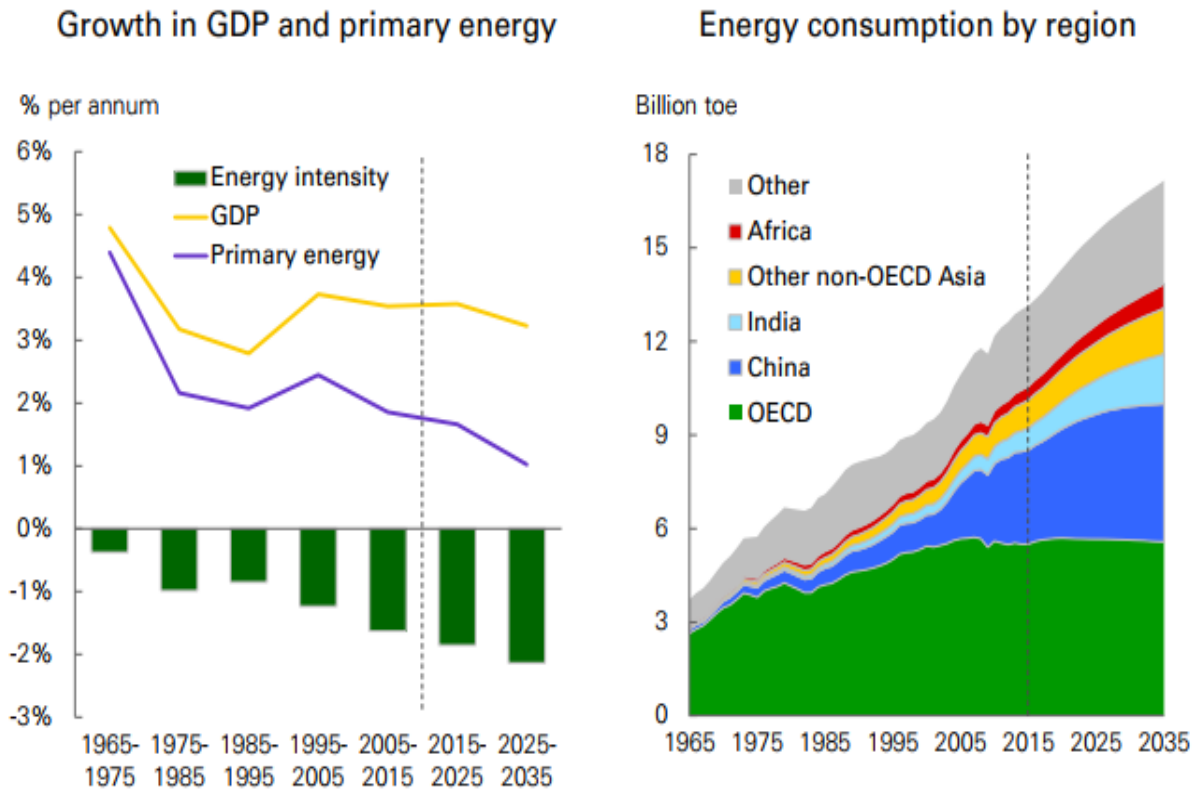



**Figure.1.1** Gross domestic product (GDP) growth over six decades with energy intensity followed by energy consumption by region (source: 2017 energy outlook)[5]

We can say that most of the sources are finishing so renewable ones are the adequate option for environment friendly clean power system. The available or developing electrical energy sources has strong daily and seasonal pattern. And the electric power demand at consumer end could have different characteristics. Therefore it would be difficult to operate an electrical system installed with only renewable generation systems due to high uncertainty and unavailability in renewable energy generation in course of time. The better option to utilize these energy sources connected with grid at distribution level [7]-[9].

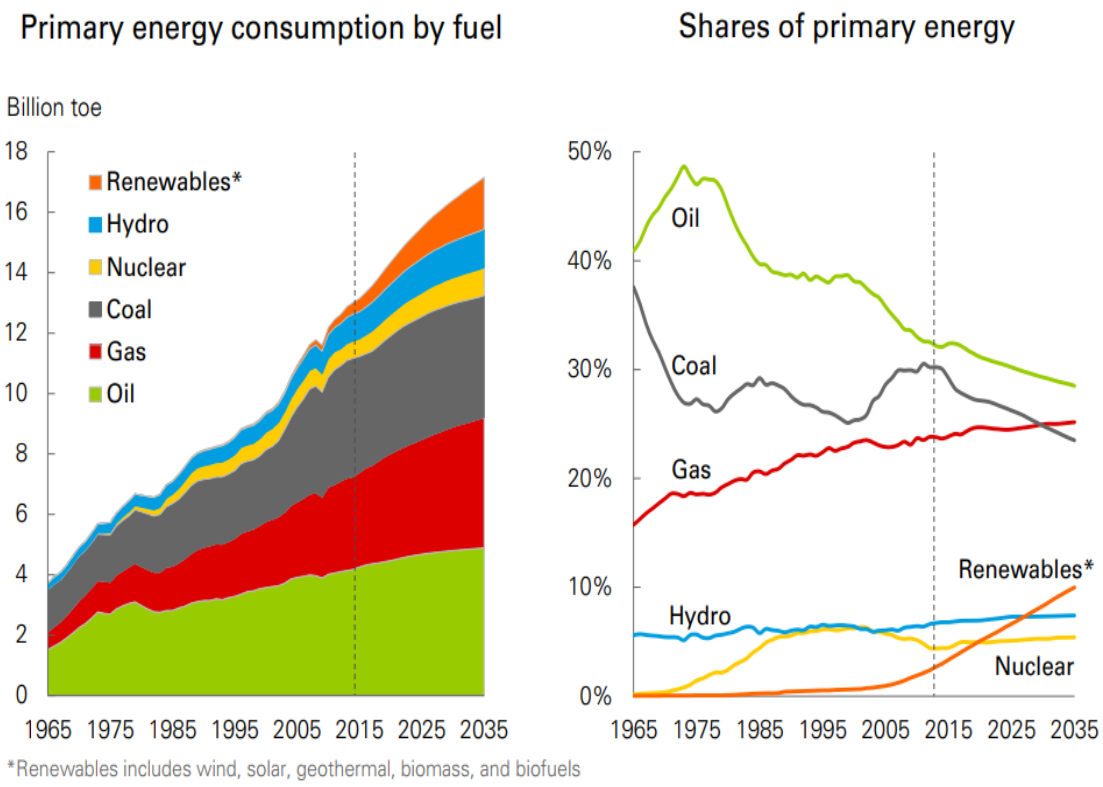



**Figure1.2** The gradual change in energy source mix continues over the decades (source: 2017 energy outlook)

## 1.2 General Trends and Literature Review

In conventional power system, large scale power generation units (plants) located at adequate places generate most of the power. Then followed by generation, it is transferred to the large consumers or distribution station through long transmission lines. The control and monitoring is continuously done by control centers mainly to ensure power quality namely voltage and frequency. However power system is changing since last two decade as large number of dispersed generation units including renewable and non-renewable such as photovoltaic (PV) generation, wind turbines, small hydro, fuel cells, gas, heat and power station have emerged[10]-[14].

The generator operate at a fixed speeding at conventional generation stations, and so total operation can be done on fixed frequency but present time sources such as wind mills generates voltage with variable frequency, similarly fuel cell and PV generated power cannot fed to the grid directly, or cannot be connected to the grid directly. Here so forth power electronics plays a important role in matching characteristics of these sources to the power grid that is associated with the conventional

energy sources. The parameters such as voltage, frequency, control of reactive and active power , high order harmonics minimization etc. are need to be controlled and optimized using power electronics technology[15].

Power electronics being the electrical energy conversion technology, plays vital role in modern industrial process and renewable energy integration to the grid [16]. It is a very essential part of the system to match the characteristics of generated power and required power by consumer. To achieve high efficiency performance of grid connected system one need to have control on power electronics energy conversion system [17]-[20].

It is well known that high efficiency and fast switching silicon power semiconductor devices e.g. thyristor, triac, gate turn-off thyristor (GTO), power MOSFET, insulated gate bipolar transistor (IGBT), and integrated gate-commuted thyristor (IGCT) comprises the power electronics. And application of these fast switching devices includes regulated dc and ac power supplies, uninterruptable power supplies electromechanical processes, lighting and heating control, distribution static synchronous compensator(DSTATCOM), static var generator(SVG), static var compensator(SVC), active power filters(APFs), HVDC transmission systems, flexible ac transmission systems(FACTS), grid integration of PV and fuel cell converters, dc and ac circuit breakers, high-frequency heating, energy storage, motor drives application that includes computer and peripherals , motor starters, transportation system, home appliances, paper and textile mills, pumps, compressors, cement and rolling mills, machinery tools and robotics, including constant frequency variable speed systems., etc. In the 21st century the widespread application of power electronics is kind of industrial revolution which has been somewhat unmatched in the history [21]-[22].

Power electronics technology associates with efficient energy conversion, control and conditioning of electrical energy from source to load. In present scenario communities are working on improvement in the efficiency of power electronics converters [23].In this process evolution of faster devices, improved topologies, advance control are key steps are being taken by researchers. Normally power electronics converters are being the part of system to convert the provided electrical power in its customized form with its own efficient capabilities. So for the example the efficiency of the system sometimes is less than efficiency of the converter in some application, such as motor drive application, PV system, etc. [24].

Application of power electronics converters for environment friendly electrical system increased in recent years. Likewise power electronics converters are main controllable unit in the renewable energy source integration to the grid and electrification of the automotive industry [25]-[26]. These two application of power electronics converters has been grown rapidly in past years and still growing on. In addition the improved electrical drives has been developed using power electronics converters and most of these drives consume easily available electrical energy in the world [27]-[28].Power electronics converters uses semiconductor devices that can be operated in switching mode to convert and control power, the conversion can be any type such as ac to dc (rectification mode),dc to ac(inversion mode),dc to dc (buck, boost or buck-boost conversion mode), and ac to ac for frequency variation of voltage regulation (at constant frequency) mode[28].

A power conditioning unit is needed for low voltage distribution system for integration of renewable energy sources or operation in non-ideal load conditions for a grid tied application. Solar PV, fuel cells, thermoelectric generator, ultra-capacitors are some example of low voltage dc output energy sources. These low voltage dc sources need to have a conditioned high voltage level before making to ac grid. Some of the low voltage dc and high voltage ac for grid connected application has been proposed to manage some specific issues, such as, low cost, high efficiency, and robustness [29].The circuit topologies for the power conversion or conditioning is always concerns with the voltage and current levels.

Keeping main focus on the dc-ac inverters can be voltage source inverter or current source inverter. Voltage source inverters have been widely used in the recent applications [30].If there is a expectation of unity power factor, then some of the switches can be replaced by diodes and some are operated at fundamental frequency, which permits to use reduced number of semiconductor devices efficiently with different combinations for example dual buck, dual boost, and dual buck boost inverters [31]-[34].

For the designing and optimization tool for the three phase voltage source inverters it has been employed with front end rectifiers. Generally IGBT based voltage source inverters with diode front rectifiers is one of the conventional choice for the three phase inverter fed ac motor drives[35]-[36]. The essential stages are front end rectifier, inverter, the dc link capacitor, the electromagnetic interference harmonic filter. So these components have inter-dependencies and tradeoffs in the

power converter, there should be system end optimization and design for the three phase voltage source inverters to describe cost and performance of the system [37][39].

These inverters require high frequency sinusoidal pulse width modulation (SPWM) and output filters to attain sinusoidal current output. And the losses associated with the high switching frequency are non-trivial. Application of the voltage source inverters where efficiency is concerned mostly, some possible improvements has been revived [40]. Such as soft switching inverters, dual buck, boost and buck-boost inverter, multilevel inverters [41][42].

Soft switching inverters are introduced for the motor drive applications using zero voltage switching (ZVS) or zero current switching (ZCS) techniques. Use of cool MOS as primary switching devices and IGBTs as auxiliary switches are used to attain high efficiency energy conversion. The voltage balancing can be done using front end diode dc-dc converter using well balanced split voltage. The components which are added to soft switched inverters are non-negligible and if the power factors has to near unity, it's essential to use dual buck type circuits where one set of antiparallel switches are replaced with diodes [42].To improve efficiency with fast switching ultrafast diode can be employed to avoid low-voltage conduction drop and reverse recovery loss. MOSFETs are optional devices which can be used to speed up the conduction and maintaining the lower cost. The benefit of these type of circuits are robustness with the high efficiency up to 99% and circuits arraignment can avoid shoot through failure[45].Similarly buck switch pair concept can be adopted to dual boost and dual buck boost voltage source inverters.

Voltage source inverters shown in Fig. 1.3 are common type of inverter that has been used for drive application [46].Classification can be done on the basis of fundamental parameter topology and connection type of direct and indirect. The former one uses directly connection between sources to load directly using logical semiconductor devices. In other hand later is connected in two stages: rectification and inversion and normally tied up with an energy storage devices. In the direct conversion type one of the common type of converter is used which is cyclo converter in high power application. It interfaces between power supply and machine directly with the use of array of power semiconductor devices. And it converts the three phase ac voltage with variable switching frequency and variable magnitude .Although it has limitation in dynamic performance but it performs the task of power flow in both the direction in very efficient way [47].Matrix

converters are also one of the emerging topology in this family but still needs more research for industrialization and high power application [48].

Indirect converters are well established for industrial and medium power drive application, the primary classification are current source and voltage source topologies with dependency on energy storage components. So as per requirement of the application these converters are employed with the optional line and motor side filters. To reduce line current distortion phase shifted transformer with multiple windings are commonly used. The common topology of rectifiers that has been used with the indirect converters are multiphase diode or thyristor rectifiers and pulse width modulated rectifiers [49]. The capacitor that provides stiff dc voltage can be used as filter or smoothing inductor can be adequate option for filter.

Classification of high power application voltage source inverter of indirect type is darkened in the diagram shown in Fig.1.4 had got more attention and noticeably developed. Voltage source inverters are more efficiently used for industrial application in last two decades compared to current source inverters. Due to limited power rating of semiconductor of devices conventional two level inverter belongs to low and medium voltage application. Series connection of two level inverter with bulky transformers make it enable for high voltage application. Or switching devices can be connected in series to meet increased voltage rating demand. And use of increased number of semiconductor devices with capacitors and diodes permitted a more advent use of these additional switches originates the multilevel voltage source inverters to enhance the quality of input and output parameters [50]-[52].

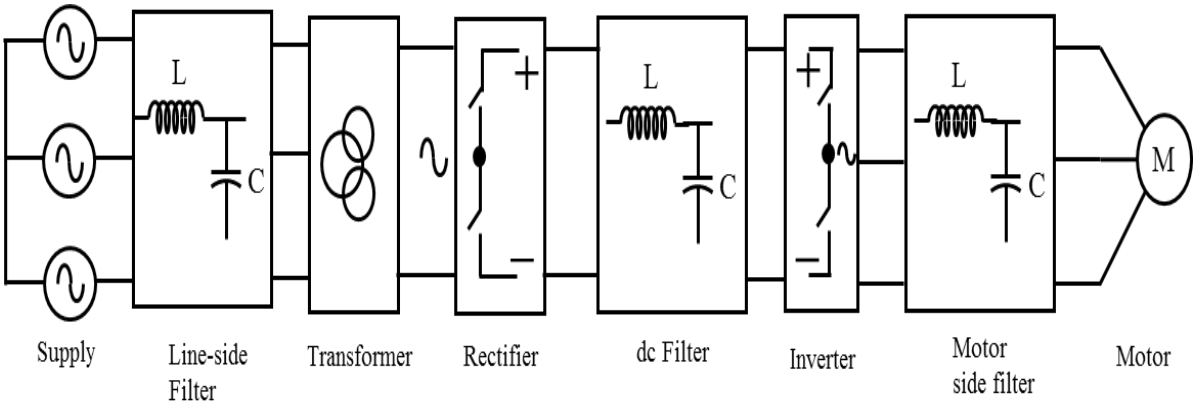



**Figure1.3** General block diagram of the medium voltage drive [46].

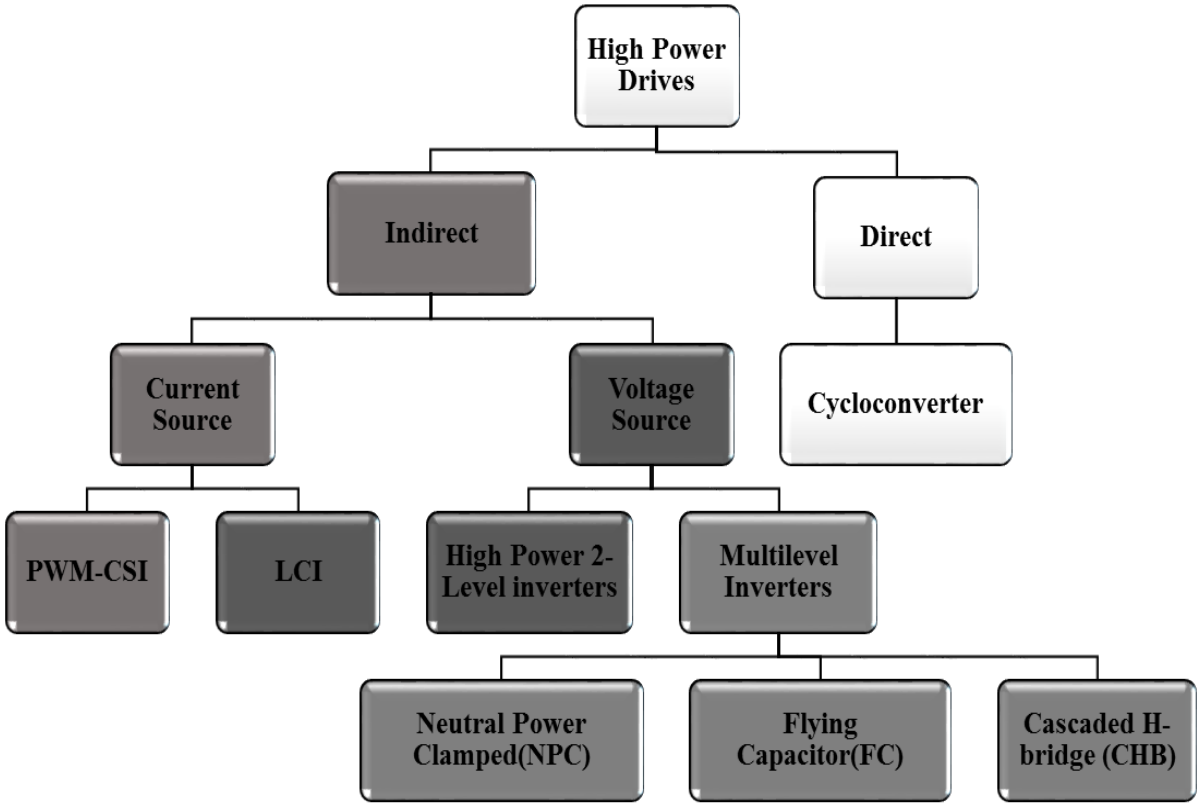



**Figure1.4**. Classification of converters for high-power drives (>1 MW).

In last two decade industries have grown rapidly and power system become more dependent on power electronics. All started with the higher power machinery which has reached to megawatt level such as ac drives are connected to medium voltage grid and it is difficult to connect these high power devices directly to the grid. To overcome with this problem a new family of inverters has come in industrial and commercial use in last two decade i.e. multilevel inverter (MLI). Although full scale industrialization is still not achieved due to complex control and design of system [53].

MLIs comprises an array of power semiconductor devices that generates synthesized stepped output voltage from capacitor voltage. Commutation of switches that permits cumulative addition of voltage across capacitors by which high voltage output can be achieved by maintaining low voltage across power semiconductor devices. The basic extended schematic diagram of capacitor voltage source inverters are shown in Fig.1.5 to generate two level, three levels and more level of output voltage. For the generation of levelled output ideal power switches are shown with different positions.

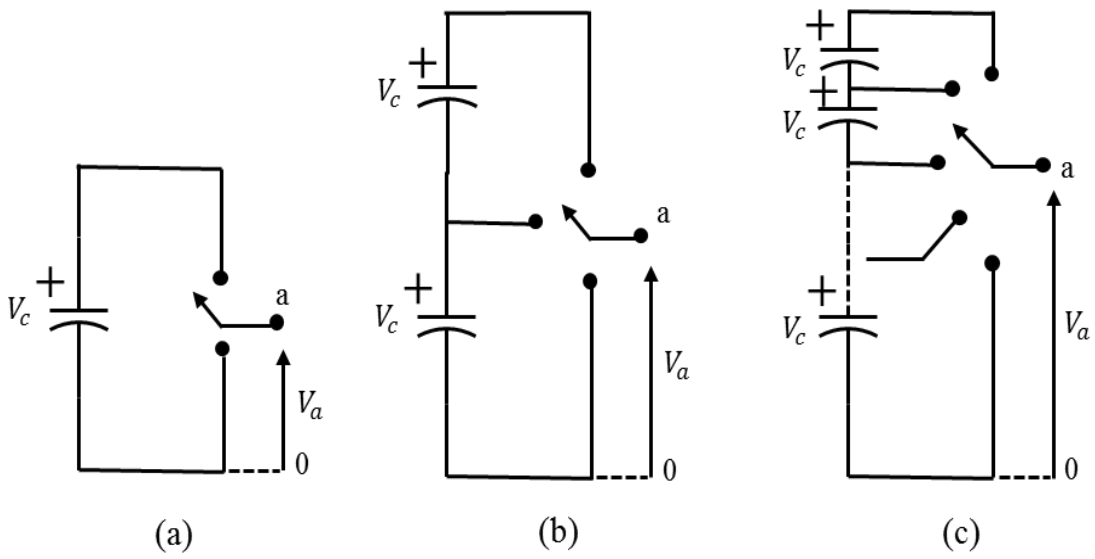



**Figure1.5** One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels [53].

In (a) two level inverter output (two values) i.e. positive value and negative value with respect to ground or negative terminal of capacitor. In other hand using three level of inverter, three values i.e. positive value, negative value and zero or more levels can be generated. For single phase, m is defined as the number of levels or steps generated then steps in voltage between two phases of the load are 2m+1. Similarly for wye connected load the steps in phase voltage can be determined. The terminology of multilevel inverters started by Nabae [54] and it started with three level inverter. The output voltage have more steps generating a staircase waveform, by increasing the number of levels in the inverter, which possess less harmonic distortion.

The reason behind there has been lots of attention paid to MLIs, because these inverters has some attractive features which are summarized as follows,

1. MLIs can generate synthesized output voltage with very low distortion and low dv/dt.
2. The load current supplied by MLIs consists very low distortion.
3. Common mode voltage has been very critical issue with conventional inverters, MLIs offers very smaller common mode voltage.
4. In addition some novel or hybrid PWM control can be implemented to achieve low stress on switching devices.
5. MLIs can operate at lower switching frequency compared to conventional multilevel inverters.

6. For medium voltage high power applications transformers can be eliminated from the systems as it offers less stress on switches.
7. The electromagnetic interference can be tolerated by use of MLIs and many more.

Table 1.1 shows the basic comparison between multilevel inverters and conventional two level inverters.

**Table 1.1 Comparison of conventional and multilevel inverters**

| S.No. | Conventional VSI | Multilevel Inverters |
|---|---|---|
| **1** | High total harmonic distortion(THD) in output voltage | Low THD in output voltage |
| **2** | Higher switching stress on power switches | Reduced switching stress on power semi-conductor devices. |
| **3** | Not suitable for high voltage application. | Applicable for high voltage high power application. |
| **4.** | Higher voltage levels cannot be produced | Higher voltage level can be produced. |
| **5.** | Electromagnetic interference (EMI) is high due to high dv/dt. | Since dv/dt is low the EMI from the system is low |
| **6.** | Higher switching losses due to high operational switching frequency. | Lower switching losses due to lower operational switching frequency. |
| **7.** | Power bus structure hence control scheme is simple. | Complexity in control scheme increases as number of level increases. |

The results shown in a patent [58] are evident that the multilevel topology have been in the research since last 35 years but not commercialized on full scale yet. As in that patent cascaded inverter was evaluated by connecting H-bridges to isolated dc sources to generate synthesized staircase output ac voltage [59]. Following the manipulation in cascaded MLIs , diodes has been used to

block sources at different steps and diode clamped MLIs were introduced [60].The diode clamped inverters become very common at that time three level output voltage was achieved by introducing mid-level voltage as neutral point voltage in addition named as neutral point clamped(NPC) MLIs. NPC inverter topology doubled the device voltage level effectively with any restriction of precise voltage matching and this topology is prevailed for research and commercial usage.

The application as an extended multilevel inverters for NPC topology was found in [61].Besides early recognition of the cascaded MLIs and its broad level application did not subjugated till 1990s.Two major applications have been found that to advocate its use in motor drive and utility grids [62][63].As requirement of medium voltage high power inverter increases with the development and vast industrialization, cascaded inverters has drawn major interest ever since. Many patents can be found on the cascaded multilevel inverter use for regenerative type motor drive or utility grids [64][65]. A major MLI topology which was introduced followed by cascaded MLIs and diode clamped is capacitor clamped MLI [66]. These three topologies of multilevel inverters are extensively used in medium voltage high power application. The application of MLIs are extended but not limited to laminators, mills, blowers, conveyors, pumps, fans compressors and so on.

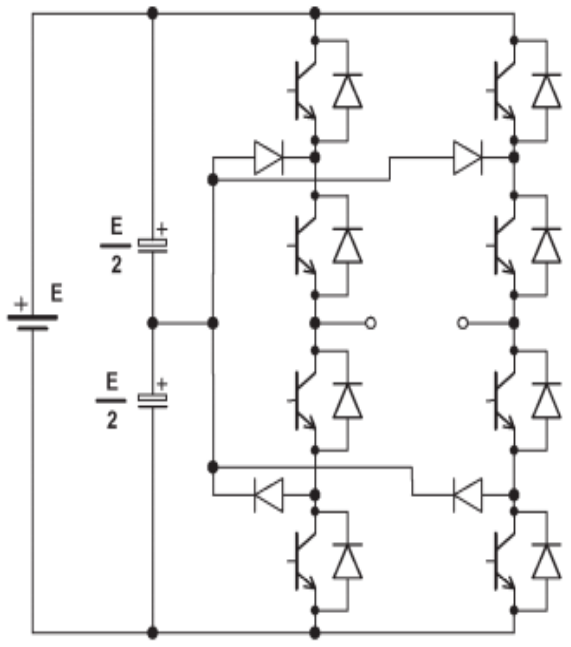



**Figure1.6** Diode clamped multilevel inverter topology [61]

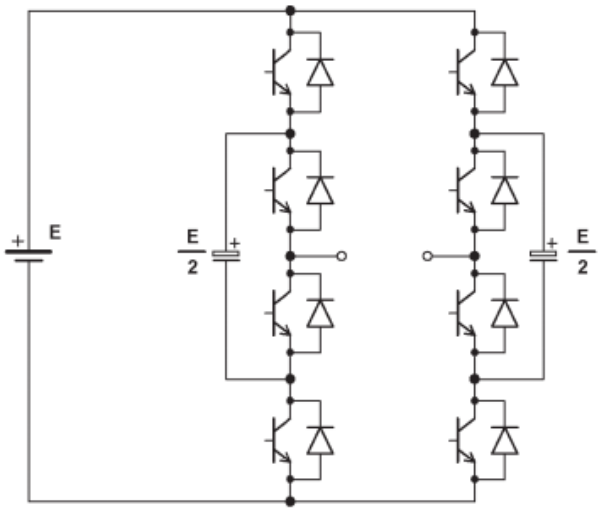



**Figure 1.7** Capacitor clamped multilevel inverter topology [66]

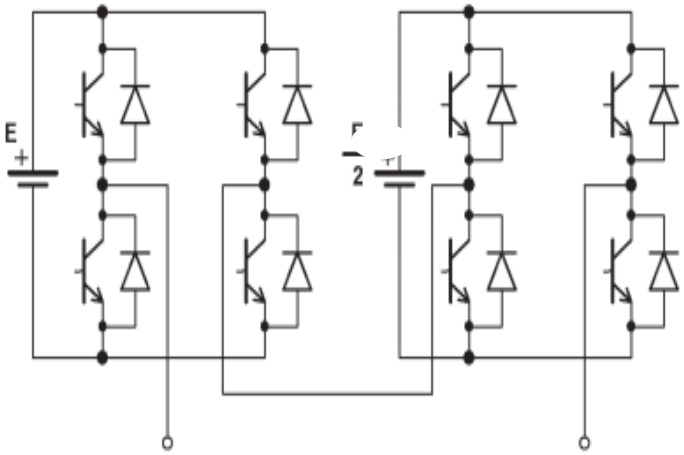



**Figure 1.8** Cascaded H-bridge multilevel inverter topology [72]

The use of multilevel inverters tremendously increased in last few years for renewable energy source integration to grid. MLIs have used for medium voltage high power applications as a static synchronous reactive power compensator and motor drives. Due to limitation of currently available power semiconductor devices MLIs are gaining attention for these application and unique alternatives for the conventional inverters because it can operate at lower switching frequency [67].In these topologies current and power sharing between power semiconductor devices can be done easily. For lower power applications (less 10kW) where high efficiency is a major concern MLIs have been competing with the conventional inverters which operates at high switching

frequency .Although low prices of power semiconductor devices and some new power devices technologies have fulfilling the current demand of high performance inverters needed in renewable energy source integration, MLIs have been used for these extended application [68].

MLIs, specially three level inverter emerges as good solution for trading off the performance and cost in high voltage high power application. The key advantages of MLIs are good harmonics spectrum, reduced power stress on switches, and making possible to use minimum size of inductor filter and better dynamic response[69].In other hand control or modulation techniques are bit complex for MLIs, there are some critical issues with different topologies such as for diode clamped MLI, dc link voltage at neutral point need to be regulated and for cascaded inverters there`s need of isolated dc sources for the each H-bridge cell and need to regulate the voltage across each bridge in some application to avoid uneven power stress or undesired harmonics spectrum[70][71].

Some other application of the MLIs have found in the literature such as static synchronous compensator (STATCOM), static var compensator (SVC), superconductivity magnetic storage system (SMES) [72]-[75].A grid connected cascaded H-bridge MLI for the photovoltaic power source integration is presented in [76].In this thesis main attention is kept to cascaded H-bridge multilevel inverters (CHMLI) due it's some of the advantageous qualities over other topologies. CHMLI establishes a capable alternative, among the available MLI topologies, benefiting with modular structure that can be prolonged to make possible transformer less connection to the grid [77]-[78]. Additionally, this topology features cost effective lower rating of the power semiconductors in comparison to the standard two-level configurations [79]. Last but not the least, This CHMLI features numerous degrees of freedom that make possible its operation even under faulty conditions and hence reliability of the system can be managed to be good enough. In spite of all these characteristics, the cascaded multilevel topology has also some disadvantages, such as isolated dc source requirement and complex control of dc bus voltage regulation in some application such as PV string panels are not grounded and additional actions need to be taken in order to dodge currents due to stray capacitances between the earth and the panel [80].

In last few years apart from well-known topologies of multilevel inverter such as CHMLI, diode clamped multilevel inverter and capacitor clamped inverters, some new inverter topologies have been introduced in the industry, especially for the application in medium voltage high power

application. And some example for those topologies are: five level active NPC [81], modular multilevel converters (MMC) [82] transistor clamped converters (TCC) [83], stacked multi-cell [84] etc. Some of the leading key factors for these new topologies are: higher power density, lower torque ripples and fault tolerant capabilities.

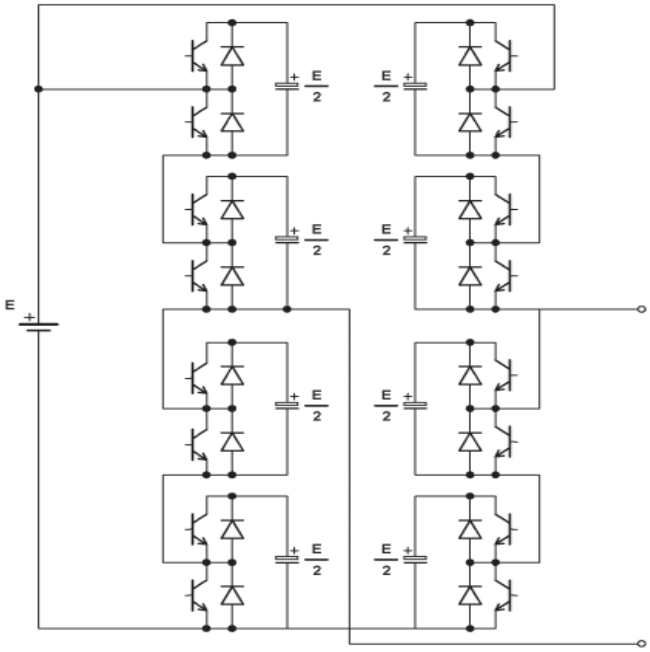



**Figure1.9** Modular multilevel converter [82]

All these new topologies requires special attention to the modulation control. Some established control techniques which are accepted for the conventional and multilevel inverters are not applicable to these new topologies. Such as open-winding fed drives also possess several different space vector distribution and need to be extended from straight forward classical method[85]-[88].

Modulation techniques are the method to provide gate signals for the power semiconductor devices to obtain switched output waveform in a way to maintain adjustability with an arbitrary magnitude, frequency and phase. Which is important for the proper control of inverter or power controlled by inverter. In starting days of power electronics converters generally pulse width modulation (PWM)[88] has been adopted as mainstream modulation technique for the conventional two level inverters. It has simplicity and effectiveness in a process of generating pulsed or switched voltage output with frequency is matching with the reference signal.

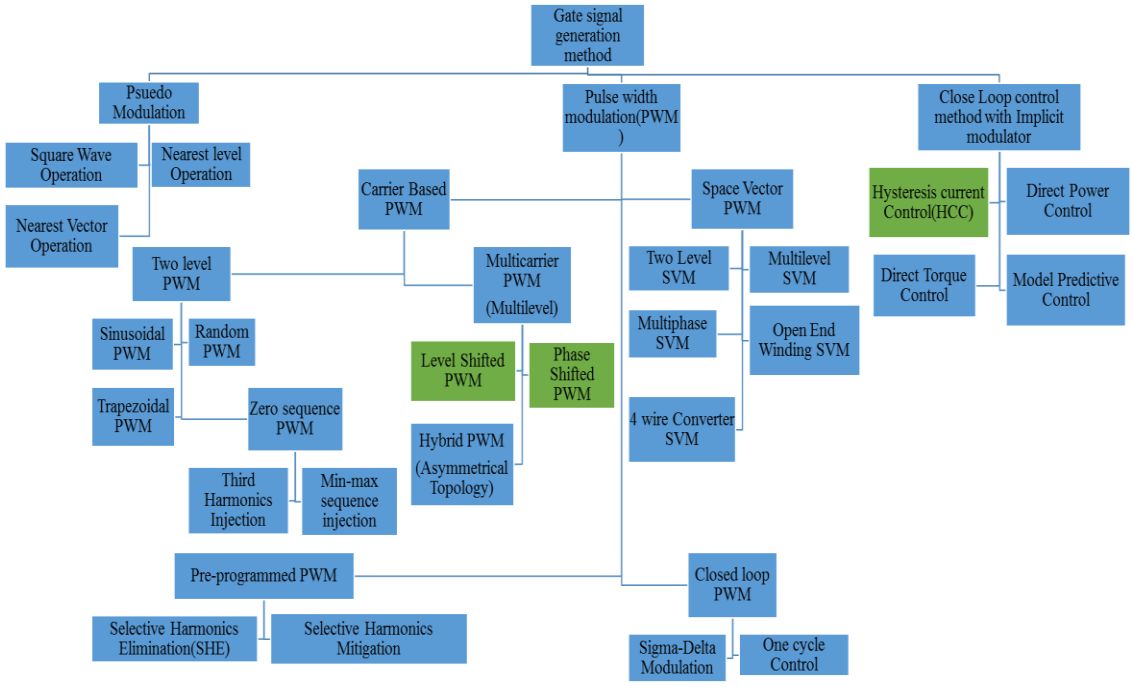



**Figure1.10** General Classification of gate signal generation methods for voltage source inverters [89].

However it's evident that every new converter topology requires a novel modulation techniques for the corresponding switching pattern to generate the switched output voltage. Generalized classification for the gate pulse generation techniques for voltage source inverters are shown in Fig1.10[89].The challenges with different topology of converters, are to be dealt with the modulation technique such as dc voltage balancing, circulating current, extra available switching redundancies and some other issues.

As shown in Fig.1.11 and 1.12, voltage source inverters can operate in open loop or close loop control loop that generates reference voltage or current for determining the switching signals [90].In the open loop operation of the inverter modulator has to generate the switching signal based on the reference that does not depend on any measurements. Normally in this case on certain operation point, the reference is externally determined by operator or outer loop control. These type of controller are used in applications such as pumps, fans, and fixed frequency drives where dynamics of the system is not a major issue. These open loop controllers for inverter gained huge success and become primarily useful due to its extreme simplicity at the verge of using a fixed operation point usually leads to performance degradation.

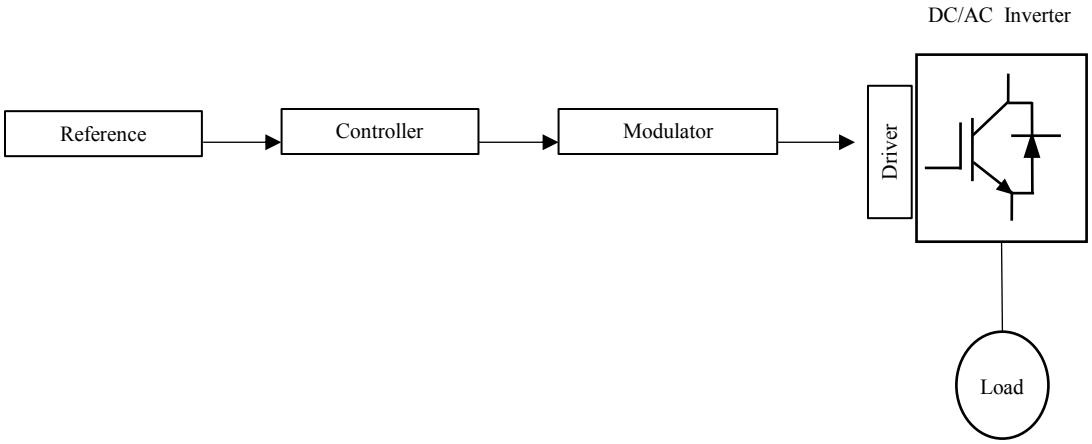



**Figure1.11**. Open loop control and modulation

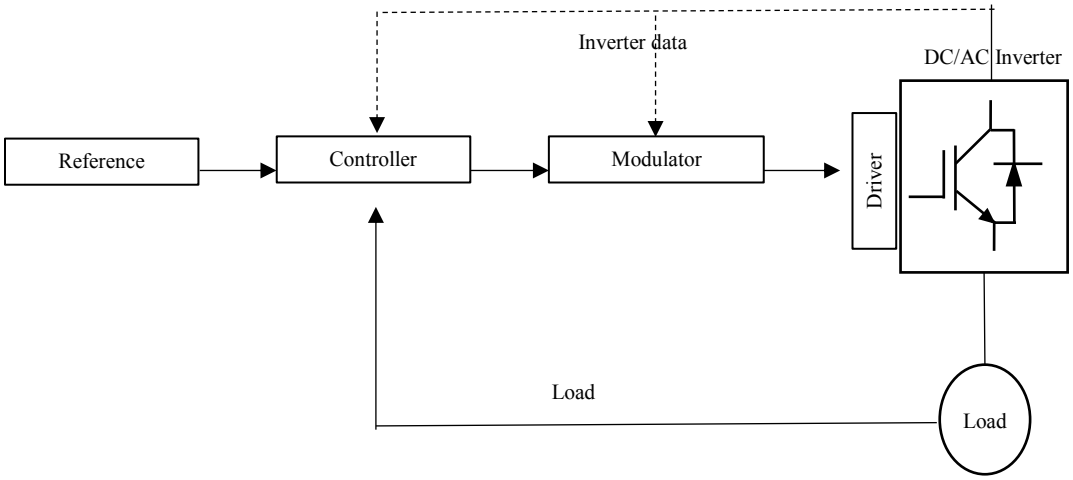



**Figure1.12** Close loop control and modulation

To overcome the drawbacks of the open loop controllers, close controller has been introduced. In this case main objective of the controller is to track one or combination of references define by user or customer. It can be any variables in various electric application such as voltage current, torque, active power, reactive power, flux etc. The controller generates the reference for the modulator and it is usually the voltage reference, and modulator has to generate reference for next sampling time [91]. This modulation scheme become very common solution where customize phase, frequency and amplitude is required for robust performance of adjustable speed drive or any other applications. There are two control techniques are mainstream controller which are used proportional-integral (PI) controller in synchronous reference frame and proportional-resonant (PR) controller in stationary frames in applications of active harmonic filters [92].

In last one decade closed loop controllers have been emerged as a better option because these controllers offer close loop implicit modulator with in controller as shown in Fig 1.13. These controllers are termed as direct controller and conceptually simple for the digital implementation in the system to generate switching signal for the inverter as in direct consequence of the controller avoiding extra burden of modulator. During last decade these type of controller which itself works as a modulator has been successfully introduced to the industry level. For example hysteresis current control or direct torque current control comprises implicit modulation with in direct controller [93].

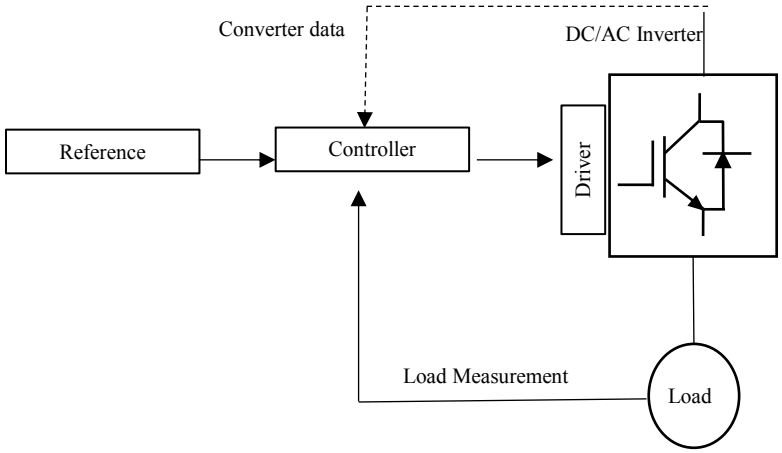



**Figure 1.13** Close loop control with implicit modulation

In modulation process of a power converters, due to instant switching pattern it might be chance of overlapping and short circuit in in the power converter so before final feeding of gate signal to the devices it is essential to insert a dead time to avoid the shoot through of inverter arms. The higher dynamic switching of inverter switches waiting time or dead time is necessary to sustain safe operation. The dead time cannot be exceeded by certain limit due to increment of non-negligible phenomena and low order harmonics in voltage/current if high power devices are used in high power systems. There are some methods have been proposed to insert dead time without its adverse effects [94].

The commonly used open loop and close loop modulation techniques for conventional inverters are extended for multilevel inverters. Some established modulation techniques still needs to be enhanced for different multilevel inverter topology [95][96].Usually controllers are designed to track a desired reference in any close loop control system to achieve some specified targets such

as reactive power compensation , active power control, dc-link voltage control, phase current balancing etc. by switching converter. The modulator generates a gate pulse in result inverter pertains desired switched average waveform over the sampling period. By use of duty cycle concept modulator has to generate switching sequence to properly switch the semiconductor devices. In the output voltage, harmonics spectrum evidences the undesired harmonics present due to high frequency switching. This is advocated by industrial and research societies that these undesired harmonics are required to be eliminated so this leads to the requirement of costly and bulky passive filters [97]. By adopting lower switching frequency and optimized design of harmonics filter for the system, the situation can be handled possibly.

Since controller and modulator plays an essential role and these are key element of power electronics system. Advanced control for open loop, close loop and close loop with implicit modulator is needed to implement either based on software or hardware prototype to check its reliability in term of processing time and cost. The prime challenges for a power electronics engineer are listed as following,

- The management of the input/output power, bidirectional flow, maintaining the better efficiency to satisfy the operational expectancy.
- Control operation and prototyping that offers high precision, flexibility, communication capability and reliability.
- Reduced complexity with corresponding reduced cost.

To achieve these expected functioning of a control unit in power electronics system in spite of disturbances and non-ideal conditions, a controller is required to interact between converter and load or grid on the basis of sampled measurement of input and output.

In early days evolution of control system consisting analog system was considered which possesses some disadvantages such as

- Passive component, large number of subsidiary parts in results lower reliability and increasing hardware complexity with required wider space.
- Limitation of the applicability of simple PI controllers and lower level of computation.
- The effect of aging, temperature dependency and maintenance.

- And the most important one it is not possible to reconfigure the controller without changing the hardware circuit.

However the analog controller are still having better bandwidth and rapidity in terms of presently growing alternatives for control systems. In the field of power electronics and drives, high performance of controller is essential due to involvement of complexity, high precision and short interval of control time. One of the optimal solution to overcome these issues, real time digital controller has been introduced in 1970s and become more attractive to power electronics. Digital controller allow user to implement complex control strategies with inherent algorithm and mathematical calculations. [98].

Growing interest for the real time digital controller to implement and made it applicable in power electronics and drives is due to, the tremendous advantages of digital controller over analogous one. Some leading advantages are flexibility, reduced design time and possibility to implement complex control in real time. Real time digitally controlled system can implemented using several technological methods, such as microcontrollers, digital signal processors (DSPs), field programmable gate array (FPGA), real time prototyping, programmable logic controllers(PLCs) etc. Among all these microcontrollers, DSPs and FPGA are used commonly due to their leading advantages for power electronics converters.

However the current DSPs offers higher integration rate and timing performance but it cannot achieve bandwidth of analog controller [99]. The primary reason is integration of these digital controller to analog environment with the use of interfaces such as analog to digitals (ADCs), and zero order hold circuits. Since these interface circuits introduces delay which is burden for the processors and reduces the bandwidth of the close loop control system by effecting computing time mainly [100].

It's evident that a digital controller can execute quasi-instantaneous control algorithm which is great advantage of cumulating both analog and digital controllers. In this process it leads to a third category of controllers the digital quasi-analog controller. FPGA emerges as a good candidate for these expectations in present time scenario [101]. FPGA accelerates the processing time of a control due to its ability to implement a specific architecture that is suitable for the salient features of the algorithm to implement [102].FPGA can be defined as matrix of configurable logic blocks

(combinational and/or logical) interconnected with each other with reprogrammable capabilities [103].FPGA based control design considerations can be summarized as shown in Fig.1.14.The possible ways of control design with FPGA can be easy for the control engineer who is not expert in the area of digital circuit design. Therefore it totally depend on the application engineer and there capabilities that which methodology to follow and more details can be found in [104].

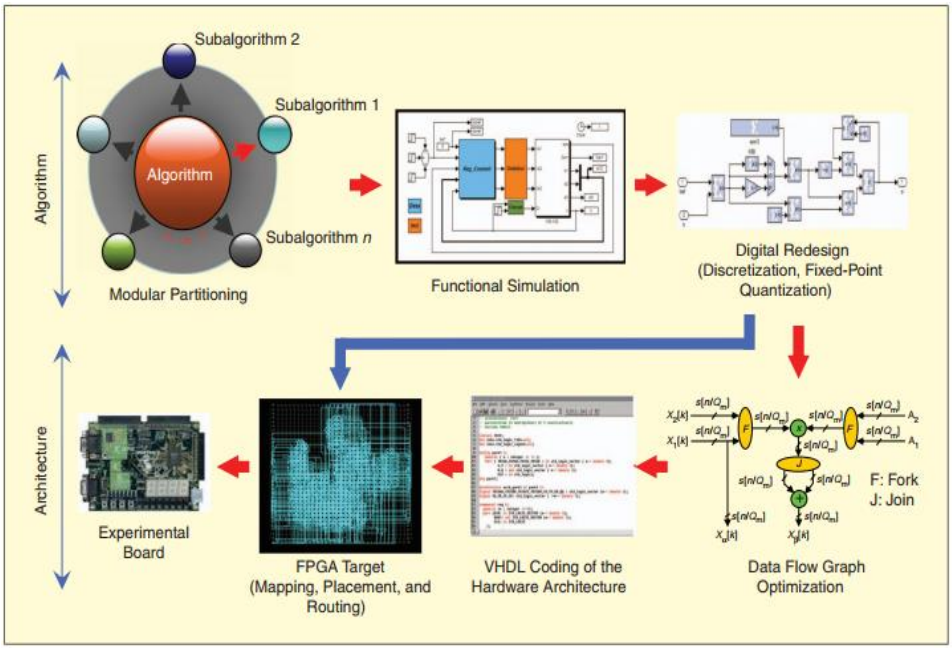



**Figure1.14**.Design methodologies for FPGA based real time implementation [104].

Some key steps to be taken by a control engineer to real time implementation of FPGA based control.

1. Validation of the synthesis of the controller in time continuous mode via MATLAB Simulink.
2. Designing of the system on digital platform with fixed point simulation and it crucial because it includes digital realization of filter, sampling time fixation, some modifications have be done to make it less complex in[104].
3. Optimizing the data flow graph of the control algorithm to get the balance in terms of time and area performances.
4. To generate or obtain a HDL code for the architecture.

5. To implementation on FPGA which is an automatic process to map, place and route design and analyze its dynamic and static performance.
6. At final step the controller validation can be done on experimental setup or using hardware in loop co-simulation.

With the growing development of advanced controller design and its testing in real time becomes essential for prior validation. Hardware co-simulation is method used by researcher and industrial processes in data acquisition, control strategies in large number of processes concerned with cost, safety and full scale prototyping. The real time FPGA based controller design requires knowledge and development of HDL. XSG provides a midlevel platform for implementing controller through co-simulation process. Its importance for the power electronics technology is to rapid testing of controller without expertness in HDL programming. The prototyping of controller can easily done using FPGA hardware co-simulation [105].

For the evaluation of the performance of controller an application based analysis is important. In this thesis three type of controller such as open loop control, close loop control and close loop control with implicit modulation are adopted in general. For open loop controller (LSPWM and PSPWM) a linear inductive load is connected to CHMLI, for close loop high performance control system(LCL filter interfaced system) is developed for CHMLI based DSTATCOM and close loop control with implicit modulation ( digital multiband HCC) is performed on single phases grid connected CHMLI system. All of these applications are significant in present day's electricity usage and efficiency should be improved to tackle the energy issues. Before concluding the introduction part of the thesis it is essential to focus some light on literature review of available DSTATCOM.

As power converters adequately offers highly capable and efficient electrical energy flow in a close loop system for any application such as DSTATCOM, motor drive, industrial processes and electric vehicles. Adding more application of power electronics converters in a low, medium and high power system including renewable energy integration, distribution generation etc.

Now a days consumption of power concerns with the reactive load such as fan, pumps, etc. These loads requires and force the grid to draw lagging power factor currents and in results grid had to supply reactive power to the different loads. Condition of unbalanced load may worsens the

situation. In other hand in very poor power factor load condition, excessive reactive power need to be supplied from the grid which causes feeder losses and reduced active power supply capability of the grid. The grid including transformers and generator affected by these reactive and unbalanced load. Distribution static compensator (DSTATCOM) emerges as good option as a compensator at distribution level.

DSTATCOM comprises the voltage source inverters and the close loop controller to aid the required operation. The important attempts to controller design with the topology manipulation has been done for the DSTATCOMs. Two level inverters based DSTATCOM has become very common in the last twenty years .Moreover DSTATCOM performance depends on the control technique applied, there are many control techniques available for these system control such as instantaneous reactive power theory (IRPT), synchronous reference theory (SRFT), current control techniques combined with dc bus voltage regulation, power balance theory [106], computation based on per phase, neural network scheme [107]. Apart from the control method in DSTATCOM application the topology variation has been attempted for inverter. By designing and control of a multilevel inverter based DSTATCOM the improved and transformer less system has been utilized .CHMLI has been used for this application in mainstream technology. Many attempts by the improved control, improved filter size, dynamic controller with implicit modulator has been proposed for the multilevel inverter based DSTATCOM [108].

Since it's difficult to connect conventional inverter based DSTATCOMs to the utility grid or medium voltage system, due to high power stress on single power devices. CHMLI which consists H-bridge modules have gained more attention among all available topology of multilevel inverter. It possess some disadvantage such as balancing dc bus voltage at each H-bridge cell to get a proper operation of DSTATCOM. The basic objective of the multilevel inverter based DSTATCOM is to force the grid to supply only active component of power and remaining current responsible for the reactive power or unbalancing of load are supplied by the DSTATCOM system [109]. Some of the leading benefits of using multilevel inverter are lower operating switching frequency, smaller filter size, lower electromagnetic interference, low power stress on devices, lower acoustic noise.

The ultimate use of multilevel inverters in a DSTATCOM system is an elimination of transformer from the system. Also it is noticed that these topologies offers better dynamic behavior in continuous control, in results reduces the power quality problems .Application of CHMLI for the

distribution system has been proposed and discussed in [110].In all the prosed work it is advocated that assumption of source stiffness, it means the voltage at the common coupling point (PCC) must be regulated and kept fluctuation less despite of variation in the load or current injected by the shunt device. However in practical applications it not possible because these shunt devices inject some circulating currents to the grid and affects the supply in certain points. If the stiffness of the grid is kept by increasing impedance of the supply side in result degraded performance of the DSTATCOM is possible [111-112].

The complete literature review consisting energy and electricity, future scenario, role of power electronics in 21$^{st}$ century, modern power electronics converters, and essential role of modulation, control system, digital real time control and FPGA technology is carried out in this dissertation. Some key issues which has been noticed and focused for the presented work in this thesis.

- In an electrical system, it is required to control the voltage, current, power, frequency, from generation end to user end.
- To achieve environment friendly electrical energy conversion system for the better future for power systems and sustainability. Power electronics technology emerges as adequate option and spread to every corner of growing technology. For operation and control of electrical power conversion, there is need of special attention and rigorous attempts to be made.
- As growing demand of electrical energy persuaded the use of non-conventional energy sources. The renewable energy generation has become one of the suitable option to fulfill the demand of electric power. But it is important to note that renewable energy sources generates electrical power with different electrical characteristics.
- Grid tied power electronics converters are needed to match the electrical characteristics of generated power and grid. Also an optimized design of filter is required for high frequency ripple attenuation.
- Grid integration in medium voltage high power application involves transformers to achieve certain voltage and power ratings.
- There are two option to achieve high power application either to develop high voltage devices or to develop high voltage application of available medium voltage devices.

- For medium voltage high power application multilevel inverters is used as transformer less interfaced connection due to their high current rating and reduced stress on devices.
- Multilevel inverters topologies involves higher number of components to achieve toggled output between different levels. For better performance in a close loop system one need to have a proper control and modulation of MLI.
- Modulation techniques for the conventional inverter is developed and performed the task quite successfully at industrial level. However in case of multilevel inverter there is still lot of attempts to be made for enhanced switching control of MLIs.
- Close loop controllers with implicit modulators are new category of controller applied to conventional converter. Hysteresis current control for voltage source inverter is accepted for drive application and power quality improvements. Development of hysteresis current controller for multilevel inverters are still has broad scope of improvement.
- Implementation of controllers in digital platform has several advantages however control and application is still in the growing phase.
- FPGA based control for real time implementation involves rigorous programming skill and complex high level synthesis process.
- In application of grid connected MLI, problem of harmonics at different frequency (switching) level occurs, which has to be monitored and enhanced for lower switching frequency operation with improved bandwidth.

### 1.3 Objectives

All the issue noticed in the above list are somehow critical issues with present electrical energy conversion systems. In this dissertation some key contribution to issues which are taken in to account and objectives of the research presented are as follows,

Grid tied cascaded H-bridge multilevel inverter is considered which possess some adequate advantages such as, modularity, reliability, fault tolerant capability. Transformer less integration of CHMLI to the grid, which allows low electromagnetic interference in close loop operation.

The main focus of the dissertation is to develop high performance digital control system for grid tied CHMLI. The key proposals are filter design for lower switching frequency operation and digital controller with implicit modulator for grid connected CHMLI.

To develop a basic controller based on open loop SPWM control of five, seven, and nine level CHMLI and its digital implementation using FPGA based digital controller. It would be essential to investigate compare and analyze the performance of available control techniques.

In addition, to investigate the performance of third harmonics injected PWM (THIPWM) which possess the advantage of improved dc bus utilization, extended linear and over modulated operation for conventional inverters. FPGA hardware co-simulation is proposed for rapid controller prototyping of CHMLI. It offers rapid and cost effective tool for validation of controller design prior to real time implementation on system plant.

A design of LCL filter considering modified constraints for the lower switching frequency operation of proposed LCL filter interfaced DSTATCOM. Combination of CHMLI and LCL filter pertains improved dynamics for the DSTATCOM. Also analyzing the system performance with respect to voltage sag-swell, dc voltage ripple, switching frequency variation and dynamics of grid system.

A novel digital multiband HCC is proposed for grid tied CHMLI. Design and control of grid connected CHMLI based on simulation and experimental system for performance evaluation of proposed digital controller. Then the digital multiband HCC is proposed for DSTATCOM system. The comparison of digital multiband HCC with SPWM techniques with conventional linear controller.

## 1.4 Organization of Dissertation

This dissertation contains six chapters, first chapter focusing on the energy and electricity demand by different countries in present and future scenario, role of power electronics in the present electrical energy conversion system. Also it includes literature review for the presented work that includes multilevel inverters, modulation techniques, power grid issues and the available solutions to those issues.

Chapter 2 focuses on the basic operation of the cascaded H-bridge multilevel inverter connected to simple linear load. The study aims to have proper understanding of conventional open loop control techniques such level shifted and phase shifted carrier based PWM. Digital control for phase shifted and level shifted carrier based modulation is investigated on a FPGA based open

loop system. And FPGA hardware-in-loop co-simulation is proposed for controller prototyping of CHMLI. Level shifted and phase shifted carrier based THIPWM technique is used for controller prototyping. Mathematical analysis of THIPWM control is investigated for improved dc bus voltage utilization, extension of linearity range and compared with co-simulation results.

In chapter 3, LCL filter interfaced cascade H-bridge inverter based DSTATCOM is proposed and its performance is analyzed with varying system parameters. Designing based on modified constraints of LCL filter for lower frequency operation of CHMLI is carried out. For improved performance evaluation of the DSTATCOM system, abnormalities such as voltage disturbance and unbalanced, non-linear loads are considered.

In chapter 4, digital multiband HCC is proposed for CHMLI, performance evaluation of multiband HCC is investigated on simulation. Prototype of the grid connected CHMLI system is developed and FPGA based real time control of is presented with supporting experimental results.

Chapter 5 focuses on the digital multiband HCC for DSTATCOM application. Comparison of linear control techniques such as PI controller with level shifted and phase shifted PWM and hysteresis current control is carried out for the DSTATCOM system. Leading advantages of multiband hysteresis current controller over linear controller under load abnormalities are demonstrated.

Chapter 6, this chapter concludes the work presented in whole dissertation, summarizes the work and leads to the future possibilities in the ongoing research.

# CHAPTER 2

## Cascaded H-bridge Multilevel Inverter and FPGA Hardware Co-Simulation

### 2.1 General

Multilevel inverters (MLIs) are progressing and evaluating topologies of voltage source inverters (dc-ac converters) family. These topologies provide a cost effective solution in the medium-voltage high power energy management market. MLIs have been employed in wide application such as chemical, oil, liquefied natural gas plants, hydro plants, marine propulsion, power generation, energy transmission, renewable energy integration, utility grid and power quality improvement system such as FACTs devices.

Now a days three topologies of MLIs have been commercially accepted and utilized to provide better solution for electrical energy at the level of transmission and distribution: Neutral point clamped (NPC), flying capacitor and cascaded H-bridge. Apart from these topologies some hybrid topologies or cascaded topologies have been evaluated and proposed in some recent patents but still needs wider and comprehensive research to elaborate its efficiency enhancement. Among three common commercialized topologies, cascaded H-bridge multilevel inverter (CHMLI) has reached higher output voltage and power (13.8kv, 30MVA) with sustaining higher reliability due to its modular structure. CHMLI is basically comprises a cascaded or series connection of several single-phase voltage source inverter i.e. H-bridge cells containing four semiconductor devices. This structure has advantage of reaching higher level of voltage and power utilizing standard low voltage technology component. In practical, number of H-bridge cells connected in cascade is decided by voltage rating, cost and required efficiency. For example in a medium voltage (MV) drives with a rated line to line voltage of 3300 V a nine level inverter can be made applicable where the three phase system consist of 12 H-bridge cells each consisting 4 power switches (semiconductor devices) and generally for three phase system it is necessary to connect three to nine single phase inverters to attain the required synthesized output voltage with optimized efficiency. CHMLI offers a feature of high modularity degree because each inverter can be operated as a module with identical circuit topology, control structure, dc supply/capacitor and modulation.

With this tremendous feature CHMLI offers a fault tolerant nature, explaining it as case of fault in one of the module it might be possible to replace or repair it quickly without disturbing the whole inverter unit. Therefore it also possible if a robust control is applied to avoid or bypass the fault effect module without interruption of load supply, this enables the almost continuous availability. As it comprises multiple units of H-bridges cells and H-bridges are normally connected in cascade on their ac sides to achieve medium voltage by summing the voltage of each cells. Cascade connection of H-bridges also offers the selectivity of dc bus voltage and low harmonic distortion in output voltage. Also utilizing an identical H-bridge cells leads to a modular structure, which is very effective in term of cost reduction and sustainability.

The CHMLIs requires a separate isolated dc supplies for each bridge cell, each of dc supply feeds an H-bridge cell and contribute to achieve stepped high level of ac output voltage. The isolated dc supplies mainly obtained from diode rectifiers or capacitor dc bus used in some application such as active power filter, DSTATCOM etc. For instance nine level and seven level inverters can be fed by 24 pulsed or 18 pulsed diode rectifies respectively to attain high input power factor and low line current harmonic distortion.

In this chapter, the cascaded H-bridge multilevel inverter is comprehensively discussed from basic H-bridge cell to the building a three phase CHMLI. For the operation and control of CHMLI phase shifted and level shifted carrier based sinusoidal pulse width modulation (SPWM) is selected. The digital control is implemented for the cascaded H-bridge multilevel inverter using Xilinx system generator based simulation in Matlab and programming of FPGA is done using Vivado software. The SPWM techniques can be modified to third harmonics injected PWM (THIPWM) for CHMLI. FPGA hardware-in-loop co-simulation is proposed for controller prototyping of the THIPWM controlled CHMLI. Mathematical and co-simulation results are compared for phase shifted and level shifted THIPWM.

## 2.2 H-bridge Inverter

A simplified single phase H-bridge inverter is shown in Fig 2.1.It consists two inverter legs with two power semiconductor devices (IGBT) in each leg. The inverter dc bus voltage is at each bridge, $V_{dc}$ is normally fixed except in some special application. An ac output voltage can be manipulated or adjusted by modulation methods applied. Pulse width modulation (PWM) is commonly used for the power electronics converters.

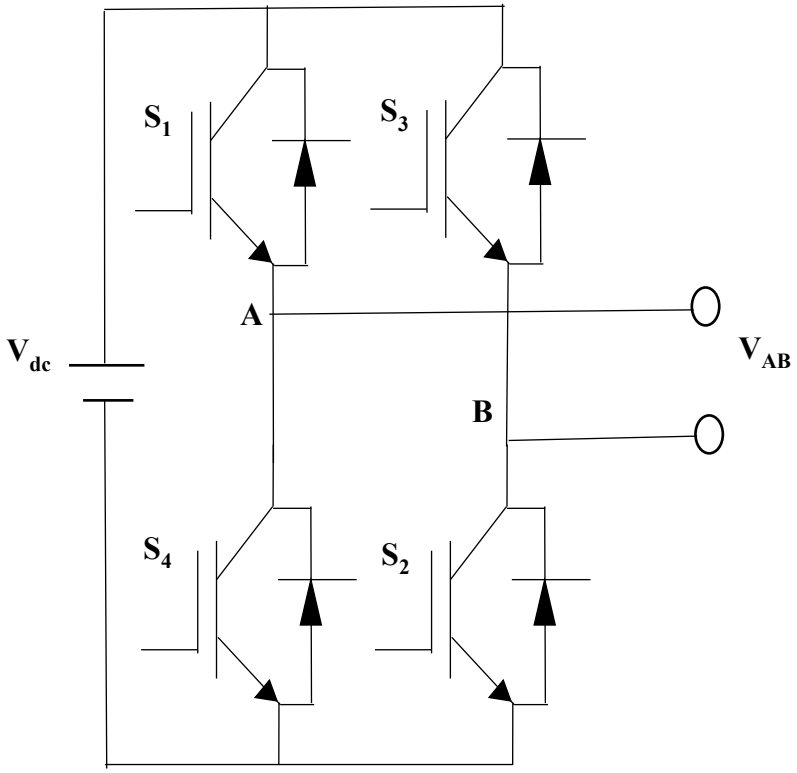



**Figure 2.1** Single phase H-bridge inverter

In case of H-bridge inverter it can be classified as bipolar and unipolar modulation schemes.

### 2.2.1 Bipolar Pulse Width Modulation

As shown in Fig 2.1 the H-bridge cell consists four switches $S_1$, $S_2$, $S_3$, $S_4$ and the required gate signal can be generated by carrier based PWM techniques. In this section bipolar pulse width modulation for H-bridge inverter is discussed. As shown in Fig. 2.2 the typical wave form for bipolar PWM where $X_M$ is modulating wave, $X_{CR}$ is carrier (triangular) wave and $X_{G1}$ and $X_{G3}$ are the gate signals for the primary (upper) switches $S_1$, $S_3$ respectively. The upper and lower switches in same leg operate in complementary manner which means one switch is turned off when other is turn on. This enables the easiness of considering only two gate signals for the H-bridge inverter by comparing modulating wave and triangular carrier wave. The voltage at point A and B in mid-point of two legs are $v_A$ , $v_B$ can be derived by applying bipolar modulation, inverter ac output can be written as potential difference between these two point A and B, $v_A - v_B = v_{AB}$ .It is evident that potential difference or ac output voltage toggles between positive and negative voltage i.e. $\pm V_{dc}$

and this is the main reason for which it is called bipolar modulation. The switching frequency of the IGBT devices is called as operating switching frequency of H-bridge inverter which is equal to carrier frequency $f_{cr}$ .Modulation index can be defines as ratio of magnitude of modulating signal to magnitude of carrier wave m= | $X_M$| / |$X_{CR}$|.

### 2.2.2 Unipolar Pulse Width Modulation

Unipolar modulation for H-bridge inverter requires two reference wave which are having identical magnitude and frequency but shifted by 180 degrees in phase. As shown in Fig 2.3 two modulating waves $X_M$ and $X`_M$ are compared with a single common carrier wave $X_{CR}$ and generation of two gate signal for the primary switches of H-bridge inverter. Similar to bipolar modulation, in unipolar modulation, gate signal are provided to the complementary switches by inverting primary gate signal. It is evident from figure that two primary switches do not switch simultaneously, which is different from the bipolar modulation where all four switches are switching at the same time. The output voltage of the inverter $v_{AB}$ toggles between $+V_{dc}$ and 0 during positive half cycle and 0 and $-V_{dc}$ during negative half cycle of the fundamental period/frequency. Thus technique is called as unipolar pulse width modulation.

Similar to bipolar modulation switching frequency of IGBT devices is termed as switching frequency of H-bridge inverter which is equal to the frequency of carrier wave. The unipolar pulse width modulation can be implemented by using one modulating wave and two carrier wave. The condition which should be followed is, these carrier wave should be 180 degree out of phase. This modulation technique is frequently used for the Cascaded H-bridge multilevel inverters.

## 2.3 Cascaded H-bridge Multilevel Inverter

The basic structure of three phase star connected cascaded H-bridge inverter it can be implemented by simply cascading H-bridge cells as shown in Fig. 2.4.Each H-bridge cell is fed by dc link voltage to generate a switched output voltage at output terminal. Total output voltage of a cascaded H-bridge inverter can be obtained by adding an output voltage of individual H-bridges. Each H-bridge is capable of generating three level of output voltage e.g. if $V_{dc}$ is dc voltage connected to H-bridge then generated output voltage would be + $V_{dc}$, 0,-$V_{dc}$ .The generalized equations that relate dc voltage and ac output voltage is derived in Eq.(2.1) to (2.4). In case of multilevel CHMLI,

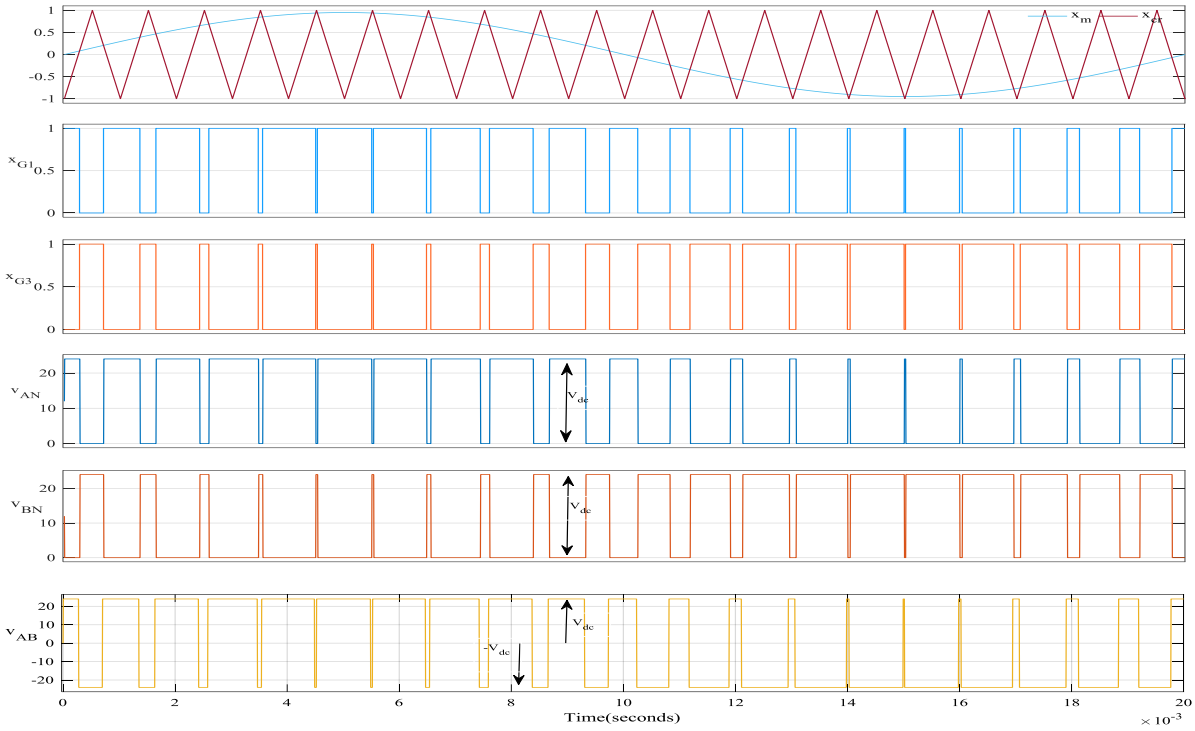



**Figure 2.2** Bipolar modulation of H-bridge inverter.

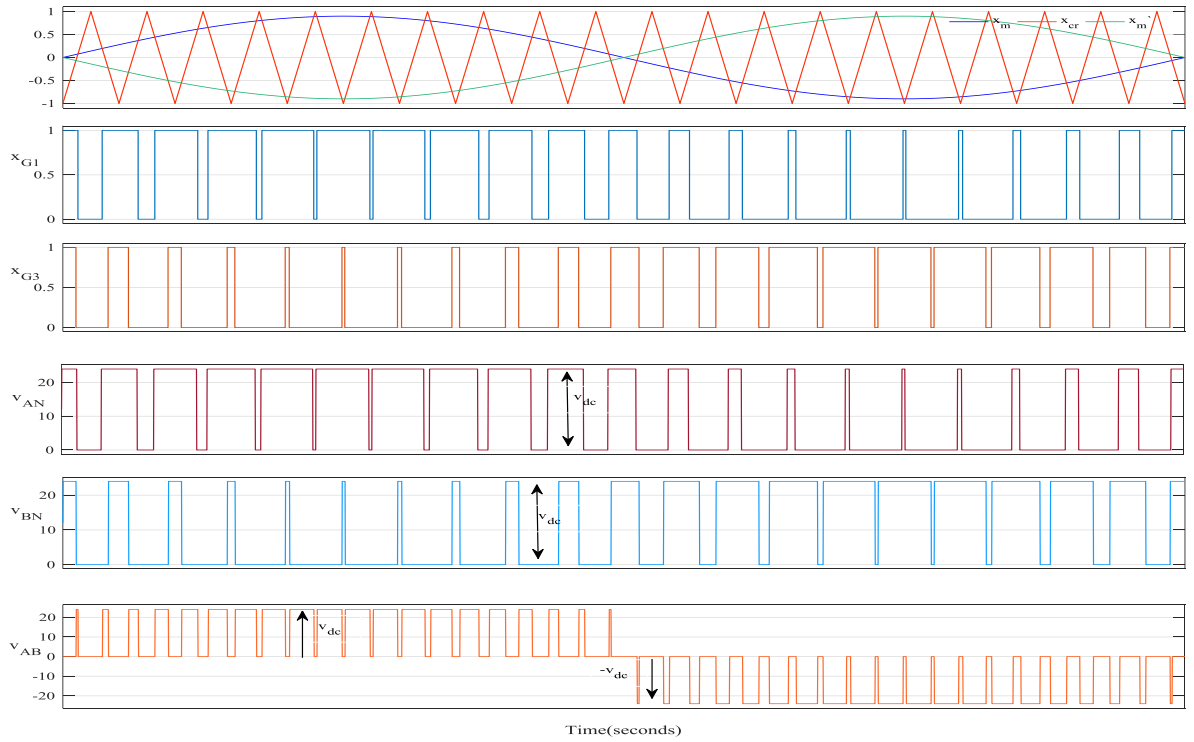



**Figure 2.3** Unipolar modulation of H-bridge inverter.

increased level of inverters has linear relation with the required number of H-bridge cells and dc sources/capacitors for implementation of the system . However it is not the case with the output voltage quality, the improvement in the quality of synthesized output voltage does not follow the linear relation and there will not be a considerable improvement corresponding to the increased levels, therefore five to nine level inverters are predominantly used for the medium voltage high power systems.

The peak value of the output voltage per phase for n H-bridges connected in one phase can be written as:

$$V_a = V_{adc1} + V_{adc2} + \ldots + V_{adc[n-1]} + V_{adcn} \quad (2.1)$$

By assuming that each of the H-bridges has an equal DC bus voltage, i.e., $V_{adc1} = V_{adc2} = \ldots = V_{adc[n-1]} = V_{adcn} = V_{dc}$.

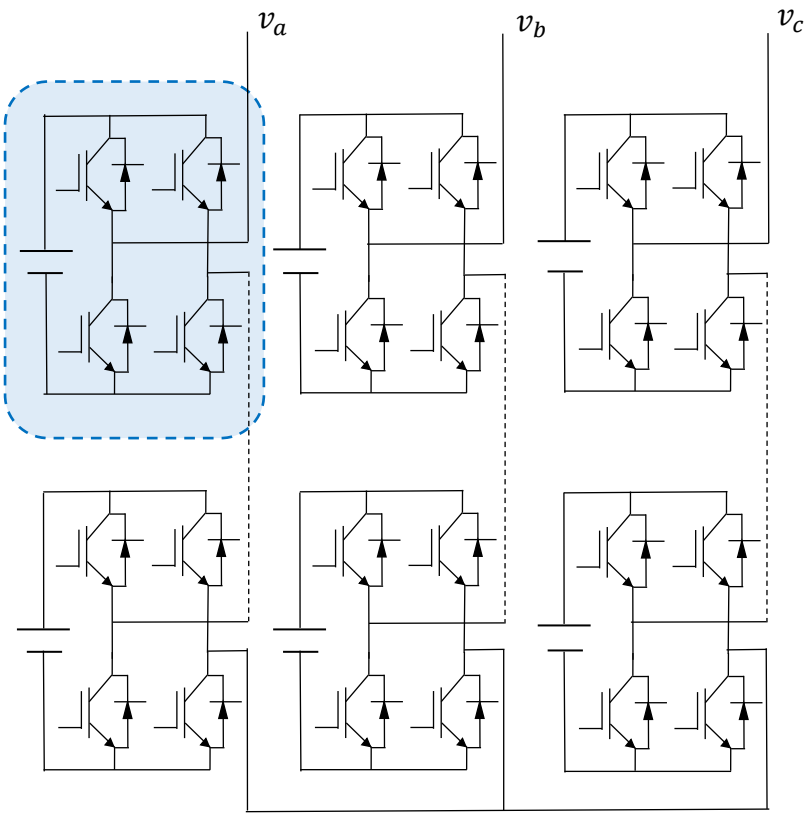



**Figure** 2.4 Three phase CHMLI topology.

The output voltage of the CHBMLI is also written as:

$$V_A(\omega t) = \sum_{m=1}^{m=\infty} f(x,m)(\sin\ m\omega t) \tag{2.2}$$

Where,

$$f(x,m) = \frac{4V_{\mathrm{dc}}}{m\pi} \sum_{k=1}^{n} (a_m \cos m\alpha_k) \tag{2.3}$$

It is necessary for the switching angles to be restricted such that:

$$\frac{\pi}{2} > \alpha_m > \ldots\ldots \alpha_2 > \alpha_1 \tag{2.4}$$

For the increment of level the number of H-bridges connected in cascade can be increased, in a single phase CHMLI normally n number of H-bridges connected in cascade will generate 2n+1 levels in output voltage if symmetrical topology is considered it means identical dc supply is connected to the H-bridges. The requirement of isolated dc supply is usually fulfilled by three phase or single phase rectifiers. For simplicity identical isolated dc supply is used however in some cases where active power from the inverter is not required such as each dc supply of active power filter can be floating and control strategy maintains the balanced dc voltage with respect to reference.

For generation of five level output voltage from symmetrical ($V_{dc1} = V_{dc2} = V_{dc}$) CHMLI two H-bridges are connected in cascade supplying a linear load (R+jL) as shown in Fig.2.5.The operation and quality of output voltage and current depends on the modulation control applied to it. The CHMLI can generate voltage output with five levels when two H-bridges are connected in cascade. The switching operation and control is done in way to cumulate the output voltage of two H-bridges for example, switches $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ are on/conduct the output voltage of each H-bridge cell is $v_{H1} = v_{H1} = V_{dc}$ and net output voltage of the five level CHMLI is $v_{out} = v_{H1} + v_{H1} = 2V_{dc}$ . In same way when S13, S14, S23, S24 is on/conducting the cumulative output voltage at output terminal is -2Vdc.Various combinations of switching can be done to achieve different level of output.

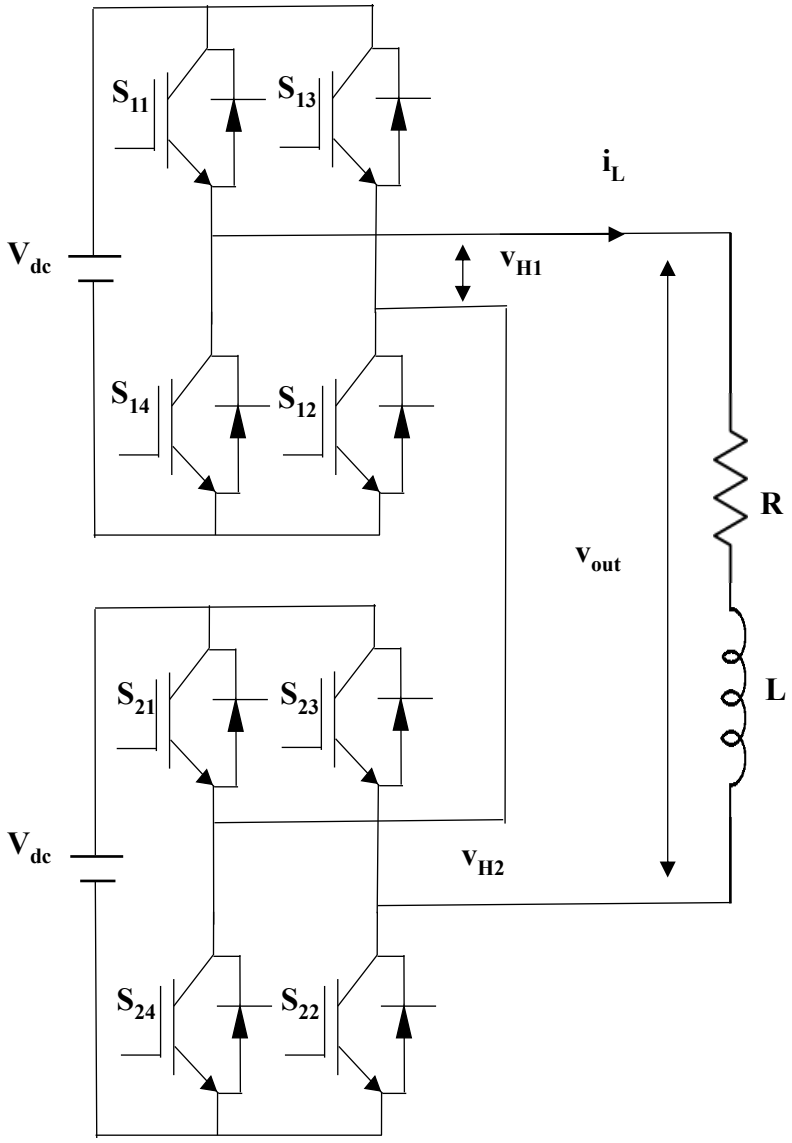



**Fig.2.5** Single phase five level inverter connected to linear load

By deriving a switching table for the different states of switches it is observed that different voltage levels can be obtained at different switching states. For example four set of different switching state generate the voltage level of $V_{dc}$. With this modular topology it is enabled for modulation pattern that can deploy higher flexibility. In table 1 only primary switches of two bridges has been considered, rest of complementary devices are switched by providing corresponding inverted signals.

**Table 2.1 Voltage level and switching state of single phase five level inverter**

| $S_{11}$ | $S_{13}$ | $S_{21}$ | $S_{23}$ | $v_{H1}$ | $v_{H1}$ | $v_{out}$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | $V_{dc}$ | $V_{dc}$ | $2V_{dc}$ |
| 1 | 0 | 1 | 1 | $V_{dc}$ | 0 | $V_{dc}$ |
| 1 | 0 | 0 | 0 | $V_{dc}$ | 0 | $V_{dc}$ |
| 1 | 1 | 1 | 0 | 0 | $V_{dc}$ | $V_{dc}$ |
| 0 | 0 | 1 | 0 | 0 | $V_{dc}$ | $V_{dc}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | $V_{dc}$ | $-V_{dc}$ | 0 |
| 0 | 1 | 1 | 0 | $-V_{dc}$ | $V_{dc}$ | 0 |
| 0 | 1 | 1 | 1 | $-V_{dc}$ | 0 | $-V_{dc}$ |
| 0 | 1 | 0 | 0 | $-V_{dc}$ | 0 | $-V_{dc}$ |
| 1 | 1 | 0 | 1 | 0 | $-V_{dc}$ | $-V_{dc}$ |
| 0 | 0 | 0 | 1 | 0 | $-V_{dc}$ | $-V_{dc}$ |
| 0 | 1 | 0 | 1 | $-V_{dc}$ | $-V_{dc}$ | $-2\ V_{dc}$ |

## 2.4 Experimental evaluation: FPGA based digital control

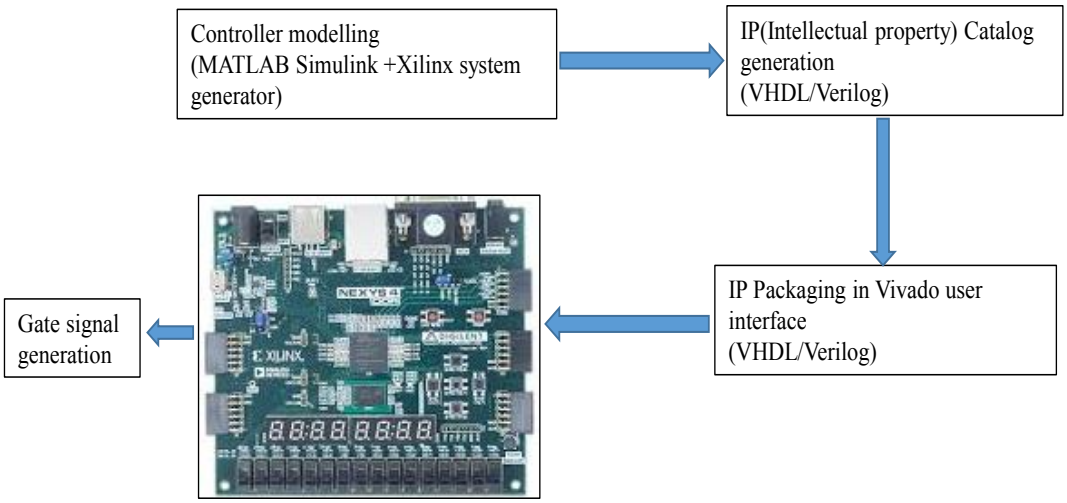



**Figure 2.6** Methodology of digital control based on FPGA

Before proceeding to evaluation of performance for five, seven and nine level inverters based on simulation and experimental results, it is essential to explain the FPGA based digital control methodology as shown in Fig2.6. In this study phase shifted and level shifted carrier based switching controls are investigated and supported by simulation and experimental results.

### 2.4.1 Xilinx system generator based simulation

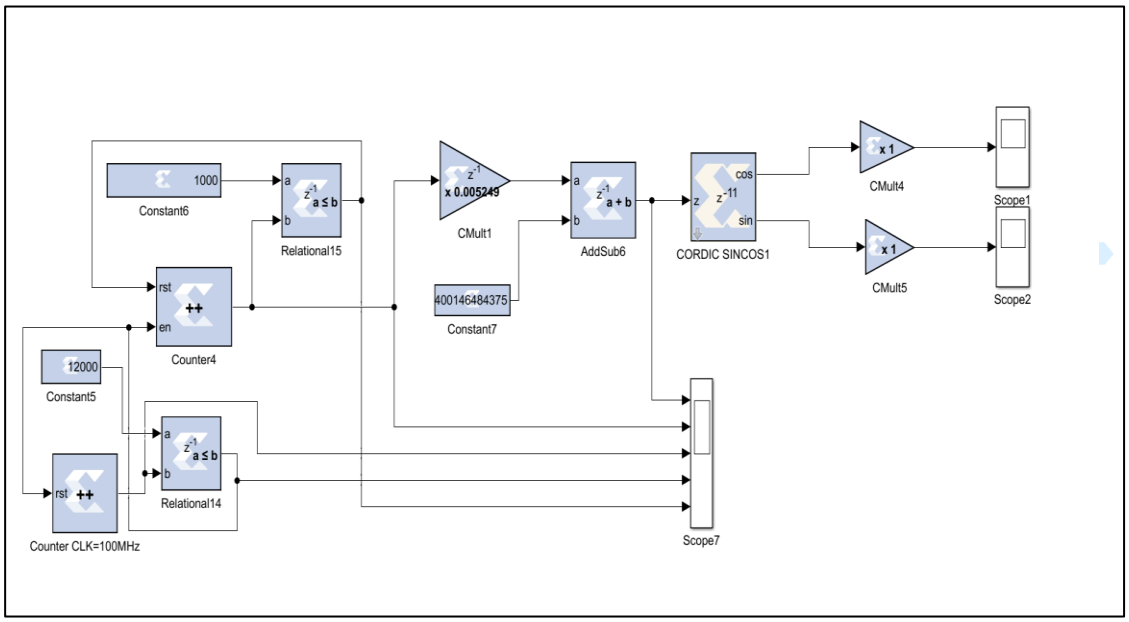



**Figure 2.7** XSG block set based modulating wave (sinusoidal wave) generation in simulink.

For the digital control of CHMLI, Xilinx system generator (XSG) based simulation is done followed by real time simulation. XSG enable the application of special category of block set in simulink and it can generate HDL code based intellectual property (IP) catalog. IP catalogs generated by user is called as user defined IP blocks, Vivado software interface enables use of some commonly used application based IP blocks defined by software developers itself. User based IP catalogs consists HDL codes of control designed by user. As discussed in chapter 1, FPGA based digital control is adopted and required hierarchical steps has been taken to follow high level synthesis and bits stream generations. Nexys 4 DDR FPGA board is used for the hardware based control and it possesses inbuilt high speed clock of frequency 100 MHz.

For the SPWM control of CHMLI it is desired to modelling and generation of modulating and carrier waves in simulation based on XSG block sets. For the FPGA with clock frequency of 100 MHz, frequency of modulating and carrier waves are normalized in XSG block set based simulation. For example the 50 Hz of fundamental frequency is normalized to $5\times10^{-7}$ Hz and carrier frequency of 1 KHz is normalized to $1\times10^{-5}$ Hz. Basic design and modeling of sinusoidal (modulating) and triangular (carrier) wave in XSG based simulation are shown in Fig.2.7 and Fig.2.8.

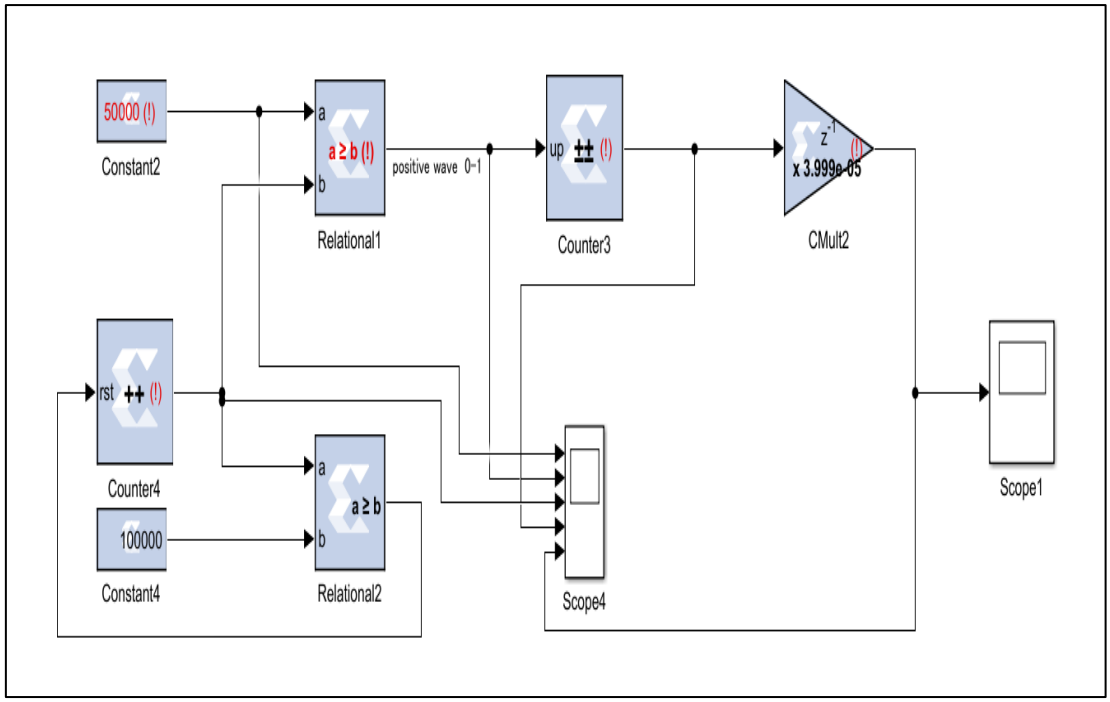



**Figure 2.8** XSG block set based carrier wave (triangular wave) generation in simulink.

## 2.5 Carrier based pulse width modulation

Modulation technique to obtain synthesized output voltage of multilevel inverters are extended from the conventional modulation techniques used for two level inverters. Eventually it is essential to apply hierarchal switching for obtaining multileveled output voltage. There are many control techniques have been proposed in recent years for multilevel inverters such as linear and non-linear with and without implicit modulator. Commonly used SPWM techniques offers linear behavior of modulator with better input power factor.

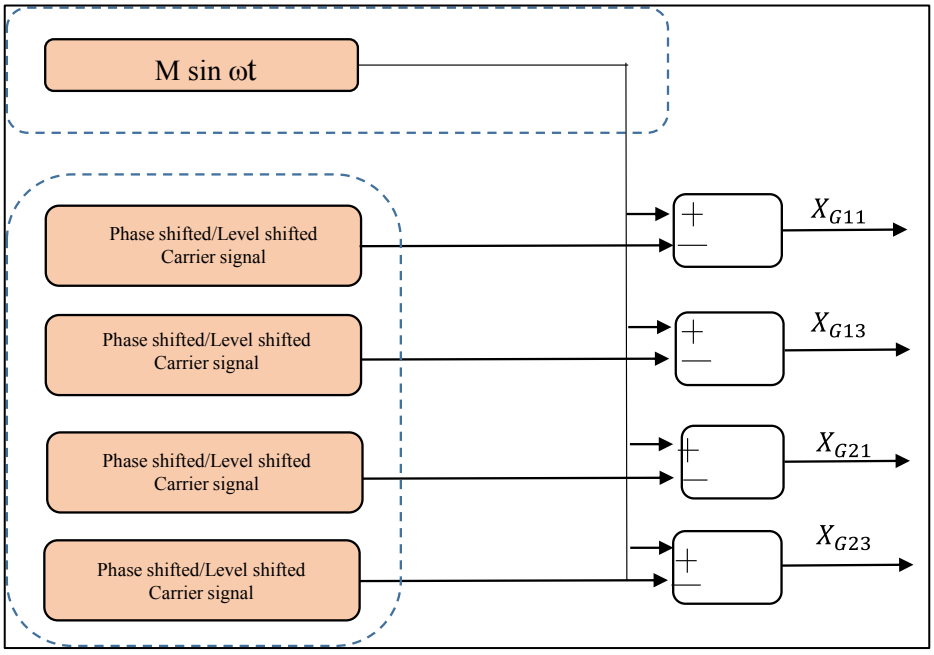



**Figure 2.9** Carrier based pulse width modulation for five level inverter

For the open loop control of five level inverter carrier based PWM is adopted and the control block diagram is shown in the Fig.2.9. For five level inverter four gates signals are generated for primary switches. In both cases either real time simulation or fixed point simulation based on XSG the triangular and sinusoidal waves are compared to generate required gate signals. For extended level of multilevel inverters the number of carrier eaves increases and correspondingly more number of gate signal can be generated.

Operation in open loop is simple so at first open loop operation of SPWM techniques are elaborated in this section. SPWM for CHMLI can be classified as, Phase shifted carrier based SPWM and Level shifted carrier based SPWM.

### 2.5.1 Phase shifted carrier based PWM technique

As name suggests phase shifted carrier based SPWM technique for multilevel inverter involves the comparison of modulating wave with the phase shifted carrier waves. Multiple carrier signal is utilized due to multiple gate signal requirement for CHMLI topology. To enhance and elaborate the performance of modulator, carrier wave is employed with the equal phase difference between two adjacent waves. In this techniques, for inverter with n level of output, number of carrier waves required for the modulation are (n-1). And phase difference between adjacent waves is calculated as follows,

$$\phi_{cr} = \frac{2\pi}{(n-1)}\ rad$$

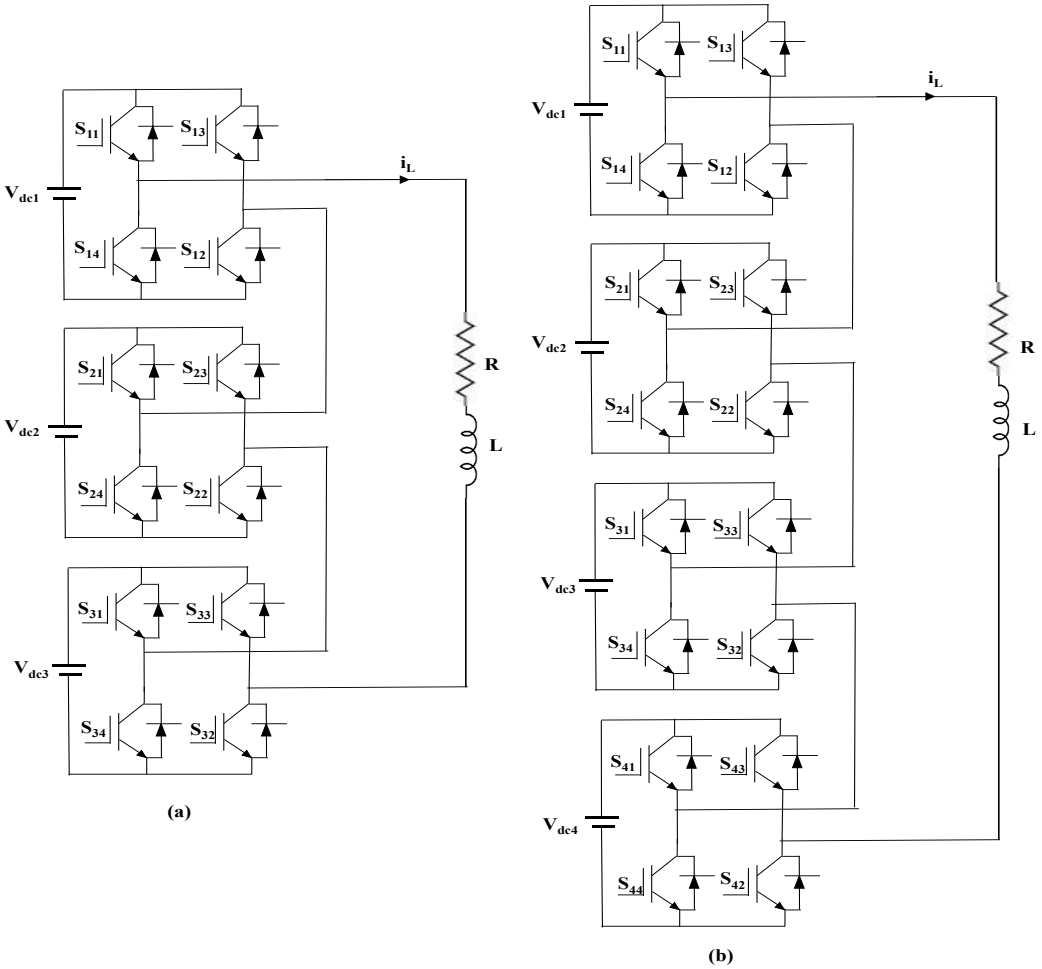



**Figure 2.10. (a)** Seven level **(b)** Nine level inverter connected to linear load

And all the carrier wave should have equal magnitude (peak to peak amplitude) and frequency. For three phase inverters modulating waves are generally sinusoidal waves with adjustable amplitude and fundamental frequency. Fig. 2.10(a) and (b) shows the single phase seven level and nine level inverter feeding linear inductive load.

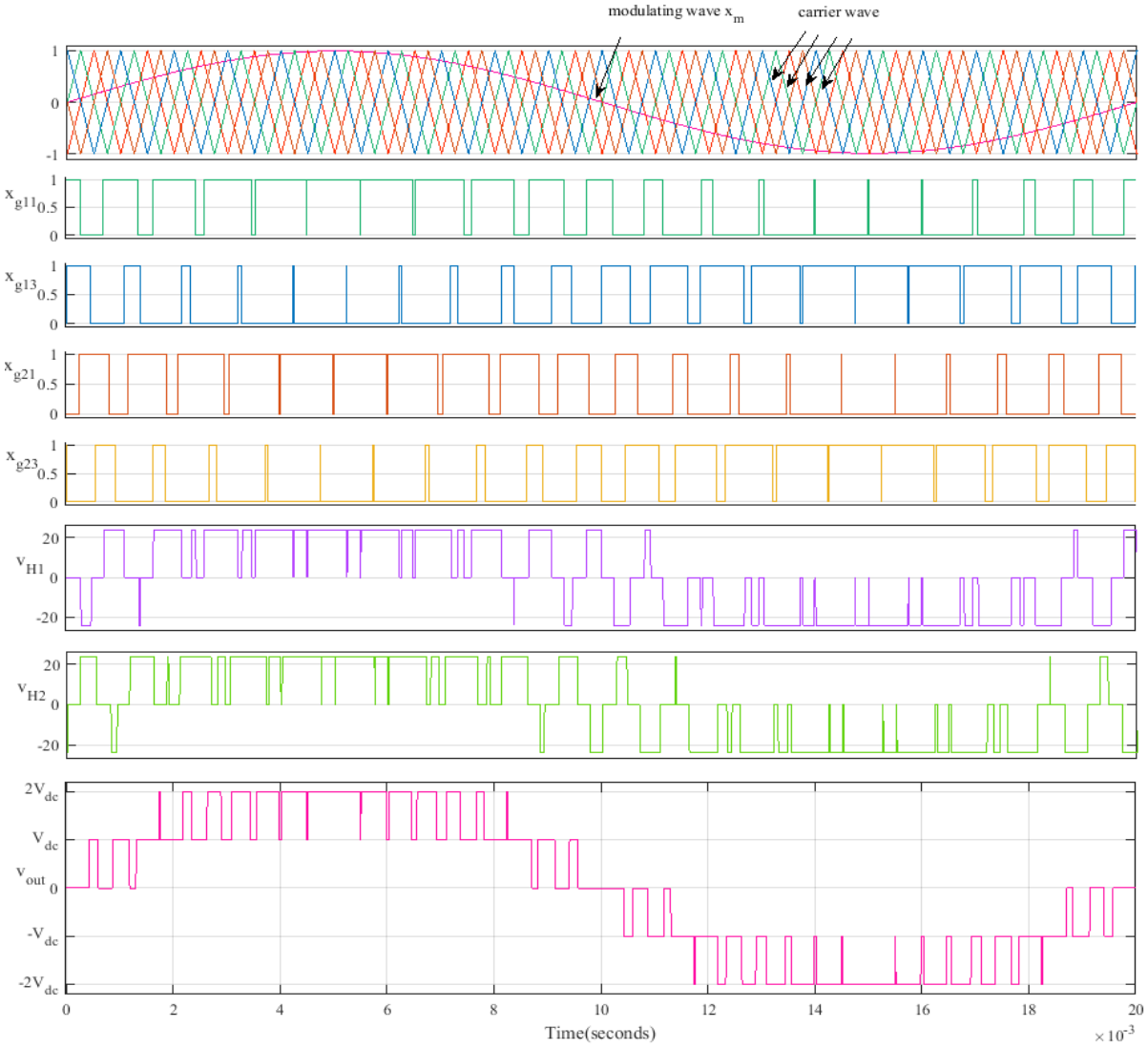



**Figure 2.11**. Phase shifter carrier based PWM for five level inverter

The circuit diagram of five level CHMLI is shown in Fig. 2.5 and considered for explaining the phase shifted carrier based SPWM. For five level inverter four carrier waves are required which are $\pi/2$ rad out of phase as shown in Fig. 2.11. These carrier are compared to the modulating signal having fundamental frequency of 50 Hz and amplitude of 0.98. The magnitude of the

modulating signal decides the modulation index (M) in this case. As we can see that four gate signals are required for four primary switches of five level inverter. The corresponding four gate signals $x_{g11}$, $x_{g13}$, $x_{g21}$, $x_{g23}$ are shown in the Fig. 2.11 for primary switches of two H-bridges of five level inverter. Output of each H-bridge is also shown in results as $v_{H1}$ and $v_{H2}$ which is switched and cumulate to generate five level inverter output voltage $v_{out}$ .

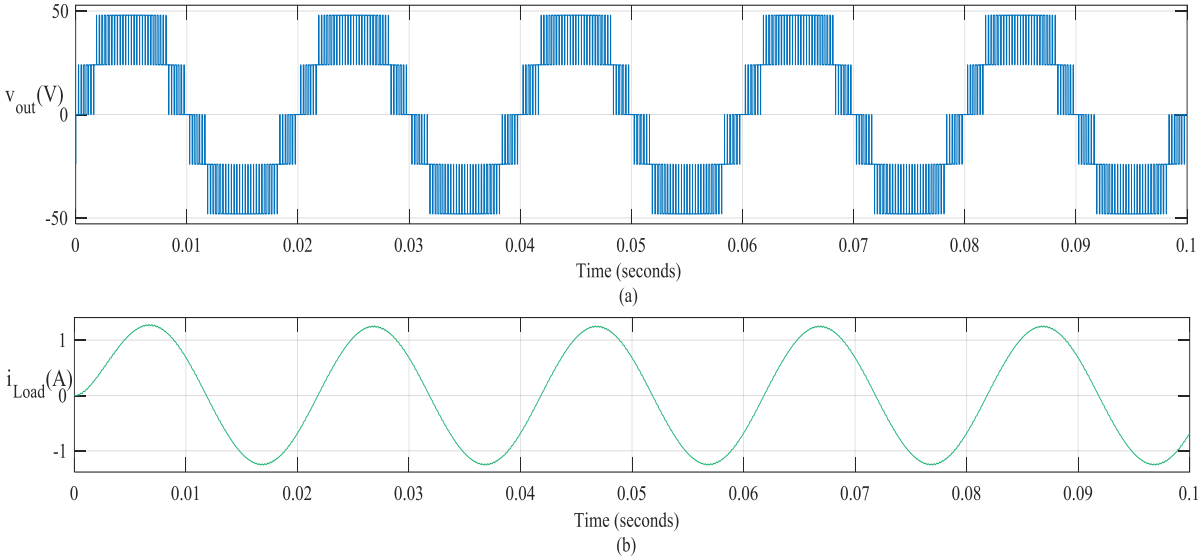



**Figure 2.12** (a) Phase shifted carrier based five level inverter output voltage, (b) load current.

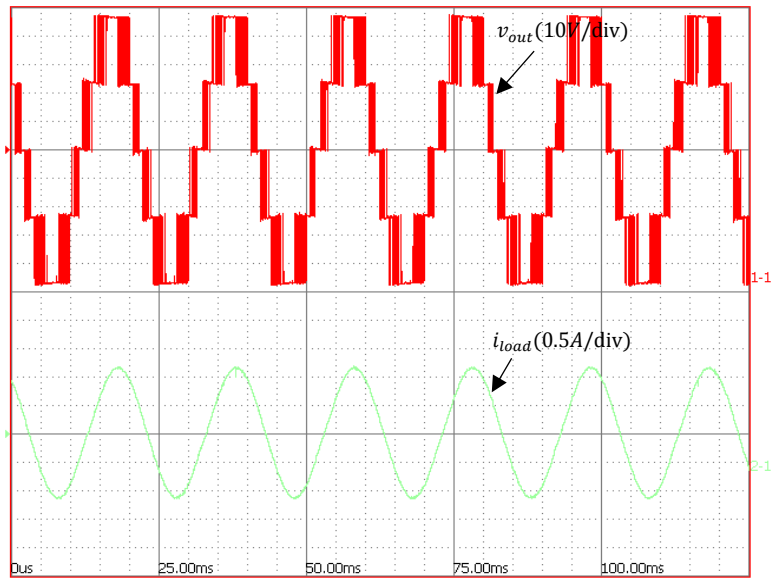



**Figure 2.12(c)** Experimental results of five level inverter for phase shifted PWM: output voltage and load current.

The wave forms shown in Figure 2.12(a) and (b) are output voltage of, multilevel inverter with corresponding load current. 24 V isolated dc supply is connected to each H-bridge cell and load of R=32 ohm and L=66mH is connected to CHMLI. Fundamental frequency of modulating wave is 50 Hz and switching frequency is maintained 4 kHz. It is observed that in phase shift modulation absolute switching frequency of inverter is equal to the switching frequency of one carrier wave multiplied by number of carrier wave required. In shown result the frequency of carrier signal is selected 1 kHz and absolute switching frequency for five level inverter is 1 × 4 kHz. Total harmonic distortion (THD) in output voltage is 25.02 % as shown in Fig. 2.13 through FFT analysis. Performance evaluation of five level inverter with phase shift carrier based modulation is elaborated by simulation as well as experimental results as shown in Fig 2.12(c).

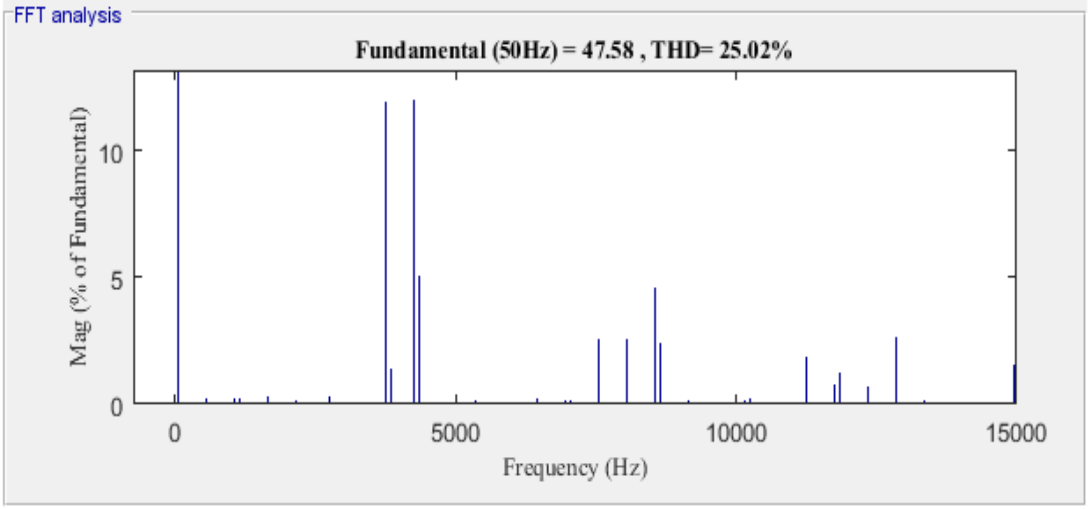



**Figure 2.13** FFT analysis of inverter output voltage.

The performance analysis of phase shifted carrier based PWM technique for seven and nine level inverter is presented in this section. As shown in Fig 2.10(a) seven level inverter consist of three H-bridges in cascade and three isolated dc supply of equal magnitude of 24 volts is fed to the inverter unit. The wave forms shown in Figure 2.14(a) and (b) are output voltage of, multilevel inverter with corresponding load current .The load is varied from five level because seven level inverter has increased voltage level therefore for maintaining nearly equal load current. This will ease the comparison of performance of CHMLI with the different levels of inverters. For seven level inverter 24 V isolated dc supply is connected to three H-bridge cells and load of R=44 ohm and L=100 mH is connected to CHMLI.

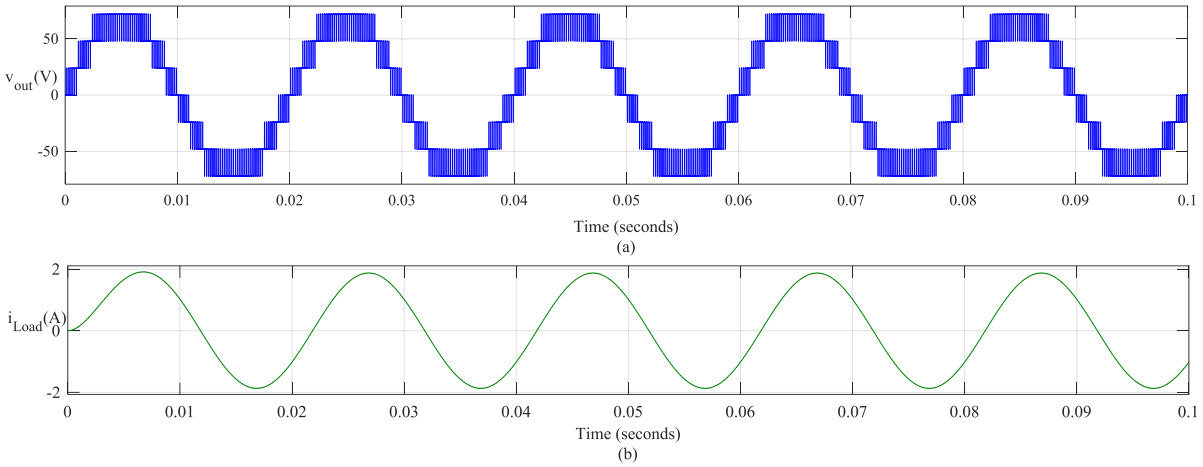



**Figure 2.14** Phase shifted carrier based (a) seven level inverter output voltage, (b) load current

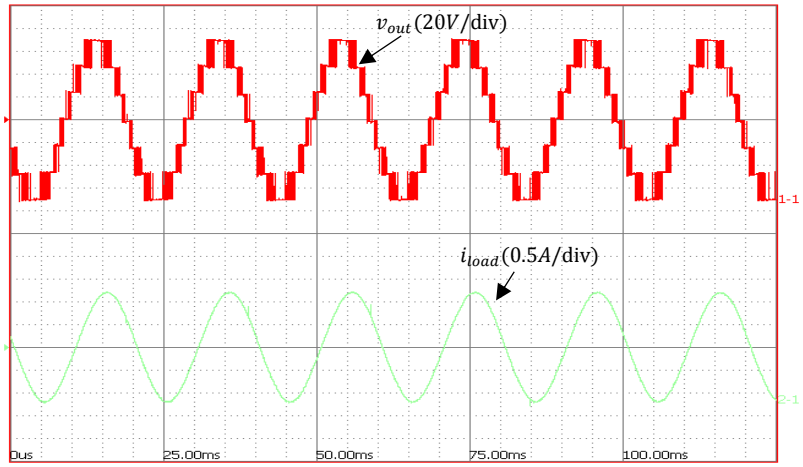



**Figure 2.14(c)** Experimental results of seven level inverter for phase shifted PWM:output voltage and load current

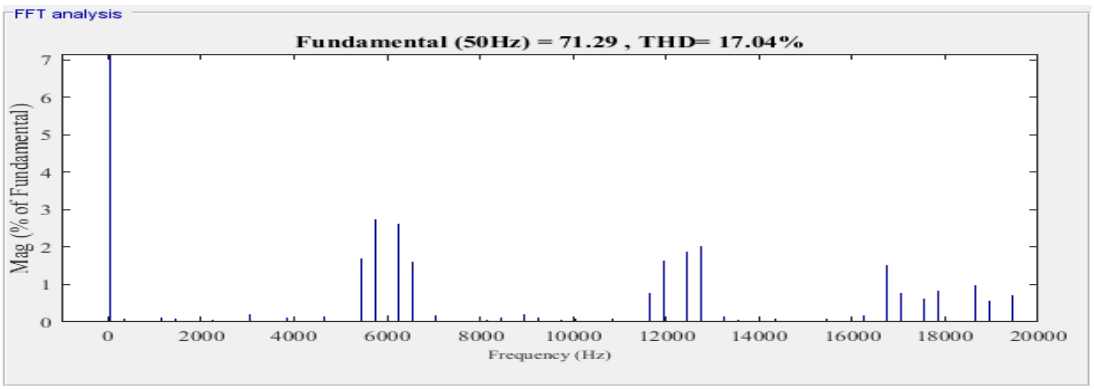



**Figure 2.15** FFT analysis of seven level inverter output voltage.

It is observed that that with three H-bridge cells, seven level output voltage can be generated using phase shifted carrier modulation. The 72 volts of peak voltage level is obtained, when 24 volts is supplied to each of three bridge cells. The wave forms shown in Fig. 2.14(a) and (b) are output voltage of, multilevel inverter with corresponding load current The absolute switching frequency of the inverter is 6 kHz when six carrier wave with 1 kHz switching frequency is used. Experimental results supporting simulation results are shown in Fig 2.14(c) consisting output voltage and load current of seven level inverter. THD of 17.04 % in output voltage of seven level CHMLI is shown in Fig. 2.15 through FFT analysis.

Coming to next that is nine level inverter, four H-bridge cell is connected in cascade to feed the load. The performance analysis of phase shifted carrier based PWM technique for nine level inverter. As shown in Fig 2.10(b) nine level inverter consist of four H-bridges in cascade and four isolated dc supply of 24 volts is fed to the inverter unit. The wave forms shown in Figure 2.16(a) and (b) are output voltage of, multilevel inverter with corresponding load current. For nine level inverter 24 V isolated dc supply is connected to each of four H-bridge cells and load of R=64 ohm and L=200 mH is connected to CHMLI. Nine level output voltage in single phase CHMLI is achieved by cascading four H-bridges in a single phase system. Further increment of levels can be achieved either cascading more H-bridges or applying hybrid control techniques. Experimental results are shown for nine level inverter connected to RL load is shown in Fig. 2.16(c) that consists output voltage and load current. THD of 12.65% in output voltage of nine level CHMLI is shown through FFT analysis in Fig. 2.17.

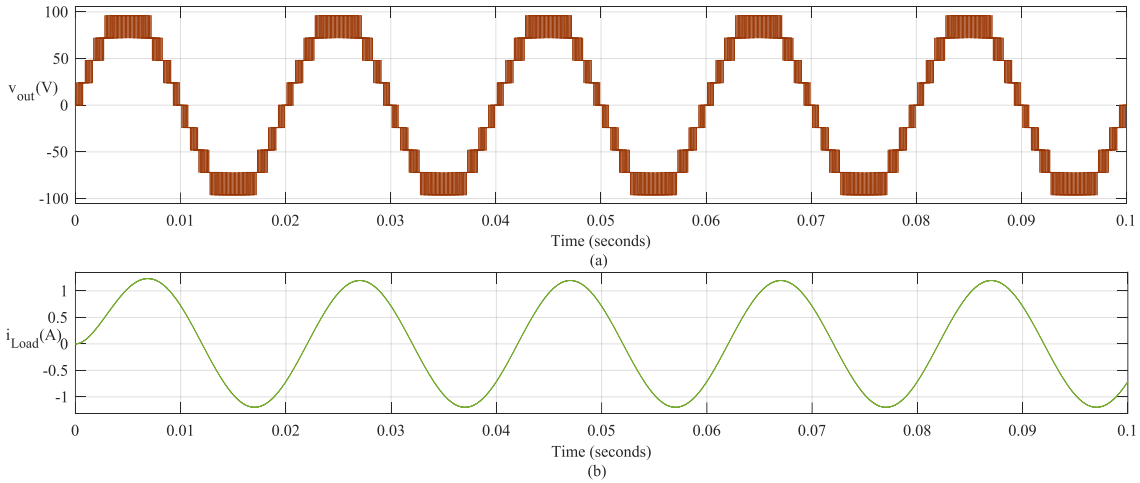



**Figure 2.16** Phase shifted carrier based (a) Nine level inverter output voltage, (b) load current

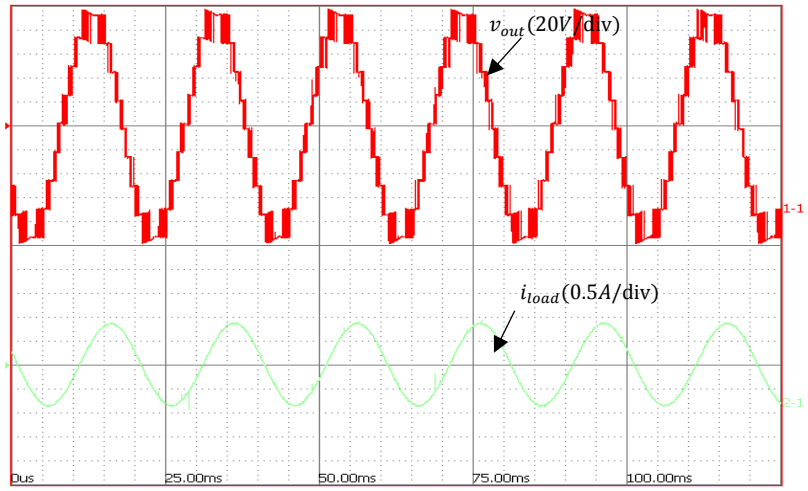



**Figure 2.16(c)** Experimental results of nine level inverter for phase shifted PWM: Output voltage and load current.

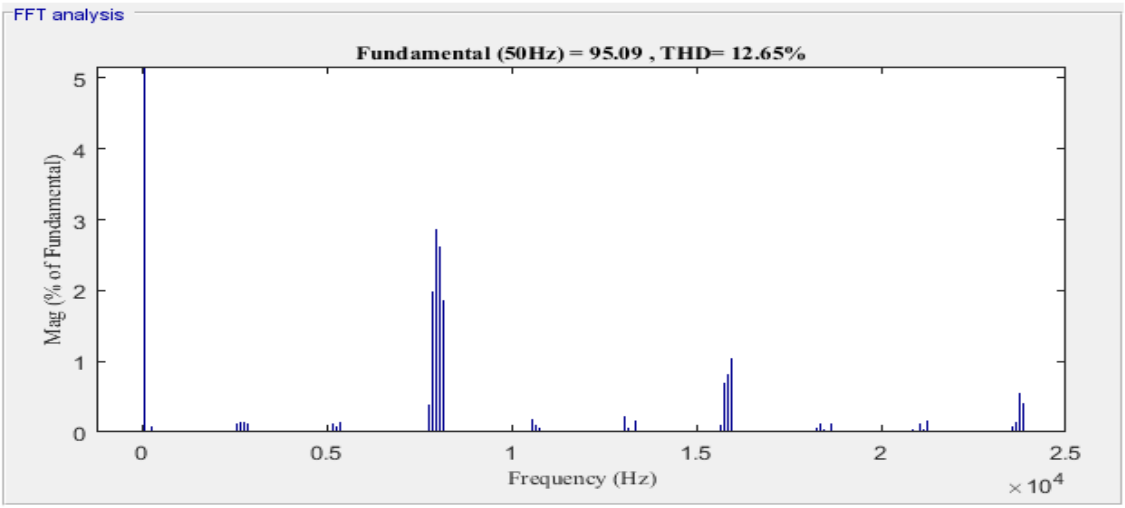



**Figure 2.17** FFT analysis of nine level inverter output voltage with phase shifted SPWM

## 2.5.2 Level shifted carrier based PWM technique

Similar to phase shifted carrier based pulse width modulation, an n level CHMLI requires n-1 triangular carrier waves for implementing level shifted carrier based pulse width modulation. All carrier must have same frequency and phase but the triangular carrier waves must be vertically disposed in such a way so the band they occupy are contiguous. The absolute frequency of inverter remains as the frequency of the carrier wave irrespective of number of H-bridge cells involved. Modulation index of the level shifted carrier based modulation is defines as m.

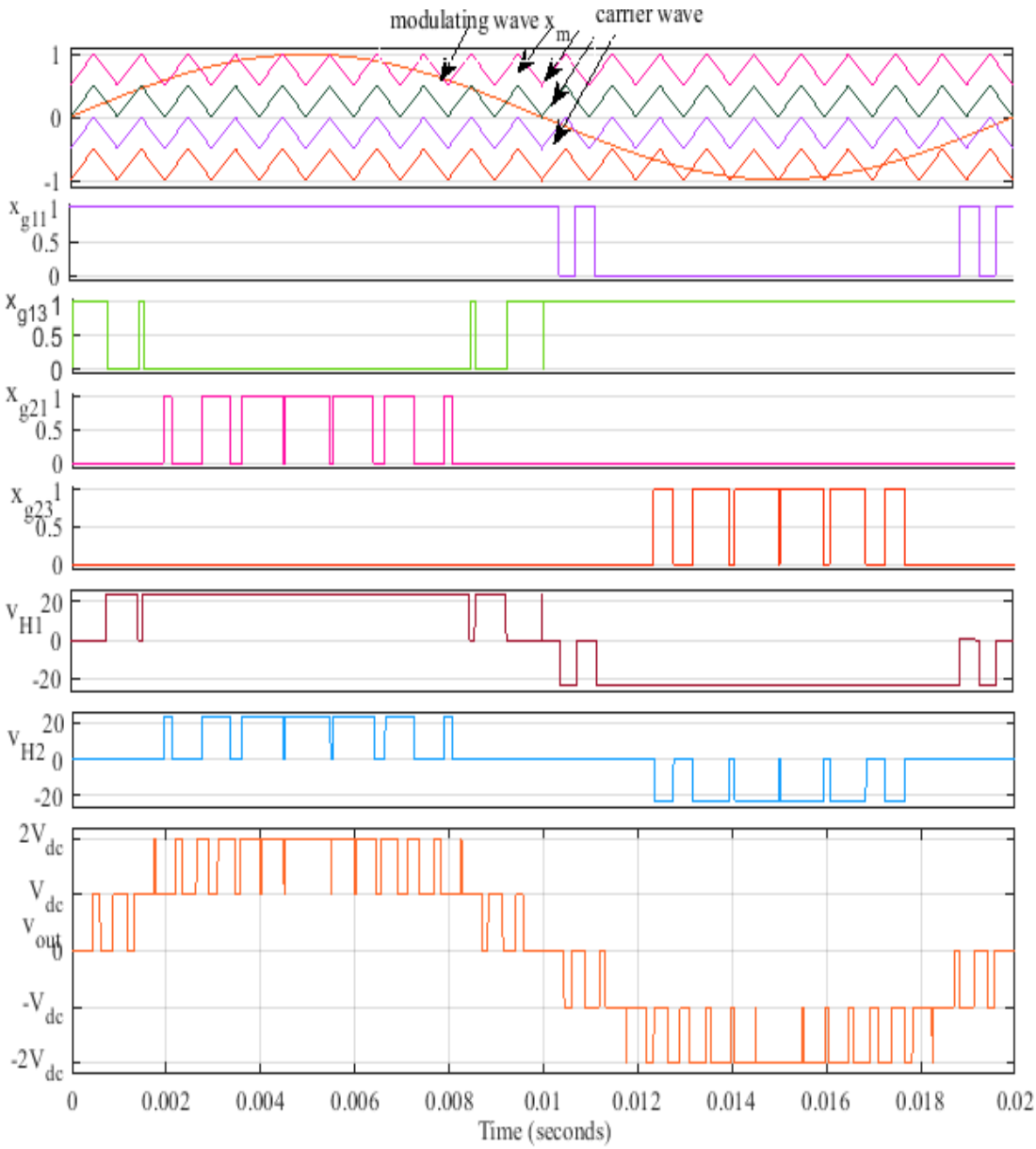



**Figure 2.18** Level shifted carrier based PWM for five level inverter.

$$\mathrm{m} = \frac{|x_m|}{|x_{cr}|(n-1)}$$

Where $|x_m|$ and $|x_{cr}|$ are the peak amplitude of the modulating and carrier waves. For three phase inverters modulating waves are generally sinusoidal waves with adjustable amplitude and fundamental frequency. This modulation technique has disadvantage as it possess unequal switching stress on power semiconductor devices. The further classification of the level shifted carrier based modulation can be, in phase disposition (IPD) in which all disposed carriers possess

same phase, alternative phase disposition (APOD) in which all the carrier waves are alternatively in opposite disposition and phase opposite disposition (POD) in which all the carrier wave above zero are in same phase and opposite in phase with those below zero. In these techniques IPD modulation has better harmonics profile and it is discussed in detail here.

For basic circuit of five level CHMLI two H-bridges connected in cascade have four primary switches. Inverted gate signals are provided to the complementary switches of each leg of H-bridges. As shown in Fig. 2.18 the four disposed carrier waves are compared with the modulating wave the combined amplitude of the four carrier waves is equal to one and modulating signal have magnitude of 0.98.So the modulation index of the level shifted modulation is selected 0.98.The four gate signal are $x_{g11}$, $x_{g13}$, $x_{g21}$, $x_{g23}$ and three level output of each bridge $v_{H1}$, $v_{H2}$ are shown in the results. The switched output of five level inverter is generated using level shifted carrier based modulation. $v_{out}$ is magnitude of the output voltage having five levels $-2V_{dc}$,$-V_{dc}$, 0, $V_{dc}$, $2V_{dc}$.

For performance analysis of level shifted carrier based modulation for five, seven and nine level inverters shown in figure 2.9, 2.10(a) and (b) are considered respectively. Load is varied for each increased level of inverters for maintaining almost same load current in system. Similar to phase shifted carrier based SPWM, in this case it will ease the comparison of different level of inverters.

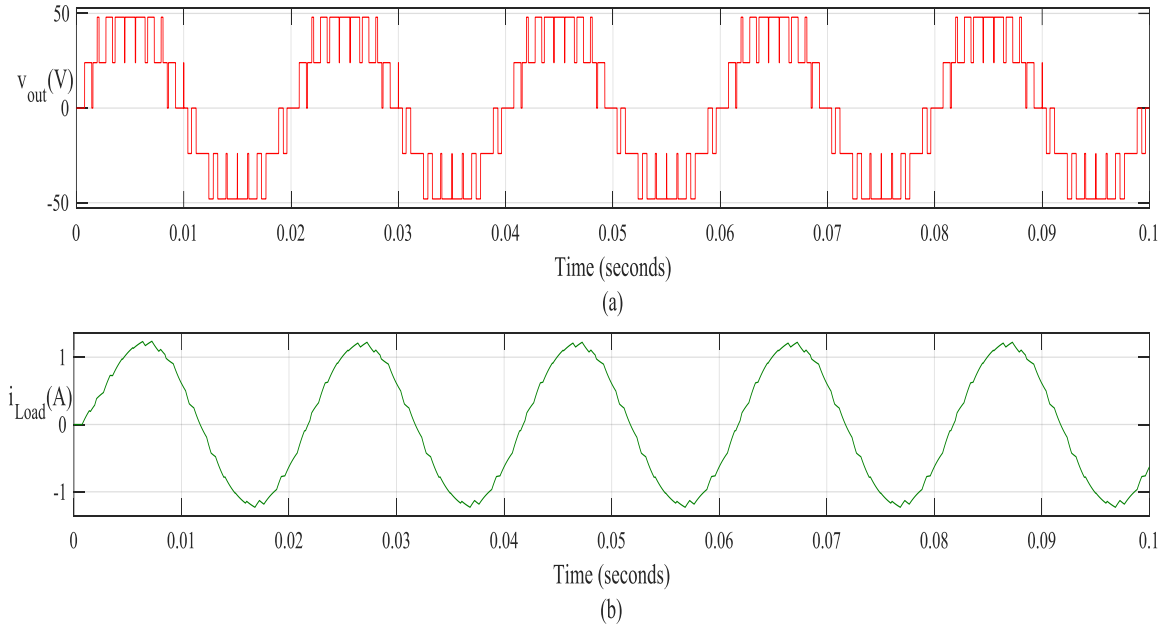



**Figure 2.19** Level shifted carrier based Five level Inverter (a) output voltage,(b) load current.

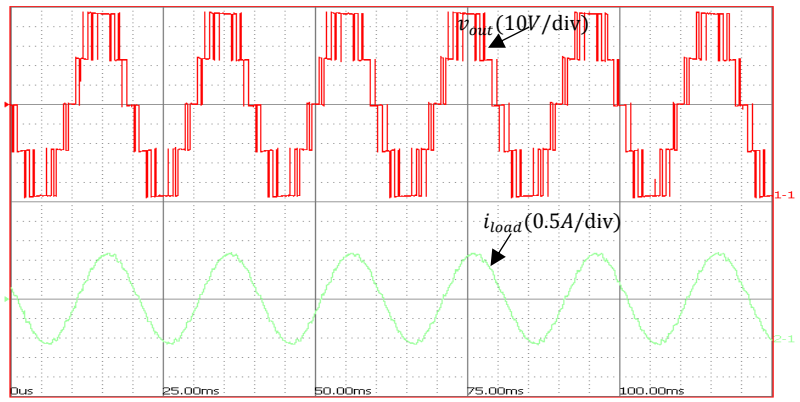



**Figure 2.19(c)** Experimental results of five level inverter for level shifted PWM:output voltage and load current.

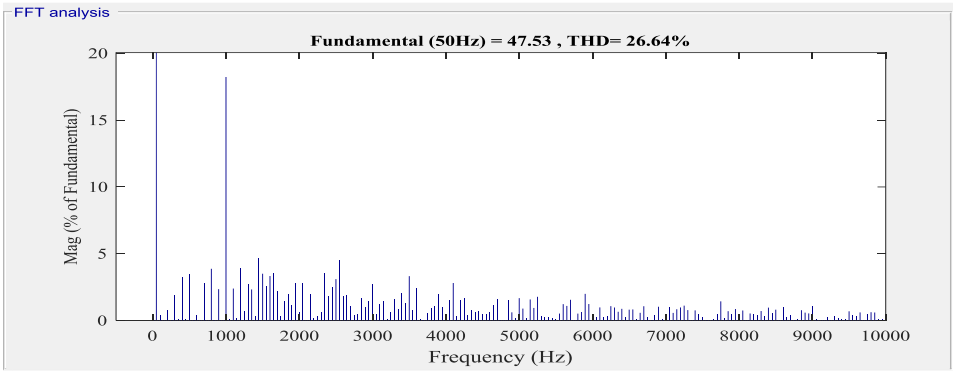



**Figure 2.20** FFT analysis of five level inverter output voltage.

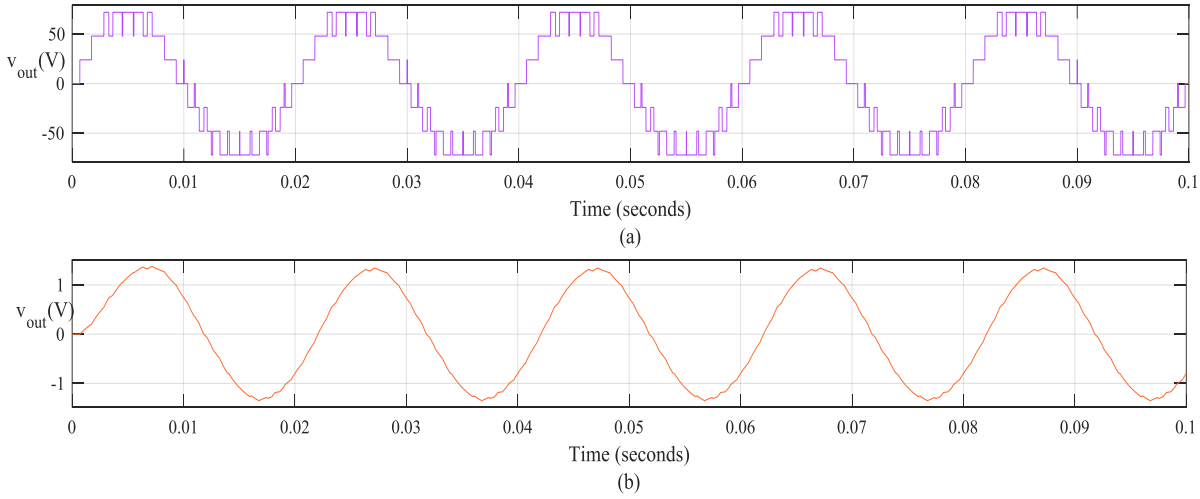



**Figure 2.21** level shifted carrier based seven level Inverter (a) output voltage,(b) load current

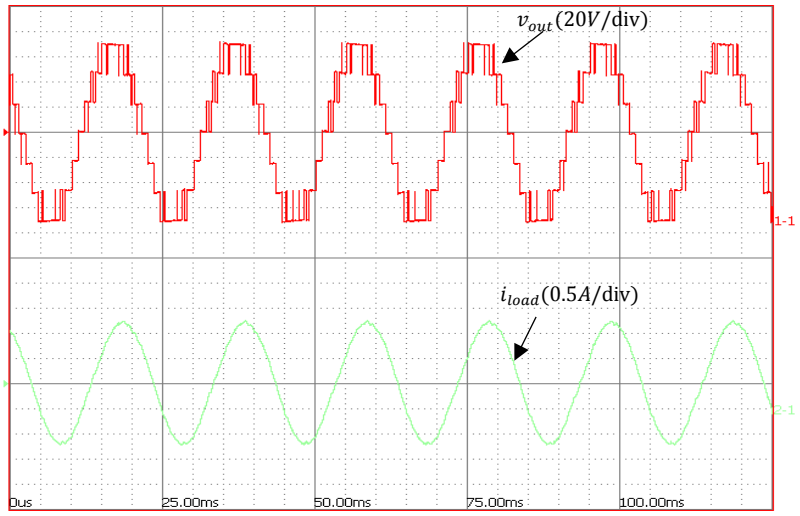



**Figure 2.21(c)** Experimental results of seven level inverter for level shifted modulation.

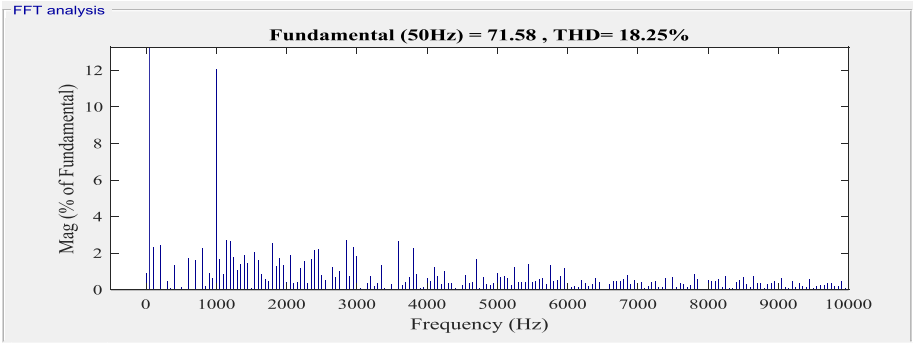



**Figure 2.22** FFT analysis of seven level inverter output voltage.

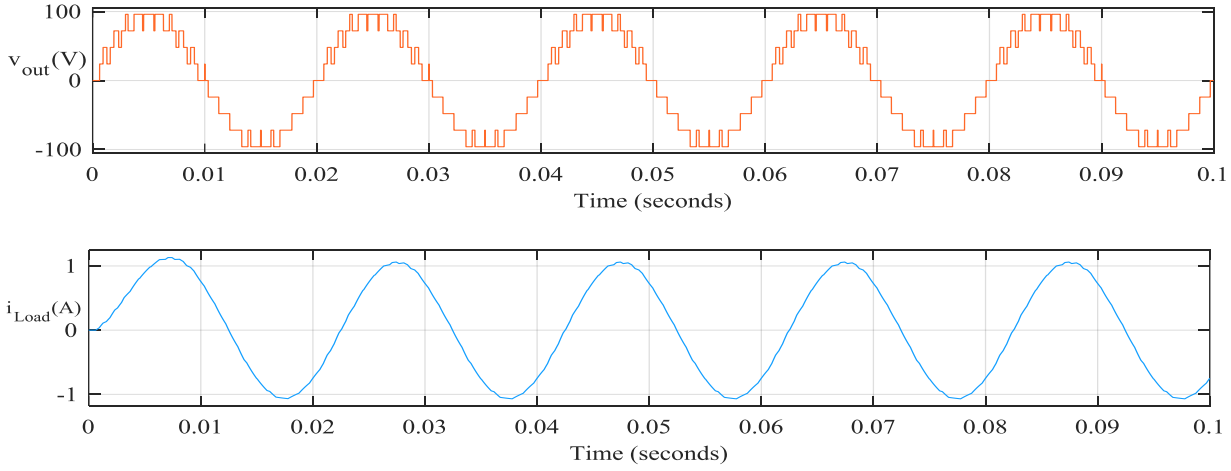



**Figure 2.23** Level shifted carrier based nine level Inverter (a) output voltage,(b) load current

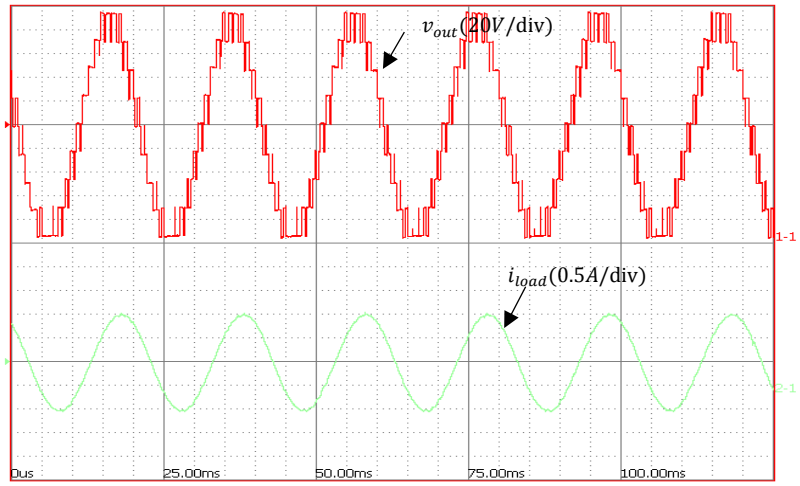



**Figure 2.23 (c)** Experimental results of nine level inverter for level shifted modulation.

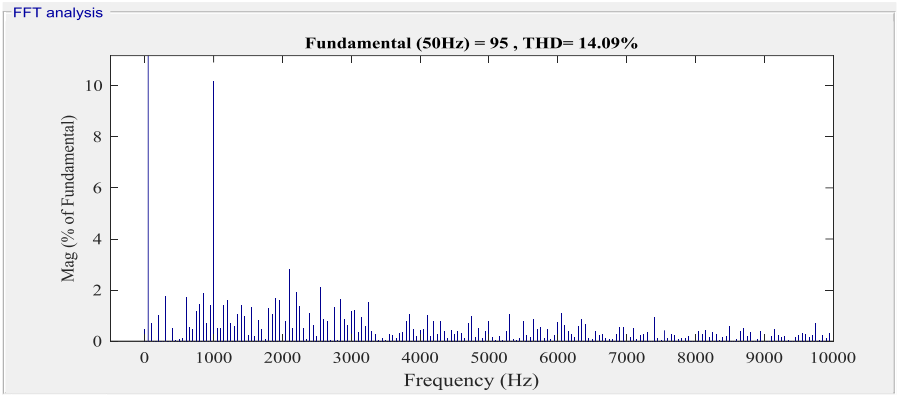



**Figure 2.24** FFT analysis of nine level inverter output voltage.

For five level inverter output voltage and current is shown in fig.2.19 (a) and (b) feeding the load of R=34 ohm and L=66 mH is connected to five level CHMLI. Simulation results are supported by experimental results as output voltage and load current is shown in Fig. 2.19(c). THD of 26.64% is shown through FFT analysis of output voltage as shown in the Fig. 2.20. Linear load of R=44 ohm and L=100 mH for seven level and R=64 ohm and L=200 mH for nine level inverter are selected. Similarly for the seven and nine level inverter output voltage and current is shown in Fig 2.21 (a),(b) and 2.23 (a),(b) respectively. Experimental results for seven and nine level inverter consisting output voltage and load current are shown in Fig2.21(c) and Fig 2.23(c) respectively. THD of 18.25% and 14.09% for output voltage is shown in Fig 2.22 and 2.24 through FFT analysis for seven level and nine level respectively.

## 2.6 Third harmonic injected PWM (THIPWM)

Switching control techniques for power electronics converters has been developed to achieve high performance and precision. Similar to the conventional two level inverters multilevel inverters also have vast scope of switching control technique development. Taking account to that a established THIPWM for conventional inverters can be extended for the multilevel inverters. Conventional SPWM for the CHMLI has great advantages in the limit of modulation index up to 1, however the performance of CHMLI in over modulation range leads to the over current problems due to non-linearity of modulators.

For high performance inverters operating in over modulation range, sensitivity to dc bus voltage sag would be less. It may results in poor performance when operating in close loop system. There are some control techniques have been developed focusing on inverter operation in over modulation range for example THIPWM, space vector modulation (SVM), DPWM1 (discontinuous PWM1), DPWM2 [118]-[120]. Among them THIPWM possess the simplest in implementation and can be applied to over modulation operation of CHMLI easily. THIPWM is simplest and provides the wider range of linearity compared to conventional PWM techniques. THIPWM have some additional advantages such as maximizing the dc bus voltage utilization and

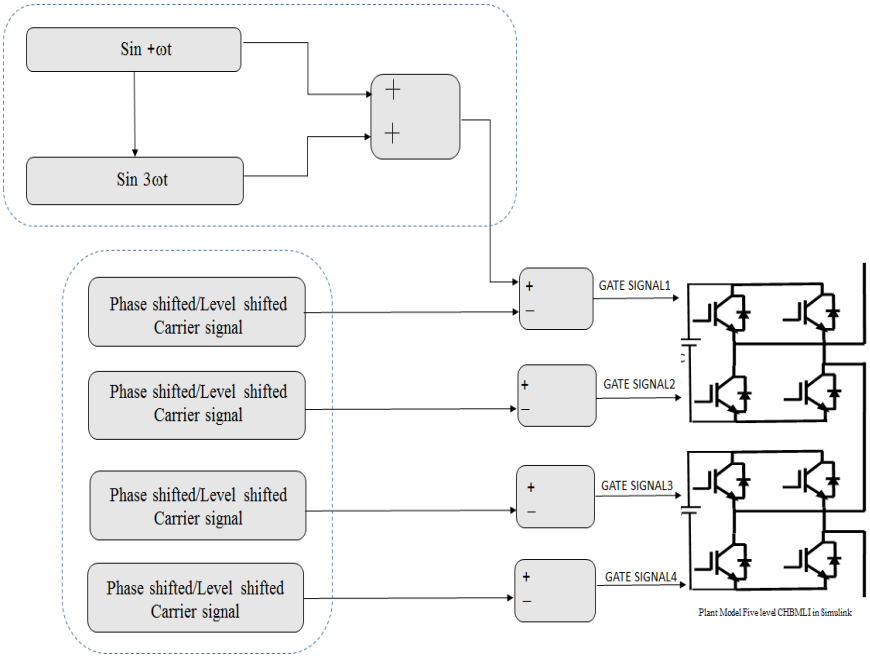



**Fig.2.25** Third harmoincs injected PWM for five level CHMLI.

improved THD in output voltage. SPWM techniques can be advanced to THIPWM by addition of third harmonics components to the modulating signal as shown in Fig 2.25. The magnitude of third harmonics component and limit of extension of modulation range is important factors. For the realization of THIPWM for CHMLI following mathematical equations are derived,

The modulating signal for SPWM switching can be represented as,

$$v = V_{max} \sin \omega t \tag{2.5}$$

Where, v is instantaneous magnitude, $V_{max}$ is peak amplitude, ω is fundamental frequency.

The modulating signal for THIPWM can be modified by injecting third harmonics and represented as,

$$v_{thi} = V_{max} \sin \omega t + \mu V_{max} \sin(3\omega t) \tag{2.6}$$

Where μ is a constant representing magnitude of the third harmonics component. The computation of $\mu$ is required to decide the over-modulation range to maintain linearity. The maximum amplitude of modulation signal corresponds to the optimum value of $\mu$. Optimum value of $\mu$ computed as using max-min conditions as follows:

$$\frac{dv_{thi}}{d\omega t} = V_{max} \cos(\omega) t + \mu V_{max} \cos(3\omega t) = 0 \tag{2.7}$$

By solving Eq.(2.7)

$$cos\omega t = \sqrt{9\mu - \frac{1}{12\mu}} \tag{2.8}$$

$$v_{thi} = (1 + 3\mu) V_{max} \sin(\omega t) - 4\mu V_{max} (\sin(\omega t))^3 \tag{2.9}$$

The maximum amplitude of modified modulating wave for THIPWM can evaluated by solving Eq.(2.8) and (2.9)

$$V_{thimax} = 8\mu V_{max} \sqrt{(\frac{3\mu+1}{12\mu})^3} \tag{2.10}$$

The optimum value of μ can be calculated as $V_{thimax}$ at its maxima.

$$\frac{dV_{thimax}}{d\mu} = V_{max}\left(\frac{6\mu-1}{3\mu}\right)\sqrt{\frac{3\mu+1}{12\mu}} = 0 \tag{2.11}$$

$$\mu = -\frac{1}{3}, \frac{1}{6} \tag{2.12}$$

The value of $\mu = \frac{1}{6}$, is selected for maximum value of $V_{thimax}$ and $-\frac{1}{3}$ is omitted.

The modulating wave for THIPWM ia as follows

$$v_{thi} = V_{max}(\sin\omega t + \frac{1}{6}\sin(3\omega t)t) \tag{2.13}$$

The equation represented in Eq.(2.13) of modulation wave have two maximum values at $\frac{2\pi}{3}$ and $\frac{\pi}{3}$ and has minimum value at $\frac{\pi}{2}$ as shown in Fig.2.26 (b) The effect of injecting third harmonics on over modulation range and on dc bus voltage utilization can be predicted at angle of $\omega t = \frac{\pi}{3}$ in Eq.(2.13),

$$V_{thimax} = V_{max}\frac{\sqrt{3}}{2}$$

This leads to the results,

$$V_{max} = \frac{2}{\sqrt{3}}V_{thimax} = 1.154V_{thimax} \tag{2.15}$$

Instead of

$$V_{max} = V_{thimax} \tag{2.16}$$

By applying THIPWM the maximum amplitude of output ac voltage with same dc bus voltage is increased to 1.154 times, an increase of 15.4 % is achieved. It is important to note that modulation index is extended to 1.154 without losing the linearity of modulator. The mathematical analysis explains the working of THIPWM control and its effect on linearity and dc bus voltage utilization.

The modification in modulating wave leads to THIPWM for CHMLI. The conventional SPWM for CHMLI are two types: phase shifted carrier and level shifted carrier PWM. THIPWM requires modification in modulating wave as well as carrier wave. THIPWM can be implemented in two ways for CHMLI either corporates with phase shifted or level shifted carriers.

### 2.6.1 THIPWM for phase shifted carriers

As phase shifted carrier based PWM possess high efficiency in term of less THD in output voltage, distributed power stress. Incorporation of PSPWM and THIPWM avails a better switching technique options for the CHMLI. Output voltage with corresponding modulating and carrier signal for five level inverter is shown in Fig.2.26 (a) & (b). For generation of five level symmetrical output third harmonics injected modulating wave is compared with phase shifted triangular waves.

### 2.6.2 THIPWM for level shifted carriers

LSPWM technique possess less complexity compare to PSPWM but have some disadvantage for CHMLI such as uneven power stress, poor THD in output voltage, distributed harmonics spectrum. LSPWM can be combined with THIPWM and output voltage with modulating and level shifted carrier waves for seven level output are shown in Fig.2.27 (a) & (b).

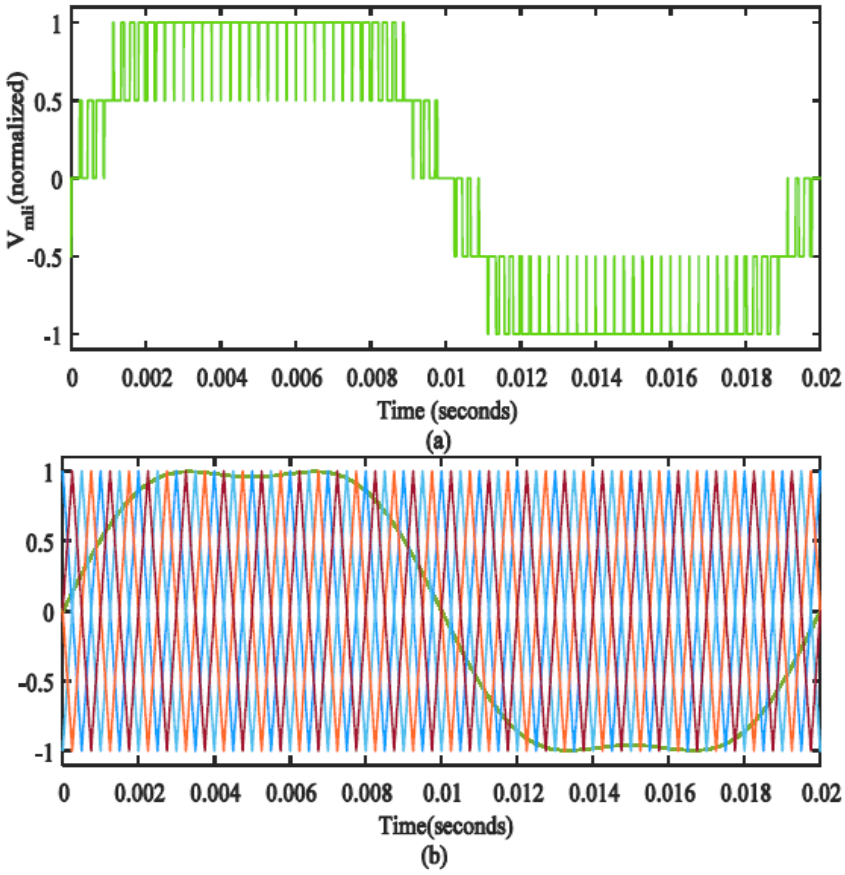



**Fig.2.26.** Phase shifted carrier based THIPWM (a) five level output voltage, (b) modulating wave and carrier wave

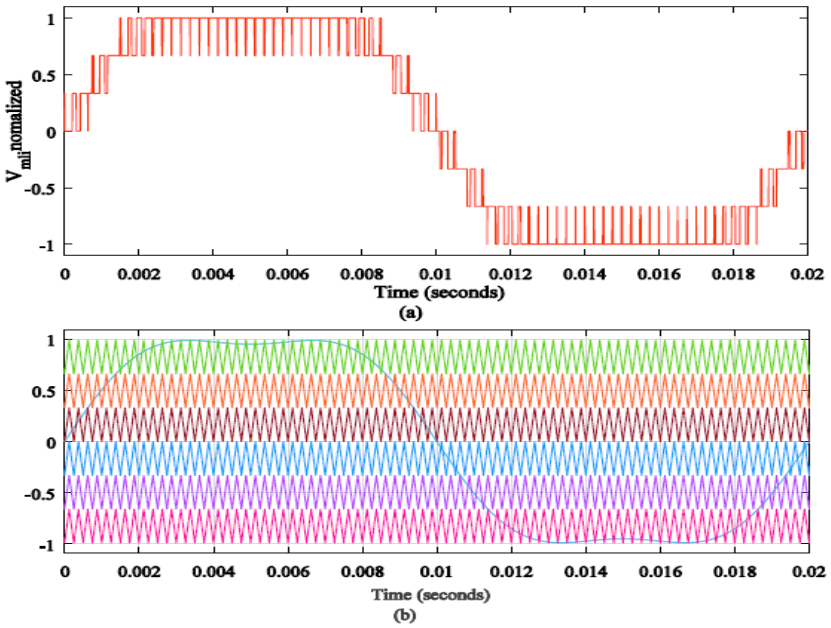



**Fig.2.27.** Level shifted carrier based THIPWM (a) seven level output voltage, (b) modulating wave and carrier wave.

## 2.7 FPGA hardware co-simulation for THIPWM controlled CHMLI

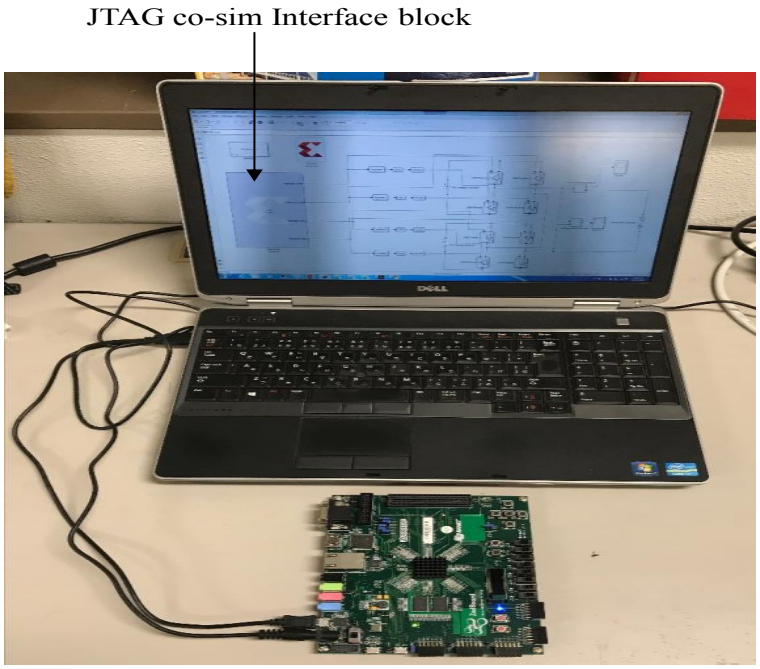



**Fig.2.28**. Hardware in loop (FPGA Zed board) co-simulation setup

Development of advanced control techniques required to be tested in real-time for ease of implementation. Hardware co-simulation method is a rapid testing tool and used for data

acquisition, control strategies in large number of industrial processes concerned with cost, safety and full scale prototyping. The development and knowledge of hardware description language (HDL) is required for FPGA based controller design. XSG provides the platform of model-based design and development of FPGA based controller. FPGA based power electronics controller can be designed using combined platform of MATLAB-Simulink and XSG without the prior knowledge of HDL. The design of controller can be readily tested using FPGA hardware co-simulation.

In this section, FPGA hardware-in-loop co-simulation is proposed for controller prototyping of THIPWM with phase shifted and level shifted carrier wave for five level and seven level CHMLI. Joint test action Group(JTAG) communication based hardware co-simulation using Zed board Zynq development and evaluation FPGA kit is performed to analyze the performance of THIPWM controlled CHBMLI as shown in Fig.2.28. CHBMLI model is developed in MATLAB-Simulink and THIPWM switching control technique modelled using XSG block sets for FPGA based control design and testing as shown Fig.2.29. The advantage of using hardware co-simulation is real time testing of control design and high speed simulation by interfacing hardware based control to software based model of inverter system.

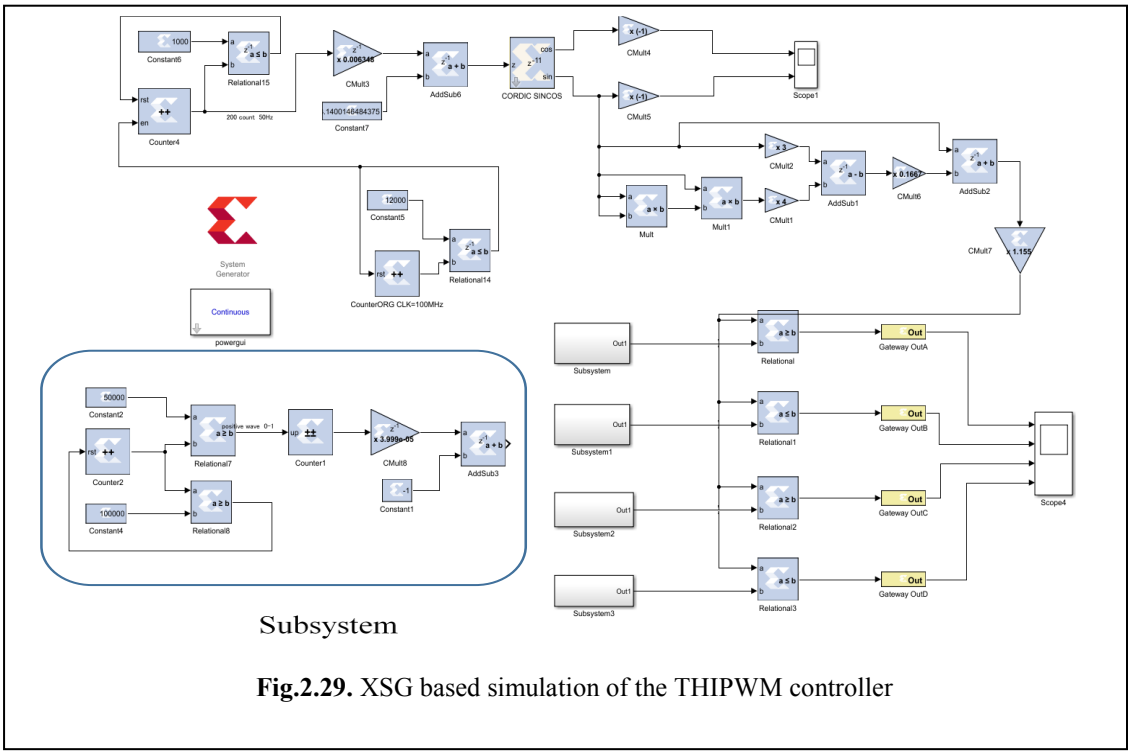



**Fig.2.29.** XSG based simulation of the THIPWM controller

### 2.7.1 Discussion on Hardware Co-simulation results

THIPWM control for five level and seven level CHBMLI is implemented. 24V isolated dc voltage is supplied to each H-bridge cell. Hardware co-simulation for THIPWM at modulation index of 1.15 without losing linearity of modulation technique is done. Over current and non-linearity of control is avoided even modulation index is exceeded the value of 1. The frequency of the system modelled in XSG is scaled corresponding to the clock frequency of FPGA. The clock frequency of FPGA used for hardware co-simulation is 100MHz. Simulink sample time set to unity while performing hardware co-simulation for system design corresponding to FPGA clock frequency. The switching frequency of 1 KHz is scaled to $1 \times 10^{-5}$ Hz and fundamental frequency of 50 Hz is scaled to $5 \times 10^{-7}$ for simulation based on XSG tools in Simulink. In XSG based simulation, time period of carrier and modulation signal are scaled up to $1\times10^{5}$ and $2\times10^{6}$ respectively. Performing fully software based simulation of complex system is time taking due to burden of high computation.FPGA Hardware co-simulation using XSG tools enables higher speed comparative to software based simulation.

### 2.7.2 Performance of phase shifted THIPWM

Phase shifted carrier signal is taken in to account to implement THIPWM technique for five and seven level inverter. The frequency of triangular signal added for the case of PSPWM so the resultant switching frequency is multiplied by number of carrier signals used for switching. The number of carrier signal for five and seven level inverter is four and six respectso for the carrier signal of 1 kHz the resultant switching frequency is 4 kHz and 6 kHz for five level and seven level respectively. Output voltage of five level and seven level inverter using phase shifted THIPWM is shown in Fig.2.30 and Fig.2.32. Five level and seven level synthesized output of CHBMLI using THIPWM with phase shifted carrier signal is tested through hardware co-simulation. The dc voltage utilization is also confirmed through co-simulation. The fundamental output voltage achieved through co-simulation is nearly same as the theoretically possible output.

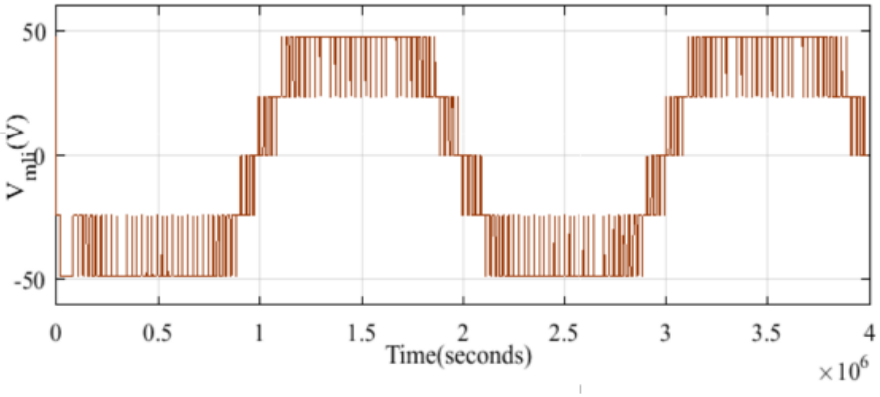



**Fig. 2.30** Output voltage of five level inverter based on phase shifted THIPWM.

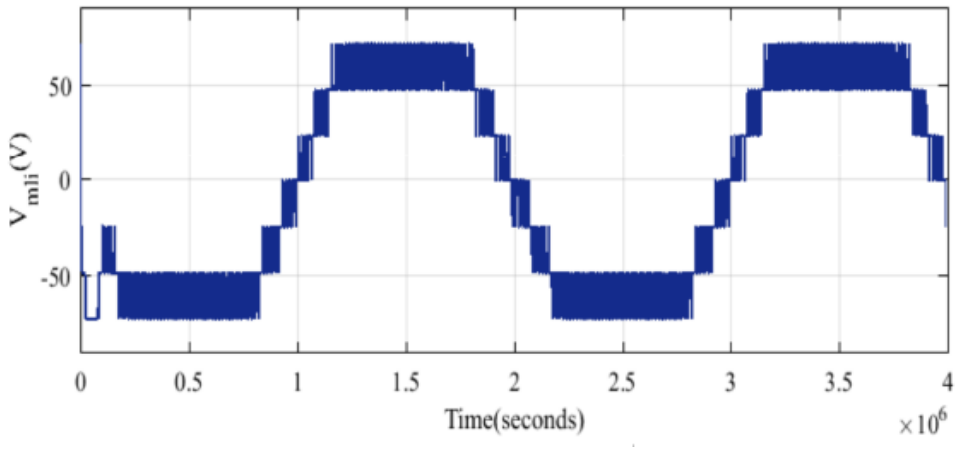



**Fig. 2.31** Output voltage of five level inverter based on phase shifted THIPWM.

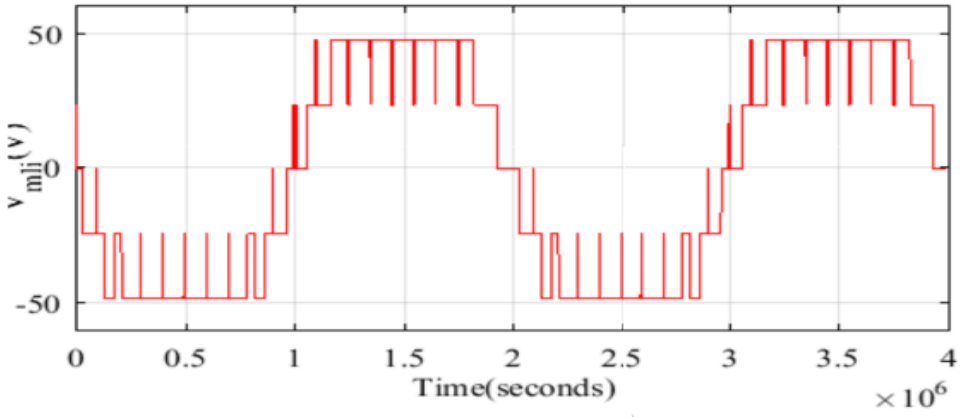



**Fig. 2.32** Output voltage of five level inverter based on phase shifted THIPWM.

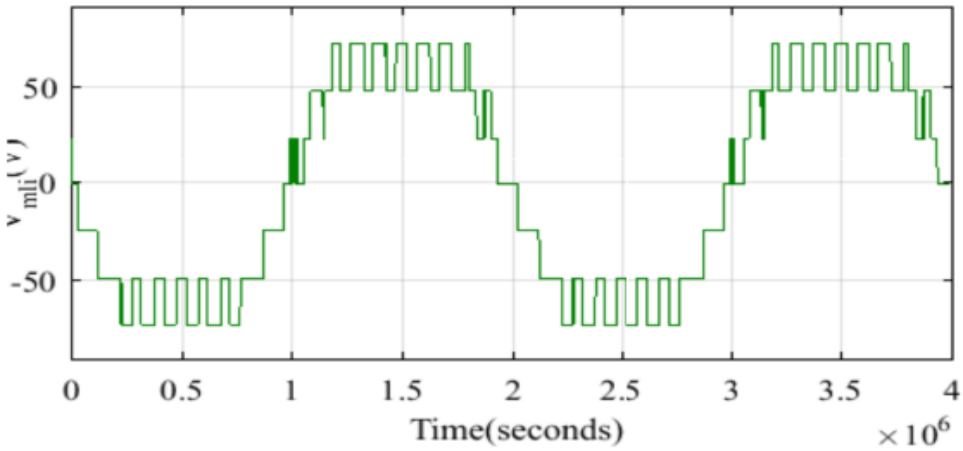



**Fig. 2.33** Output voltage of five level inverter based on phase shifted THIPWM.

### 2.7.3 Performance of level shifted THIPWM

Five level and seven level synthesized output of CHBMLI using THIPWM with level shifted carrier signal is tested through hardware co-simulation. Operating switching frequency is not cumulative is in the case LSPWM. The switching frequency is exactly same as frequency of carrier signal. So the switching frequency for LSPWM is same for five level and seven level considering the carrier signal of frequency 1 kHz. As THIPWM control is applied to CHBMLI using Hardware co-simulation and modulation index is extended to 1.154 avoiding non-linearity as shown in Fig. 2.32&2.33. The increased fundamental voltage is achieved in over-modulation range. The fundamental output voltage achieved through co-simulation is nearly same as the theoretically possible output.

Fundamental output voltage of CHBMLI compared for theoretical output and output achieved through hardware co-simulation. Fundamental output voltage of inverter for five level and seven level adopting phase and level shifted THIPWM technique summarized in Table 2.2.

**Table 2.2 Fundamental Output voltage of CHMLI**

| THIPWM | Theoretical(V) | Hardware co-sim.(V) |
|---|---|---|
| Phase shifted (5L) | 55.4 | 54.8 |
| Phase shifted (7L) | 83.1 | 82.6 |
| Level shifted (5L) | 55.4 | 54.6 |
| Level shifted (7L) | 83.1 | 82.5 |

## 2.7 Conclusion

First of all single phase H-bridge inverter model is investigated for unipolar and bipolar sinusoidal pulse width modulation technique. Generation of gate pulse using SPWM is exploited for extended level of inverter i.e. multilevel inverter. A specific topology of multilevel inverter family known as cascaded H-bridge multilevel inverter is constructed using H-bridge cells. Phase shifted and level shifted carrier based modulation is used for gate signal generation for increased number of power semiconductor devices. The performance of CHMLI under open loop operation connected to linear inductive load is evaluated in Simulink. XSG model developed corresponding to fundamental clock frequency of FPGA for real-time imitation of controller. Phase shifted and level shifted carrier based SPWM techniques is implemented for five, seven and nine level of

inverter. It is concluded that for symmetrical topology of CHMLI, phase shifted carrier based SPWM possess less THD in output voltage and switching stress are distributed throughout the whole structure in comparison to level shifted SPWM.

Additionally, FPGA hardware co-simulation is proposed for controller prototyping of CHMLI in MATLAB-Simulink-XSG platform. THIPWM is used for controller prototyping of CHMLI in real time co-simulation. Performance improvement in term of wider linearity range and better dc bus utilization of THIPWM for phase shifted and level shifted carrier is validated through hardware co-simulation results.

Some of the prominent features of CHMLI is described as follows

**Modular structure:** CHMLI topology is composed of multiple H-bridge cells connected in cascade which are identical in features, which reduces the production and manufacturing complexity.

**Lower voltage THD Profile:** By proper switching of the CHMLI a synthesized stepped output voltage can be achieved formed by several voltage levels. CHMLI generates output voltage with reduced THD.

**High voltage operation without switching devices in series:** In CHMLI structure it is evident that the H-bridge cells are connected in cascade to generate high voltages. This eliminated the issue of equal voltage sharing for series connected devices.

**Requirement of isolated dc supplies:** This is one of the drawback of the CHMLI that it requires large number of isolated dc supplies for its operation. And these isolated dc supplies are normally obtained from multi pulse diode rectifiers.

**Large number of components:** CHMLI requires less number of components compared to other topology of multilevel inverter, however it requires large number of device count compared to conventional inverters.

# CHAPTER 3

# LCL filter interfaced cascaded H-bridge multilevel inverter based DSTATCOM

## 3.1 General

Modern power system consisting non-ideal loads affect the quality of power in significant manner and that's why it is important to recognize power quality issues. Power quality can be termed as a system's capability to sustain a sinusoidal voltage and current at a rated magnitude and frequency at power distribution. Therefore, any disturbance in a system due to abnormalities in the systems is termed as a power quality issues. The main reason of originating power quality issues can be classified as: natural and manmade, which may be due to load or feeder. In fact manmade causes plays a major role in contributing to increase in power quality issues. Some mainline reasons include transformers, the process of charging and discharging of capacitors, nonlinear loads such as power electronic loads (e.g., an uninterrupted power supply), drives, and the time-variant, overload or switching of large loads.

In real, power distribution system are connected to different kind of loads and it suffers from dynamic and transient changes that causes power quality issues; to monitor the functioning of the grid, it is essential to have an online real time monitoring system. A real-time power quality monitoring system is thus needed to provide the required communication, both locally and more widely in whole distribution system. Therefore, it must be considering the adverse effects of poor power quality on the safety, reliability, and efficiency of several kind of equipment operating in the grid. The mainline aspects of power quality to be considered includes voltage sag-swell, voltage imbalance, voltage fluctuations, and higher-order harmonics in the grid current.

The use of power electronic loads are increasing by industry and local consumers, it causes issues such as harmonic injection, and a poor power factor in the grid. Conventionally, bulky passive filters have been used to eliminate the current harmonics and improve the power factor. However, the use of passive filters has many drawbacks, e.g. bulky capacitors and inductors, damping effects. Recently, with the rapid progress in power electronics technology for extended applications, the

development and use of active filters are excessively used, rather than passive filters. Some of the leading features of active filters, it is capable to compensate for randomly varying currents.

The presence of an unbalanced or nonlinear loads injects higher order harmonics or cause an imbalance in any distribution system. The shunt or series connected custom power devices are used to prevent such unbalanced and distorted currents from being drawn into the grid. One of the leading shunt-connected custom power device is the distribution static compensator (DSTATCOM), it can dynamically inject a compensating current with the desired amplitude, frequency, and phase. The DSTATCOM is one of the fastest and most reliable modular custom power device for reactive power compensation and harmonic elimination applications. DSTATCOM can be used to ensure that the current drawn from the grid is nearly sinusoidal and distortion-free. A voltage source converter (VSC) is commonly used to realize a DSTATCOM. The VSC structure determines the level or extent of compensation that the device can provide in the grid. If a balanced load is connected to three-phase four-wire system, then a balanced compensating current is required to maintain the smooth operation of the grid. However, in the above scenario, if the source current or load is unbalanced or distorted, the required compensation current must be unbalanced and distorted to mitigate the lack of balance or distortion in the system. For this purpose DSTATCOM is used like a controlled voltage or current source in the grid. DSTATCOM can supply the required reactive power to non-ideal load by circulating energy available in between phases of the AC grid.

DSTATCOM necessitates a VSC for its functioning and for medium voltage high power systems multilevel VSC is used commonly in recent years. Multilevel inverters (MLIs) are capable of generating a synthesized ac output voltage from several input dc voltage sources. A nearly sinusoidal voltage waveform can be obtained by using a sufficient number of dc sources according to topology of MLI.

Cascaded H-bridge MLI (CHMLI) have the advantages of lower operating switching frequencies, a reduced electromagnetic interference, and a modular structure. However, it requires separate DC sources/capacitors for each bridge. The modularity of topology and the ease of lower to higher level expansion are some of the application-based advantages of the CHMLI-based DSTATCOM. Some major application of CHMLI are railways, industrial process, oil refinery, electric vehicle

and renewal energy integration to the grid. Advantages and comparison of CHMLI over other topologies is discussed in chapter1 of this dissertation.

A proper current control and modulation is required to avail DSTATCOM control and gate pulse generation for CHMLI. Normally linear controller such as PI and PR combined with sinusoidal pulse width modulation (SPWM) technique are used. SPWM techniques can be adopted to provide constant switching frequency for each of the power switches.

The generation of reference current for adopting proper control algorithm is essential to get switching signals. These control algorithm can be classified based on the synchronous frames or stationary frames. Synchronous reference frame theory (SRFT) is one of the algorithm based on a set of instantaneous power equations defined in the time domain. According to instantaneous reactive power theory, it has been acknowledged that the direct axis (d-component) and quadrature axis (q-component) components of the load current are responsible for the active power and reactive power, respectively.

In this chapter, designing of LCL filter is proposed considering modified constraints for lower frequency operation of CHMLI based DSTATCOM. For improved performance evaluation of the DSTATCOM system, abnormalities such as voltage disturbance and unbalanced, non-linear loads are considered [120].

## 3.2 System Description and Design

### 3.2.1 Basis Structure

The CHMLI topology utilized for DSTATCOM offers both modularity and flexibility, in significant range of voltage level and frequency. The basic circuit of the generalized m-level consisting k H-bridges in cascade per phase, where m=2k+1 as three-phase CHMLI is shown in Fig. 3.1. The circuit consists of two cascaded cells in each phase. Each CHMLI cell requires an isolated dc source/capacitor for the generation of a synthesized output ac voltage. The generalized system equations for the dc voltage and output ac voltage of CHMLI is shown in Eq. (3.1)–(3.4). For the DSTATCOM application, the bandwidth of CHMLI must be decided based on the highest level of harmonics which need to be compensated. In the case of CHMLI, the increased level of inverters has a linear relation with the number of H-bridge cells and dc sources/capacitors required.

However, the quality of output voltage does not follow the linear relation and there will not be a considerable improvement corresponding to increased levels. Therefore, five and seven level inverters are predominantly used for system implementation at a medium voltage (415–1100 V) high power application

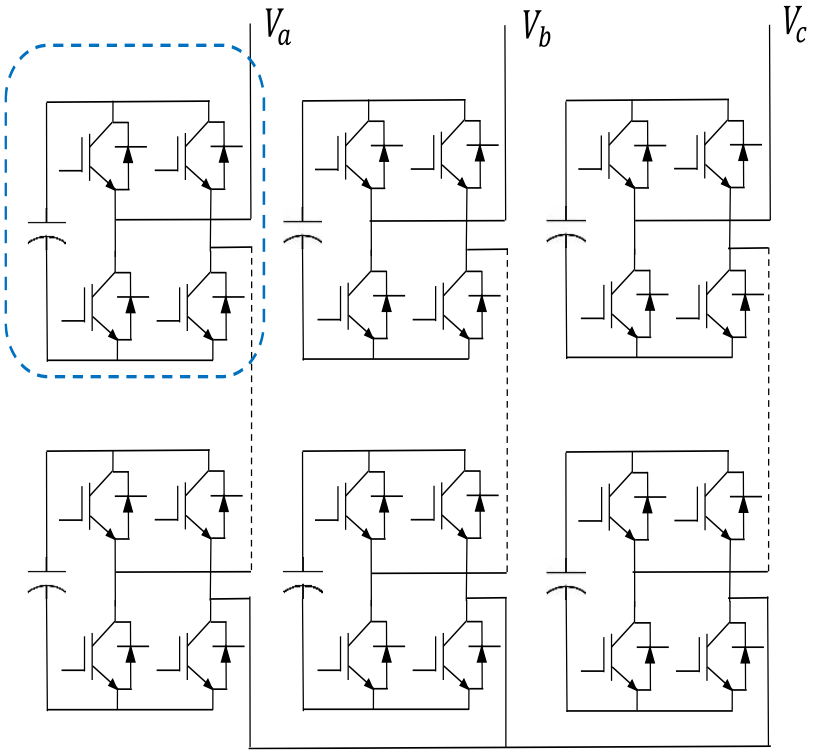



**Figure 3.1** Three-phase cascaded H-bridge multilevel inverter (CHBMLI) structure.

### 3.2.2 Implemented System

In this chapter a five-level CHMLI-based DSTATCOM is proposed utilizing modified design constraints for LCL filter, and interfaced to the grid. The CHMLI (acting as the VSC) for the DSTATCOM application offers control capabilities similar to those of the traditional three-leg inverter. The only difference between these inverters is that more gate signals are required by the earlier invertor, but one of the advantages of the proposed system is that a reduced THD (Total Harmonics Distortion) can be achieved in the converter voltage. The application of an appropriate control scheme with an optimum inverter level produces a voltage source inverter that can generate an alternating voltage in phase with the source voltage. The analysis of the DSTATCOM is also conducted, based on the filter that is applied between the system and the DSTATCOM. Similarly,

the five inverter voltage levels are $-2V_{dc}$, $-V_{dc}$, 0, $V_{dc}$, and $2V_{dc}$; these voltage levels are added to provide the synthesized output of the MLI. The voltage waveform in each phase of the five-level CHMLI consists of five leveled outputs, with two H-bridges connected in the cascade. Each phase of this voltage is fed to the distribution line through a coupling inductance, to form a shunt-connected DSTATCOM, as shown in Fig.3.3, where $V_{sa}$, $V_{sb}$, and $V_{sc}$ are the source phase voltages that are connected to a nonlinear load or reactive load, $L_s$ is the per phase line inductance, and $I_{La}$, $I_{Lb}$, and $I_{Lc}$ represent the per phase load currents. The CHMLI is connected in shunt configuration to the load, and thus, at the point of common coupling (PCC), Kirchhoff's law can very easily be applied. Generalized phasor diagrams of the leading and lagging power factor (PF) load compensation are shown in Fig. 3.2, where cos θ is a PF.

The focus of this chapter is design of LCL filter for lower switching frequency operation which is compatible with CHMLI based DSTATCOM. The analysis and effects of different parameters on the design of a DSTATCOM for reactive power and harmonics compensation. As shown in Fig. 3.3, the system configuration used is the CHMLI-based DSTATCOM. Linear, nonlinear, and unbalanced loads are connected to the system, and draw lagging or leading, distorted and unbalanced load currents from the source, respectively. The shunt-connected device allows for the compensation of the reactive power and harmonics to be performed, and the avoidable component of the current is supplied by the DSTATCOM.

After the connection of the shunt device, the current equation will be as expressed in Eq. (3.5). The nature of the compensation current generated by the shunt device is entirely dependent on the purpose of the required power quality improvement. At the PCC, the resulting source current should be sinusoidal.

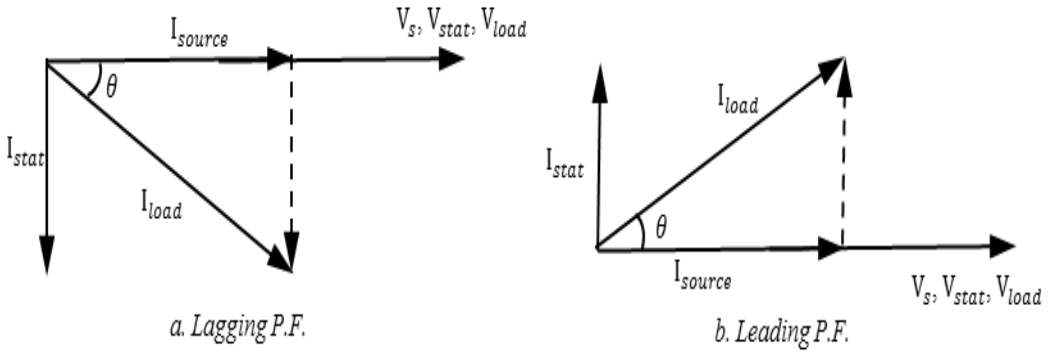



**Figure 3.2**. Phasor diagrams of DSTATCOM with (a) leading and (b) lagging PF loads.

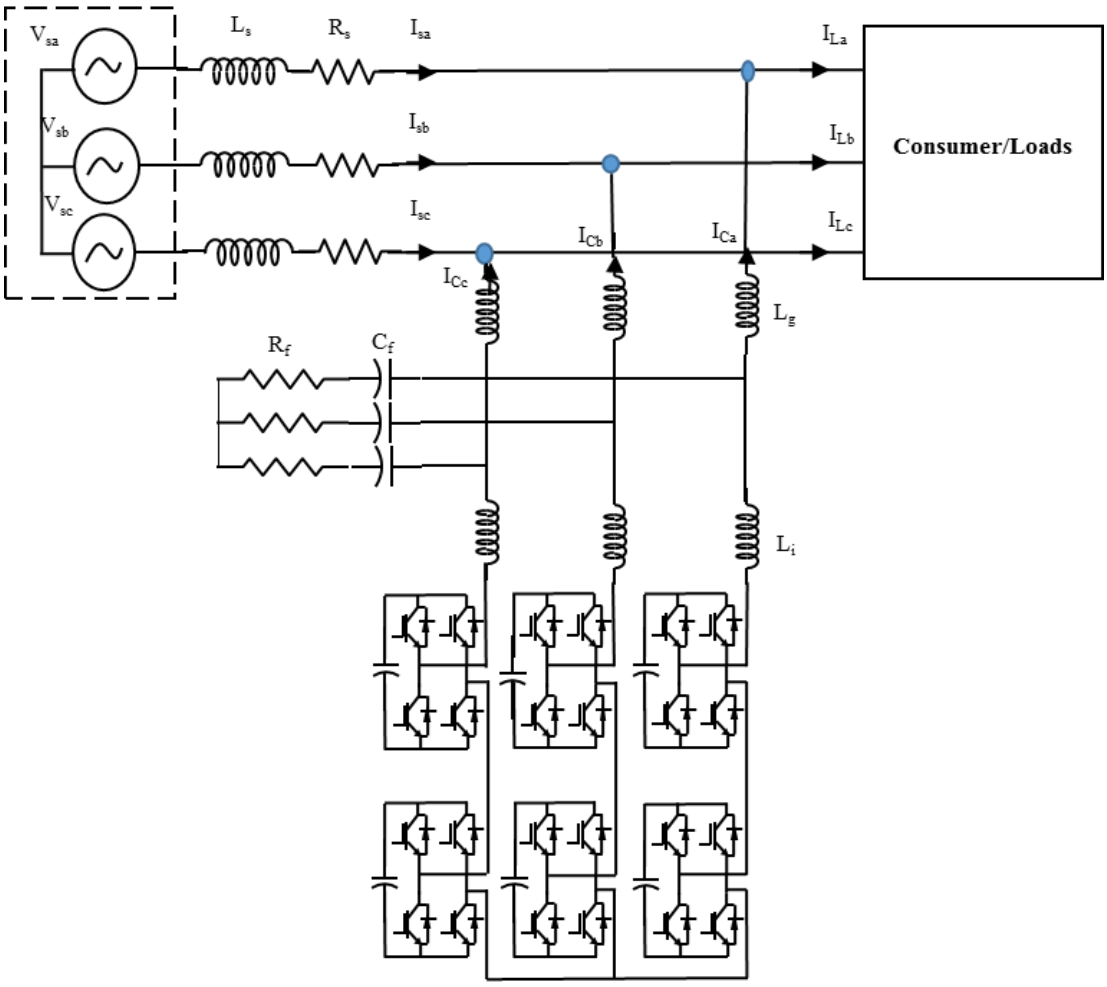



**Figure 3.3** Shunt-connected distribution static compensator (DSTATCOM) system.

$$\begin{bmatrix} I_{\mathrm{La}} \\ I_{\mathrm{Lb}} \\ I_{\mathrm{Lc}} \end{bmatrix} = \begin{bmatrix} I_{\mathrm{Ca}} \\ I_{\mathrm{Cb}} \\ I_{\mathrm{Cc}} \end{bmatrix} + \begin{bmatrix} I_{\mathrm{sa}} \\ I_{\mathrm{sb}} \\ I_{\mathrm{sc}} \end{bmatrix} \tag{3.5}$$

$I_{sa}$, $I_{sb}$, and $I_{sc}$ represent per phase source or grid currents and $I_{Ca}$, $I_{Cb}$, and $I_{Cc}$ represent the per phase DSTATCOM currents.

### 3.2.3 DC Link System

Here, the selection of the topology used for the DSTATCOM application is based on the symmetrical structure of the CHMLI. If all the parameters and all the switching pulses for the H-bridge units are symmetrical, then the actual power of each unit will be identical. However,

because of the dispersion of the capacitors and the switching losses of the IGBTs, the active power of each of the H-bridge units is different. A five-level MLI topology has been adopted for the analytical study, meaning that there are two H-bridges in each phase, and therefore, there are two capacitors per phase and a total of six capacitors in the five-level cascaded H-bridge inverter-based DSTATCOM. The voltages across each of the capacitors should be balanced throughout the operation. Many techniques are available to balance the voltages across the DC link capacitors. Many advanced and intelligent techniques have also been proposed for the balancing of the capacitor voltage, because it is a prominent part of the overall system design and operation.

A mathematical formulation for the cascaded H-bridge capacitance is derived as:[119]

$$C_{\text{dc-cascaded}}=\frac{I_{\text{rms}}}{\sqrt{2}\pi f_{\text{g}} V_{\text{r}} V_{\text{dc}}}\left[1-\sin\left(\arccos\left(\frac{M\pi}{4}\right)\right)\right] \tag{3.6}$$

where $I_{\text{rms}}$ is the root mean square (*RMS*) load current (rated), $f_{\text{g}}$ is the frequency of the system's supply, $V_{\text{r}}$ is the peak-to-peak ripple voltage, $V_{\text{dc}}$ is the DC bus voltage, and $M$ is a modulation index. The voltage balancing can be performed in a phase-wise manner, i.e., the voltages across each of the phases should be equal, and if not, this can be achieved by using an individual voltage balancing technique. An individual voltage balancing technique is used for voltage balancing of each capacitor. To distribute the total active power between all of the H-bridges and to make the capacitor voltage equal to the reference voltage, one extra loop must be added to the control system. The PI(proportional integral) controller is one of the most commonly applied linear feedback controllers, and has been used here because of its simplicity, applicability, and ease of control. The current responsible for power loss due to charging and discharging of capacitors ( $\text{i}_{\text{dloss}}$) is calculated and function of this controller can be elaborated simply, using the following mathematical equation:

$$i_{\text{dloss}} = K_{\text{p}}(V_{\text{dcref}} - V_{\text{dc}}) + K_{\text{i}}\int (V_{\text{dcref}} - V_{\text{dc}})\, dt \tag{3.7}$$

This equation shows only one PI controller, which drives the system to make the capacitor voltage equal to the reference value of the DC link voltage ($V_{\text{dcref}}$) however there are six PI controllers in the proposed feedback control loop across each bridge. All of the controllers have the same proportional gain ($K_{\text{p}}$) and Integral gain ($K_{\text{i}}$) values. The trial-and-error method is used to determine values of the proportional and integral gains.

### 3.2.4 Reference Current Generation for CHMLI

Various voltage and current control techniques are available for the control of the DSTATCOM, and because of its reduced complexity and ease of implementation, an indirect current control technique is used for reactive power and harmonics compensation. A basic block diagram that depicts the reference current generation for indirect current control, is shown in Figure 3.4, and is responsible for reactive power and harmonic compensation.

According to the current control technique implemented using the d-q component, the direct and quadrature axis current is responsible for the active power and reactive power, respectively. The load current passes through the low pass filter (LPF) to obtain the fundamental components of the current. Therefore, only the active component of the power should be required from the source, or only the average DC component ($I_{\mathrm{d}}^{*}$) is required to be fed from the grid. A certain amount of the active power is also consumed by the DSTATCOM, due of the charging and discharging of the capacitors, and this component of the current is responsible for some losses in the grid. The current that is responsible for maintaining the capacitor voltage is added to the active power component of the current, to regulate the capacitor dc voltage by compensating for inverter losses. The mathematical equation involved in the transformation of current from abc to dq0 axis, and in the dq0 to abc axis transformation, is as follows

$$\begin{bmatrix} I_{\mathrm{d}} \\ I_{\mathrm{q}} \\ I_{0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\omega t & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin\omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{\mathrm{La}} \\ I_{\mathrm{Lb}} \\ I_{\mathrm{Lc}} \end{bmatrix} \tag{3.8}$$

The inverse transformation from the dq0 to abc phases can then be written as:

$$\begin{bmatrix} I_{\mathrm{a}}^{*} \\ I_{\mathrm{b}}^{*} \\ I_{\mathrm{c}}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\omega t & -\sin\omega t & \frac{1}{\sqrt{2}} \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{\mathrm{d}}^{*} \\ I_{\mathrm{q}}^{*} \\ I_{0}^{*} \end{bmatrix} \tag{3.9}$$

The generalized reference current for indirect control is calculated using the following equations:

$$V_{\mathrm{t}} = \sqrt{\frac{2}{3}\left(v_{\mathrm{sa}}^2 + v_{\mathrm{sb}}^2 + v_{\mathrm{sc}}^2\right)} \tag{3.10}$$

$$I_{\mathrm{qt}} = K_{\mathrm{p}}(V_{\mathrm{tref}} - V_{\mathrm{t}}) + K_{\mathrm{i}} \int (V_{\mathrm{tref}} - V_{\mathrm{t}})dt \tag{3.11}$$

$$I_{\mathrm{d}}^* = I_{\mathrm{df}} + I_{\mathrm{dloss}} \tag{3.12}$$

$$I_{\mathrm{q}}^* = I_{\mathrm{qf}} + I_{\mathrm{q,t}} \tag{3.13}$$

$V_{\mathrm{t}}$ is termed as the terminal voltage of the PCC that is regulated through the PI controller to maintain the power quality of the system, considering the voltage sag and swell caused by disturbance. Phase locked loop (PLL) is used for synchronization and low pass filter is represented as LPF in the block diagram.

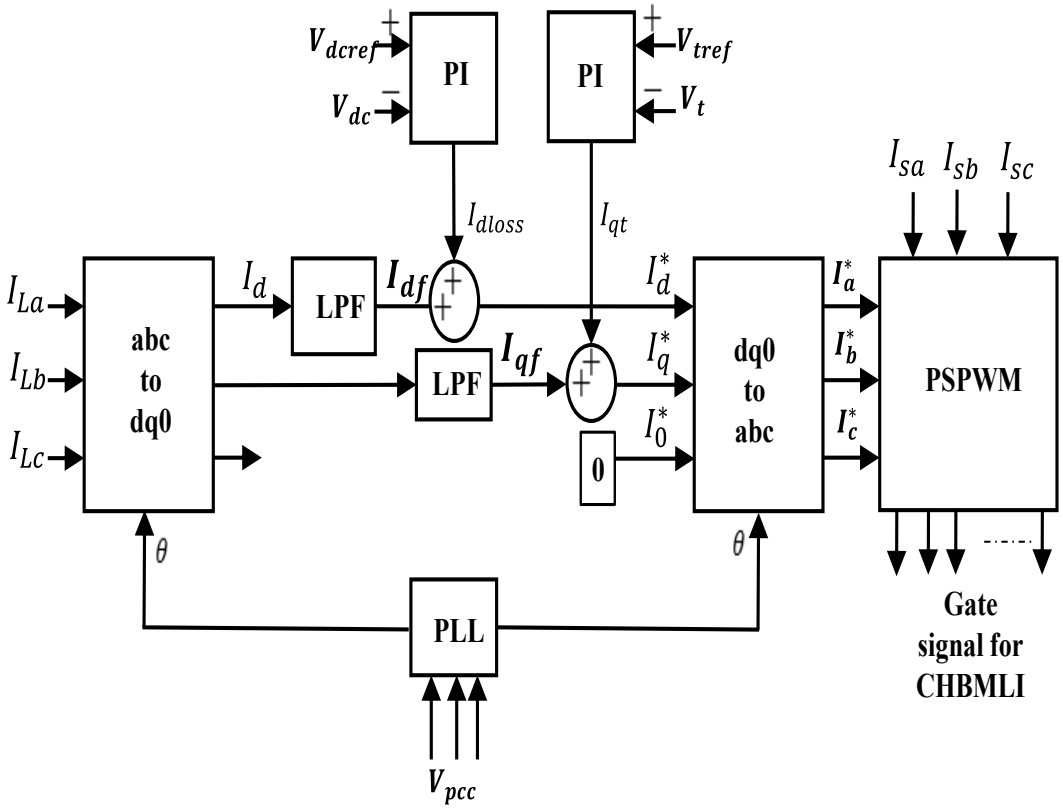



**Figure 3.4** Block diagram of control algorithm used for reactive power compensation.

## 3.3 SPWM for CHMLI

Many modulation techniques have been developed by researchers for MLIs; however, for the DSTATCOM application, SPWM techniques are modular and avoid any complexity in the system. Other commonly used modulation techniques for MLIs include SVM and the selective harmonics elimination technique, and some nonlinear modulation techniques have also been developed for the CHMLI. Two types of SPWM techniques have been utilized for CHMLISs: level shift SPWM and phase shift SPWM explained in chapter 2. Both modulation techniques have advantages, such as the ease of implementation, a constant switching frequency, and the linear nature of control. For m-level CHMLI, $(m - 1)$ carrier signals (triangular) are compared to the one modulating signal (sinusoidal) in order to generate the PWM signals.

## 3.4 Grid Interfacing Filter

### 3.4.1 LCL Filter

Another function of the proposed distribution system is to suppress the additional higher order harmonics that are present in the output voltage generated by power electronic converters, because these harmonics affect the PCC voltage and current. To suppress the harmonics generated by the power electronic devices, the LCL filter is used because it offers advantages such as a small inductor size and cost effectiveness. The minimum filter inductor required to limit the current ripple, considering the single inductor filter system, is given by:

$$L_{\text{fmin}} = \frac{V_{\text{m}}}{v_{\text{s}} f_{\text{s}}} \tag{3.14}$$

Where $f_{\text{s}}$ is the switching frequency, $V_{\text{m}}$ is the amplitude of the source voltage, and $v_{\text{s}}$ is the peak amplitude of the triangular carrier signal.

Several researchers have used an LCL filter for two-level VSC and a better performance is obtained when compared to L/LC filters, as an LCL filter is capable of providing an attenuation of 40 dB/decade beyond the switching frequency, for a large frequency range. The main objective of using the CHMLI is to provide low switching losses because the output voltage contains fewer switching ripples compared to the conventional two-level VSC . However, a CHMLI operates at a low switching frequency compared to the conventional two-level inverter. So, the parameter

design of an LCL filter is needs to be modified, according to the operating condition of the MLI system, by following fundamental design constraints. In this study, a novel design of LCL filter is proposed for an CHMLI system operating at a lower switching frequency, to avoid the use of a large-sized bulky inductor.

### 3.4.2 Design constraints for LCL Filter [113]

The design of LCL filter for a specific type of PWM converter need to have special attention to limit losses, cost, size and complexity. The aim of the LCL filter is to reduce the higher order harmonics on the grid side. To avoid lower attenuation rate that can cause distortion increase, oscillation effects it is desired to design LCL filter with considering some factors. Therefore it is necessary to design inductor considering current ripples and filter should be damped to avoid resonance. This is keeping in highlight that the damping level is limited to cost, inductor size, losses and degradation.

- In case, the resonant frequency of the LCL filter is equal to or near to harmonics generated by inverter, instead of attenuating higher order harmonics, filter will amplify them and system is become unstable. To avoid such case the resonant frequency of LCL filter is kept away from the harmonic spectrum of the multilevel inverter. So the recommendations are to keep the resonant frequency below the half of the switching frequency. But due to extraordinary harmonics profile of multilevel inverter, the upper limit of resonant frequency can be extended, and can be more than half of the switching frequency.
- In a simple words as explained in literatures, lower limit of resonant frequency should be higher than the control bandwidth, it should be greater than ten times of the line or grid frequency.
- In the LCL filter, total value of both the inductors should be less than 0.1 pu to avoid undesirable ac voltage drop.
- The capacitor value in a LCL filter is limited by the decrease of the power factor at rated power so minimum 5 % is considered.
- In this study, passive damping is used to avoid complexity but keeping the concern that passive damping is sufficient to avoid oscillation without pertaining higher losses.

The LCL filter design is required to consider constraint of the resonance frequency, switching frequency of the inverter, and fundamental frequency of the grid system as given in Eq. (3.15).

The grid impedance may vary substantially, along with its stiffness, so the filter resonance frequency may also vary, and thus specific care must be taken when designing the filter. Current filter design practices dictate that the inductor should be small in size, while the capacitor size may vary or can be large. However, the capacitor design deals with the power factor constraint. The filter design constraint in Eq. (3.16) limits the size of the capacitor. The filter design includes two inductors that are termed as grid side inductance ($L_g$) and inverter side inductance ($L_i$) and both inductors should have an optimum value so that they work correctly for the given operation.

$$10f_g < f_{res} \tag{3.15}$$

$$C_f < 0.05C_b \tag{3.16}$$

$$C_b = \frac{1}{\omega_g Z_b} \tag{3.17}$$

$$Z_b = \frac{V_{s-LL}^2}{P_{inv}} \tag{3.18}$$

$$L_g = \frac{V_{s-phase}}{2\sqrt{6} f_s i_{ripple.peak}} \tag{3.19}$$

$$L_g = aL_i \tag{3.20}$$

Where a=1 and $C_b$ is the base capacitance, $Z_b$ is the base impedance of the system, $\omega_g = 2\pi f_g$ is the angular frequency of the grid, $V_{s\text{-}LL}$ is the line to line grid voltage, $P_{inv}$ is the inverter's rated power, $V_{s\text{-}phase}$ is the RMS value of the source phase voltage, and $I_{ripple.peak}$ is taken to be 20% of the rated current. $f_g$, $f_{res}$, and $f_s$ are the grid, resonance, and switching frequencies, respectively. The Bode diagram shown in Fig. 3.7 illustrates the performance of the LCL filter with and without damping resistances of various values (passive damping). Passive damping of the LCL filter allows the resonance to be avoided. The attenuation capability of the LCL filter is reduced over the high frequency range for high values of damping resistance $R_d$, and thus, an optimum resistance value

of 0.5 Ω is selected. The filter capacitance value is determined, based on the assumption that $C_f$ = 0.015 $C_b$.

### 3.4.3 Proposed LCL Filter for CHMLI based system

The LCL filter design procedure in the proposed work has been performed, based on the consideration that the operating switching frequency ranges from 1 kHz to 5 kHz, while the resonance frequency of the designed LCL filter is 629 Hz.The converter side inductance of the filter should be selected with particular care, because the current ripples vary substantially within a single switching period. $L_g$ is designed first, and the values of $L_i$ are subsequently chosen, accordingly. Therefore, the LCL filter offers an outstanding option for the proposed system considering various constraints. The passive/active damping methods can be used to avoid resonance issues. The passively damped system is adopted by using a damping resistance for ease of system control implementation. In this study, two inductors are taken to have equal values as in Eq.(3.20).

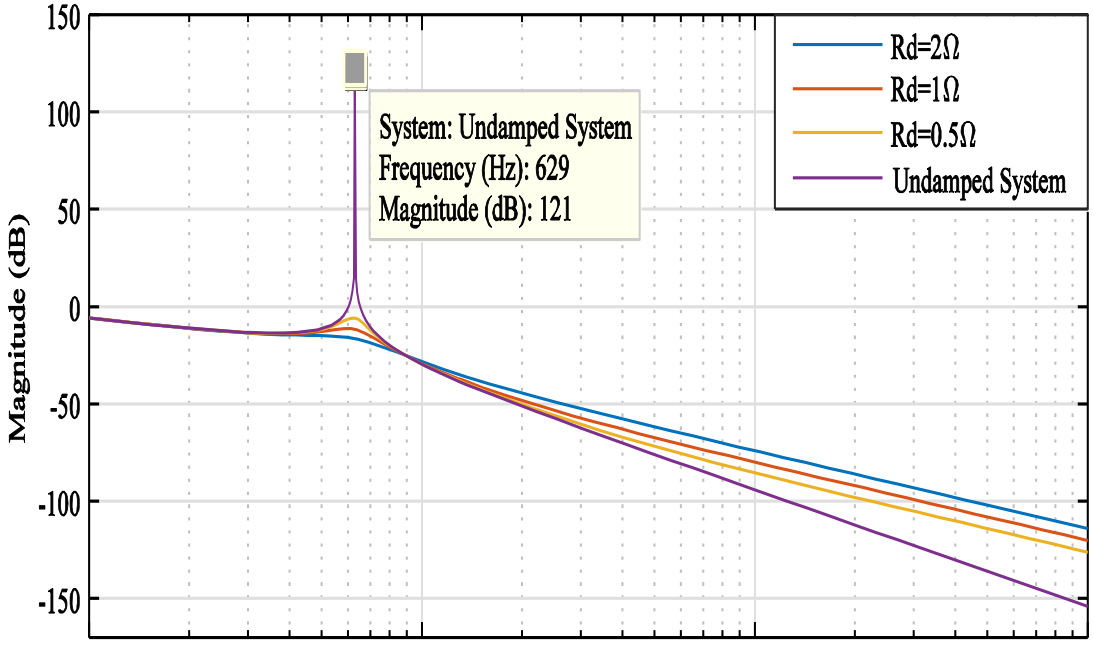
## 3.5 Performance Evaluation, Results and Discussion

The DSTATCOM system shown in Fig. 3.2 is implemented and simulated under the unity power factor (UPF) mode, to force the grid to supply the fundamental active components of the power through the proper generation of the reference current. The CHMLI-based DSTATCOM developed in MATLAB simulink was analyzed for linear and non-linear loads under UPF operation. Table 3.1 shows the values of all parameters of the proposed system. Each of these values is taken for a 1100 V line-to-line voltage system, under the condition that there are two bridges in each phase that produce the same voltage level, where a value of 450 V should be maintained across each bridge. The point of this analysis is to assess the performance of this system when using phase shift SPWM.

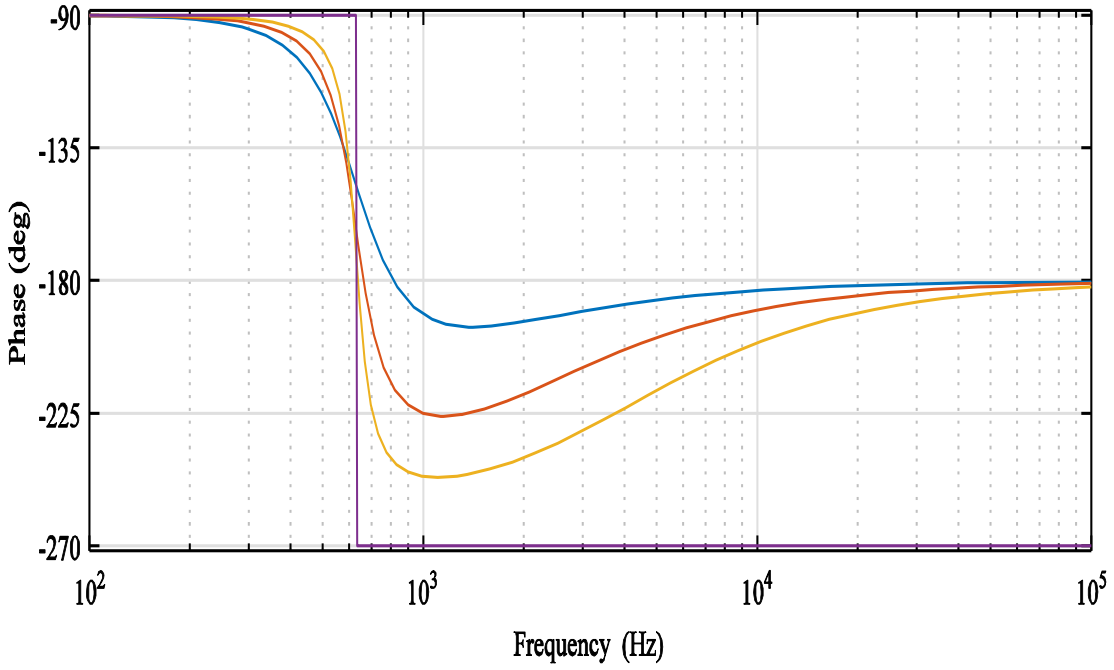
### 3.5.1 System Performance

#### 3.5.1.1 Linear Load Condition

The performance of the DSTATCOM system is analyzed considering the linear type R-L load connected to the system. The generated reference current forces the DSTATCOM to compensate for the reactive power required by the load. Therefore, the grid can operate under UPF up to the capacity of the DSTATCOM system, compensating for the reactive power.




(**a**)




(**b**)

**Figure 3.5.** Bode diagram of the LCL filter. (**a**): Magnitude vs. Frequency; and (**b**): Phase vs. Frequency

**Table 3.1 Parameters for the DSTATCOM system**

| S.No. | Simulation Parameter | values |
|---|---|---|
| 1. | Source voltage | $V_{s-LL}$ =1100 V |
| 2. | Frequency | $f_g$=60 Hz. |
| 3. | Sources impedance | $R_s$ = 0.01 Ω and $L_s$ =1.6 mH |
| 4. | LCL Filter Parameter | $L_g$ = 1.6 mH, $L_s$ = 1.6 mH, $C_f$ = 80 μF $R_d$ = 0.5 Ω |
| 5. | DC link voltage per cell | $V_{dc-bus}$= 450 V |
| 6. | $K_p$, $K_i$ | $1.2 \times 10^{-3}$, $7 \times 10^{-4}$ |
| 7. | Capacitor | $C_{dc-cascade}$= 800 μF |
| 8. | Switching Frequency | $f_s$= 1kHz–5kHz |
| 9. | Linear Load | 65 KVA 0.8 PF lagging |
| 10. | Non Linear Load | Rectifier load $R$ = 50Ω, $L$ = 500 mH |
| 11. | Unbalanced load | In phase C 10 KVA |

The PCC voltage corresponding to the DSTATCOM output is demonstrated in Figures 3.6–3.9. For the DSTATCOM performance evaluation load, the source and DSTATCOM current is shown in Figures 3.10–12 for a linear, unbalanced, and non-linear load, for a time duration of 0–15 s, 0.15–0.30 s, and 0.30–0.45 s, respectively. The load source current and DSTATCOM current under a balanced load condition from time $t$ = 0–0.15 s, are demonstrated in Figure 3.10(a)–(c), respectively. The linear load connected to the system switched to the unbalanced condition at time $t$ = 0.15–0.30 s, by disturbing phase 'c' of the load. The source current was maintained in the balanced condition during unbalance in the system as the unbalanced compensating current provided by the DSTATCOM. The compensating current enables the source current to supply balanced active power to the load, as shown in Figure 3.11a–c, during an unbalanced condition.

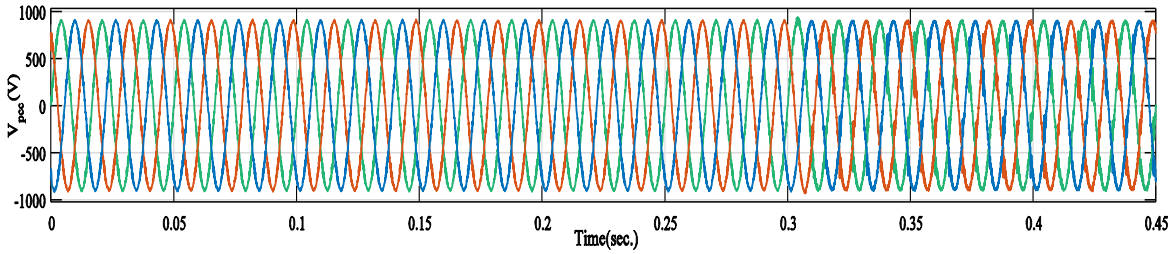



**Figure 3.6**. Point of common coupling (PCC) voltage under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

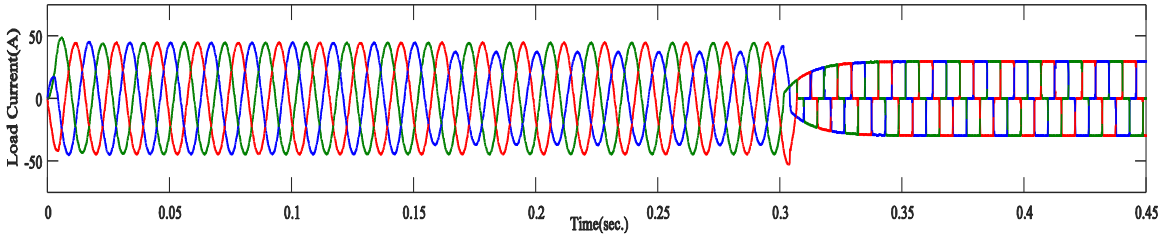



**Figure 3.7**. Load current under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

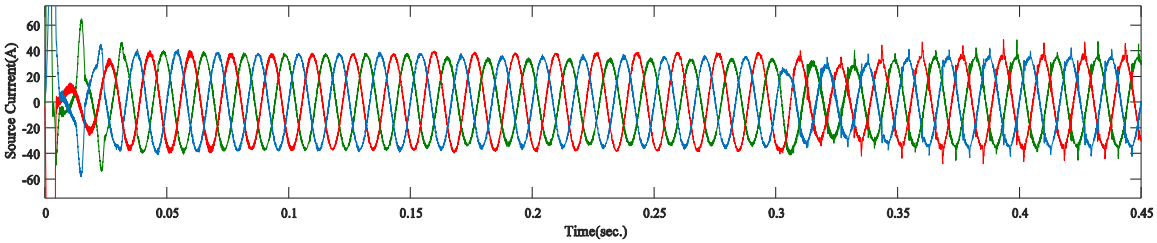



**Figure 3.8**. Source current under a balanced load (0.8 PF), unbalanced load, and nonlinear load at a time of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

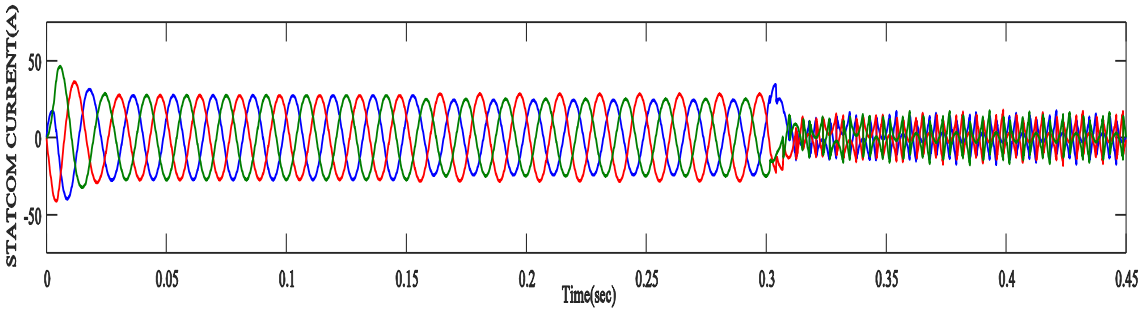



**Figure 3.9**. DSTATCOM current under balanced (0.8 PF), unbalanced, and non-linear loads at times of 0–0.15, 0.15–0.3, and 0.3–0.45 s, respectively.

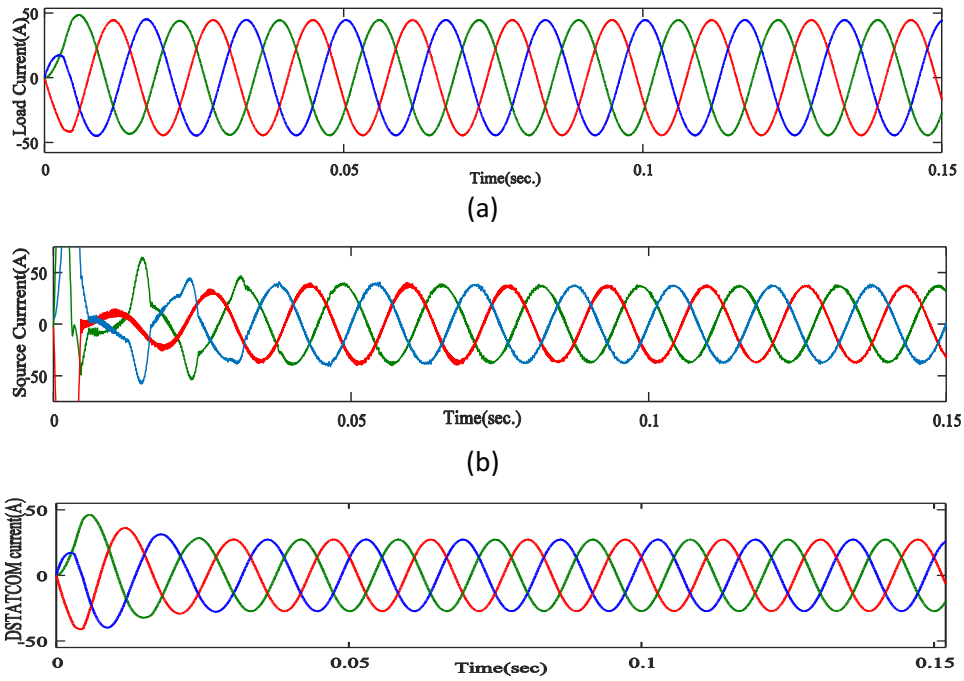



**Fig 3.10** Currents under linear load condition.

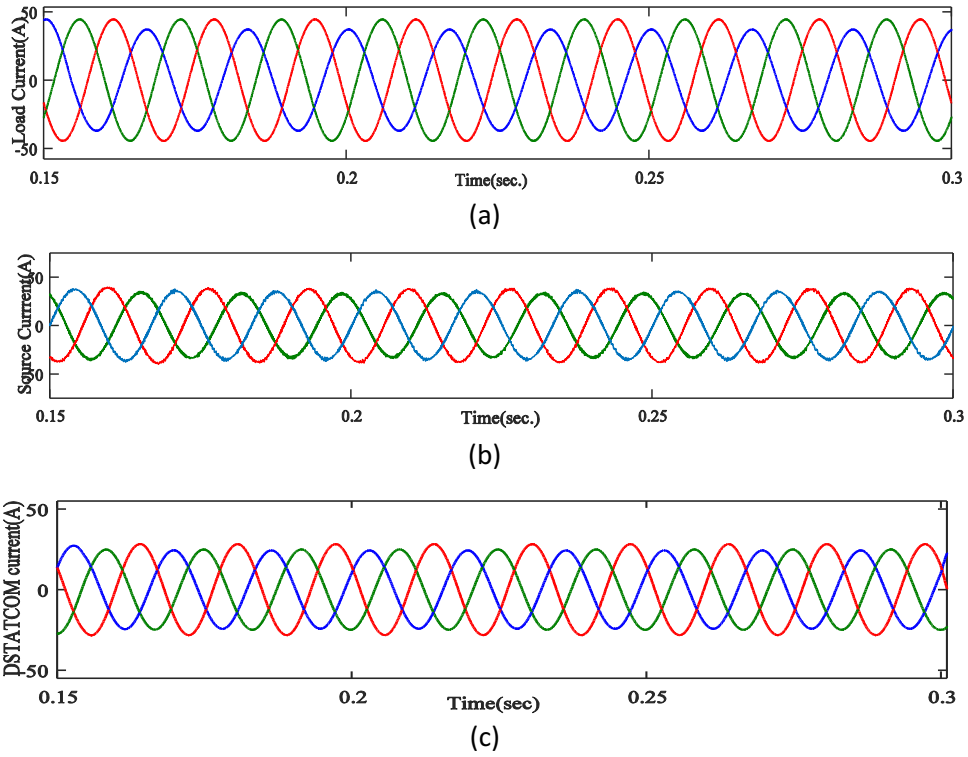



**Fig.3.11** Currents under unbalanced load conditions.

### 3.5.1.2 Non-Linear Load Condition

The DSTATCOM system was investigated considering the non-linear load condition needed to validate the system performance. The diode bridge rectifier with a R-L load was considered to be a non-linear type load, and was connected to the system at $t = 0.3$ s. The PCC voltage of the system, as shown in Figure 3.6, is maintained under a non-linear load condition. The harmonic compensating current provided by the DSTATCOM, as shown in Figure 3.12(a)–(c), forced the source current, supplying the active power component. The power supplied by the source, the DSTATCOM, and the power required by the load, are demonstrated in Figures 3.13–3.15 for linear and non-linear load conditions.

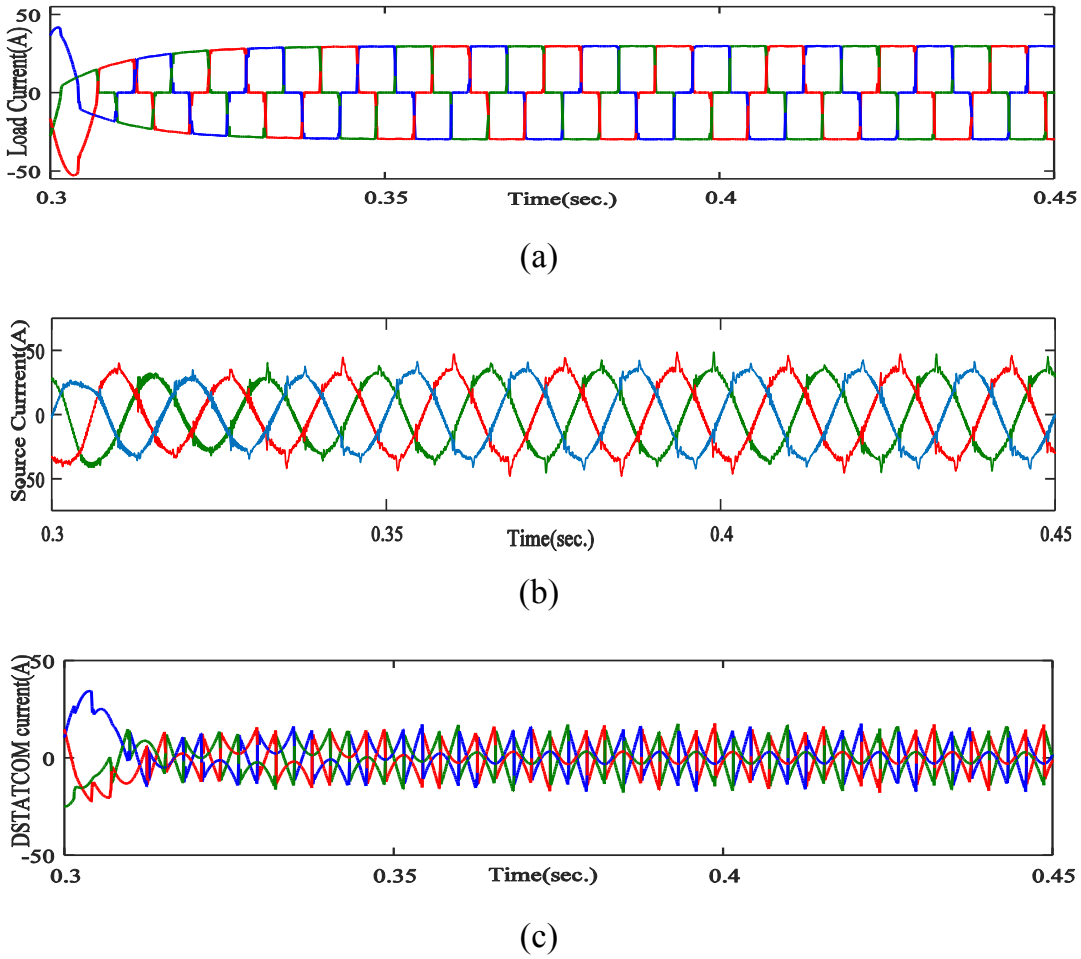



**Figure 3.12.** Currents under nonlinear load conditions. (**a**) Load current; (**b**) source current; and (**c**) DSTATCOM current.

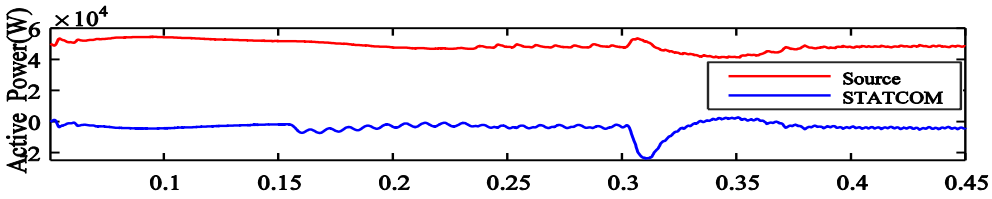



**Figure 3.13**. Active power supplied by source and DSTATCOM under different load conditions.

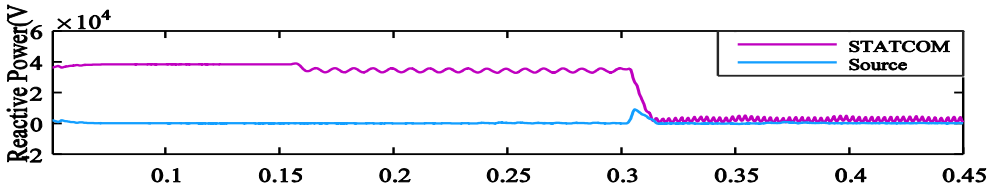



**Figure 3.14**. Reactive power supplied by source and DSTATCOM under different load conditions.

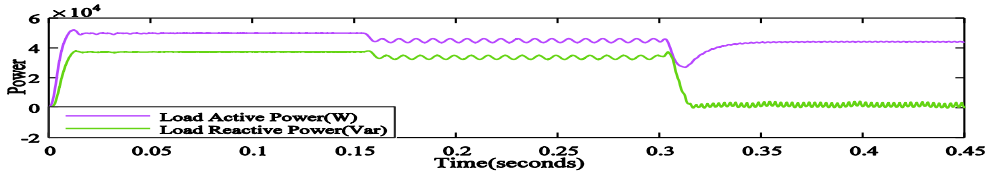



**Figure 3.15.** Load power required under different load conditions.

### 3.5.2 Power Quality Analysis

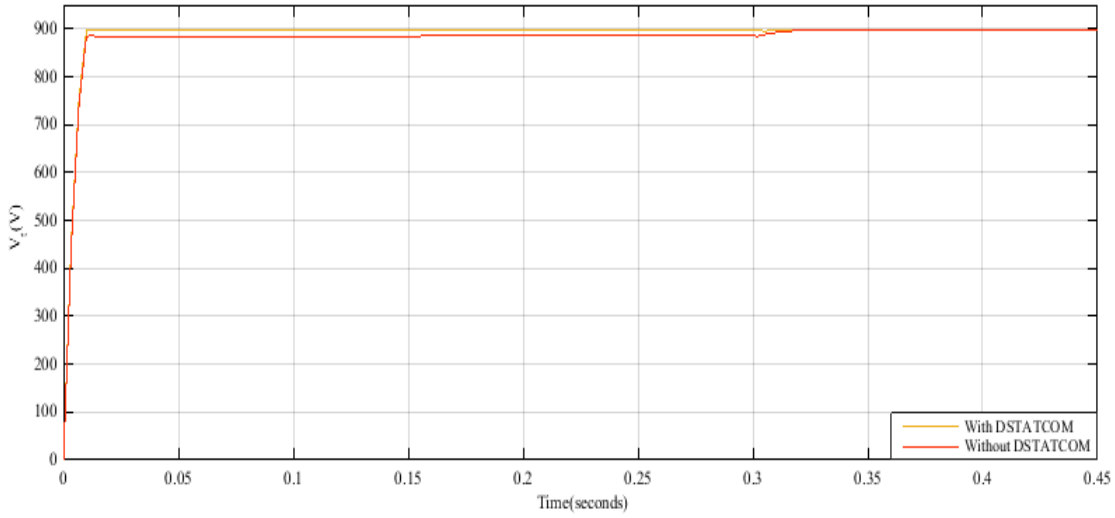
#### 3.5.2.1 Voltage Disturbance

The change in load creates a disturbance in the PCC voltage of the system, resulting in voltage sag/swell. The DSATCOM system is capable of maintaining the PCC voltage under the normal condition, by supplying a compensating current. The PCC voltage shown in Fig.3.18 (a) is balanced under the disturbance, caused by the unbalanced load condition and change in load. The terminal voltage at the PCC ($V_t$), computed using Eq. (3.10), is examined to investigate the performance of the DSTATCOM and is used as a validation of its effectiveness. The reference $V_t$ can be computed as in Eq.3.21:

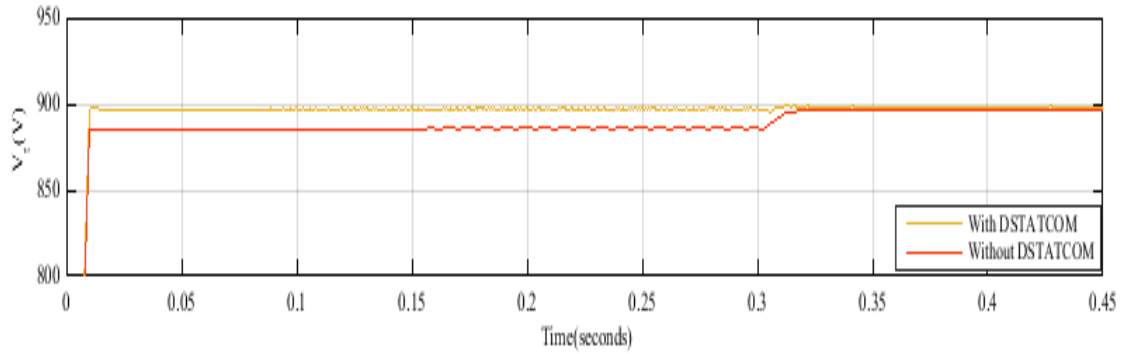
$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)} = \sqrt{\frac{2}{3}\left(3\left(\frac{1100}{\sqrt{3}}\right)^2\right)} = 898\ V \qquad (3.21)$$

The PCC voltage of the system shown in the Fig.3.16 demonstrates the condition of the DSTATCOM when it is connected and unconnected to the system. The system without

DSTATCOM is unable to maintain the $V_t$ under a linear load condition and changes when there is perturbation, due to the connection of a non-linear load in the system. Therefore, the effectiveness of the CHMLI-based DSTATCOM is investigated for $V_t$, considering the voltage disturbance due to perturbation in the load.




(a)




(b)

**Figure 3.16.** (**a**) Peak amplitude of PCC voltage during load change; and (**b**) zoomed view.

### 3.5.2.2 Fast Fourier Transform Analysis

As the switching frequency changes (i.e., increases in this case), the other important system parameter that is affected is the source current, and the THD in the source current decreases under linear load conditions, as shown in Table 3.2. Therefore, for a better application of the proposed

system, the frequency should be high, while for a multilevel operation, the frequency should be kept within optimal limits (1 kHz) to ensure that the switching losses do not exceed acceptable limits, as shown in Figures 3.17–3.19.

**Table 3.2** Source current THD (Total harmonics distortion) under different switching frequencies.

| S.No. | Switching Frequency (kHz) | Source Current (THD %) |
|---|---|---|
| **1.** | 1 | 0.62 |
| **2.** | 2 | 0.58 |
| **3.** | 3 | 0.53 |
| **4.** | 4 | 0.48 |
| **5.** | 5 | 0.43 |

A current THD of less than 5% is acceptable, as per IEEE Standard 519-1992 (IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems). The reduction in the source current distortion illustrates the effectiveness of components such as the MLI, the LCL filter, and the DC link capacitor, and that of the switching technique at different frequencies. To provide a complete DSTATCOM design with an appropriate control algorithm to prevent losses, avoid system complexity, and maintain operational stability, the control algorithm and all of the parameters must be selected correctly.

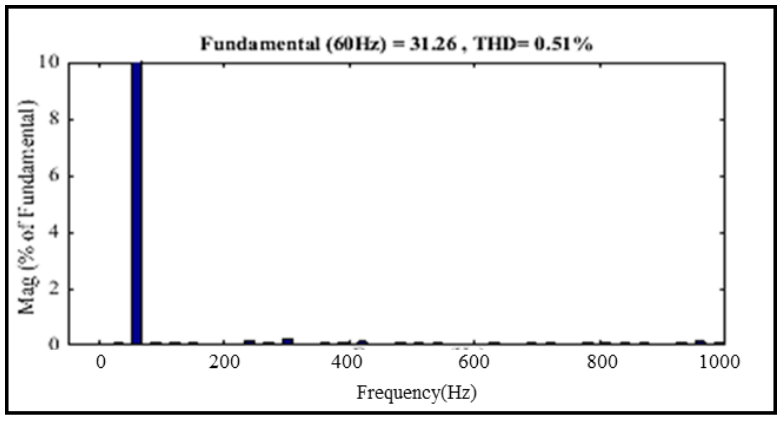



**Figure 3.17** THD of source current under linear load conditions.

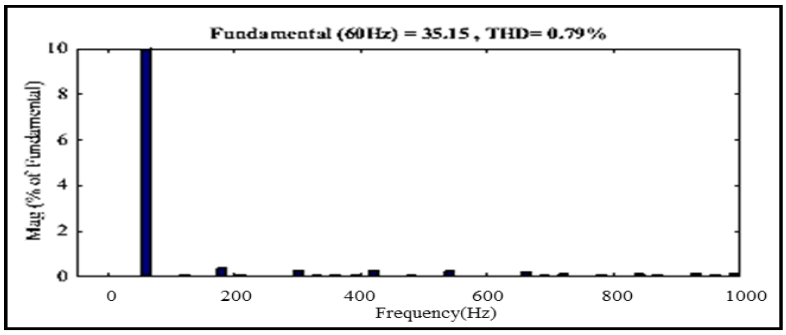



**Figure 3.18** THD of source current under unbalanced load conditions.

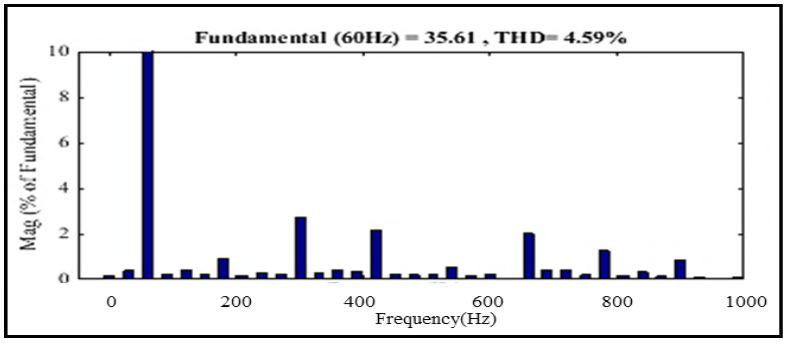



**Figure 3.19** THD of source current under nonlinear load conditions.

### 3.5.3 Effect of System Parameters

#### 3.5.3.1 DC Link Capacitor

In this analysis of the DSTATCOM, the two important components that have been analyzed are the DC link capacitor and the coupling filter. The DC link capacitor is a prominent part of the proposed DSTATCOM system, in that each H-bridge cell contains an isolated DC link capacitor. In custom power device applications, it is desirable for the DC link capacitor to be small in size when compared with the AC capacitor bank, to compensate for the same amount of reactive power.

The modulation index is kept constant by the insertion of a proportional controller into the system. The proportional controller maintains the amplitude of the error signal that is obtained by comparing the reference current with the source current. These parameters affect the capacitor value and vice versa, as depicted in Eq. (3.6); this is verified by various results that were obtained by correct modelling of the system. The DC link capacitance affects the ripple in the DC bus voltage, irrespective of the applied filter.

While the system operation is quite complex, it is often found that the value of the DC link capacitor is also a very important factor in the current system, so further analysis is conducted based on different capacitor values and the performance is illustrated in the results. As the results show, different capacitor values produce different overshoot values, which can be easily understood using the results presented here.

The voltage ripple in the DC link is inversely proportional to the capacitance value. This means that to produce a lower ripple in the DC link, it is necessary to choose the optimum capacitor value. The relationship between the voltage ripple and the capacitance is illustrated by the results shown in Fig. 3.20(a)–(c), which were obtained using capacitor values of C=650, 950, and 1200 µF during linear load operation of the DSTATCOM. The simulation results obtained verify the relationship expressed in Eq. (3.6) and we see that as the capacitor value increases, the ripples in the DC voltage decrease.

### 3.5.3.2 Switching Frequency

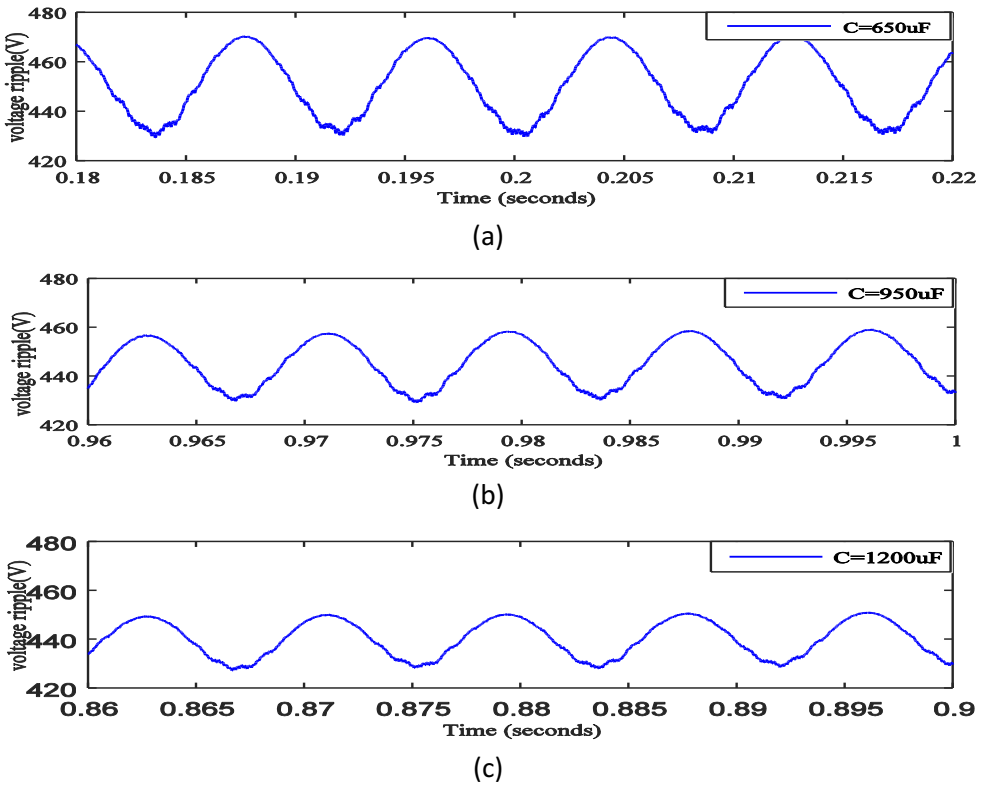



**Fig. 3.20 DC** bus voltage ripples for different capacitors.

In this paper, the LCL filter is proposed for a lower switching frequency range and the differences in the system performance under these conditions are also analyzed. The analysis is also conducted on the basis of the switching frequency, as it varies from 1 kHz to 5 kHz. As we see, the switching frequency does not affect the DC voltage ripples in this case, and subsequent results confirmed that a variation of the switching frequency does not affect the DC voltage ripples, as shown in Figure 3.21. The magnitude of the ripples is almost identical for the three different switching frequencies.

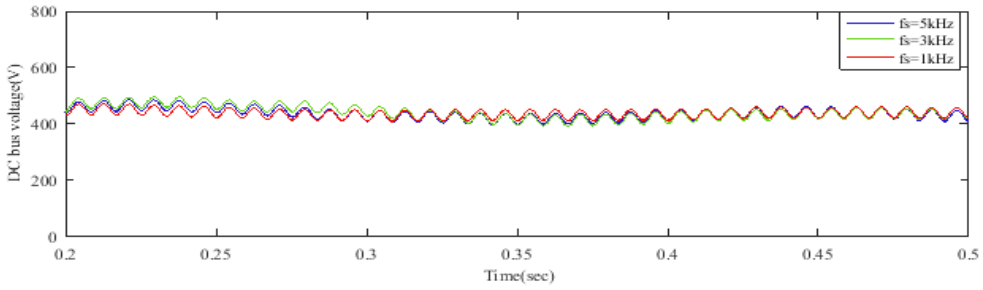



**Figure 3.21.** DC bus voltage of 450 V and voltage ripples at different switching frequencies.

## 3.6 Conclusion

The novel design of LCL filter is proposed considering the modified constraints for a lower operating switching frequency (1–5 kHz) of CHMLI. Combination of LCL filter and CHMLI for grid connected application has better solution to the power quality issues. The effect of system parameters on the DSTATCOM system is also considered for the analysis. The DC-link voltage for each H-bridge is maintained at e referenced value using PI controller. The power quality issues are investigated for a disturbance in the PCC voltage (voltage sag and swell) under an unbalanced load and load change condition. The source current THD under different load conditions (0.51% linear load, 0.79% unbalanced load, 4.59% nonlinear load) is achieved and is well within the IEEE-519 standards of 5%. The effect of switching frequency and the DC link capacitor on the DC link voltage ripples is investigated, to provide the optimum selection of system parameters.

# CHAPTER 4

## Multiband Hysteresis Current Controlled CHMLI

### 4.1 General

Power electronics converters are an essential part of modern electrical energy conversion system. Application of these converters is extended to power distribution and transmission system. Power electronics technology become one of the leading solutions to issues like increasing cost and unsustainable demand for electrical energy. Usually, two level three phase VSI is used for dc-ac conversion involved in different industrial processes and renewable energy source integration to the grid. It's become essential to use bulky filter inductance and electromagnetic transformers with VSIs when it is used in medium voltage and high power application. Some contribution for the improvement of efficiency in the conventional inverter is attempted in and further improvisation is still under research. However high electromagnetic interference, large inductance size, and high power stress on devices are major concerns related to conventional VSI.

As explained in chapter 1, multilevel inverters (MLIs) evolved as better option to replace conventional VSI in some application. Expansion of MLI application to other areas are still in the process of research. MLI is used to overcome limitation associated with the conventional VSI. Some of the major application of MLIs are active power filter, electric vehicles, locomotives traction drives, motor drive application. Some of the primary advantages associated with the MLIs are the higher quality of output voltage, less power stress on devices, electromagnetic interference less operation.

In last one decades many closed loop controllers have been emerged as a better option because these controllers offers close loop implicit modulator with in controller. These controllers are termed as direct controller and conceptually simple for the digital implementation in the system to generate switching signal for the inverter as in direct consequence of the controller avoiding extra burden of modulator. During last decade these type of controller which itself works as a modulator has been successfully introduced to the industry level. For example hysteresis current control or

direct torque current control are in the conventional formulation are comprises implicit modulation with in direct controller

CHMLI possess some merits compared to other topologies such as modularity in structure, reliability, less number of component, fault-tolerant capability. Some limitation or drawbacks of the CHMLI are the requirements of isolated dc supply and dc bus voltage control if used in active power filter application. It is more complex to operate and switching control of CHMLI due to a large number of power semiconductor devices involved compared to conventional VSI.

Switching control of CHMLI is the important part of the system always because some control techniques involve generation of gate signal within itself. Some control techniques which are accepted industrially are sinusoidal pulse width modulation (SPWM), space vector modulation (SVM). SPWM techniques are commonly used in many application of CHMLI. Some of the benefits using SPWM technique in a close loop system, are increased input power factor, decreased harmonic distortion, linearity. Hysteresis current control (HCC) is widely used for conventional VSI because it offer dynamic control with implicit modulator. Hysteresis current control for MLIs have been recently proposed. Working of basic hysteresis control works on logic of hysteresis band. HCC for conventional VSI has been adopted commercially in different applications such as motor drives, electric vehicle, pumps, industrial automation, robotics, active power filter, DSTATCOM etc. HCC for the multilevel inverter has been proposed for the application of multilevel inverter based DSTATCOM, hierarchical switching pattern is required to generate stepped synthesized output of CHMLI. Variable switching frequency, complex design of signal conditioning filter, linearization of HCC are attempted to overcome the limitation of conventional HCC. Implementation and digitalization of modern controller has virtuous effect on system efficiency and robustness.

Digital controller have been employed to improve efficiency and reliability of analog based controller. Implementation of HCC on digital platform for traditional inverters have been attempted since last few years. Effect of sampling frequency is analyzed for digitally controlled HCC, sampling frequency adjustment for nearly constant switching frequency is proposed in for single phase grid connected inverter. Modern digital control platform have significant importance in a Grid connected systems for active load or renewable energy integration.

In this chapter a new digital HCC is proposed for the CHMLI operation in grid connected mode with its implicit modulation. Digital implementation of HCC is achieved using S-R flip-flops, digital multiband HCC offers better dynamics and re-configurability by its digital means. It is desired to operate gird in UPF mode even when connected to inductive load. So avoiding complex controller design, A digital multiband HCC is employed which is capable of control and implicit modulation. Simulation and experimental work is demonstrated for the proposed controller.

## 4.2 Grid Connected Cascaded H-bridge Multilevel Inverter

The multilevel topologies are being used for grid connected system by replacing traditional converters. CHMLI offers modularity, reliability, and fault tolerant nature with the ease in change of voltage levels and switching frequency. Single phase grid connected system is considered for the performance evaluation of the controller and its implicit modulator to attain multilevel output voltage. Further change (increase or decrease) of levels in output voltage and power rating can be easily done due to hierarchical structure of CHMLI. Grid connected CHMLI is shown in Fig. 4.1 with inductor L load and grid or motor with back emf of $v_s$ .

### 4.2.1 Control Strategy

There are many stablished control techniques available for grid connected system or motor drive system has been commercially accepted. For the inverter to follow its objective in a current control technique, user defined current tracking is a major concern. It means control of the system is dependent on the current flowing in the control loop. Similar to traditional VSIs, CHMLI also requires higher dynamic control for better inner current control loops. These control techniques are classified as linear or non-linear control techniques. Major expectations from a robust controller for a close loop system are: better dynamics, wider bandwidth of controller, reduced steady state error, reduced transient time and lesser complexity on implementation. Modulation of CHMLI with tracking of desired reference current multiband HCC is selected and have advantages over SPWM and SVM such as ease in implementation, better dynamics, and wider bandwidth almost desired minimum steady state error for controller. Actual current is compared with the desired reference current and current error is fed multiband HCC to achieve multiple gate signal for higher number of switches as shown in Fig4.2.Hysteresis bands should be divided in

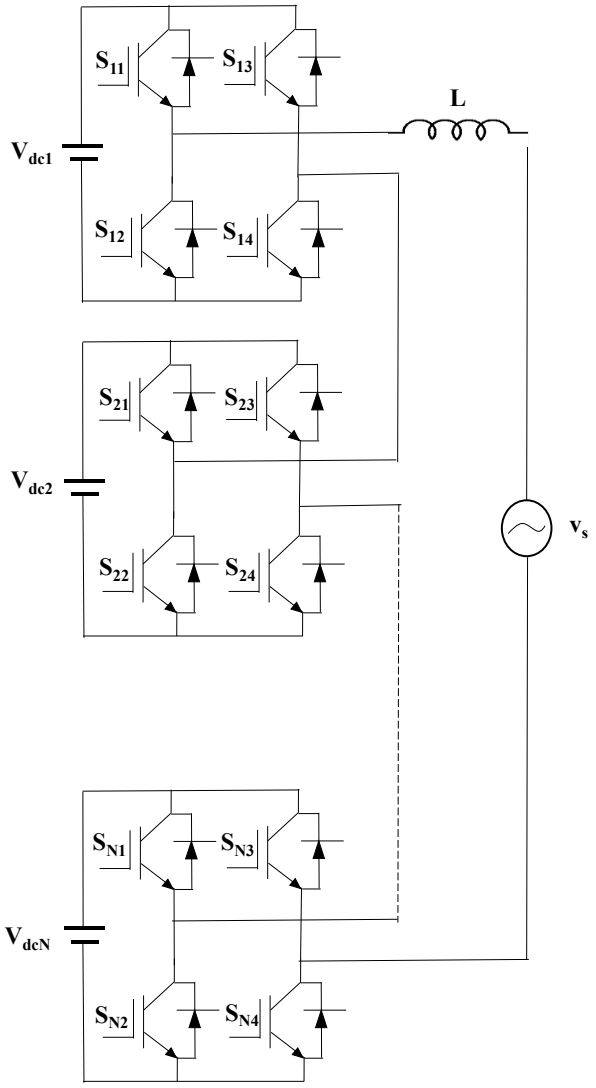



**Figure 4.1** Grid connected CHMLI

hierarchical manner to get synthesized multilevel output of CHMLI. Similarly during implementation on digital platform subdivision and hierarchy should be followed to achieve better dynamic performance.

The complete control strategy is depicted in block diagram in Fig. 4.2, single phase grid connected CHMLI and FPGA based digital control setup. PLL is used for synchronization of grid voltage and reference current. Actual current is sensed using current sensor and sampled input of reference and actual current is fed to the FPGA based controller using high speed analog to digital converter (ADC). The digital multiband HCC is prototyped in XSG based fixed point simulation and controller porotype to generate VHDL code to bit stream generation. The gate signals are isolated through isolator to provide gate signal to two H-bridges of five level CHMLI.

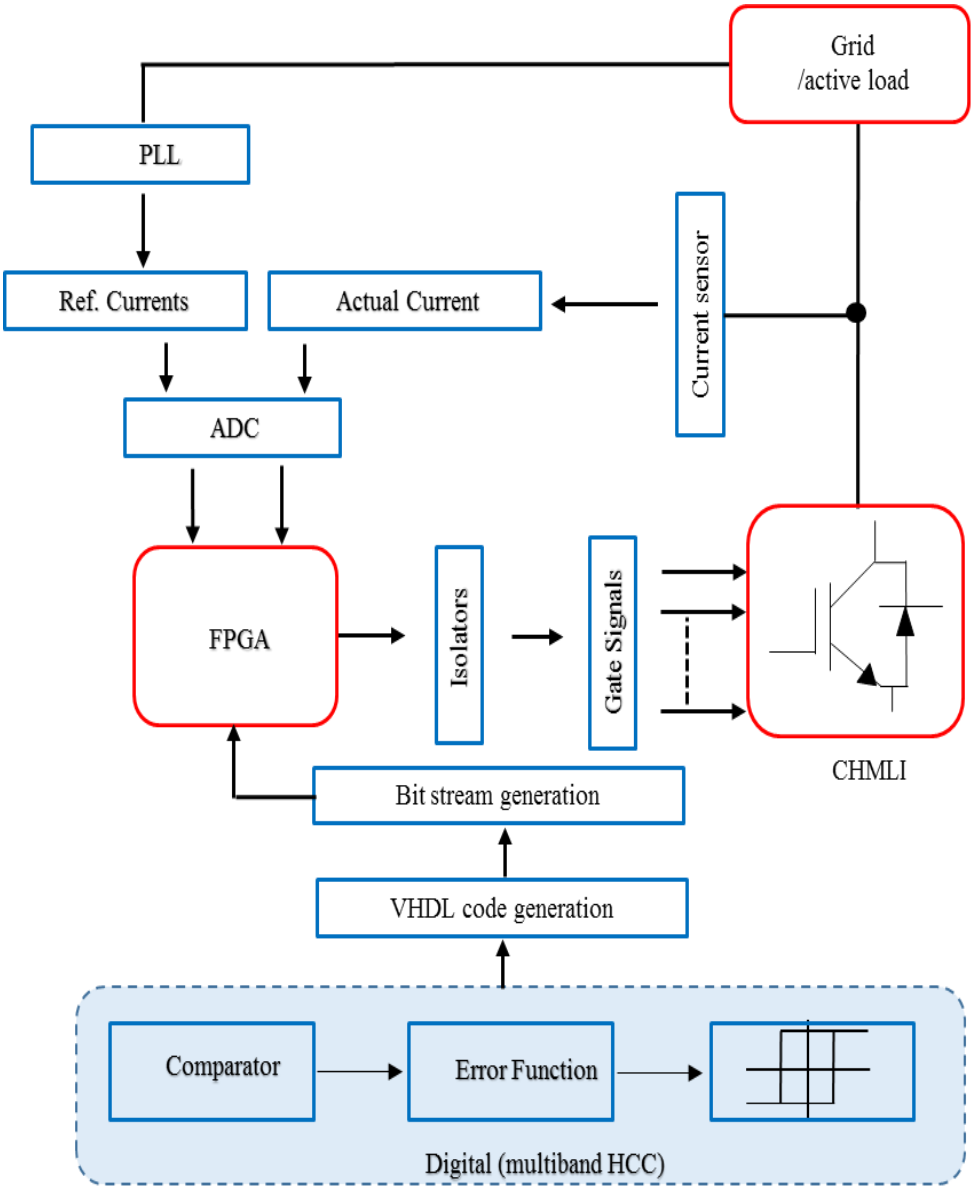



**Figure.4.2** Block diagram of control strategy for digital multiband HCC.

## 4.3 Digital Hysteresis Current Control for CHMLI

Current regulation using HCC for CHMLI can be achieved by subdivision of hysteresis band. Essentially hysteresis current control for conventional converters has been used and implemented by feeding sampled error to analog circuitry of relays. The basic functioning of relays and switching transition rule based on tsypkin‘s method has been used. For the implementation on the digital platform one need to have high level programming skill or interconnection of analog to digital platform should be done. In this paper digital multiband HCC is implemented using logical

operation of SR flip-flop by feeding the reference current and actual current using analog to digital converter. Number of divisions for hysteresis band is depends on the number of levels required for the CHMLI output. Unlike two level inverters, operation of HCC for CHMLI corresponds to multiple bands. When current error reaches to corresponding band limit, next lower or upper level of voltage should be selected for ensuring the commutation of single switch in the same leg. In multiband operation it might be possible that state of inverter does not adequate to enforce current error to zero, consequently CMHLI should be switched to next lower or high voltage level. This can be possible by selecting proper voltage level in between different bands so that it reverses the current error direction simultaneously. The parameter δ is introduced as dead band between each adjacent segment of divided hysteresis band. The net hysteresis band decides continuous switching frequency consequently the total switching losses and total harmonics distortion in output voltage and current.

### 4.3.1 Multiband HCC

#### 4.3.1.1 Three level operation

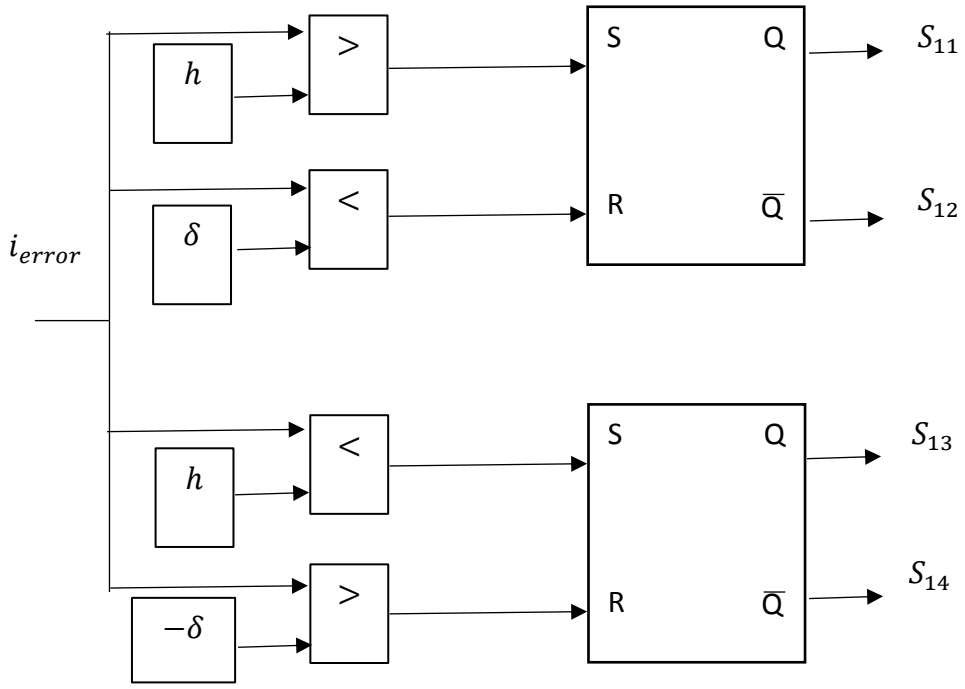



**Figure 4.3** Multiband HCC for thee level inverter.

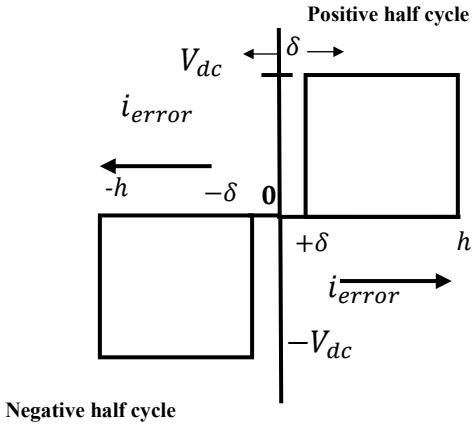



**Fig.4.4** Output voltage and hysteresis band variation.

For three level CHMLI it is required to divide band in two equal parts. For bipolar switching CHMLI the half band corresponds to positive half cycle and remaining half band correspond to negative half cycle of output voltage. Operation of multiband HCC for three level inverter that consist single H-bridge cell is shown in Fig.(4.3) and (4.4) Considering single H-Bridge cell the two bands corresponds to limit then current within considerable magnitude of error. Instantaneous current error is fed to digital HCC controller and upper and lower bands are provided to generate gate signals for primary switches $S_{11}$ and $S_{13}$ of H-bridge inverter. Inverted gate signals are provided to complimentary switches of corresponding legs. As shown in Fig4.5,for positive half cycle actual current ripples are lies between lower band and reference current in results Gate signal $S_{11}$ are generated and corresponding output voltage $v_{mli}$ toggles between 0 to $+V_{dc}$. For negative half cycle, actual current ripples lies between upper band and reference current, in results gate signal for $S_{13}$ is generated and corresponding output voltage toggles between 0 to $-V_{dc}$. So the three level of voltage i.e. $+V_{dc}$,0,$-V_{dc}$ is obtained using logical operation of S-R flip flop. Dead band δ is introduced to avoid overlapping of switches, functioning and synthesize the CHMLI output. As referred to three level operation dead band of δ is inserted at 0 + δ and 0 - δ. Following algorithm describes the three level ($-V_{dc}$,0, $V_{dc}$) inverter modulation,

Positive half cycle:

$i_{error} > +\delta$

$V_{mli} = V_{dc1} = V_{dc}$ $\qquad\qquad$ $for\ i_{error} > \delta\ , and\ i_{error} < h + \delta$

$V_{mli} = 0$ $\qquad\qquad$ $for\ i_{error} < +\delta$

In this case semiconductor switches are operated at switching frequency corresponding to band between h and $+\delta$ and output voltage toggles between (0, $V_{dc}$).

Negative Half cycle:

$i_{error} < -\delta$

$V_{mli} = -V_{dc1} = -V_{dc}$ $\qquad\qquad$ $for\ i_{error} < -\delta\ , and\ i_{error} < -(h + \delta)$

$V_{mli} = 0$ $\qquad\qquad$ $for\ i_{error} > -\delta$

In this case semiconductor switches are operated at switching frequency corresponding to band between -h and $-\delta$ and output voltage $v_{mli}$ toggles between (0, -$V_{dc}$). is observable that the positive and negative half cycle operation for quasi-symmetrical output of CHMLI obtained on net band width of 2 |h-δ|.

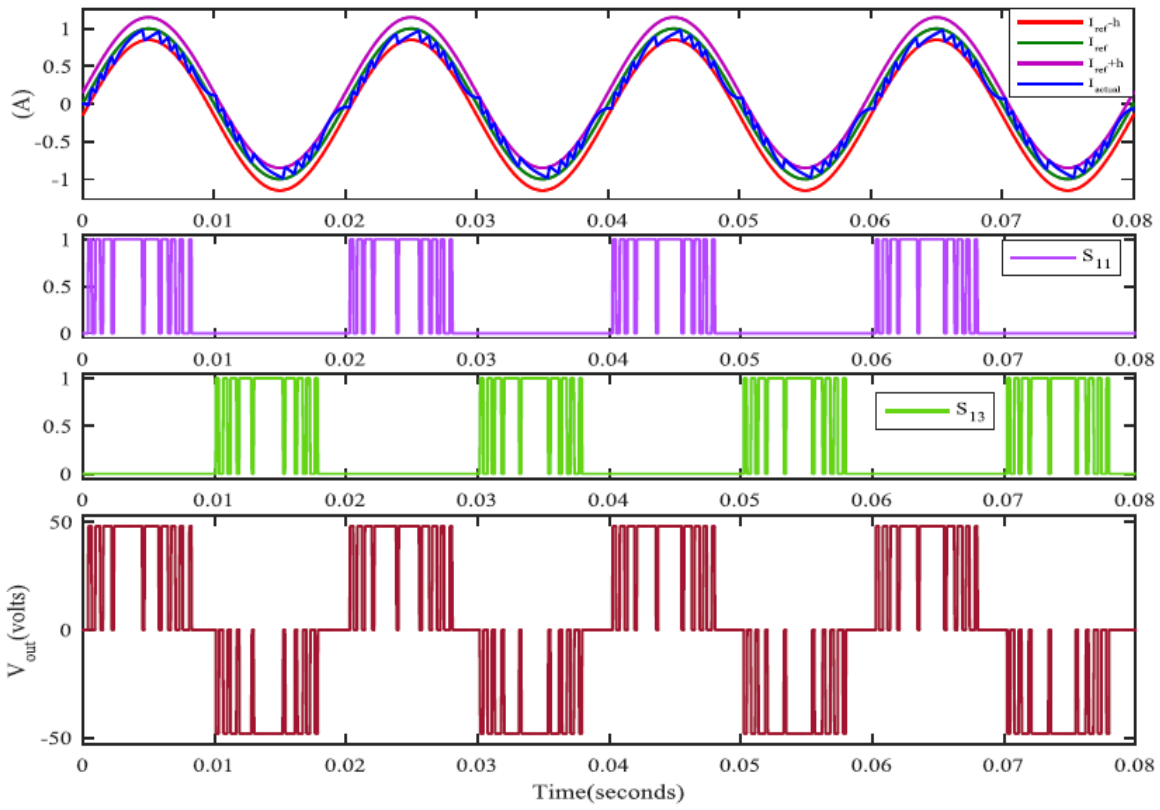



**Figure 4.5** Multiband HCC controlled inverter output voltage with corresponding gate signals and actual current with reference current for three level inverter.

### 4.3.1.2 Five level operation

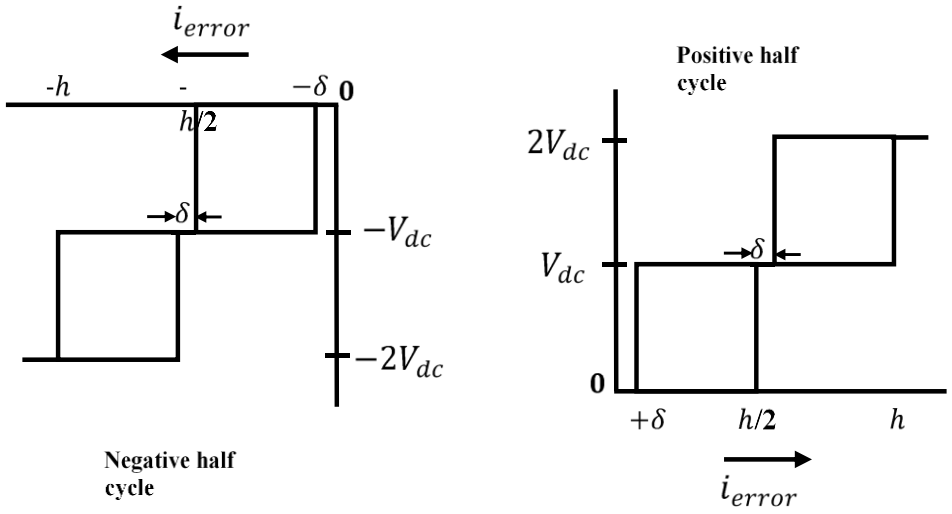



**Figure 4.6(a)** Output voltage and hysteresis band variation,(b) Multiband HCC for the Five Level Inverter

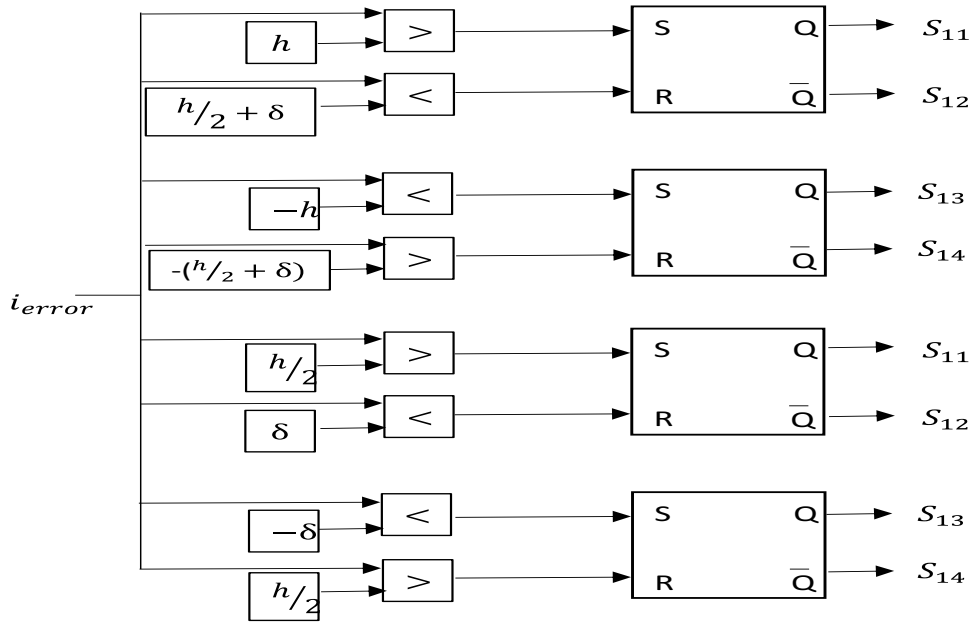



**Figure 4.6(b)** Multiband HCC for the Five Level Inverter

In case of five level CHMLI the number of required division in bands are four and therefore equally divided bands for three level inverters are subdivided in two parts and responsible for Negative half cycle and positive half cycle. Multiband HCC operation for five level inverter consist two bridges as shown in Fig.4.1Current error is fed to Multiband HCC and corresponding four bands

are fetched to limit the current error between adjacent bands to generate output of five level. S-R flip flop based five level HCC is shown in Fig 4.6. Switches $S_{11}$, $S_{13}$, $S_{21}$, $S_{23}$ are primary switches of two bridges connected in cascade for five level inverter and $S_{12}$, $S_{14}$, $S_{22}$, $S_{24}$ are complementary switches operating at same switching frequency as their primary switches. Dead band δ is introduced to avoid overlapping due to switching function and synthesize the CHMLI output. As referred to five level operation dead band of δ is inserted at-$(\frac{h}{2}+\delta)$,-δ,+δ, and $(\frac{h}{2}+\delta)$.

Positive half cycle:

Case (i)

$i_{error} > +\delta$

$V_{mli} = V_{dc1} = V_{dc}$ $\quad for\ i_{error} > +\frac{h}{2}, and\ i_{error} < \frac{h}{2}+\delta$

$V_{mli} = 0$ $\quad for\ i_{error} < +\delta$

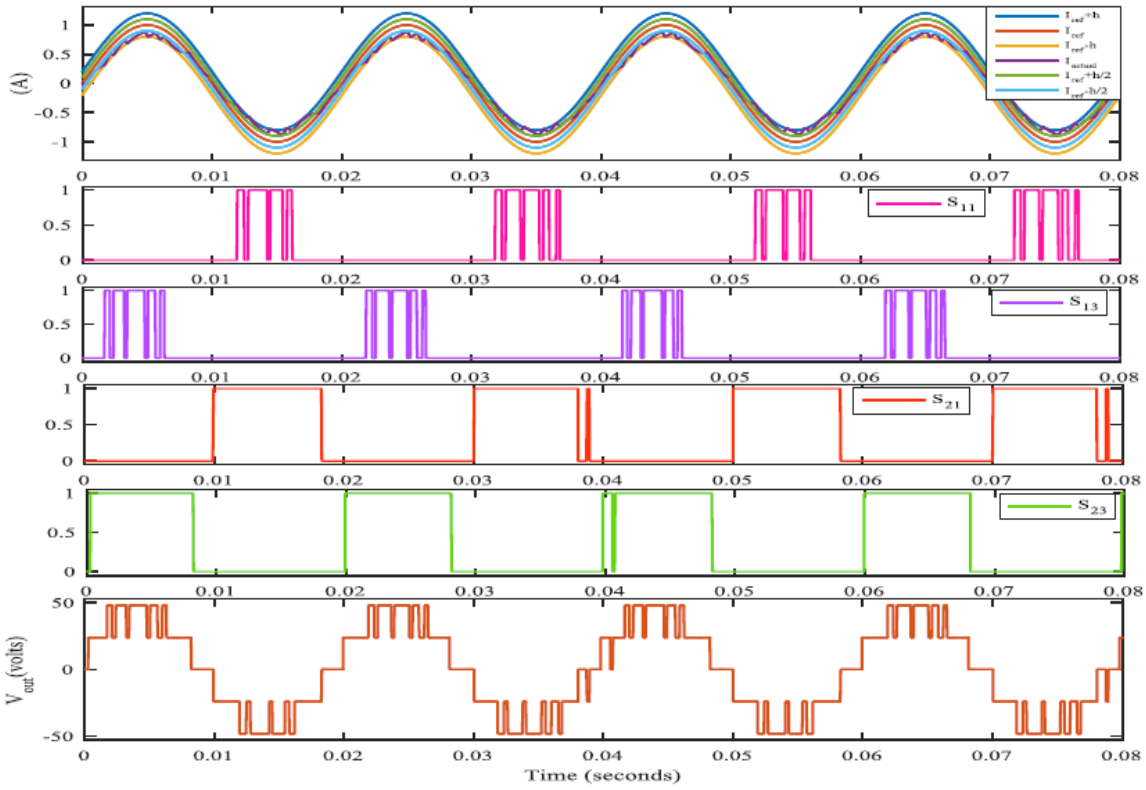



**Figure 4.7** Multiband HCC controlled inverter output voltage with corresponding gate signals and actual current with reference current for five level inverter.

In this case semiconductor switches are operated at switching frequency corresponding to band between $\frac{h}{2}$ and $\delta$ so output voltage toggles between (0, $V_{dc}$).

Case (ii)

$$i_{error} > \frac{h}{2} + \delta$$

$$V_{mli} = V_{dc1} + V_{dc2} = 2V_{dc} \qquad for\ i_{error} > h$$

$$V_{mli} = V_{dc1} = V_{dc} \qquad for\ i_{error} < \frac{h}{2} + \delta$$

In this case semiconductor switches are operated at switching frequency corresponding to band between $h$ and $\frac{h}{2} + \delta$ and output voltage toggles between ($2V_{dc}$, $V_{dc}$).

Negative half cycle:

Case (i)

$$i_{error} < -\delta$$

$$V_{mli} = -V_{dc1} = -V_{dc} \qquad for\ i_{error} < -\frac{h}{2}, and\ i_{error} < -(\frac{h}{2} + \delta)$$

$$V_{mli} = 0 \qquad for\ i_{error} > -\delta$$

In this case semiconductor switches are operated at switching frequency corresponding to band between $\frac{h}{2}$ and $\delta$ output voltage toggles between $(-V_{dc}, 0)$.

Case (ii)

$$i_{error} < -(\frac{h}{2} + \delta)$$

$$V_{mli} = -(V_{dc1} + V_{dc2}) = -2V_{dc} \qquad for\ i_{error} < -h$$

$$V_{mli} = -V_{dc1} = -V_{dc} \qquad for\ i_{error} > -(\frac{h}{2} + \delta)$$

In this case semiconductor switches are operated at switching frequency corresponding to band between $h$ and $\frac{h}{2}+\delta$ and output voltage toggles between$(-V_{dc}, -2V_{dc})$. it is observable in Fig4.7 for five level operation too, the positive and negative half cycle operation for quasi-symmetrical output of CHMLI obtained on net band width of $2|h-\delta|$.And two bridges are operating for three

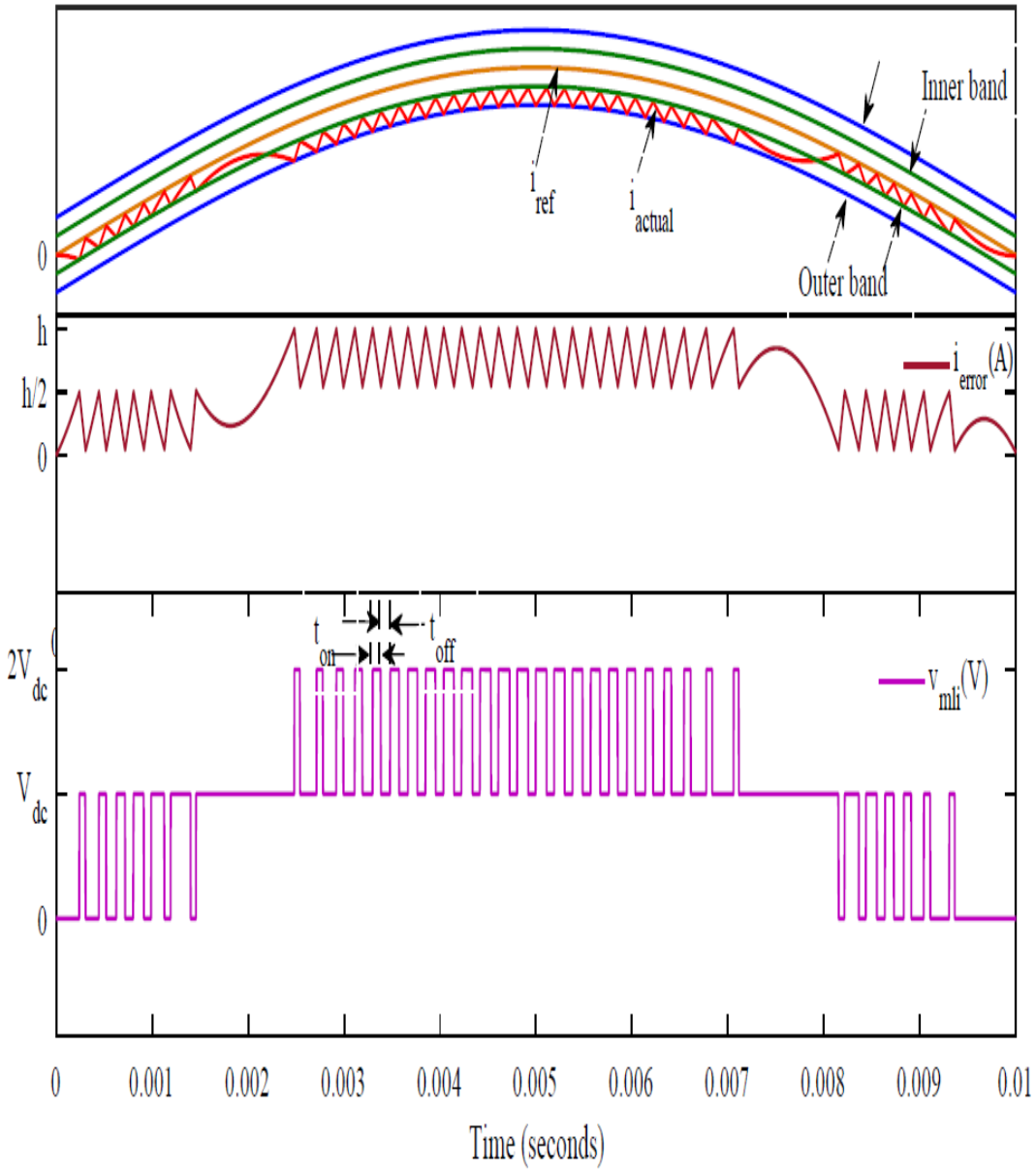



**Figure 4.8** Multiband HCC controlled inverter output voltage with current error, reference current and actual current.

level output each and net band width for each bridge is $2|\frac{h}{2}-\delta|$. In five level operation the net band width for each bridge is reduced to half as compared to three level inverter. As other parameter kept constant it might be the case that net hysteresis band for each bridge is reduced by increasing level of CHMLI. So the operating average switching frequency can be adjusted according to the hysteresis band optimization for any level of inverters.

### 4.3.2 Effect of Parameters

For CHMLI to operate in a grid connected mode or active load mode, it is essential to estimate the switching frequency. CHMLI should operate at lower switching frequency compare to conventional inverters. It is observed that current ripples are shortened by subdividing the band that have effect on absolute switching frequency. As conventional HCC possess a limitation of variable switching frequency, same way Multiband HCC also operate at variable switching frequency for CHMLI .To estimate losses maximum or instantaneous switching frequency calculation is essential[114].

It is prominent to evaluate effect of parameters such as switching frequency, hysteresis band, and inductance on the multiband HCC operation. For the basic operation of close loop system as shown in Fig.4.1 and considering two bridges are connected in cascaded for five level CHMLI,following equations can be written,

$$L\frac{di^{-}}{dt} = V_{dc} - v_s \tag{4.5}$$

$$L\frac{di^{+}}{dt} = 2V_{dc} - v_s \tag{4.6}$$

Where $i^{-}$ and $i^{+}$ are actual currents with negative and positive slope with respect to reference current. Considering this analysis for five level inverter the output voltage with corresponding current error is shown in Fig4.8.Error is limited to the maximum band limit and switching of power devices is done according to hierarchical pattern. Hysteresis band +h to -h in positive and negative side respectively are subdivided in equal parts. Actual current possess ripples and values depending upon value of operating hysteresis band. Where $t_{on}$ and $t_{off}$ is switching ON and OFF time respectively. For determination of net operating switching frequency, following equation can be derived,

$$t_{off}\frac{di_{error}}{dt} = t_{off}\frac{d(i_{ref}-i^{-})}{dt} = \frac{h}{2} \tag{4.7}$$

$$t_{on}\frac{di_{error}}{dt} = t_{on}\frac{d(i^{+}-i_{ref})}{dt} = \frac{h}{2} \tag{4.8}$$

Substituting values of $L\frac{di^{-}}{dt}$ and $L\frac{di^{+}}{dt}$ from Eq.(4.5) and Eq.(4.6) in Eq.(4.7) and Eq.(4.8),

$$t_{off}\frac{di_{error}}{dt} = t_{off}(\frac{di_{ref}}{dt} - \frac{di^{-}}{dt}) = \frac{h}{2} \tag{4.9}$$

$$t_{off}\frac{di_{error}}{dt} = t_{off}(\frac{di_{ref}}{dt} - \frac{V_{dc}}{L} + \frac{v_s}{L}) = \frac{h}{2} \tag{4.10}$$

Similarly

$$t_{on}\frac{di_{error}}{dt} = t_{on}\left(\frac{di_{ref}}{dt} - \frac{2V_{dc}}{L} + \frac{v_s}{L}\right) = -\frac{h}{2} \tag{4.11}$$

Instantaneous net switching frequency $f_s$ can be calculated as,

$$t_{on} + t_{off} = \frac{1}{f_s} \tag{4.12}$$

$$f_s = \frac{2L}{3hV_{dc}}\left[\frac{V_{dc}}{L} - \left(\frac{di_{ref}}{dt} + \frac{v_s}{L}\right)\right]\left[\frac{3V_{dc}}{L} - \left(\frac{di_{ref}}{dt} + \frac{v_s}{L}\right)\right] \tag{4.13}$$

The operating instantaneous switching frequency implementing multiband HCC for switching at outer bands between h/2 to h is depicted in Eq.4.13.For the frequency analysis dead band is neglected due to lower operating switching frequency in result higher switching time. Similarly instantaneous switching frequency can be estimated for any level of inverter. The maximum switching frequency ($f_{smax}$) can be obtained by differentiating Eq.4.13.

$$f_{smax} = \frac{(2V_{dc})}{4hL} = \frac{V_{dcnet}}{4hL} \tag{4.14}$$

Where $V_{dcnet}$ is net DC bus voltage fed to CHMLI. From Eq.4.14 it is observed that maximum switching frequency is directly proportional to net dc bus voltage and inversely proportional to hysteresis band and load inductance. Varying these parameters can effect operation of CHMLI consequently.

### 4.3.3 Effect of Equal Band Division

As in multiband HCC current error is toggled between corresponding bands, with effect the resultant ripples are reduced and switching frequency can be controlled. The main reason of dividing bands in equal parts is to maintain equal average switching frequency for power semiconductor devices associated with each H-bridge cell therefor equal power stress on each bridge. The swapping of H-bridges would become possible that will be advantageous for the system operated from dc bus voltage. Equal power stress on each bridge also affects the symmetrical operation of CHMLI. If the bands are divided in unequal parts with equal dc bus voltage on H-bridge cells, It might possess unequal power stress on power devices.

## 4.4 Digital HCC Based on Xilinx System Generator

There is requirement to develop control logic of proposed digital multiband HCC on a particular designated platform for the real time implementation. For that purpose Xilinx system generator (XSG) tool box is used that is able to resemble a control logic in to HDL code to implement on a VHDL programmable FPGA device. For real time implementation of proposed controller, design and simulation algorithm using XSG tool based MATLAB, Simulink modelling is adopted. It is possible to generate HDL code for Xilinx line FPGAs following the fixed point simulation using Xilinx specific block set model design. XSG supports to develop highly flexible parallel operation environment using XSG tools, digital control unit is designed that works similar to analog relay for injected current error.

Designing of digital HCC using digital components such as counters, comparative logic circuits are much cheaper than analog relays. Implementation on fully digital platform makes its application more reliable. Therefore generation of gate signals and current control is achieved using simple logical operation of S-R flip-flop and implemented using XSG block set in MATLAB/ Simulink. The logical operation and intermediate state is shown in Fig.4.9 and Fig.4.10.When the current error is exceed the upper hysteresis band limit so the counter is injected by enable signal. And when the current error reaches to lower hysteresis band limit so the reset signal injected to the counter. Counter has some parameter such as count steps, count step limit and no. of bits per count, these factors decides the maximum count reached in each switching cycle for generation of logical gate signals the counter signal is compared with any non-zero constant,

for example it has been taken one here. As shown in Fig.4.9 similar to analog hysteresis operation when the current error lies between hysteresis bands switching states is not changed. The switching states are altered whenever the current error reaches the upper or lower limit of hysteresis band.

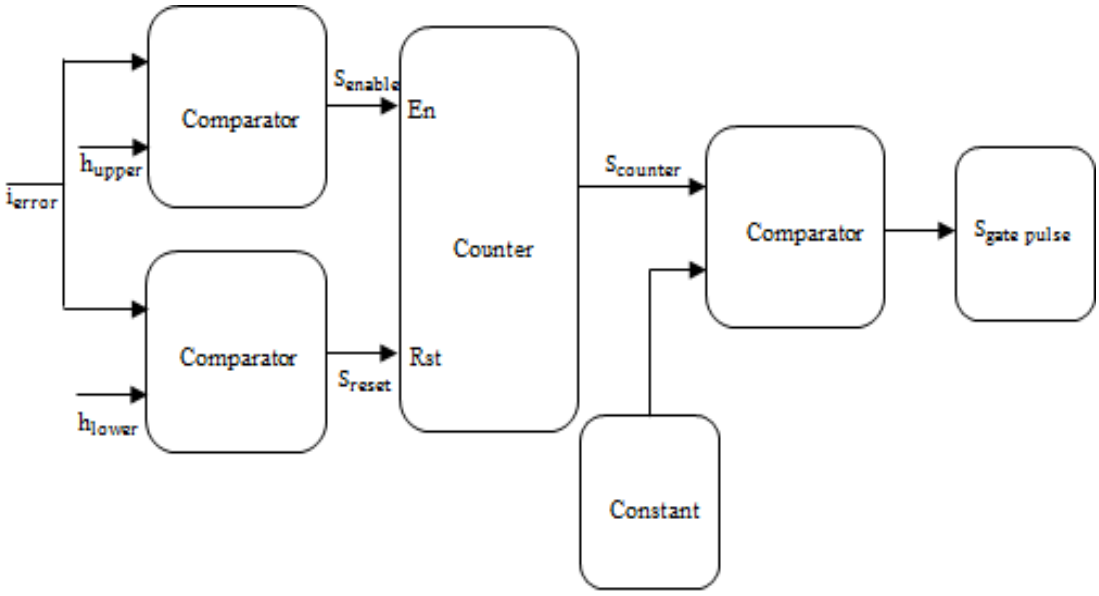



**Figure 4.9** Block diagram of XSG based Hysteresis controller

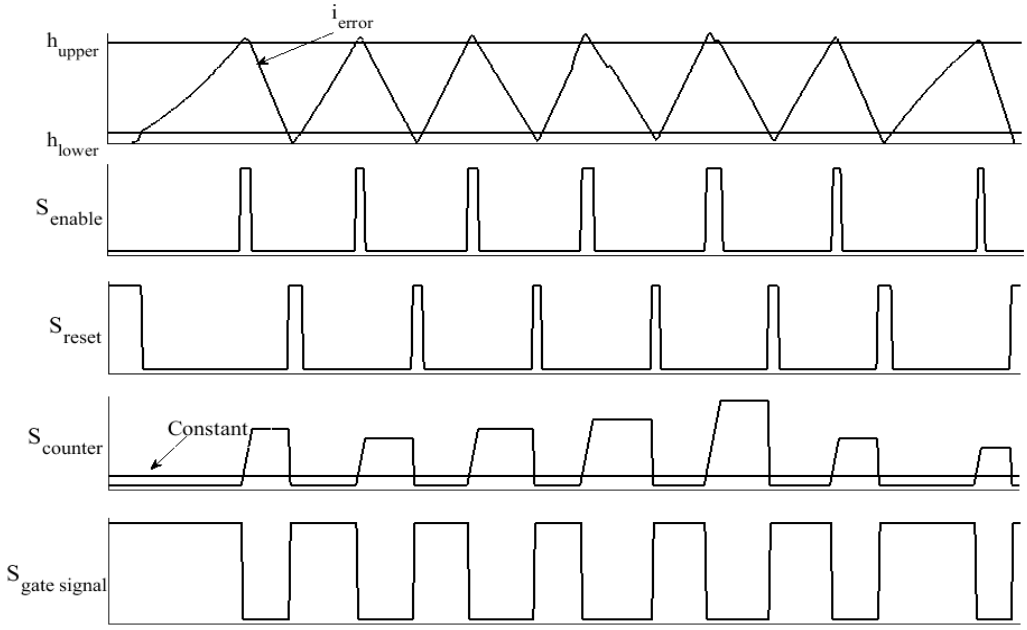



**Figure 4.10** Intermediate signal synthesis and operation of digital hysteresis current controller

## 4.5 Performance Evaluation of Digital Multiband HCC

### 4.5.1 Simulation Results

The proposed Digital multiband HCC is simulated on MATLAB/Simulink, basic circuit is considered as shown in Fig 4.1. The five level grid connected CHMLI operation is evaluated and the parameters are $V_{sm}$ = 28V, L = 33mH; 65mH R = 18Ω, ω= 314rad/s, Vdc = 24V, $I_{refm}$ = 1A, where $V_{sm}$, $I_{refm}$ are peak values of the grid voltage and reference current respectively.

First five level inverter is operated with grid connected system and digital HCC performance is evaluated for unity power factor (UPF) operation of the grid. It means under inductive load condition grid should operate in UPF in results actual current $i_{actual}$ should be in same phase with the grid voltage $v_s$. For the evaluation of the performance of digital HCC over simulation platform synchronization has been done using phase locked loop (PLL).It provides smooth and accurate phase and frequency tracking of reference i.e. grid voltage. As generation of gate signals by hierarchical switching of power electronic devices of CHMLI in corresponding band as shown in Fig 4.5 and 4.7 for three level and five level CHMLI respectively. The Figures has been placed in section 3 for better understanding hierarchical switching pattern. It's clear from the results shown that digital multiband HCC performing close loop control for UPF operation with its functioning as implicit modulator of three level inverter output with improved quality.

In second part of simulation results elaborates the performance of the digital multiband HCC in a close loop system. For this five level CHMLI is considered, similarly higher or lower level of CHMLI can be operated. Actual current tracking the reference current with the output voltage of five level and corresponding error signals has been shown from Fig. 4.11 to 4.14.

In next part Effect of parameters such as hysteresis band and inductance on grid connected CHMLI's performance is evaluated. At first hysteresis band is kept constant h = 0.2A and inductance of the system is varied and selected as 33mH and 66mH respectively and corresponding results are shown in Fig. 4.11 and 4.12. The effect of changing inductance is observed on maximum switching frequency of the system which is varied from 1.818 kHz to 0.909 kHz. As Eq 4.14 dictates the relation between inductance and switching frequency, maximum switching frequency is reduced to its half value. In actual system the load is cannot be decided through user end but the relation of maximum operated switching frequency and circuit parameter is highlighted through

these analysis. The effect of varying the hysteresis band for with varying inductance together is also evaluated in Fig. 4.12 and 4.13. The hysteresis band is changed from h = 0.2A to h = 0.1A and inductance is again varied from 33mH to 66mH and multilevel output voltage with grid voltage and current are shown in Fig. 4.13 and 4.14.The maximum switching frequency is changed from 3.636 kHz to 1.818 kHz by varying inductance from 33mH to 66mH with h = 0.1A for five level CHMLI.

By changing these parameters as results shown in Fig. 4.11 to 4.14 which elaborates performance and higher dynamics of digital HCC controller for five level CHMLI. The Fast Fourier transform (FFT) analysis of the actual current is carried out ant total harmonics distortion (THD) for the actual current. With corresponding values of the THD is shown in the Fig. 4.15.It is observed that minimum THD of 1.54% for actual current is achieved when L = 66mH and h = 0.1A.

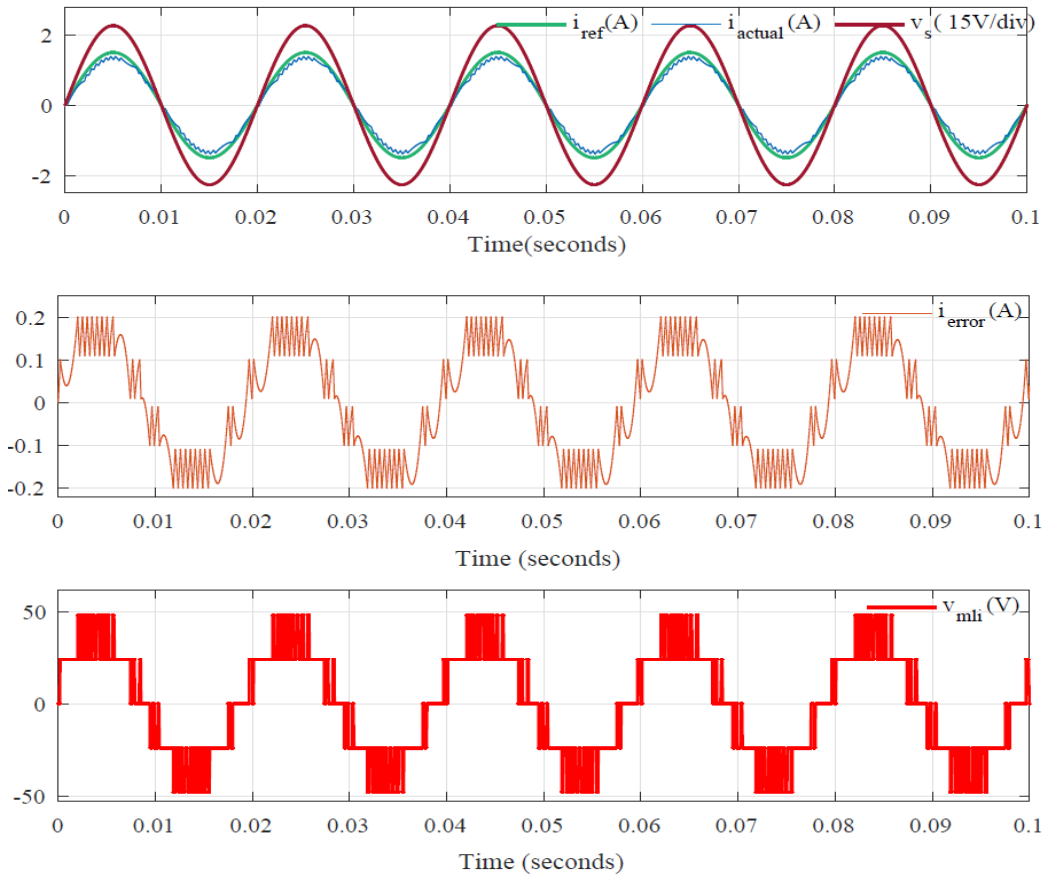



**Figure 4.11** Grid voltage, reference current, actual current and Multiband HCC controlled inverter output voltage with corresponding current error when h = 0.2A and L = 33mH.

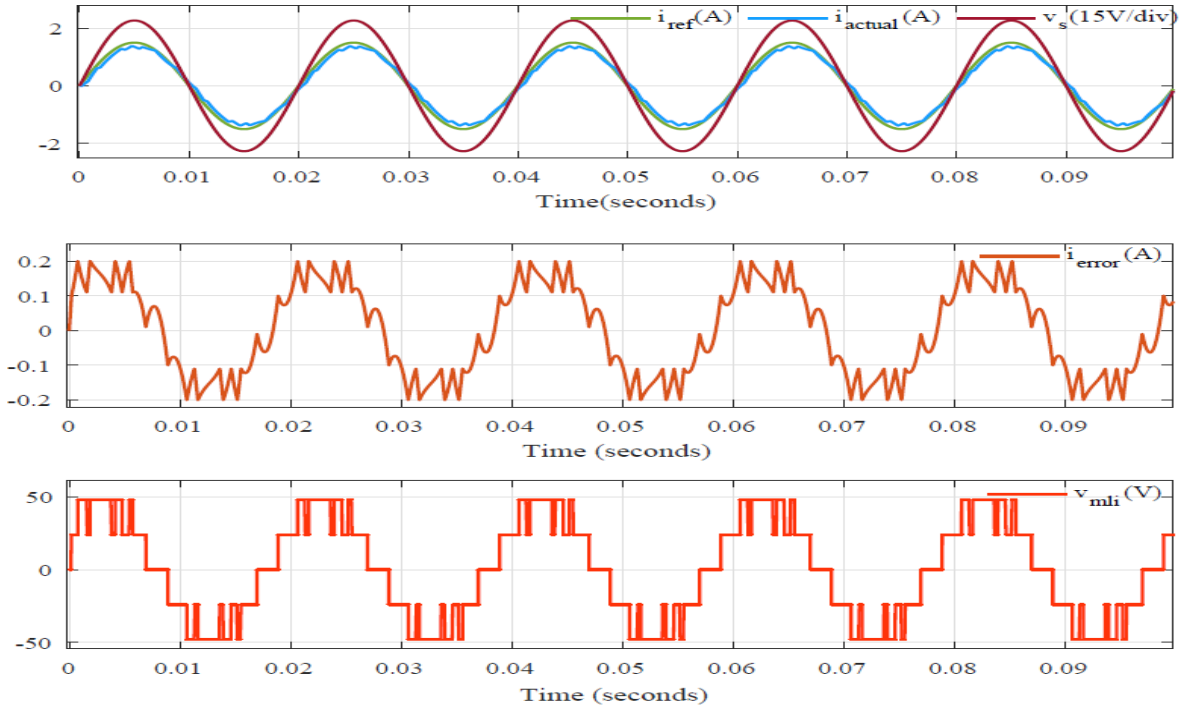



**Figure 4.12**.Grid voltage, reference current, actual current and Multiband HCC controlled inverter output voltage with corresponding current error when h = 0.2A and L = 66mH.

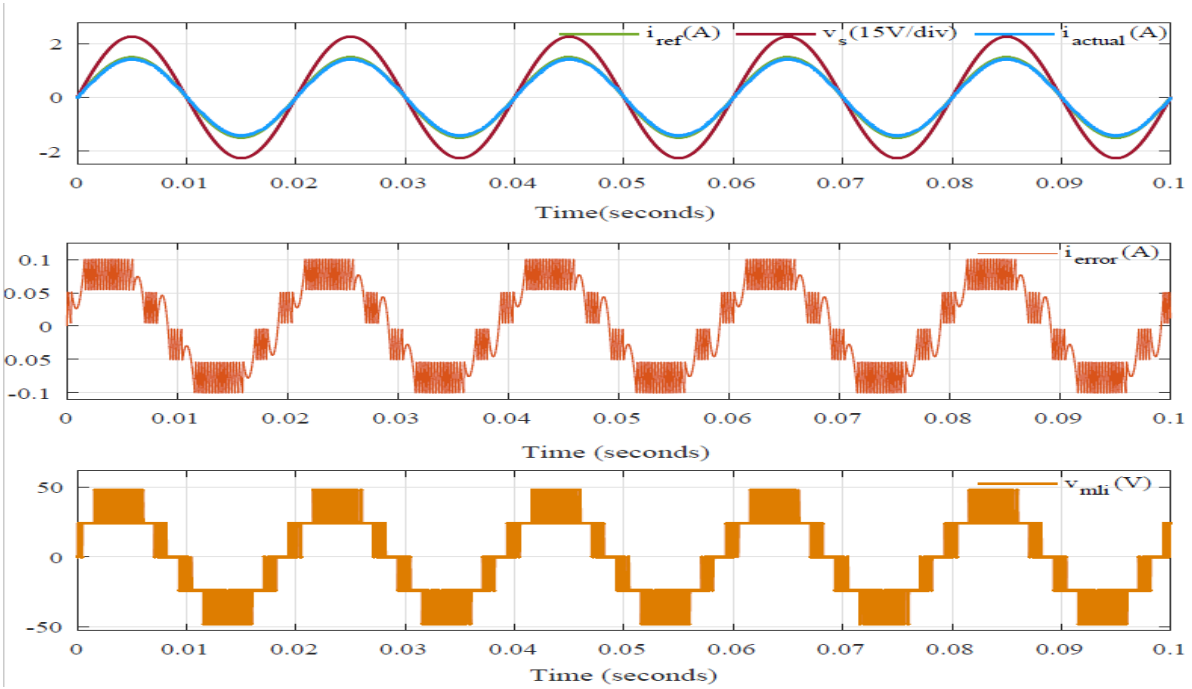



**Figure 4.13** Grid voltage, reference current, actual current and Multiband HCC controlled inverter output voltage with corresponding current error when h = 0.1A and L = 33mH.

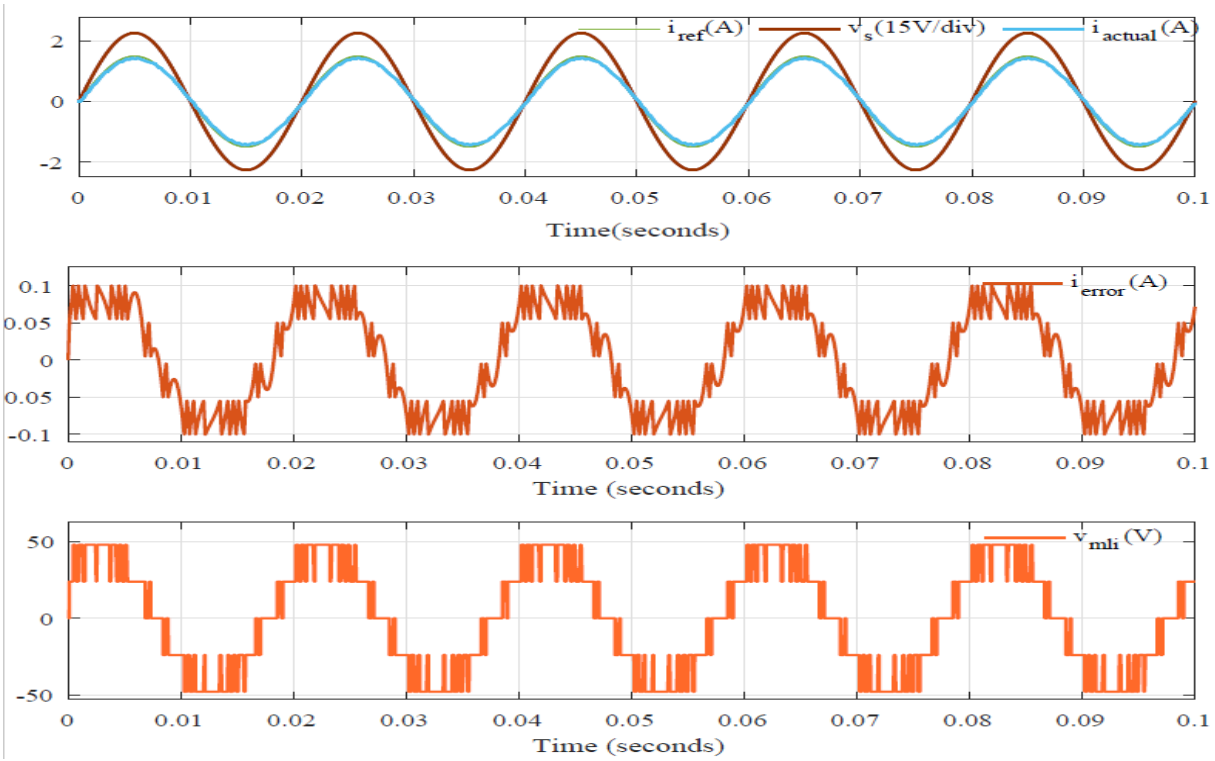



**Figure 4.14**. Grid voltage, reference current, actual current and Multiband HCC controlled inverter output voltage with corresponding current error when h = 0.1A and L = 66mH.

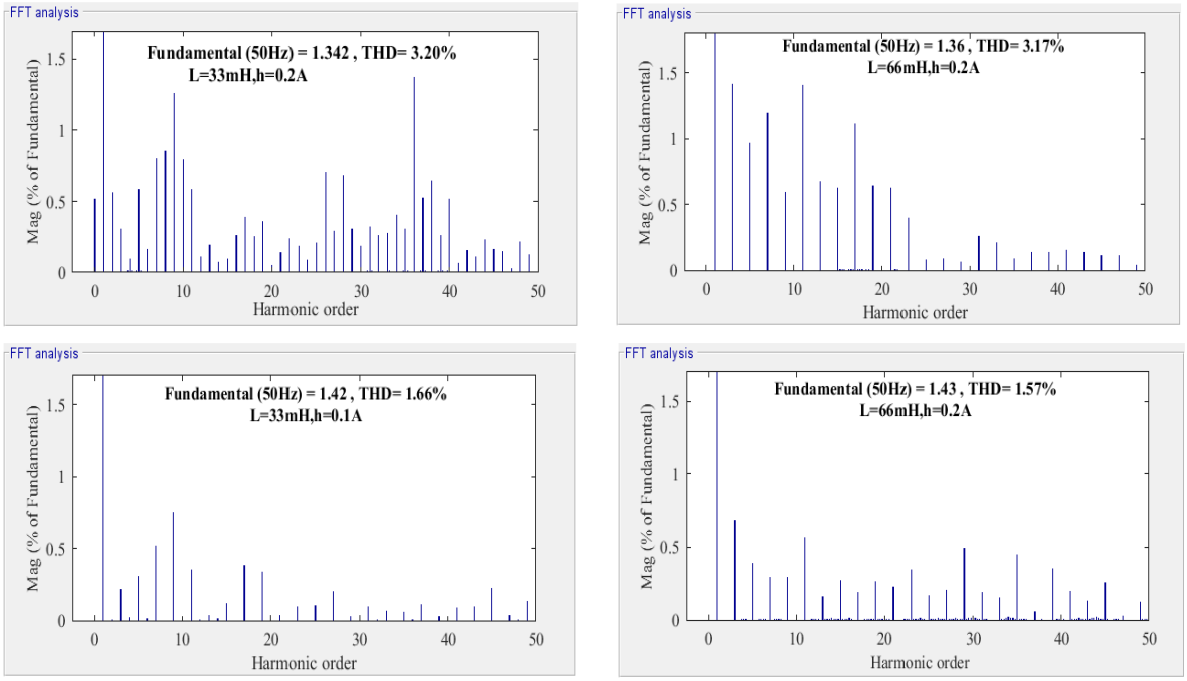



**Figure 4.15**. FFT analysis of the actual current and Corresponding THD for different values of hysteresis band and inductance.

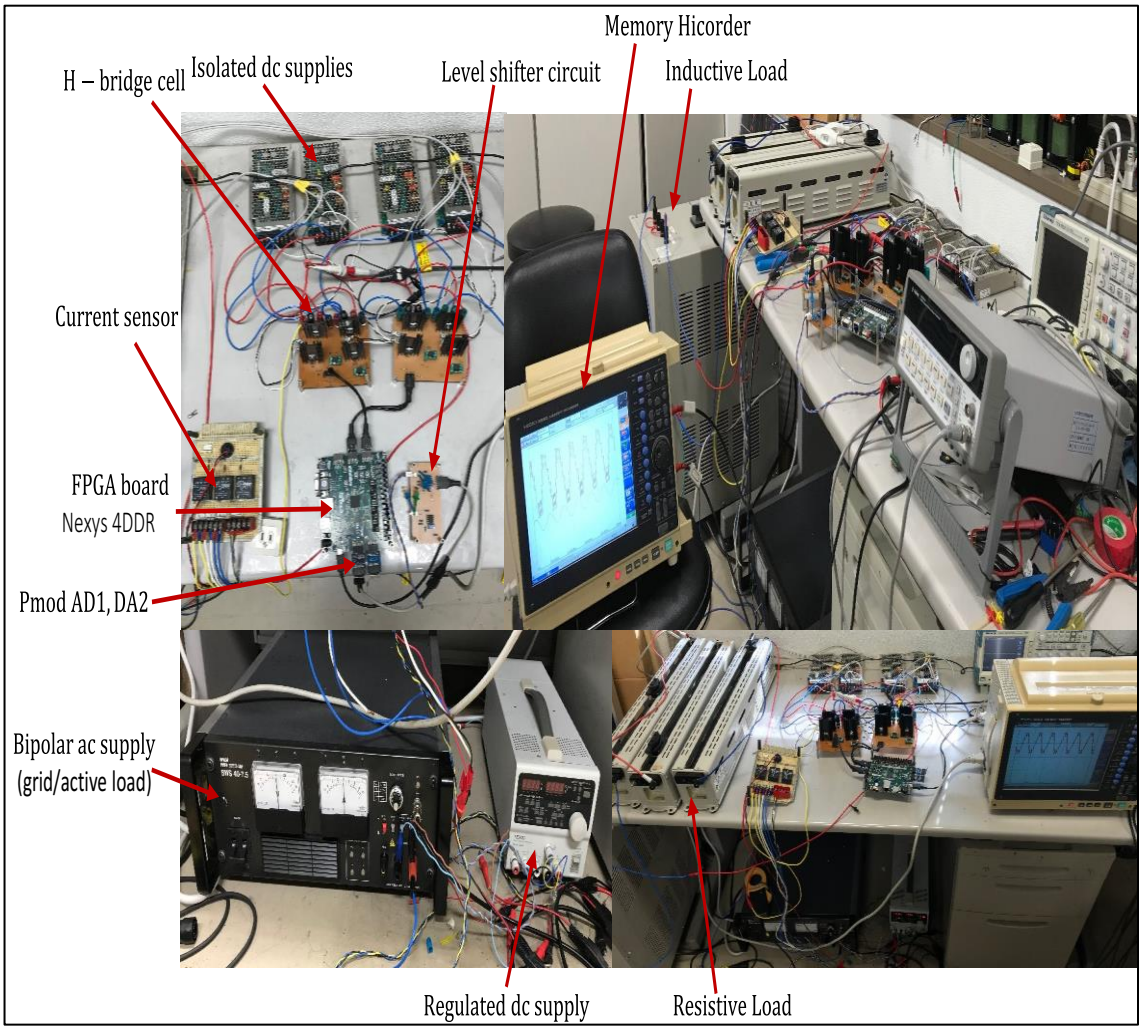



Figure 4.16. Experimental set up for the system

### 4.5.2 Experimental Verification

As part of performance evaluation of the Digital HCC real experimental system is developed, the basic circuitry is as shown in Fig 4.1 is realized using H-ridge units, isolated dc supplies, bipolar ac supply as a grid(four quadrant operation is possible),and variable inductance as shown in Fig 4.16. The XSG based model is developed for controller design and the latest vivado 2017.3 interface is used to develop register transfer level (RTL) design. RTL is a design abstraction that executes modeling of a synchronous digital circuit in the form of the flow of digital signals (data) between logical operations performed on those signals and hardware registers.Vivado IP integrator including sub IP design for the A/D and D/A and digital HCC comprises whole controller designed

in Vivado based IP block design and VHDL code is generated for bit stream generation of combined control system.PMOD AD1 and DA2 is used for Xilinx NEXYS4 FPGA board to realize fully FPGA based digital controller. PMOD AD1 provides significant high speed of sampling frequency up to 1 MHz that effects the dynamic performance of the close loop system and reduces the effect of delays caused by slow rate conversion of AD converters. The complete hardware set up is shown in Fig.4.16 and the vivado and XSG tool based model are developed on PC to execute program on FPGA.

As Experimental results are shown in Fig 4.17 and 4.18 dictates the performance of digital HCC and its implicit modulator for five level CHMLI with corresponding current error signal and four gate signal required for primary switches of two H-bridges, complimentary switches are provided gate signal by inverting these signals inside H-bride module itself. For switching frequency variation can been be observed when load inductance is changed from 33mH to 66mH respectively in Fig 4.17 and 4.18.

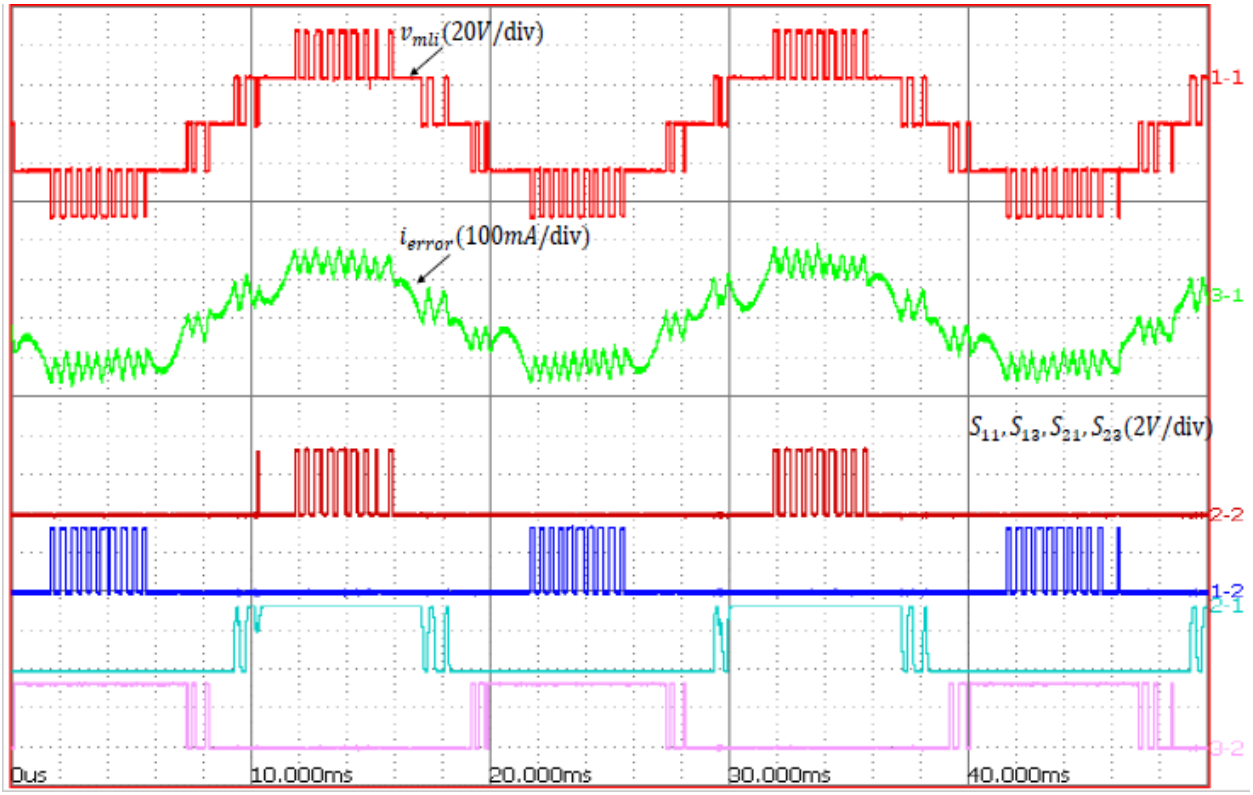



**Figure 4.17** Experimental results for generated five level output voltage, current error and corresponding gate signal when L = 33mH and h=0.2A.

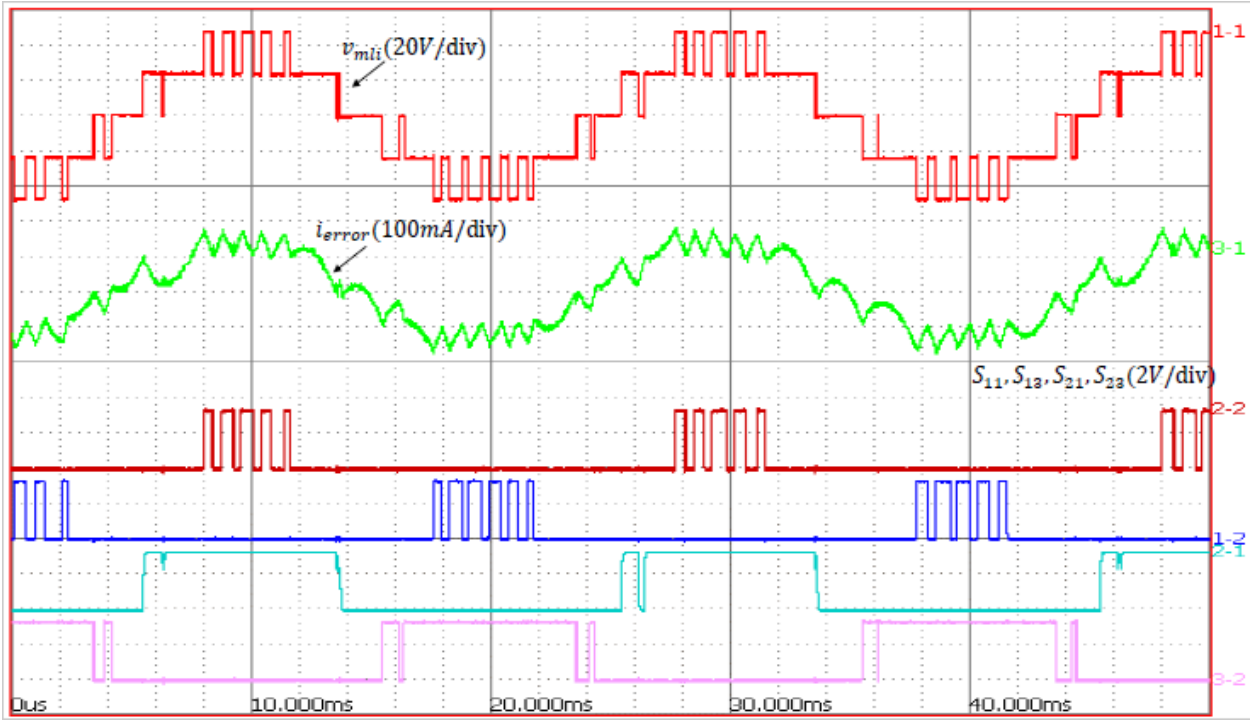



**Figure 4.18** Experimental results for generated five level output voltage, current error and corresponding gate signal when L = 66mH and h=0.2A.

In next part of experimental verification performance of close loop controller i.e. digital multiband HCC is evaluated with effect of parameter variation. In a grid connected system, objective of controller is to operate grid in unity power factor in condition even if the load is inductive. Grid operating in a unity power factor exploiting digital hysteresis current control is shown in Fig 4.19 to 4.26.Actual current tracks the desired reference current as taken $i_{refm}$ = 1.4A for experimental verification.

The effect of parameters such as hysteresis band and inductance is analyzed and verified similar to simulation analysis. As effect of inductance on switching frequency can be observed, reduced maximum switching frequency is observed by increasing the inductance as well. For first case hysteresis band is kept 0.2A and inductance is changed from 33mH to 66mH and corresponding results are shown in Fig. 4.19 to 4.22.And next for hysteresis band of 0.1A inductance is changed in former manner and results are shown in Fig 4.23 to 4.26.The UPF operation of grid under Digital HCC is verified with smaller inductance size. From experimental results it is evident that the actual current is tracking the reference current and generation of five level output is accomplished by digital multiband HCC.

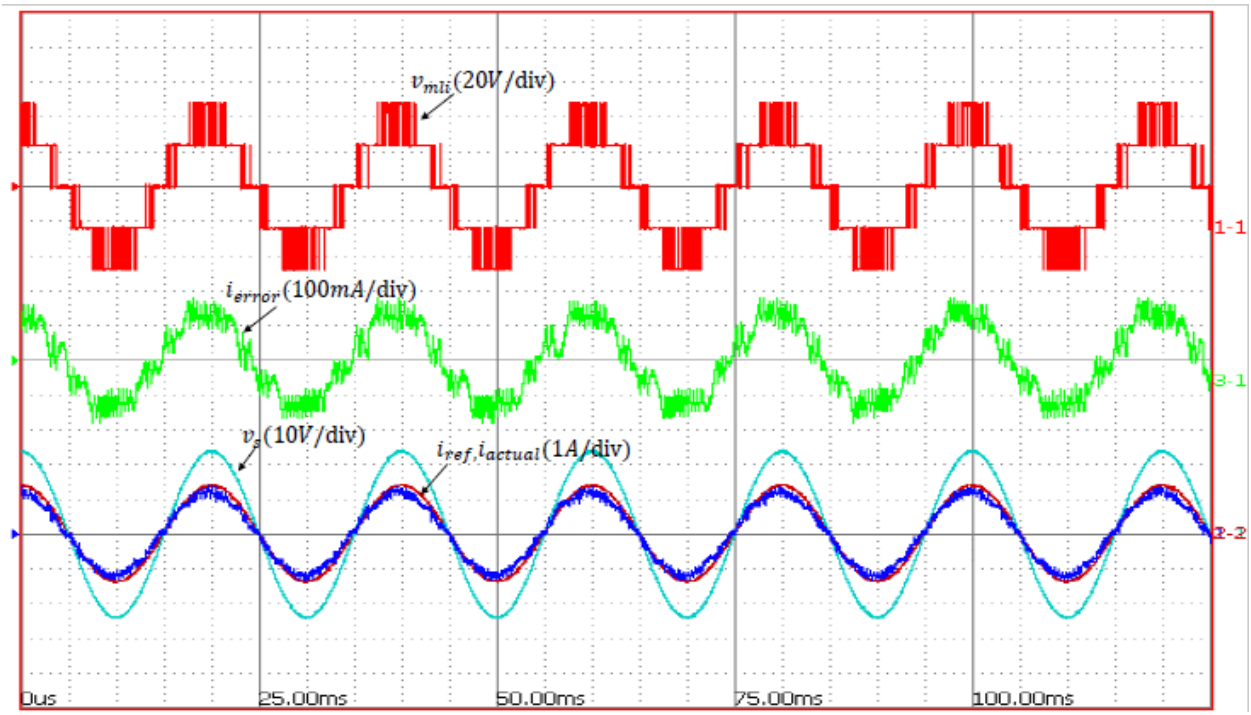



**Figure 4.19** Experimental results for the five level voltage output, current error, grid Voltage, actual current and L =33mH,h=0.2A.

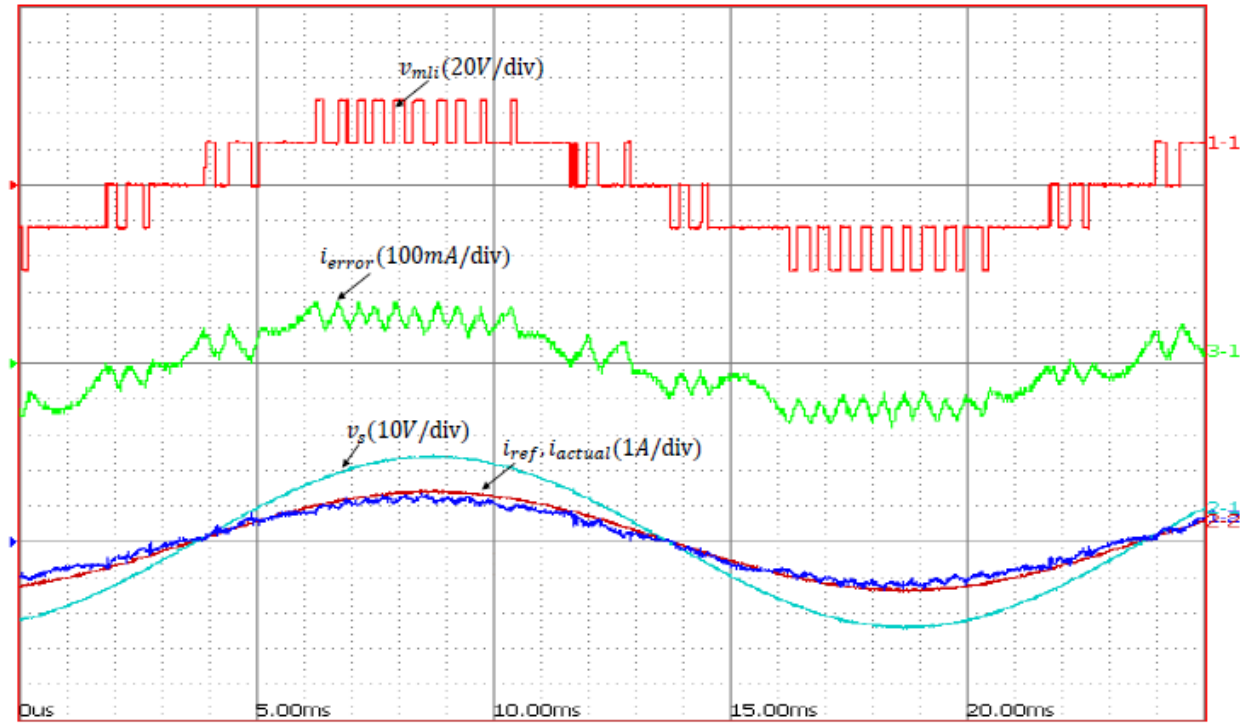



**Figure 4.20** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =33mH,h = 0.2A(zoomed view).

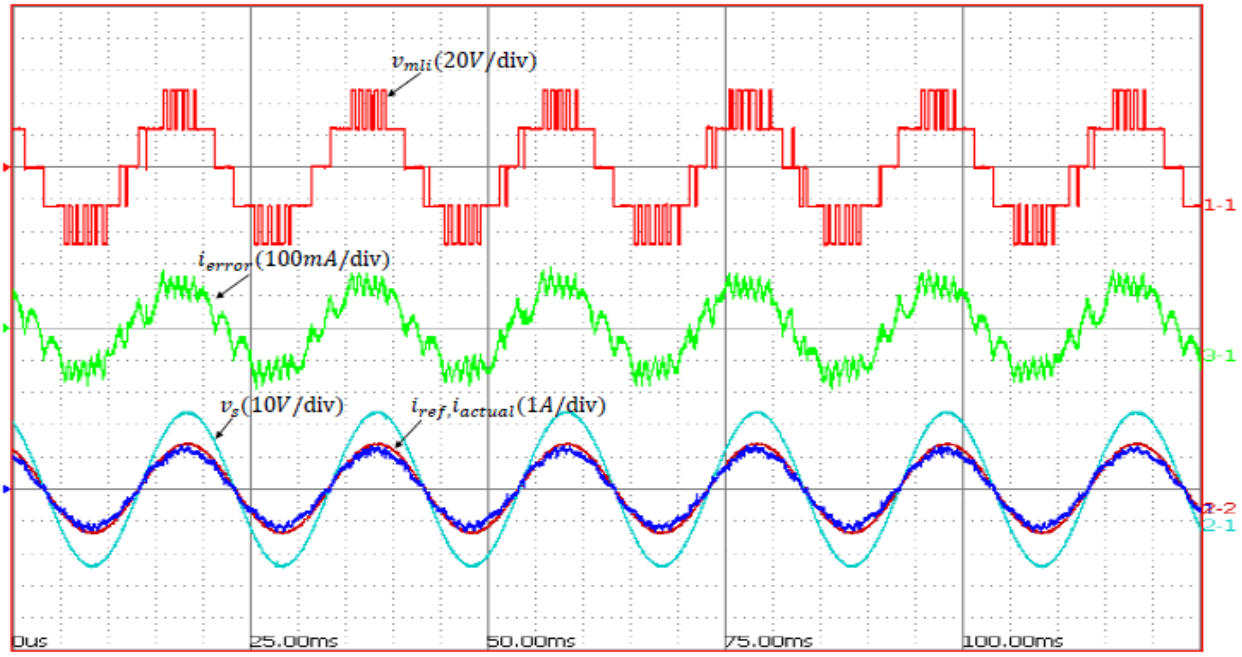



**Figure 4.21** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L = 66mH,h = 0.2A.

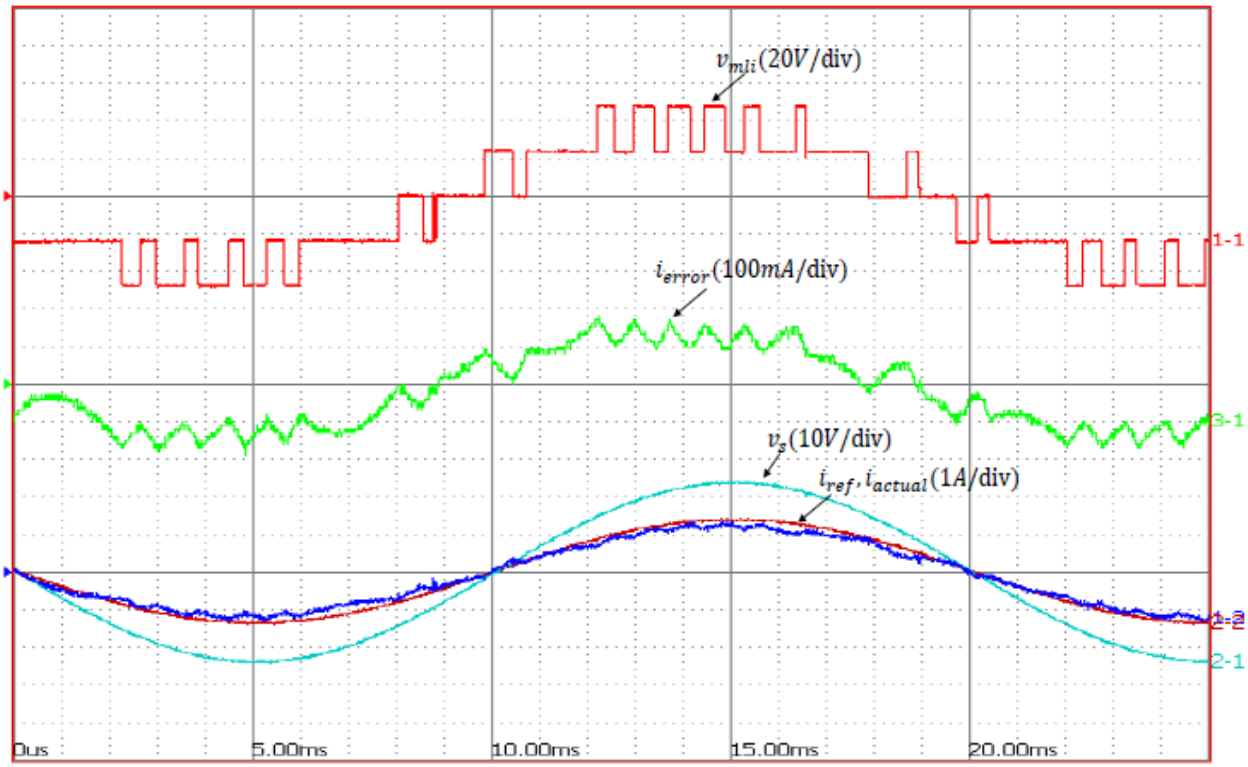



**Figure 4.22**. Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =66mH,h = 0.2A(zoomed view).

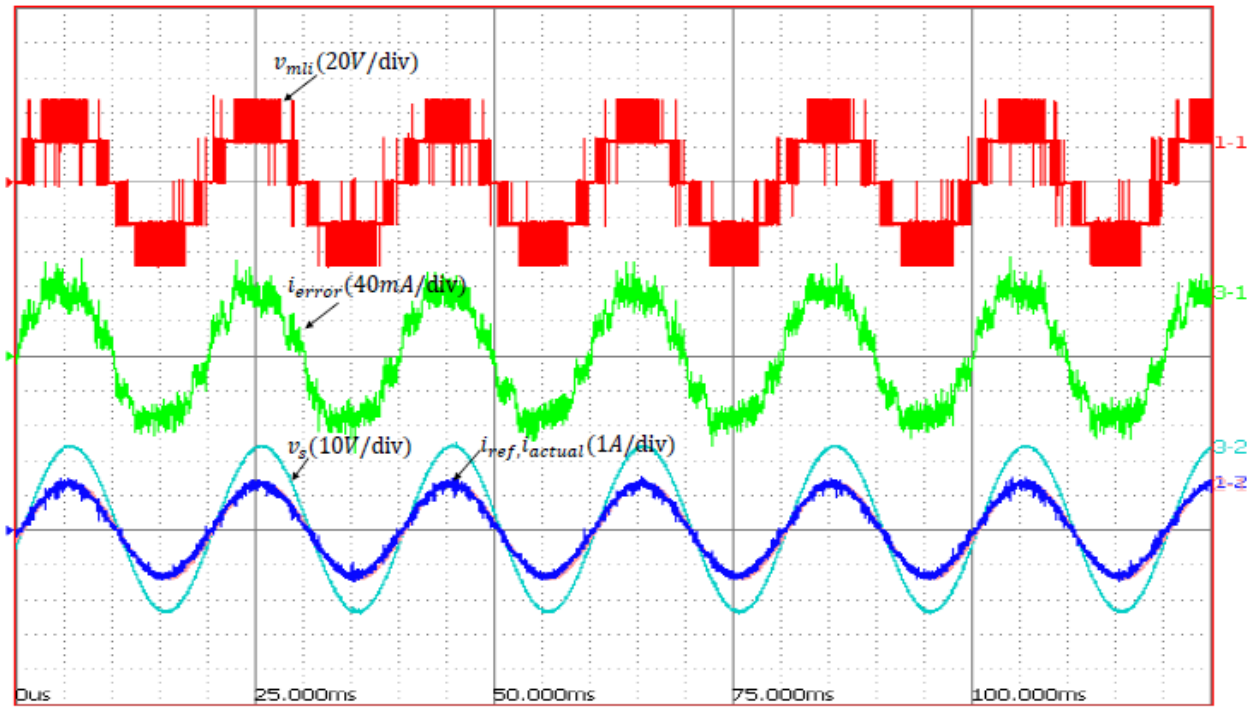



**Figure 4.23** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =33mH,h = 0.1A.

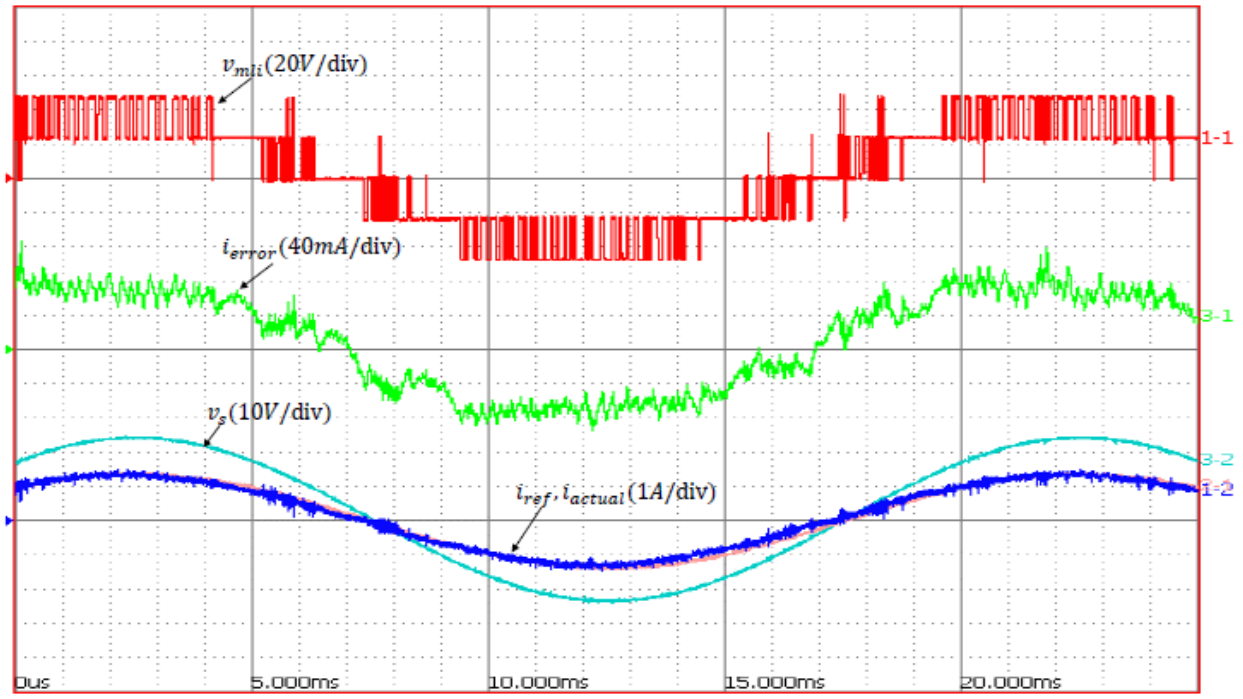



**Figure 4.24** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =33mH,h = 0.1A(zoomed view).

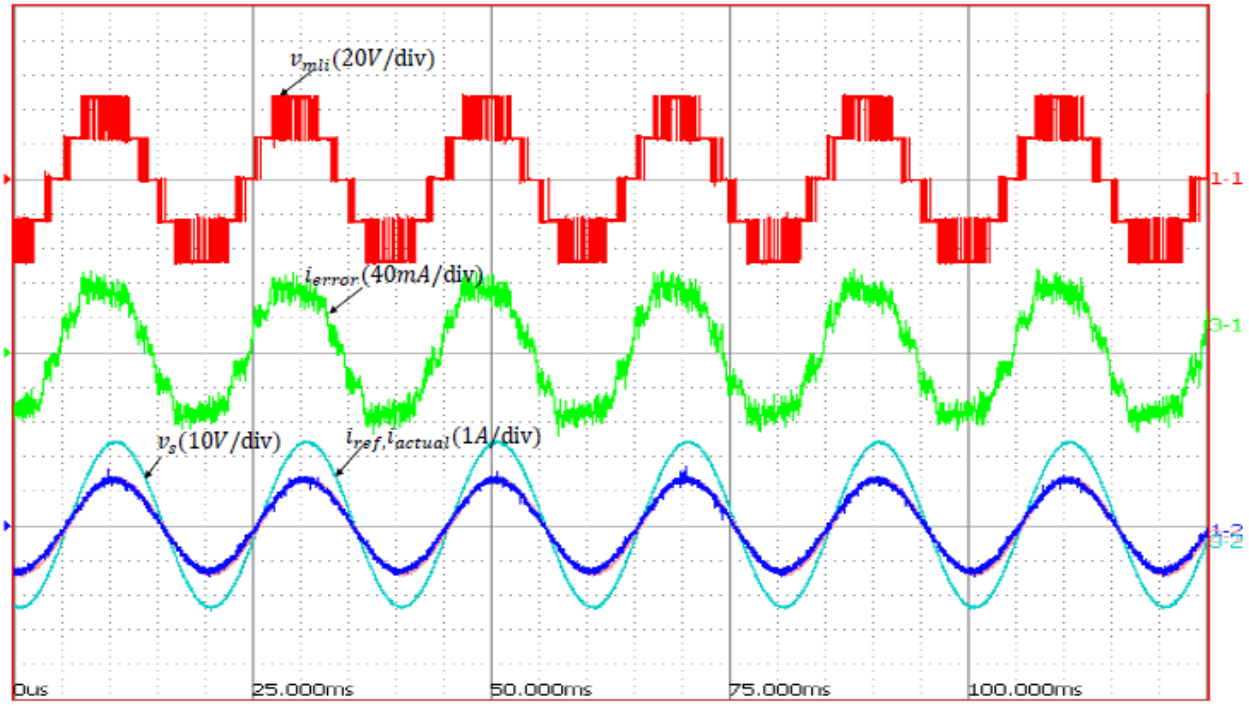



**Figure 4.25** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =66mH, h = 0.1A.

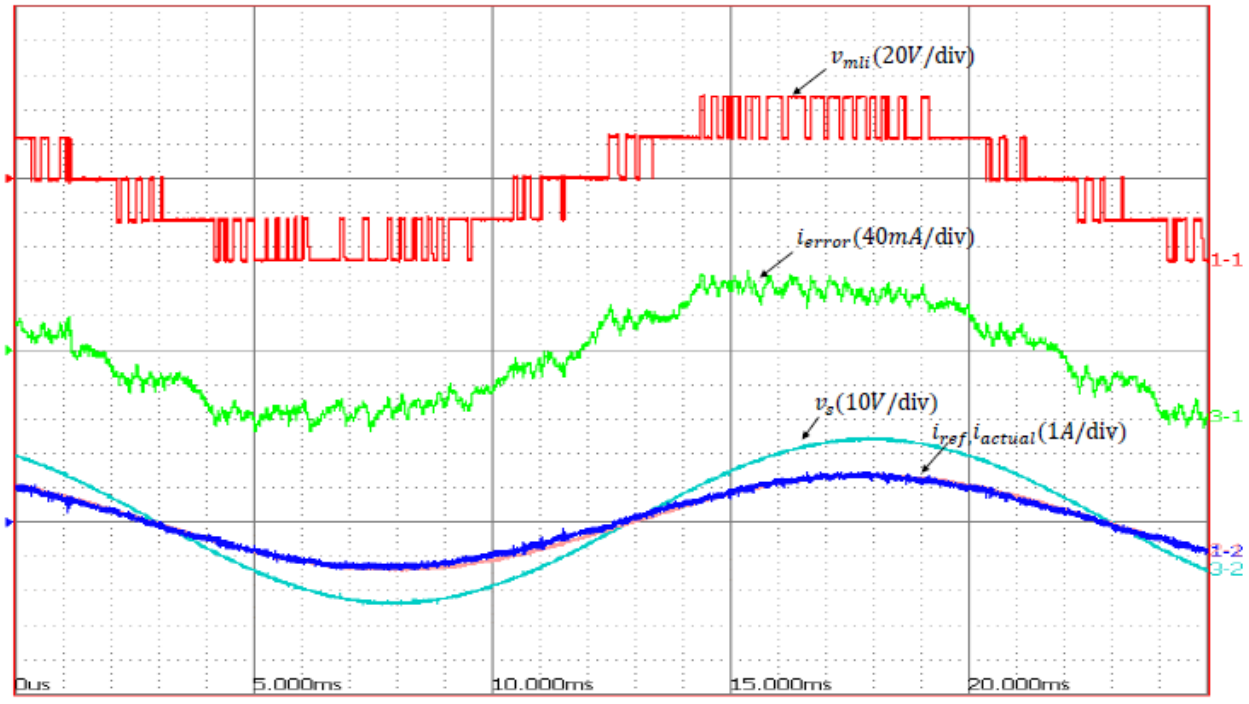



**Figure 4.26** Experimental results for the five level voltage output, current error, grid voltage, actual current and reference current with L =66mH, h = 0.1A.(zoomed view)

## 4.6 Conclusion

Digital multiband HCC is proposed for grid connected CHMLI for grid current control and implicit modulation of inverter. Multiband HCC performing close loop control of grid current and implicit modulation of multilevel output is eventually simulated on MATLAB and validated with experimental results using FPGA based real time control. Performance of digital multiband HCC is analyzed by variation of system parameter such as switching frequency, hysteresis band and grid inductance. As digital multiband HCC enables control of grid current with desired modulation of CHMLI it benefits the system with less complexity, cost, better dynamic performance, reduced steady state error.

The outcomes of the work included in this chapter can be summarized as follows

**Novel Multiband Hysteresis current controller:** A digital hysteresis current controller is designed utilizing basic circuitry of S-R flip flop for cascaded H-bridge multilevel inverter. It is capable of controlling the grid current with implicit modulation of inverter.

**Improved Close loop control:** Better close loop control for grid connected CHMLI is achieved with reduced steady state error while tracking a user defined reference current.

**Digital implementation:** Digital implementation of the HCC is done for the faster and reliable application of CHMLI. Reference current and actual current is sampled with high sampling rate, therefore reduced delays in the system.

**Complexity:** In the proposed work Digital HCC is employed to operate grid in a UPF mode irrespective of connected inductive load, this method is quite simple in comparison to other linear control techniques.

**XSG based system design:** Implementation of digital multiband HCC is done using Xilinx system generator as user interface to develop system level modelling in fixed point simulation. Generated VHDL code for the system model is used for FPGA based real time implementation.

# CHAPTER 5

# Multiband HCC for Cascaded H-bridge inverter based DSTATCOM

## 5.1 General

In this chapter digital multiband HCC is proposed for CHMLI based DSTATCOM and direct control is adopted for the reference current extraction different from DSTATCOM discussed in chapter 3(indirect control is used). This chapter mainly deals with the current control of DSTATCOM system using three type of controller. Inner current controller should achieve two function in the system tracking of reference and implicit modulator. MHCC performance is compared with the linear controller such as PSPWM and LSPWM. Relation between modulation function and inverter output voltage is illustrated that shows the linear and non-linear behavior controller. Robustness and dynamic behavior of these different modulation techniques make this comparative analysis very critical and important. The controller is designed for reducing steady state error during linear and non-linear load condition and its effect on stability of the system is evaluated. Basically LSPWM, PSPWM and MHCC all of these modulation methods have instant impact on the STATCOM operation, efficiency, cost, and power quality optimization capability.

## 5.2 Cascaded H-bridge Inverter based DSTATCOM

### 5.2.1 DSTATCOM System and Operation

DSTATCOM is defined as a shunt connected voltage source converter based distribution static compensator, which used for compensation of reactive power and voltage regulation. Normally it is connected at the point of common coupling for injecting controlled amount and quality of current in to the grid. A five level CHB inverter based DSTATCOM connected to the load at the PCC, as shown in Fig.5.1. Symbols such as, $I_{L,}V_{s,}I_{s,}I_{c,}I_{ref}$ used in this paper represents are Load current, source voltage, source current, compensator current and reference current respectively In this paper low voltage distribution system with grid is considered, however, power devices can be chosen with different voltage rating and can be extended to medium voltage grid. L filter is commonly used for the STATCOM operation because of simple structure and easy to control but because of low to high frequency attenuation rate, the filtering effects of high frequency ripple are restricted. These days filters can be replaced by higher order filters like LC, LCL etc. Due to lower switching frequency and modular structure of CHBMLI, L filter can perform well with the

proposed system. Main focus of this paper is to compare the modulation technique for STATCOM and it is briefly explained following reference current generation. CHB multilevel inverters are having advantage over other topologies due to its modular structure and reduced number of component required.

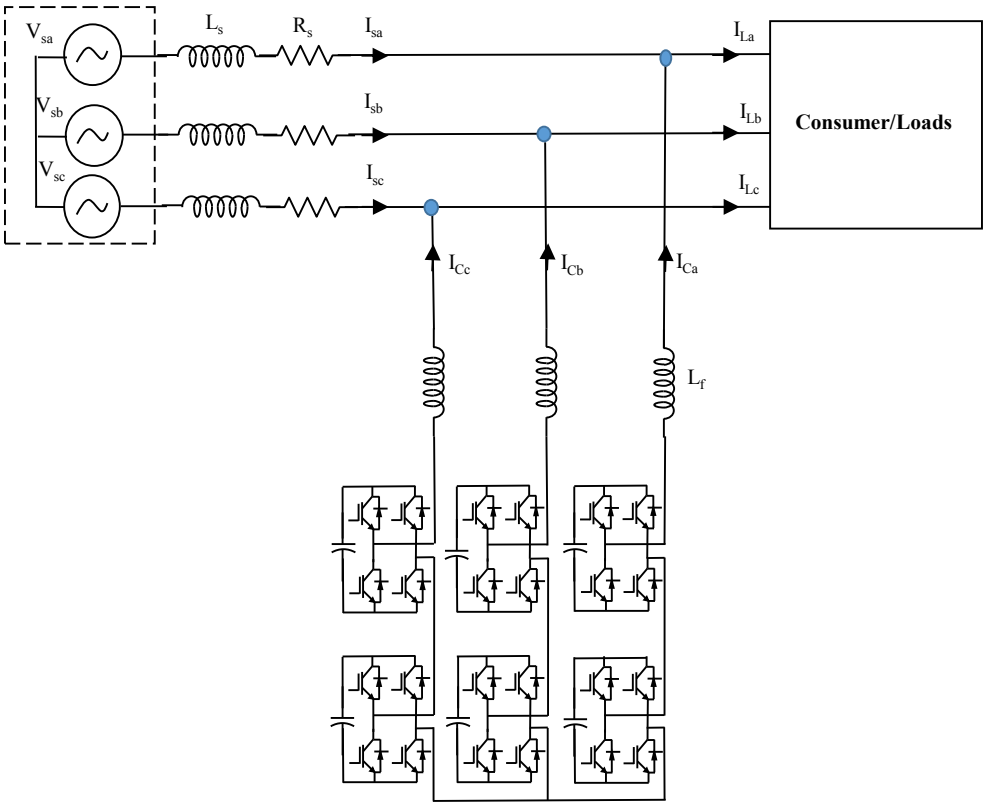



**Figure 5.1** Operational diagram of CHMLI based DSTATCOM

## 5.2.2 Direct Current Control SRFT for Reference Current Generation

Voltage and current control techniques are available for control of the STATCOM, due its reduced complexity and ease of implementation, direct current control technique is used for reactive power and harmonics compensation.Fig.5.2 shows the complete control algorithm that is used for the generation of reference current. Load current is transform abc to dq0 axis i.e. stationary frame to rotating frame. From the d-q theory of power fundamental, dc component direct axis of current is responsible for active component of power if quadrature axis voltage is zero and remaining current is responsible for harmonics

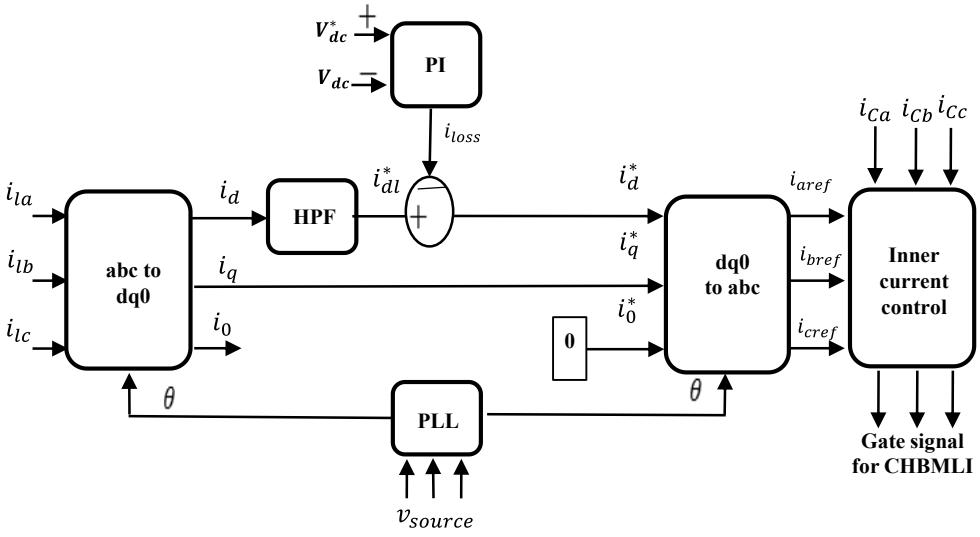



**Figure 5.2** current control algorithm for generation of reference current

And reactive power of load. Equation used in abc to dq0 transformation of load current and inverse transformation dq0 to abc of load cuuent is used for synchronization of the current control with grid and transformation took place on fundamental frequency of grid. To compensate required harmonics and reactive power the DSTATCOM need to force the grid to supply the active and fundamental components of the power only. After passing through the high-pass filter, the high frequency component of the *d*-axis current is added to the current component that is responsible for the power losses due to charging and discharging of the capacitors across each bridge.

The PI controller is one of the most commonly feedback controllers, and has been used for balancing of dc voltage across each capacitor. Due to its simplicity, applicability and ease of control. Tuned using trial and error method PI controller can achieve negligible steady state error for dc reference tracking. The function of this controller can be elaborated simply using the following mathematical equation:

$$i_{loss} = K_p\left(V_{dcref} - V_{dc}\right) + K_i \int (V_{dcref} - V_{dc})dt \qquad (5.1)$$

Where $K_p$ and $K_i$ are proportional and integral gains. Proposed system consist of many feedback loop so tuning of PI controller using trial and error method is quite possible easy method.

### 5.2.3 Current control and Modulator

Inner current control loop plays a important role in current controlled DSTATCOM system. Regardless of application inner control loops are responsible for the torque control in AC machines, harmonics compensation in DSTATCOM system and in micro grid for voltage regulations. Hence prominence control of inner loop plays a vital role for voltage and current or both to satisfy desired feature of different applications. To achieve any such application demanding features of inner control loops are: achieving zero steady state error, higher range of bandwidth as much as possible, tracking performance should be accurate during transients, and minimization of lower order harmonics. In this paper for reference current generated using SRFT is converted into stationary frames. After that current regulator as proportional controller (proportional gain) is applied. This gain consist of controller gain and modulation gain together. The proportional controller combined with SPWM is required to maintain a inner loop sustain its features such as nearly zero steady state error or better tracking performance when it has to follow sinusoidal reference. The block diagram is shown in Fig.5.3 the non-linear controller (MHCC) is also applied for comparison. Operation under linear and non-linear controller is investigated with three different modulation techniques.

Many other modulation techniques have been developed to date by researchers for MLIs, but for the STATCOM application, these two SPWM techniques are modular and simple and enable any complexity in the system to be avoided. Phase shift modulation also has one important advantage over level shifted in that it eases the modulation index change process. Phase shift modulation possesses equal power stress on each switching device, so as switching losses are distributed across

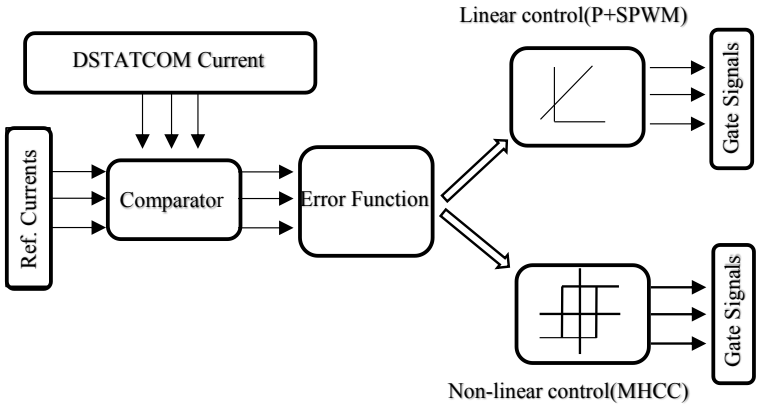



**Figure 5.3** Inner current control for DSTATCOM

the entire MLI structure. LSPWM and PSPWM techniques are comes under category of linear control for inverter. LSPWM and PSPWM is already discussed in chapter 2 for a open loop control, In this chapter reference current is generated using direct current control based SRFT and feed to the inner current control.

## 5.3 Multiband Hysteresis Current Controller for DSTATCOM

MHCC algorithm consists switching pattern which leads to generate multilevel output. It requires hierarchical switching scheme to generate gate pulses for CHB multilevel inverter as discussed in chapter 4. Instantaneous current error between reference current and STATCOM current is fed to MHCC for inner current control system. For modulator the input is current error and output is voltage output i.e. multilevel output. MHCC is one of the best technique that can be applied to support the current controller in selecting the correct voltage level. Such as for m number of levels, m-1 hysteresis bands are required. Switching between two adjacent levels are done in corresponding hysteresis band. To generate five level output for inverter the two outer and two inner hysteresis band with reference current shown in Fig.5.4.switching frequency is the main concern with this type of switching control. Just like three phase two level inverter for HCC, variable switching frequency is its drawback. But proposed method of MHCC can possesses equal average switching frequency for each H-bridge if hysteresis band is divided equally among

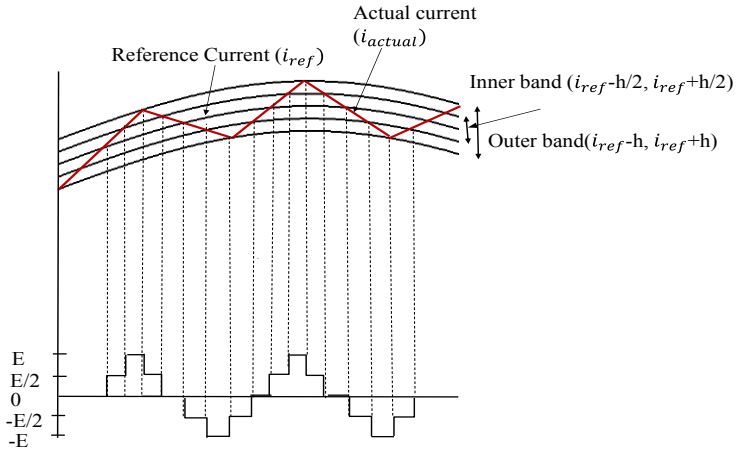



**Figure 5.4** CHB multilevel inverter output corresponding to multiple band

different voltage levels. Due to high dynamics and better tracking performance can be attained when used with PI (in rotating frame) or PR (in stationary frame) controllers. For the estimation of switching frequency range, formulation is used for corresponding hysteresis band. Hysteresis

band can be estimated according to application and suitable switching frequency can be calculated. Detailed explanation of MHCC is explained in chapter 3.

## 5.4 Performance Evaluation of DSTATCOM

DSTATCOM performance is investigated for converter topology of CHB multilevel inverter. The main focus is to compare the effect of modulation techniques and elaborate the complexity level to implement particular technique. To achieve better grid condition and track desired reference current inner current control is required. Linear and non-linear techniques are available for modulation control. Among various techniques three of switching control is considered for comparative analysis: PSPWM, LSPWM, and MHCC. For the better understanding and purpose of clearness, load and grid conditions are taken same for all three modulation technique. Results taken for performance evaluation is shown for 0.1 to 0.2 sec.(linear load),0.2to 0.3 (unbalance load),0.3 to 0.4sec.(Non-linear load) with corresponding modulation techniques. Grid and load parameters shown in Table.1 is taken for simulation work.

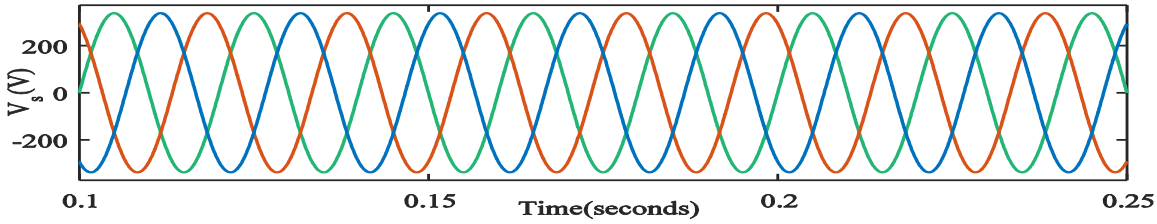
**Table 5.1 Parameters for MHCC based DSTATCOM**

| Parameter | Values |
|---|---|
| Grid voltage | 415 V (line to line) |
| DC bus voltage | 250V |
| Grid frequency | 50 Hz |
| Filter inductor | 8mH |
| Load | 50kVA 0.8 pf lagging, rectifier load of (15+j2.5)Ω, 12.5kVA 0.8 pf lagging(Phase A) |

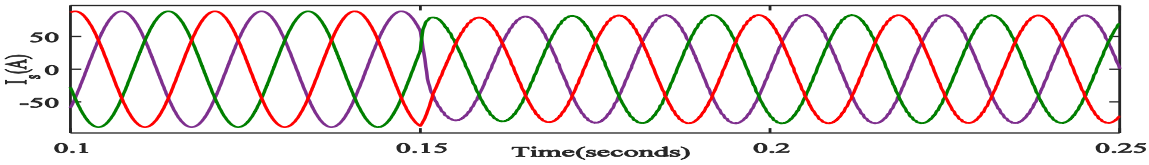
### 5.4.1 Performance for Level Shifted PWM for DSTATCOM

Performance of CHMLI based DSTATCOM under LSPWM is found similar to PSPWM. The differences are power stress on switching devices are not even in the case of LSPWM. Grid performance under different load condition and current tracking performance are shown in Fig.5.5 to 5.7. In LSPWM, switching frequency of power semiconductor devices are equal to each carrier frequency. Scaled multilevel output voltage and modulation function is shown in Fig 5.5 (e) and 5.7(e) with carrier wave of 2 kHz. Grid operating close to unity power factor under different load

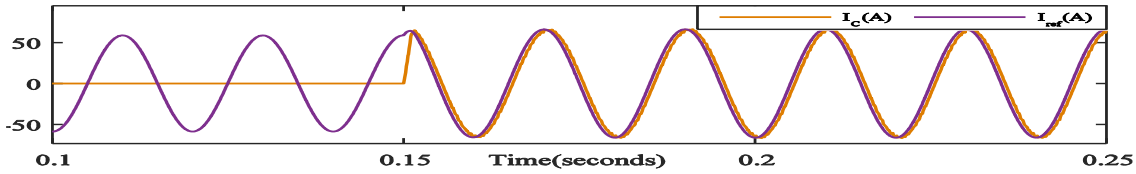
condition. Compensator operation is investigated as compensator current is following the reference current. Tracking performance is found satisfactory with proportional controller to achieve better



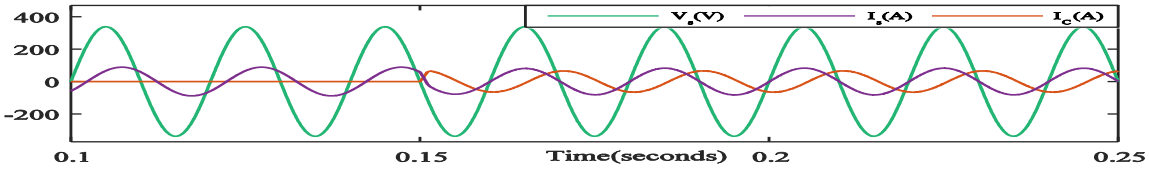

(a) Grid voltage



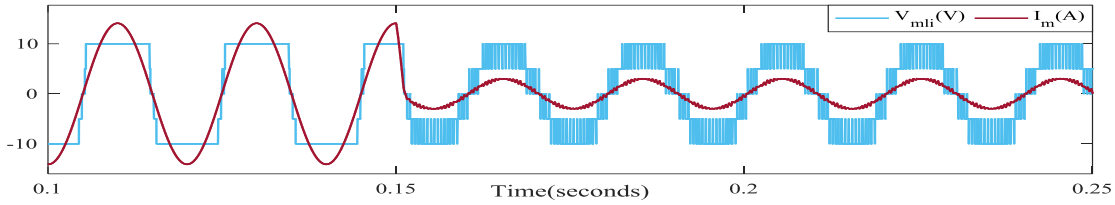

(b)Grid current with LSPWM




(c) Reference current tracking with LSPWM (Phase A)

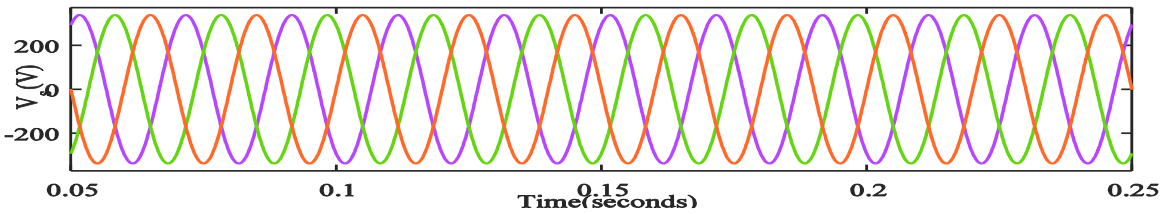



(d) Grid voltage and current and compensator current (Phase A)

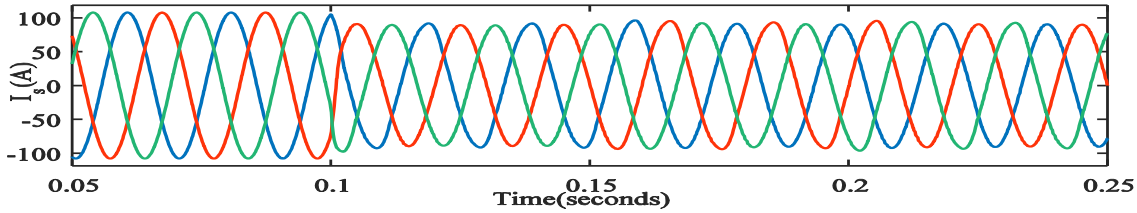



(e) Output voltage (×0.02) and modulation function (×3) at 2 kHz

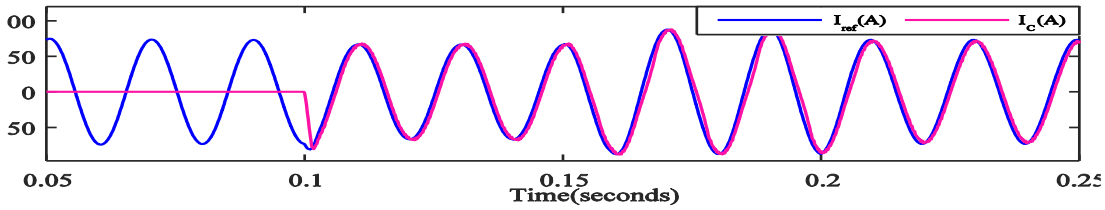
**Figure 5.5** Performance of LSPWM with linear load condition (DSTATCOM switched at t=0.15 sec.



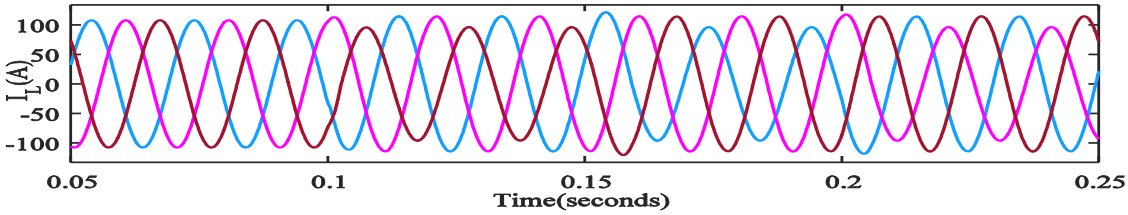

(a) Grid voltage



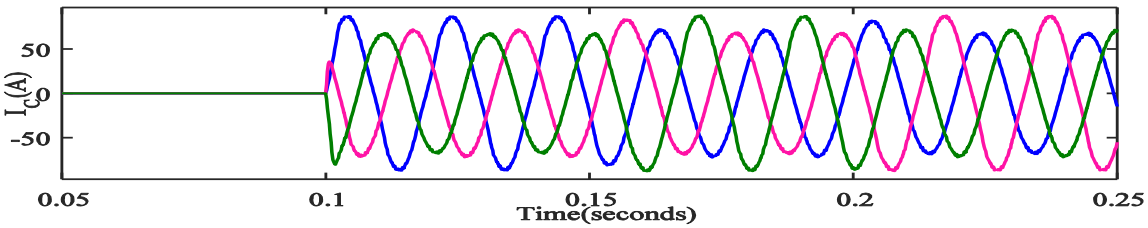

(b)Grid current




(c) Reference current tracking with LSPWM (Phase A)

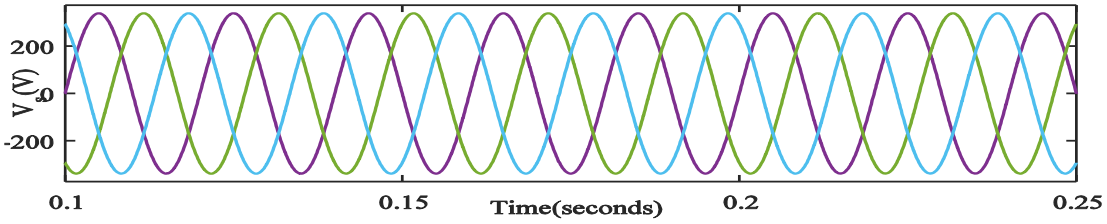



(d) Load current

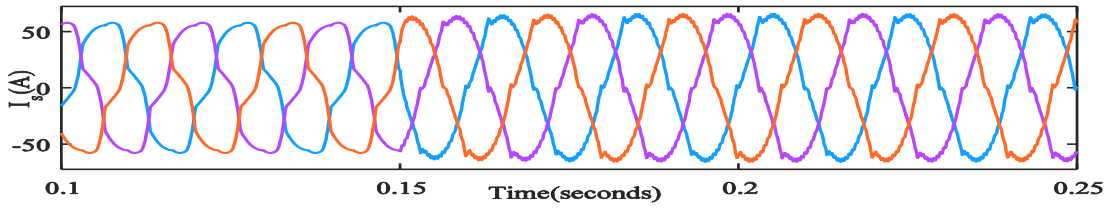



(e)DSTATCOM current

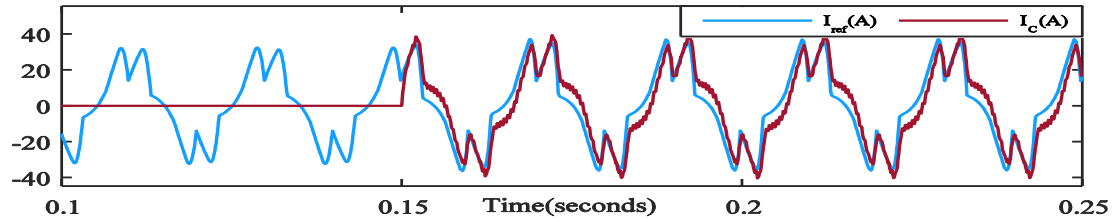
**Figure 5.6** Performance of LSPWM with unbalanced load condition (unbalance load switched at t=0.1 sec.)



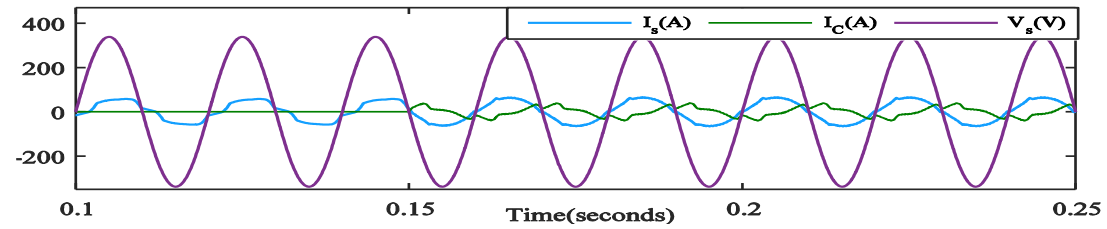

(a) Grid voltage



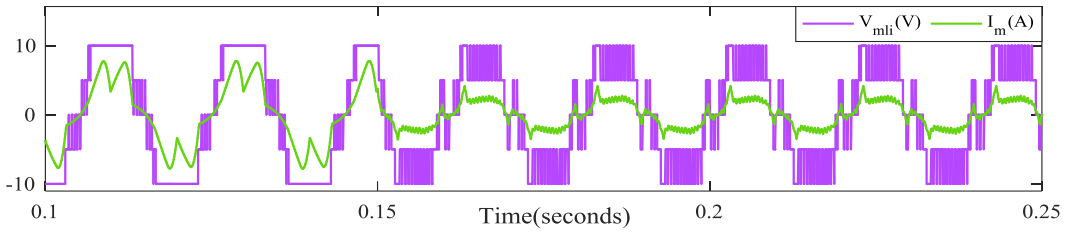

(b) Grid current




(c) Reference current tracking with LSPWM (Phase A)




(d)Grid voltage and current and compensator current (Phase A)

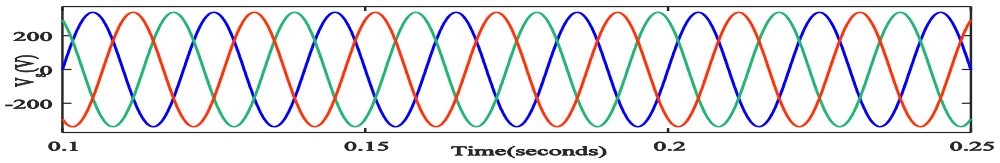



(e) Output voltage (×0.02) and modulation function (×3) at 2 kHz

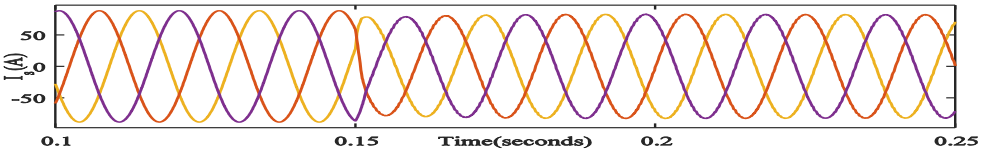
**Figure 5.7** Performance of LSPWM with non-linear load condition (DSTATCOM switched on at t=0.15sec.)

### 5.4.2 Performance under Phase Shifted PWM for DSTATCOM

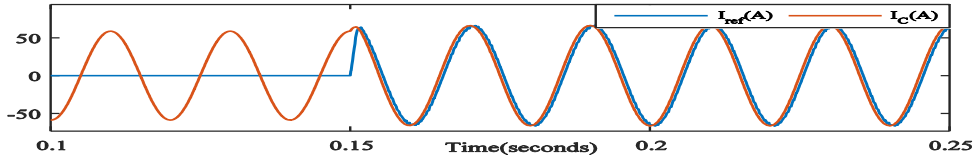
For performance evaluation of CHB multilevel inverter based DSTATCOM under PSPWM grid condition with linear, non-linear, and unbalanced load is shown from Fig5.8 to Fig 5.10.To achieve grid operation in unity power factor under different load condition, the requirement of design of inner current control is required. Presented results are shown for reference current fed to proportional controller to get optimum modulation function. In Fig. 5.8(e) and 5.10(e) multilevel



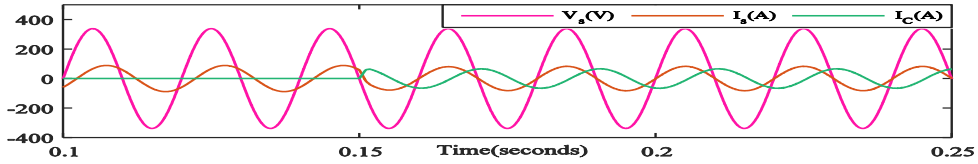

(a) Grid voltage



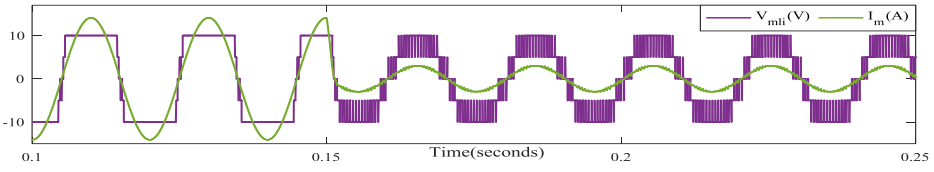

(b)Grid current




(c)Reference current tracking with PSPWM (Phase A)



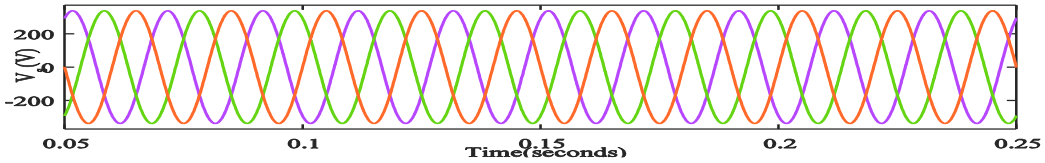

(d)Grid voltage and current and compensator current (Phase A)



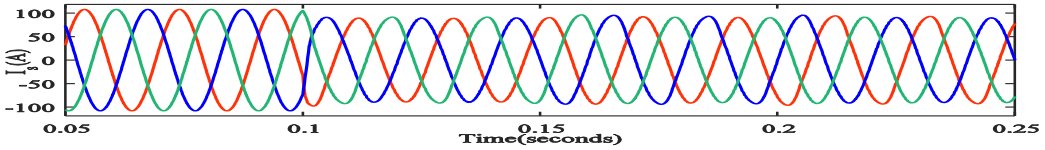

(e) Output voltage (×0.02) and modulation function (×3) at 2 kHz

**Figure 5.8** Performance of PSPWM with linear load condition (DSTATCOM switched on at t=0.15 sec.

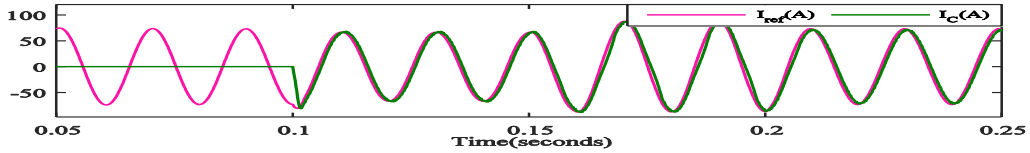
voltage output and modulation function are shown with carrier wave frequency of 0.5 kHz. In PSPWM the ultimate switching frequency varies such as with four carrier wave of 0.5 kHz frequency, the equivalent switching frequency is (0.5 × 4 kHz) 2 kHz for switching devices. Tracking of reference current in Fig.5.10(c), 5.10(b), 5.10(c) with different load condition depicts the average dynamics of PSPWM. For clarity multilevel output voltage and modulation function is scaled.



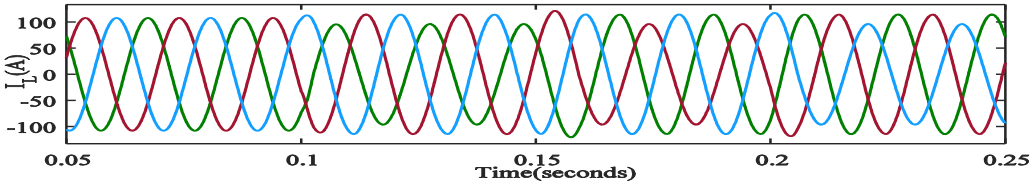

(a)Grid voltage



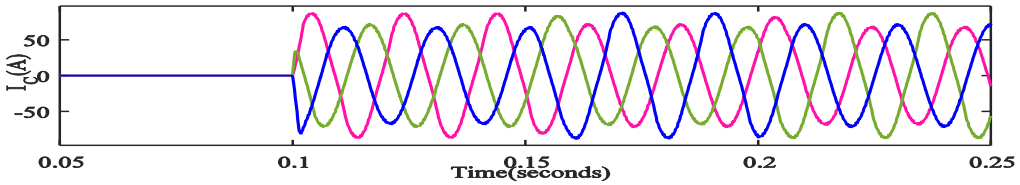

(b)Grid current




(c) Reference current tracking with PSPWM (Phase A)

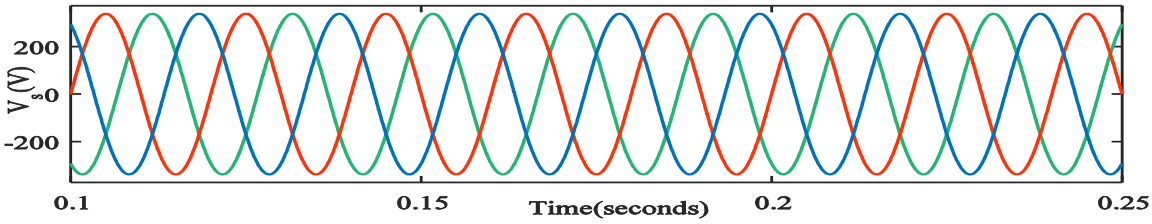



(d) Grid voltage and current and compensator current (Phase A)

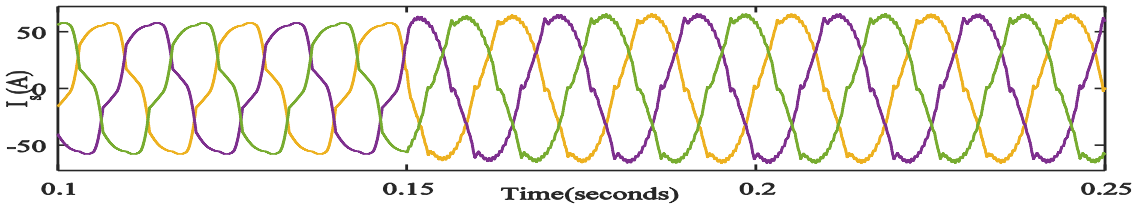



(e) Compensator current

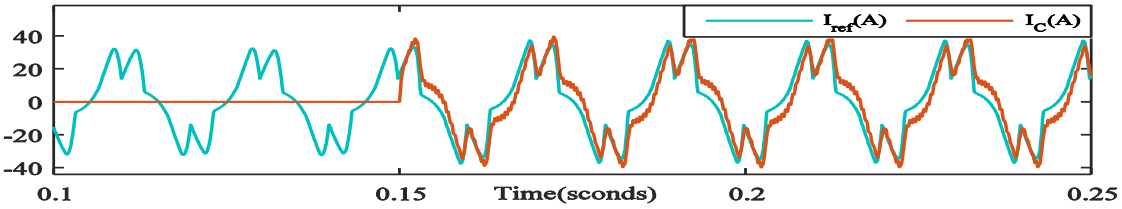
**Figure 5.9** Performance of PSPWM with Unbalance load condition (unbalancing at t=0.1s)



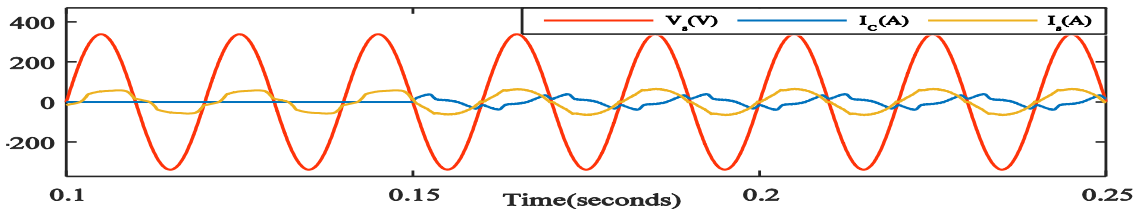

(a) Grid voltage



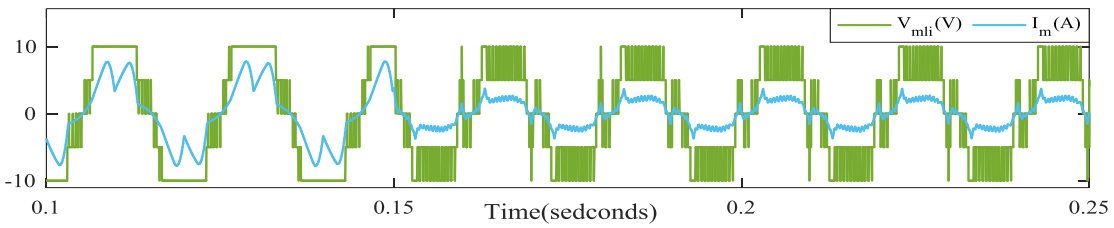

(b)Grid current




(c) Reference current tracking with PSPWM (Phase A)




(d) Grid voltage and current and compensator current (Phase A)

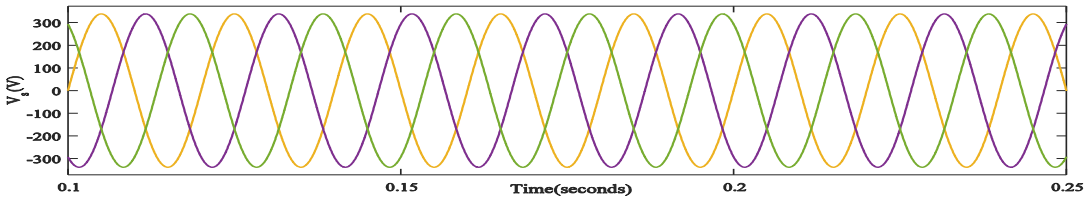



(e) Output voltage (×0.02) and modulation function (×3) at 2 kHz

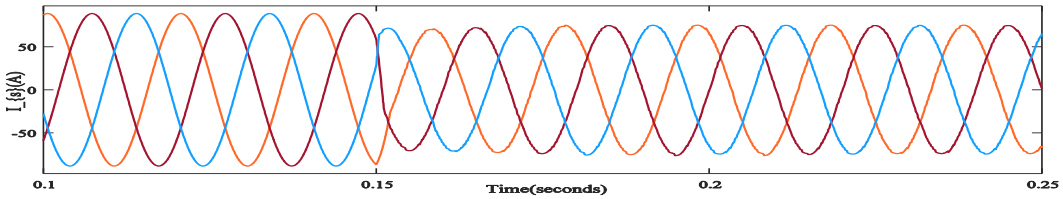
**Figure 5.10** Performance of PSPWM with Non-linear load condition (DSTATCOM is switched on at t=0.15 sec.)

### 5.4.3 Performance of digital MHCC for DSTATCOM

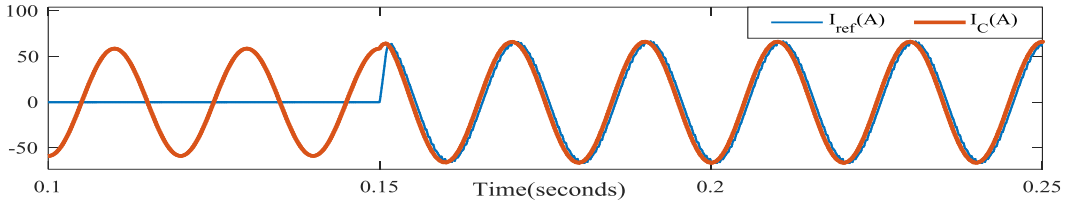
Performance of DSTATCOM under MHCC is shown from Fig.5.11 to Fig.5.13.Grid is operating under unity power factor due to higher dynamics of Current controller.



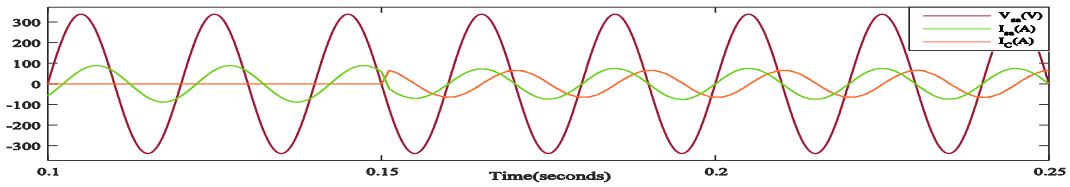

(a) Grid voltage



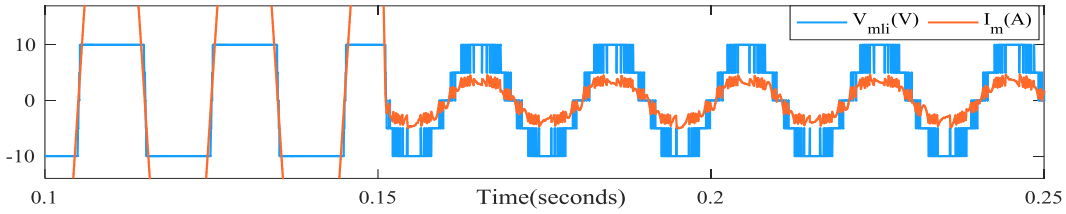

(b)Grid current




(c) Reference current tracking with MHCC (Phase A)

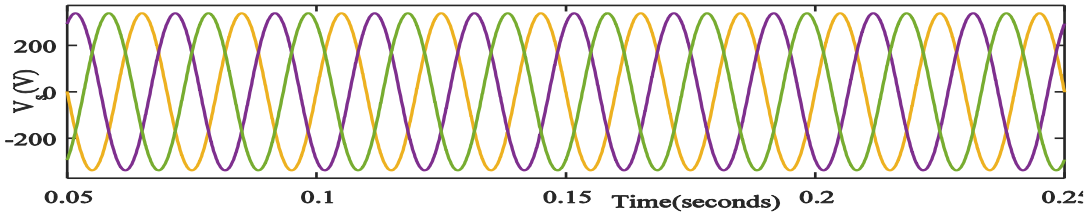



(d)Grid voltage and current and compensator current (Phase A)

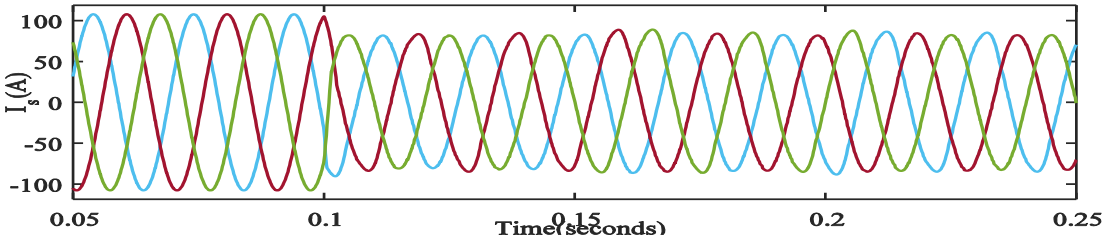



(e)Output voltage (×0.02) and modulation function

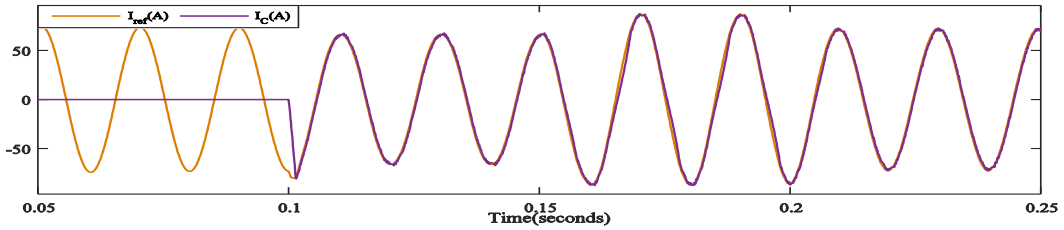
**Figure5.11** Performance of MHCC with linear load condition (DSTATCOM switched on at t=0.15 sec.



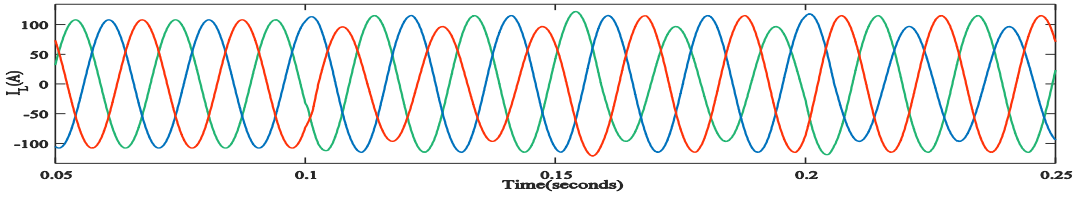

(a) Grid voltage



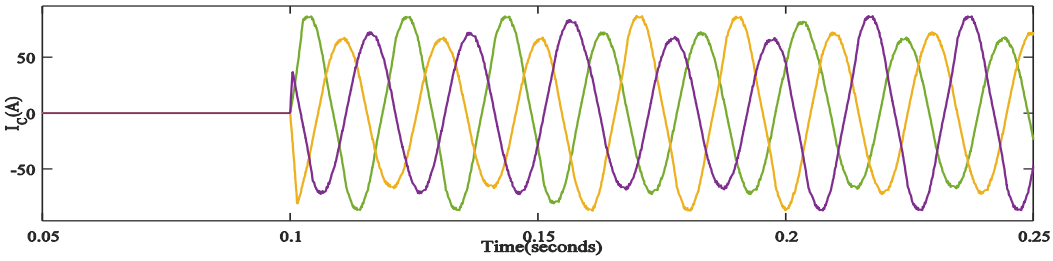

(b) Grid current




(c) Reference current tracking with PSPWM (Phase A)

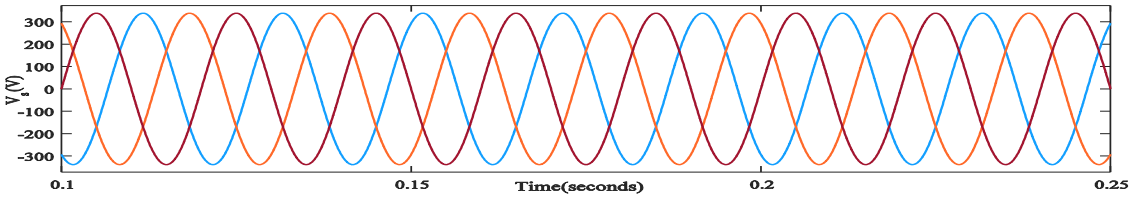



(d) Grid voltage and current and compensator current (Phase A)

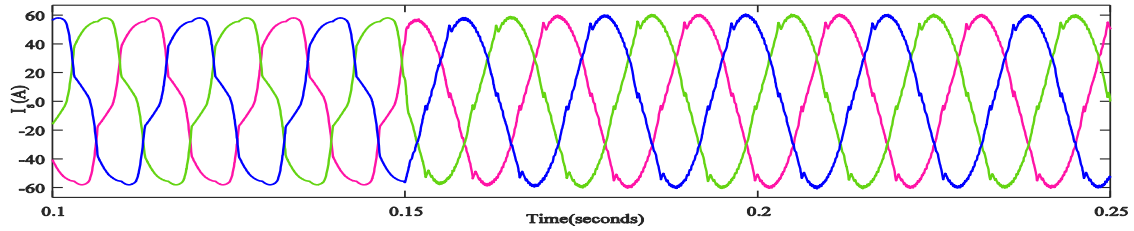



(e) Compensator current

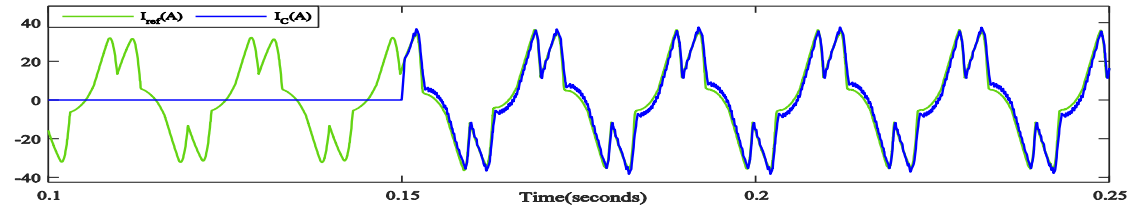
**Figure5.12** Performance of MHCC with unbalanced load condition (unbalancing at t=0.1 seconds.)



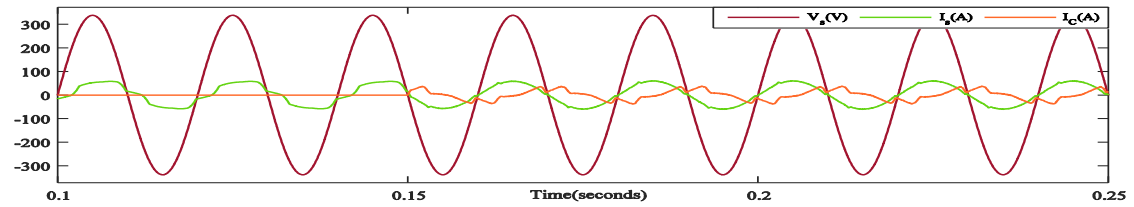

(a)Grid voltage



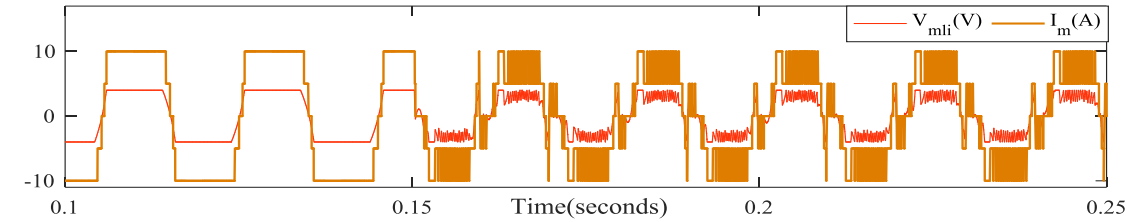

(b)Grid current




(c)Reference current tracking with PSPWM (Phase A)




(d)Grid voltage and current and compensator current (Phase A)




(e) Output voltage (×0.02) and modulation function

**Figure 5.13** Performance of MHCC with non-linear load condition (DSTATCOM switched on at t=0.15 seconds)

Tracking performance of compensator is found better than PSPWM and LSPWM. Multilevel inverter output and modulation function is scaled for clarity. And non-linear nature of controller can be predicted in Fig.5.13 (e).Multilevel output voltage contains more THD than outputs obtained from SPWM techniques. So higher order filter design that can suppress harmonics contents at better attenuation rate at PCC is required. But it consists of some disadvantages such as variable switching frequency (due to variable hysteresis band for different level of voltage) and average PCC voltage. Hysteresis band is taken (4.2×2) A for average switching frequency of 2.6 kHz. The switches are operating at two band of (-2.1~+2.1) A and (-4.2~+4.2) A with three level and five level output generation of MLI respectively. Three values of THD in percentage are shown in table 5.2 are for linear load, unbalance load, Non-linear load condition.

**Table 5.2 Comparison of PSPWM, LSPWM and MHCC for grid connected system**

| | **PSPWM** | **LSPWM** | **MHCC** |
|---|---|---|---|
| Dynamics | Average | Average | High |
| Nature | Linear | Linear | Non-linear |
| Level of complexity | Higher | Higher | Less |
| Switching frequency | Constant | Constant | Variable |
| Power stress | Equally distributed | Unequally distributed | Unequally distributed |
| Modulator | Open and close loop | Open and close loop | Close loop only |

**Table 5.3 THD of grid current ($i_s$) under different load condition**

| Nature of load | **PSPWM** | **LSPWM** | **MHCC** |
|---|---|---|---|
| Linear | 0.45% | 0.65% | 1.6% |
| Non-linear | 3.67% | 3.84% | 3.72% |
| Unbalanced | 0.89% | 1.60% | 2.60% |

**Table 5.4 THD of voltage at PCC ($V_{pcc}$) under different load condition**

| Nature of load | **PSPWM** | **LSPWM** | **MHCC** |
|---|---|---|---|
| Linear | 1.73% | 1.77% | 2.5% |
| Non-linear | 4.52% | 4.89% | 4.5% |
| Unbalanced | 4.1% | 3.78% | 3.66% |

## 5.5 Conclusion

In this chapter digital MHCC is proposed for CHMLI based DSTATCOM and compared with conventional PSPWM and LSPWM techniques. The reference current is generated using direct current control based SRFT. Model is developed in MATLAB/Simulink for performance evaluation. For the Comparative analysis LSPWM and PSPWM technique is employed and compared with the proposed MHCC under linear load, unbalance load and non-linear load condition. The relation between modulation function and output voltage of CHMLI is demonstrated and it has supported the nature of controller i.e. linear for LSPWM, PSWM and non-linear for MHCC. Some outcomes of this chapter can be summarized as follows,

**Multiband HCC based DSTATCOM**: MHCC is proposed for the DSTATCOM. Performance of the MHCC for current control is found better compare to PSPWM and LSPWM especially under distorted non-linear load condition. MHCC offers some advantages for DSTATCOM application such as ease in implementation and implicit modulation of CHMLI with enhanced current control.

**Dynamics**: It is notable that tracking performance of the MHCC is better compare to LSPWM and PSPWM in linear, non-linear and unbalanced load. It means reduced steady state error and better dynamics of the system. Overall stability of the system is improved.

**Comparative analysis**: Comparison of current controller employing linear (PSWM and LSPWM) and non-linear (MHCC) nature of control is done for the same grid and load condition.

# CHAPTER 6

# CONCLUSION

This thesis explores and proposes some solution to critical challenges for high efficiency electrical energy conversion system.

Grid connected power electronics converters are used for the application of renewable energy generation. Multilevel inverters are gaining attention due to their capability of operation in medium voltage high power application at lower switching frequency. Grid connected modular cascaded H-bridge multilevel inverter (CHMLI) offers high performance electrical energy conversion system. However, filter design for interfacing of multilevel inverter with grid is a critical issue. In this thesis design of LCL filter is proposed considering modified constraints that is suitable for lower switching frequency operation (1-5 kHz) of CHMLI. And next major challenge of complex switching control for CHMLI topology is considered, a novel digital multiband hysteresis current controller (HCC) is proposed.

At first, basic operation of CHMLI is investigated using FPGA based digital control. And it is concluded that sinusoidal pulse width modulation techniques (SPWM) such as phase shifted PWM have advantages over level shifted PWM, such as equal switching stress and better harmonic profile. FPGA hardware-in-loop co-simulation is a rapid testing tool for controller prior to real plant implementation. FPGA hardware co-simulation is proposed for controller prototyping of CHMLI. Third harmonics injected PWM (THIPWM) is used for the controller prototyping of CHMLI. It is concluded that THIPWM offers wide linearity range, maximized dc bus utilization, and improved THD using hardware co-simulation results.

In the application of the CHMLI for grid connected mode, three phase DSTATCOM based system is considered. A LCL filter design is proposed for CHMLI based DSTATCOM system, considering modified constraint for lower switching frequency operation. CHMLI combined with LCL filter offers certain advantages for DSTATCOM such as reduced inductor size, improved pcc voltage, wider bandwidth and less cost. The performance of DSTATCOM is appraised for abnormalities in load (poor power factor, unbalancing and non-linearity). The effect of sag-swell in voltage at pcc is reduced in presence of LCL filter interfaced DSTATCOM. The complete model

is developed in MATLAB Simulink and the performance of LCL filter interfaced CHMLI based DSTATCOM is evaluated with simulation results.

In another application of single phase grid connected CHMLI, a digital multiband HCC is proposed for the unity power factor operation (UPF) of the grid. A digital multiband HCC is implemented using S-R flip-flop that offers dynamic performance, reduced cost, less complexity and better re-configurability by its digital means. Digital multiband HCC is capable of reference current tracking with implicit modulation of CHMLI. The effect of independent variables such as hysteresis band, grid inductance on switching frequency is analyzed in simulation and validated with experimental results. Digital multiband HCC offers an easy alternative solution to close loop operation of CHMLI.

It is essential to compare the performance of proposed multiband digital HCC with the conventional controller. The proposed controller is compared with conventional phase shifted and level shifted PWM techniques for three phase DSTATCOM. Model is developed in MATLAB/Simulink for performance evaluation under linear, non-linear and unbalance load conditions. Performance of the multiband HCC is found better under the distorted load condition. It is concluded that MHCC possess better tracking performance, stability, ease in implementation for the DSTATCOM.

The proposed digital multiband HCC also work on variable switching frequency similar to conventional HCC. Special attention is need in future to maintain operating switching frequency. Digital control on FPGA provides the fast and reconfigurable prototyping of controllers for the power electronics system. Real time implementation of SRFT based direct current control for the DSTATCOM and generation of reference current for switching control of CHMLI is part of future work. Combination of digital HCC with SRFT based reference current generation have shown better stability in simulation, experimental verifications are under progress. Application of digital multiband HCC for motor drive application is having implacable scope of future work.

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