A Low Power 900MHz Superheterodyne Compressive Sensing Receiver for Sparse Frequency Signal Detection

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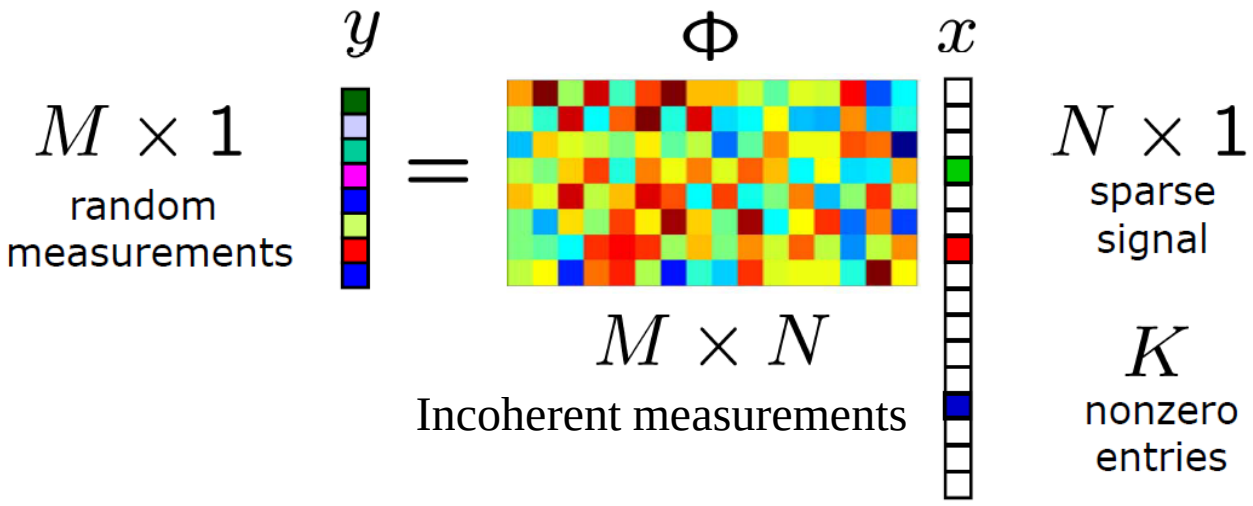
Electrical Engineering and Computer Science

Outline

- Introduction
- System level block diagram
- Compressive sensing method
- Circuit level design and results
  - LNA
  - LFSR and clock
  - Mixer
  - Integrator
  - ADC
- Conclusion

Introduction to Compressive Sensing

- Compressive sensing
  - Sensing by random sampling of the signal of interest
- Compressive recovery:
  - Solving an ill-posed problem



Courtesy of R. Baraniuk et al., Tutorial on compressive sensing (2008 Information Theory and Applications Workshop)

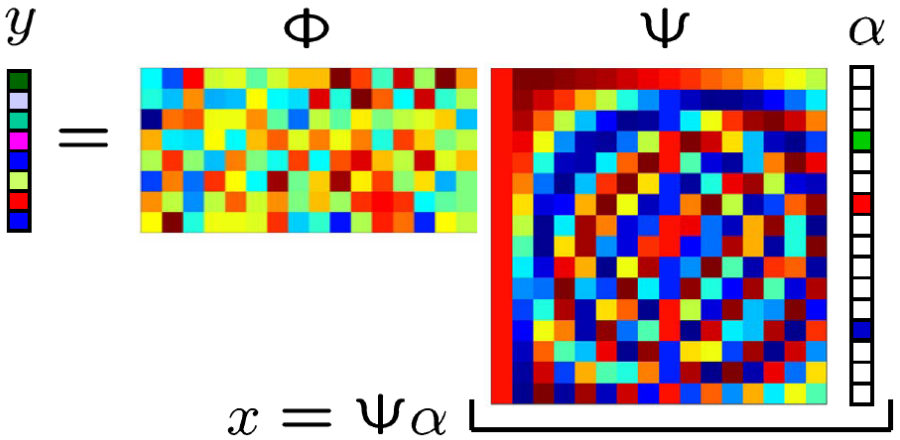
A Mathematical Model

- Random sampling of data
  - Sparse signal in one basis
- Generating data out of M measurements
- Fourier basis:

$$\psi_j(t) = n^{-1/2} e^{i\,2\pi\,jt/n}$$

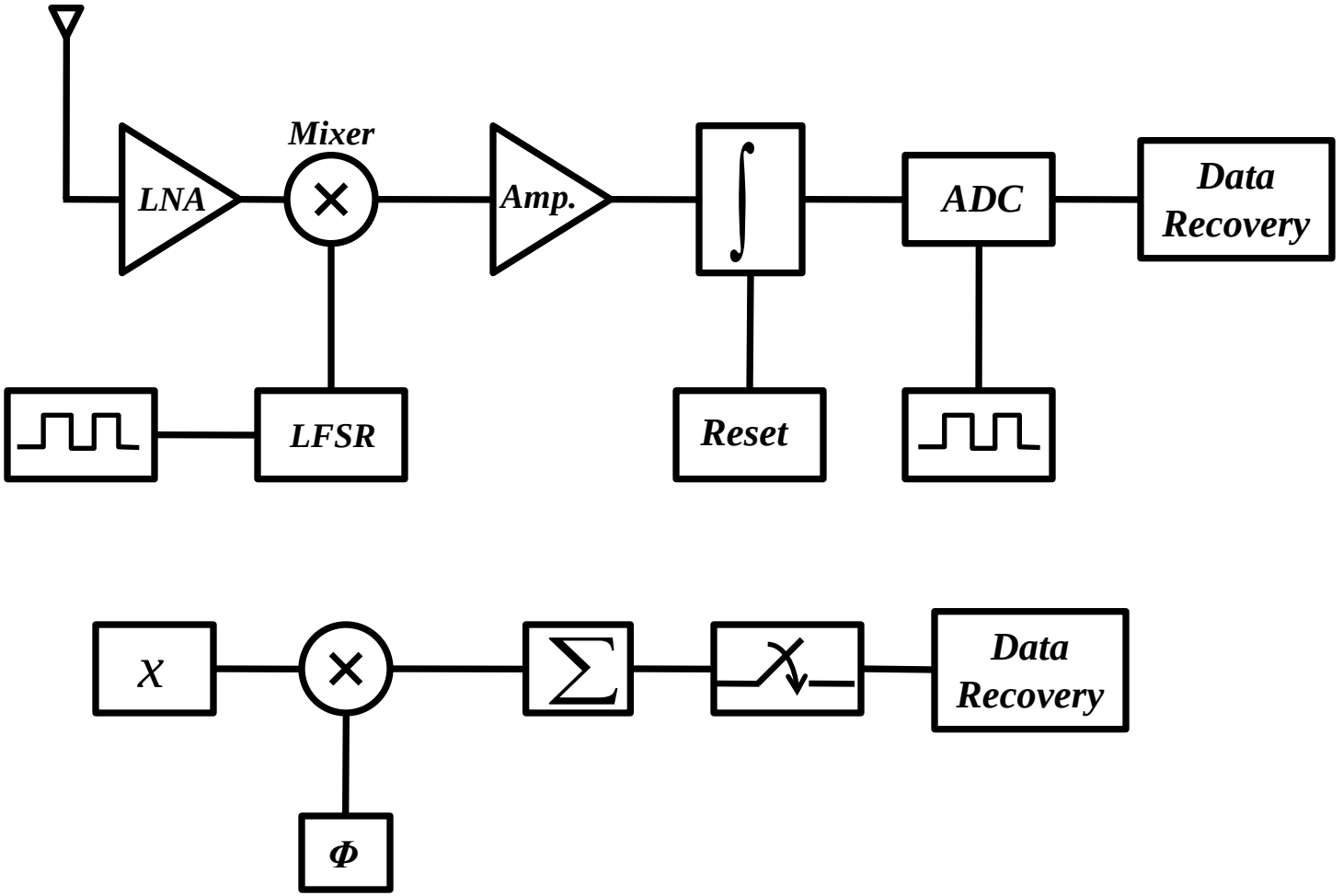
- Utilizing the Euler equality:
  - Separate the real and imaginary parts

$$y = \Phi x = \Phi\Psi\alpha$$



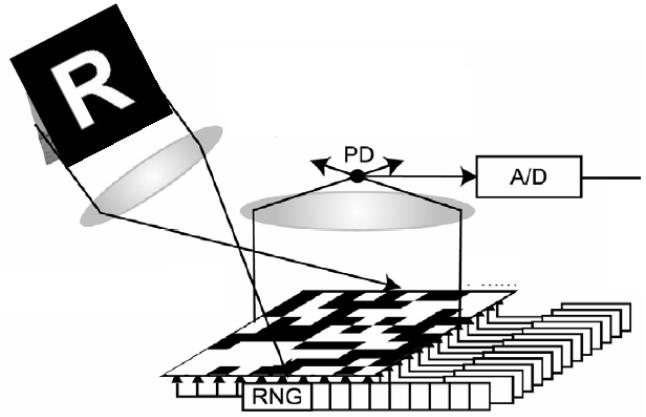
Courtesy of R. Baraniuk et al., Tutorial on compressive sensing (2008 Information Theory and Applications Workshop)

System Topology



Applications of Compressive Sensing

- Imaging
  - Single pixel camera
  - Single pixel Radar imaging
  - Remote sensing
  - Medical imaging



Single pixel camera
Courtesy of Rice University
Professor R. Baraniuk

- Analog
  - Sensor node in wireless sensor network (Tx structure)
  - Analog-to-information conversion (Replacement for ADC)
  - Compressed receiver (Rx structure)

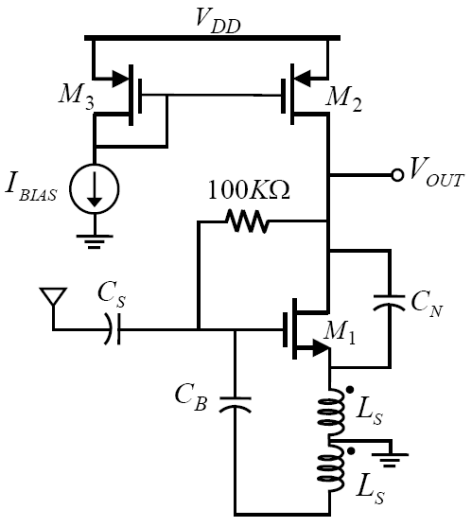
Recovery Algorithm

- Recovery algorithms can reconstruct the sparse signal components in the basis

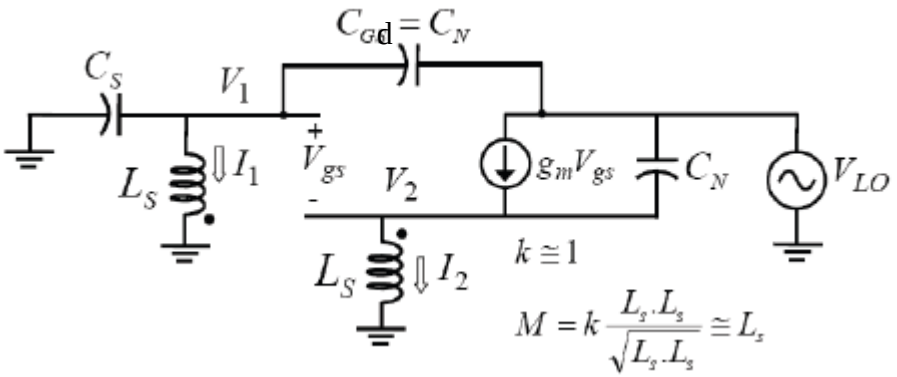
- Compressive sensing recovery algorithms:
  - Based on greedy algorithms
    - Orthogonal Matching Pursuit:
      - Utilizes the Gram-schmitt orthogonalization method
      - Convergence after the number of sparse elements

Low Noise Amplifier

- Low-power approach:



A Novel Ultra-Low Power (ULP) Low Noise Amplifier using Differential Inductor Feedback
Amin Shameli and Payam Heydari



$$Zin \approx \frac{1}{j\omega C_s} + j\omega L_s + 2\omega^2 L_s{}^2 g_m$$

$$Gain = -2 g_m V_1 Z_L$$

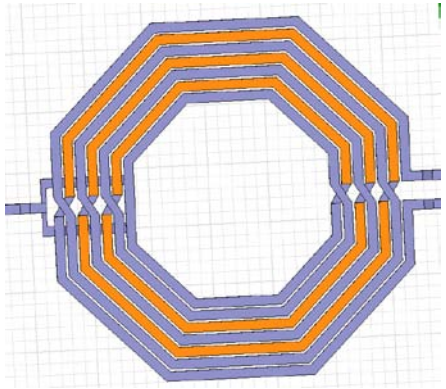
$$V_1(V_{LO}) = 0$$

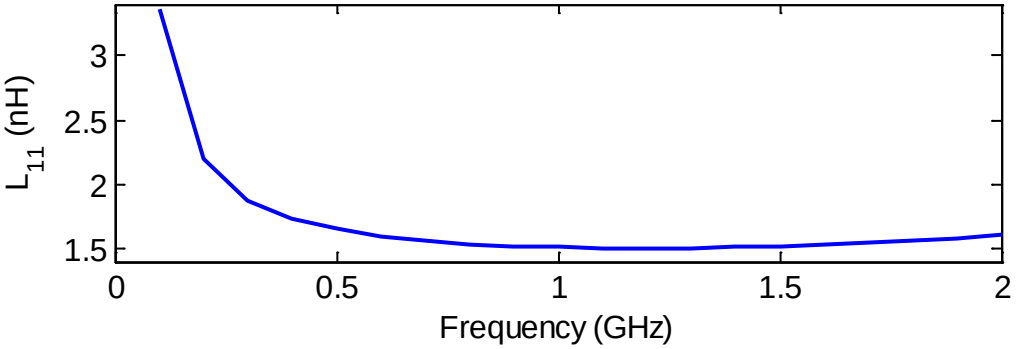
$$\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} sL_s & -sL_s \\ -sL_s & sL_s \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

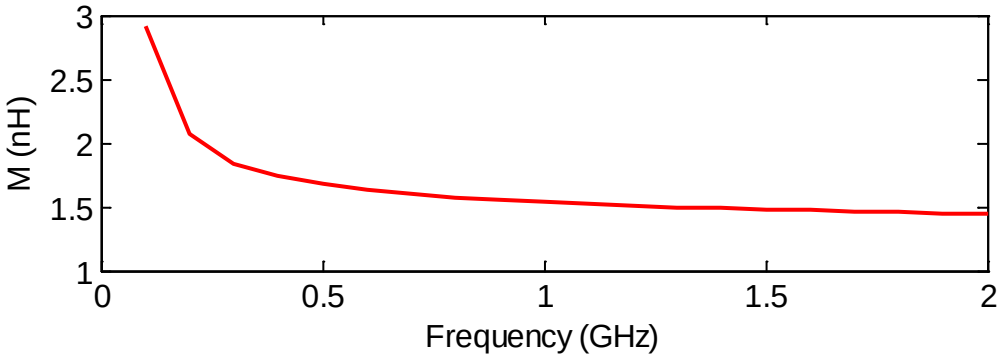
$$NF = 1 + \frac{\gamma_n}{4(1+\omega^2 g_m{}^2 L_s{}^2)} + \frac{\gamma_p g_{mp}}{2 g_{mn}}$$

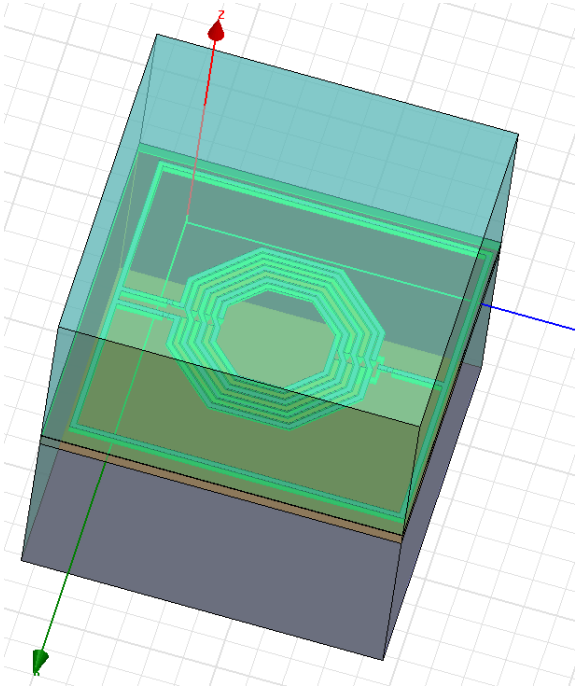
Transformer Analysis (HFSS)

- Low-power approach:
  - Center-tapped 3-port transformer



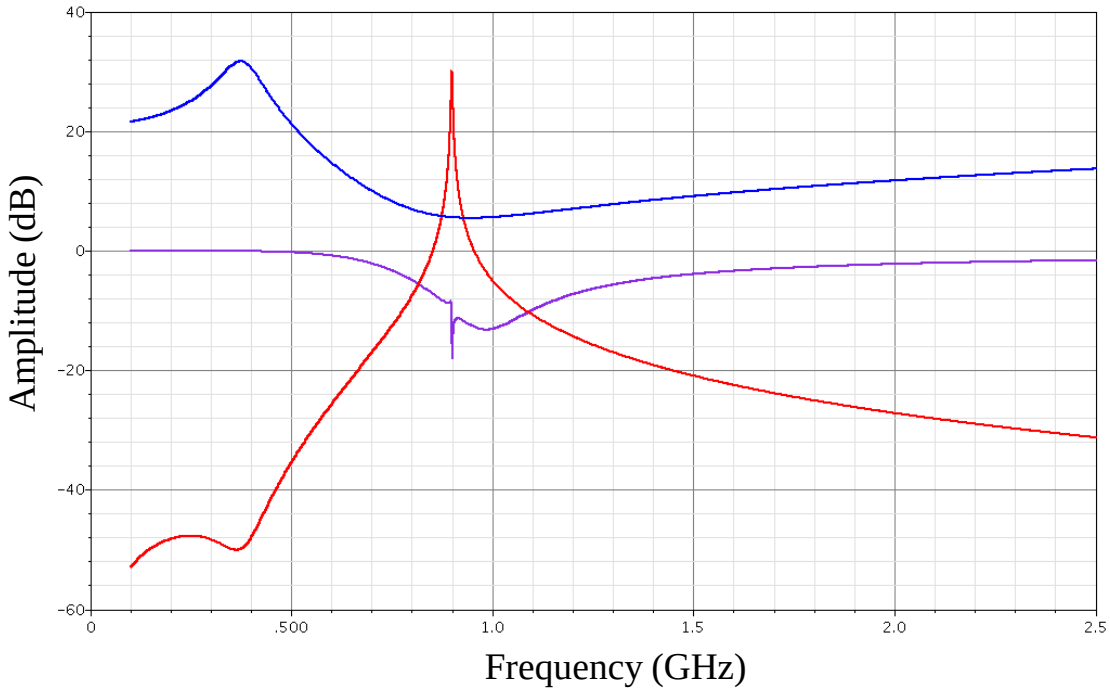






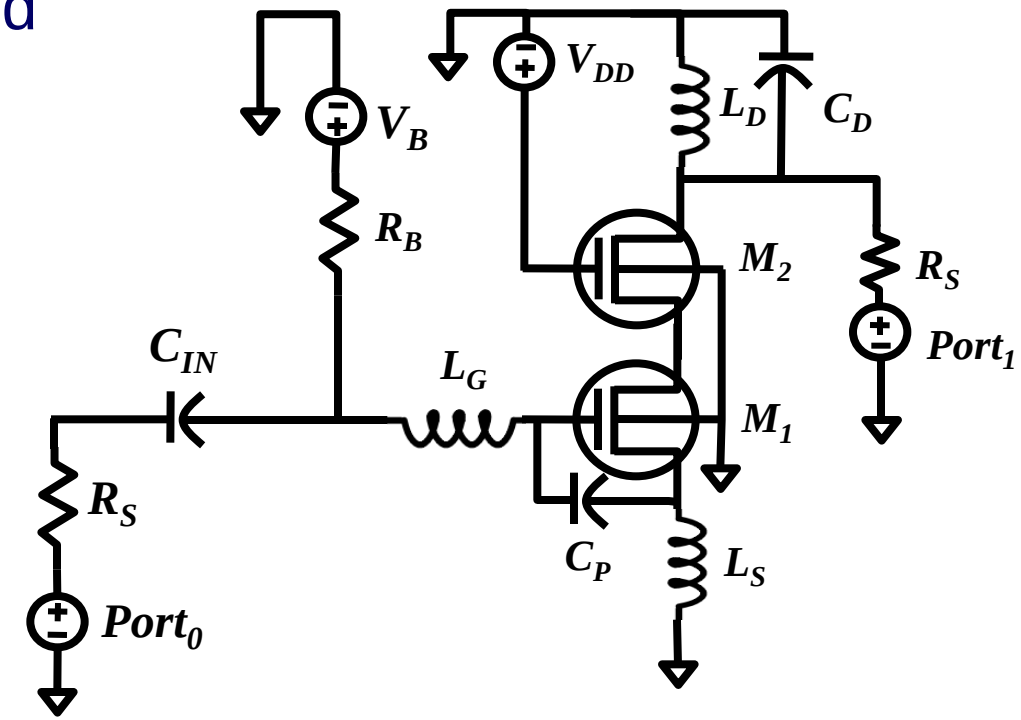
Simulation Results

- 100μW power consumption
- 5.2dB noise figure
- 30dB peak gain
- 20dB isolation



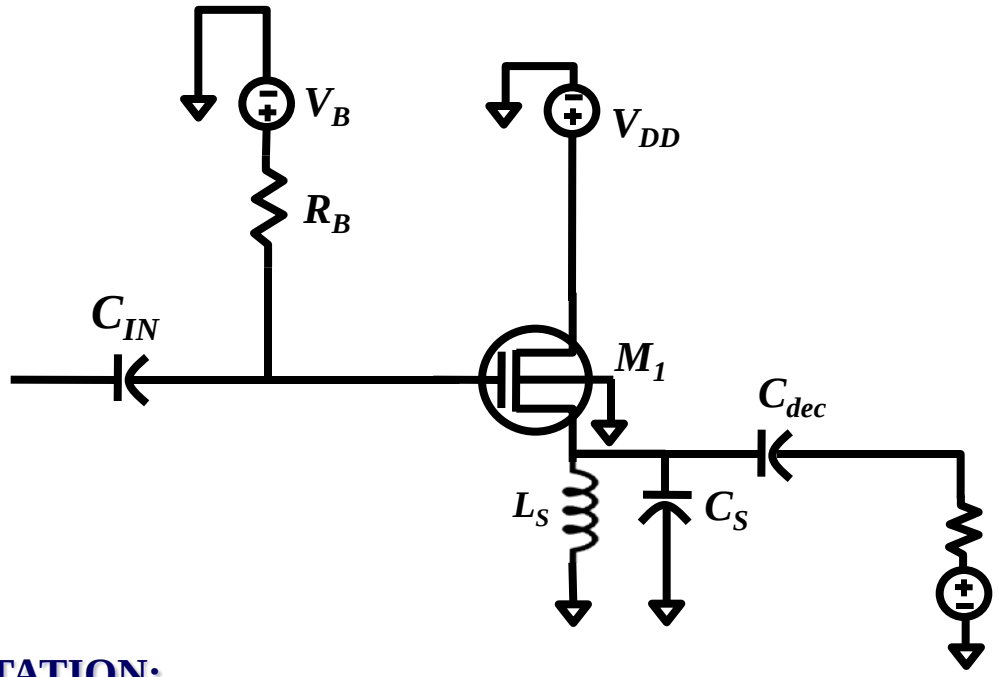
Low Noise Amplifier

- Low-noise approach:
  - Inductively-degenerated cascode topology

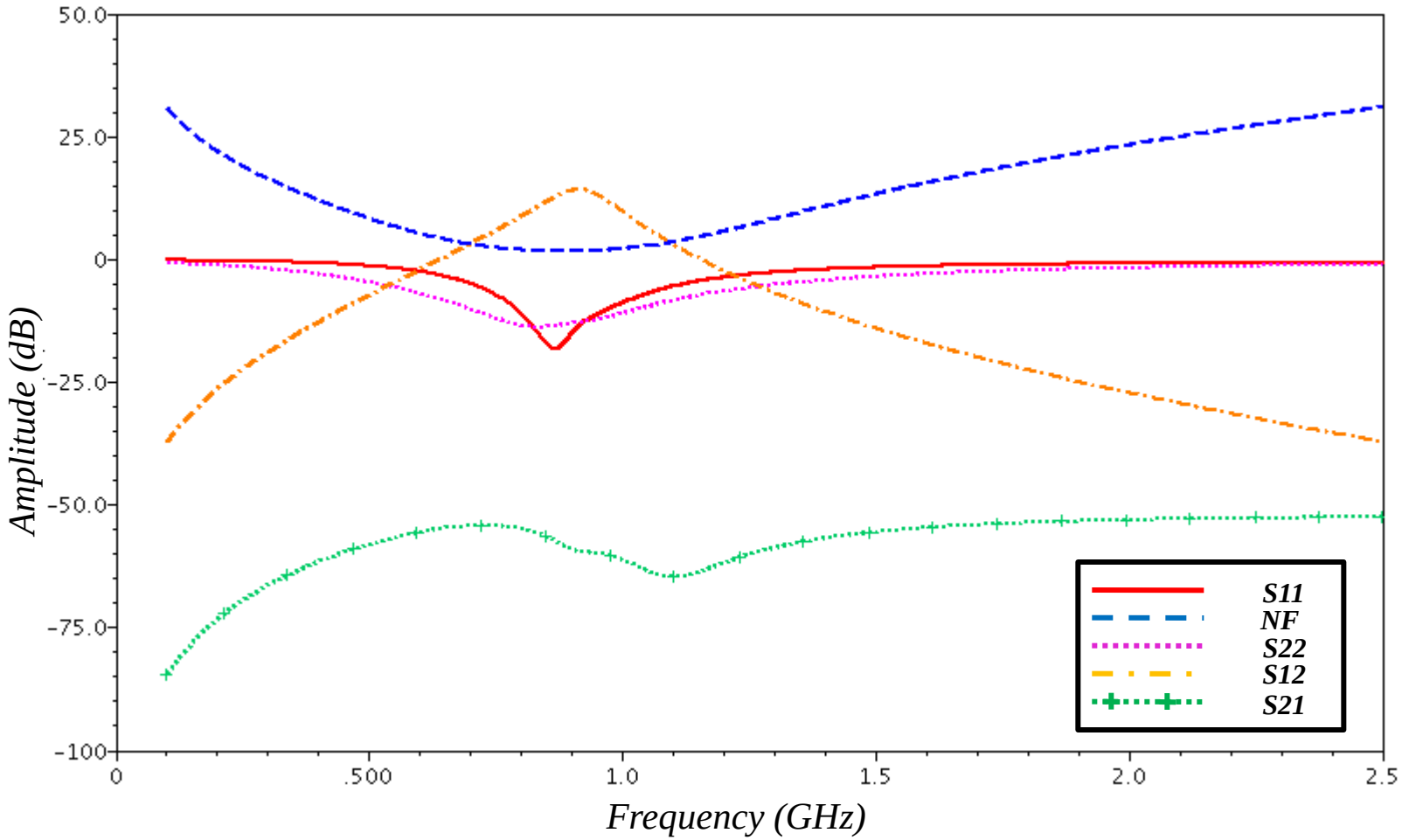


Narrowband Buffer

- Buffer is required for increasing the isolation of the LO signal from the antenna
- It can also provide output impedance matching to 50 ohm

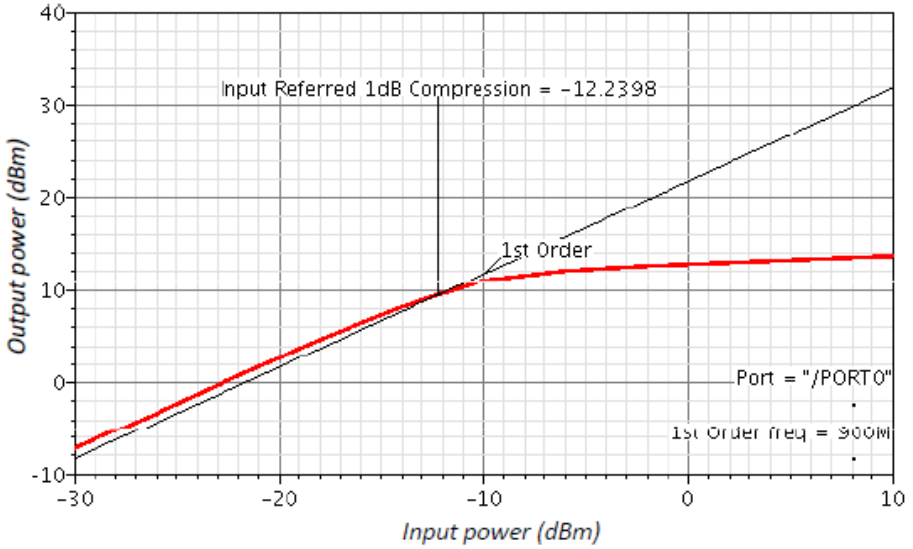


Total LNA Simulation Result

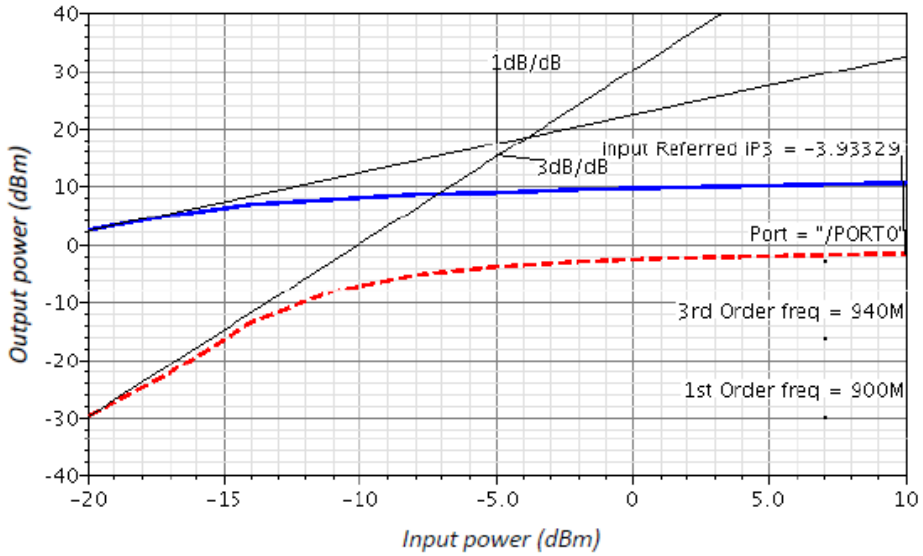


LNA Linearity

- Input referred 1dB compression point

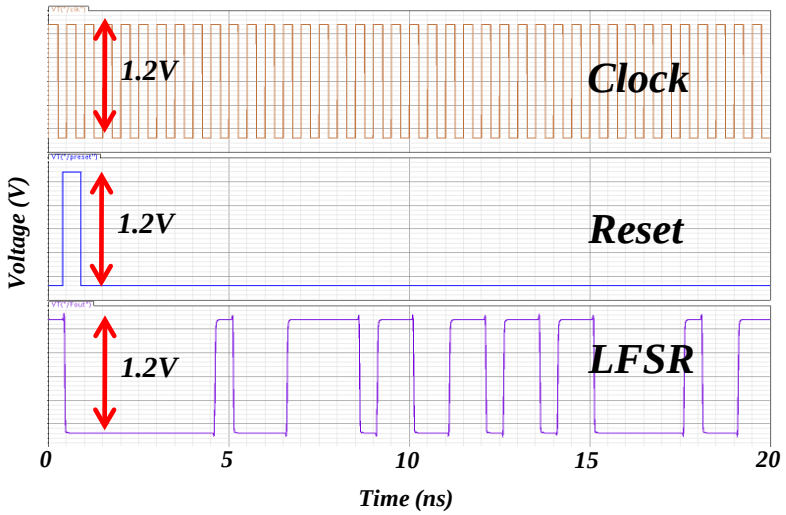


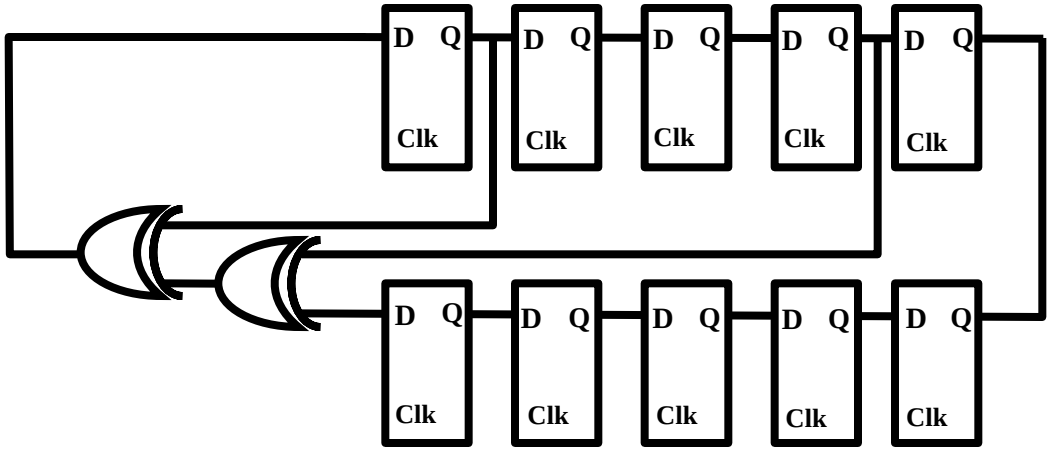
- 3rd order input referred intercept point (IIP3)



Linear Feedback Shift Register (LFSR)

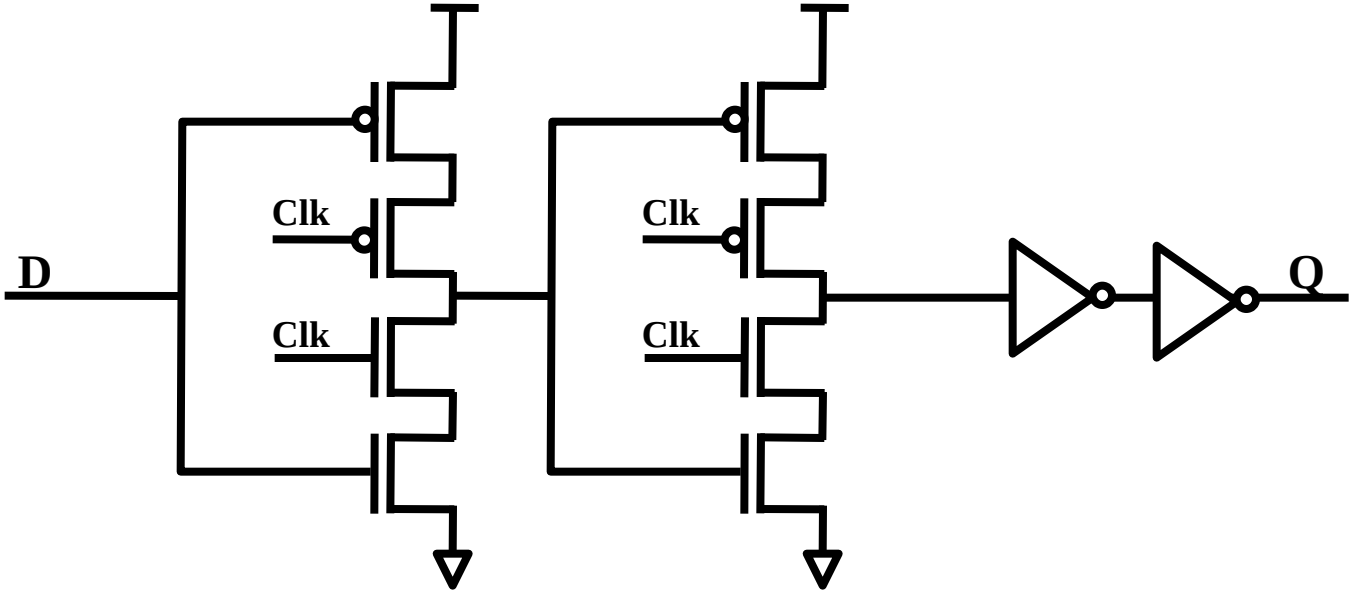
- Produces pseudo random numbers
- Is made of ten positive edge C^2MOS registers
- More than 99% success over Monte Carlo Simulation





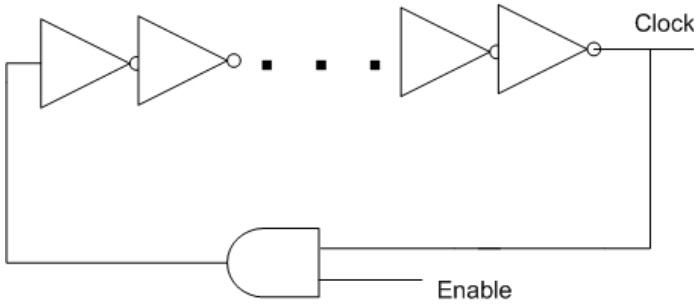
C²MOS Registers

- C²MOS structure chosen to meet the high performance, low power specs.
- Value is stored on parasitic nodes.



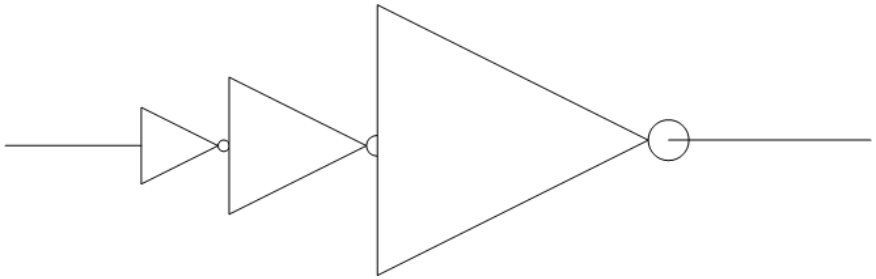
Clock Generator and Buffers

- Clock generator contains 11 inverters in a chain and one AND gate for enable signal
- Successfully passed the Monte Carlo simulation
- Phase noise < -100 dBc/Hz at the desired frequency



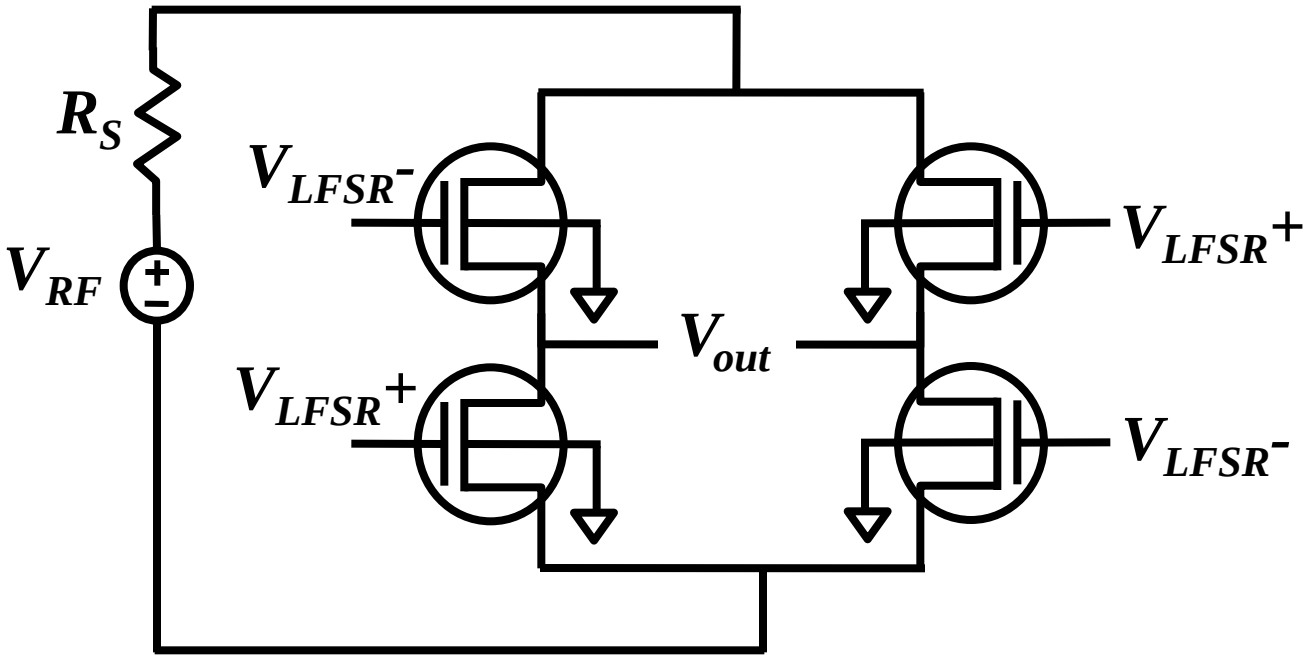
Clock Generator and Buffers

- The total load of LFSR on clock is measured to be 71fF
- One inverter loading is 8fF
- Three inverters with 2X size ratio is chosen based on the method of logical effort
- Total power consumption of the clock and clock buffers together with LFSR is 600 μW at 2GHz



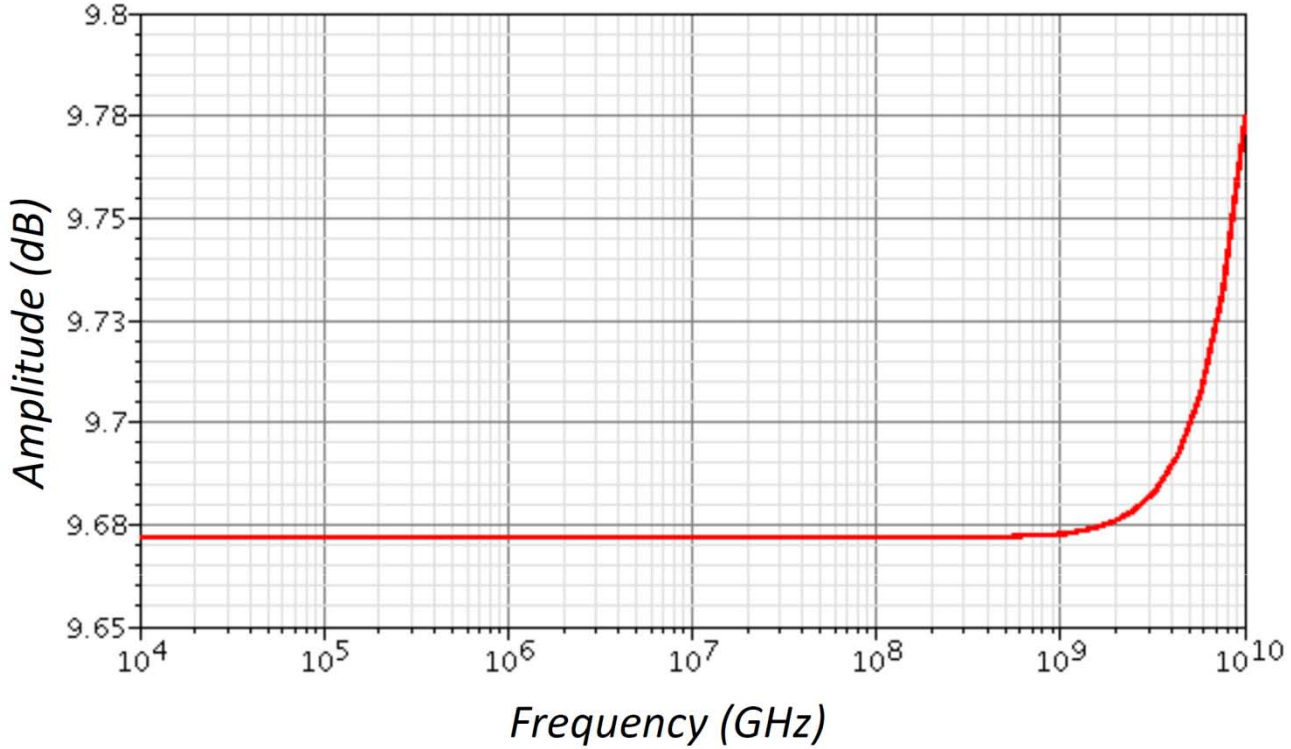
Passive Mixer Design

- Passive mixer can be utilized as a bipolar multiplier
  - The amplified RF signal is multiplied by the LFSR signal

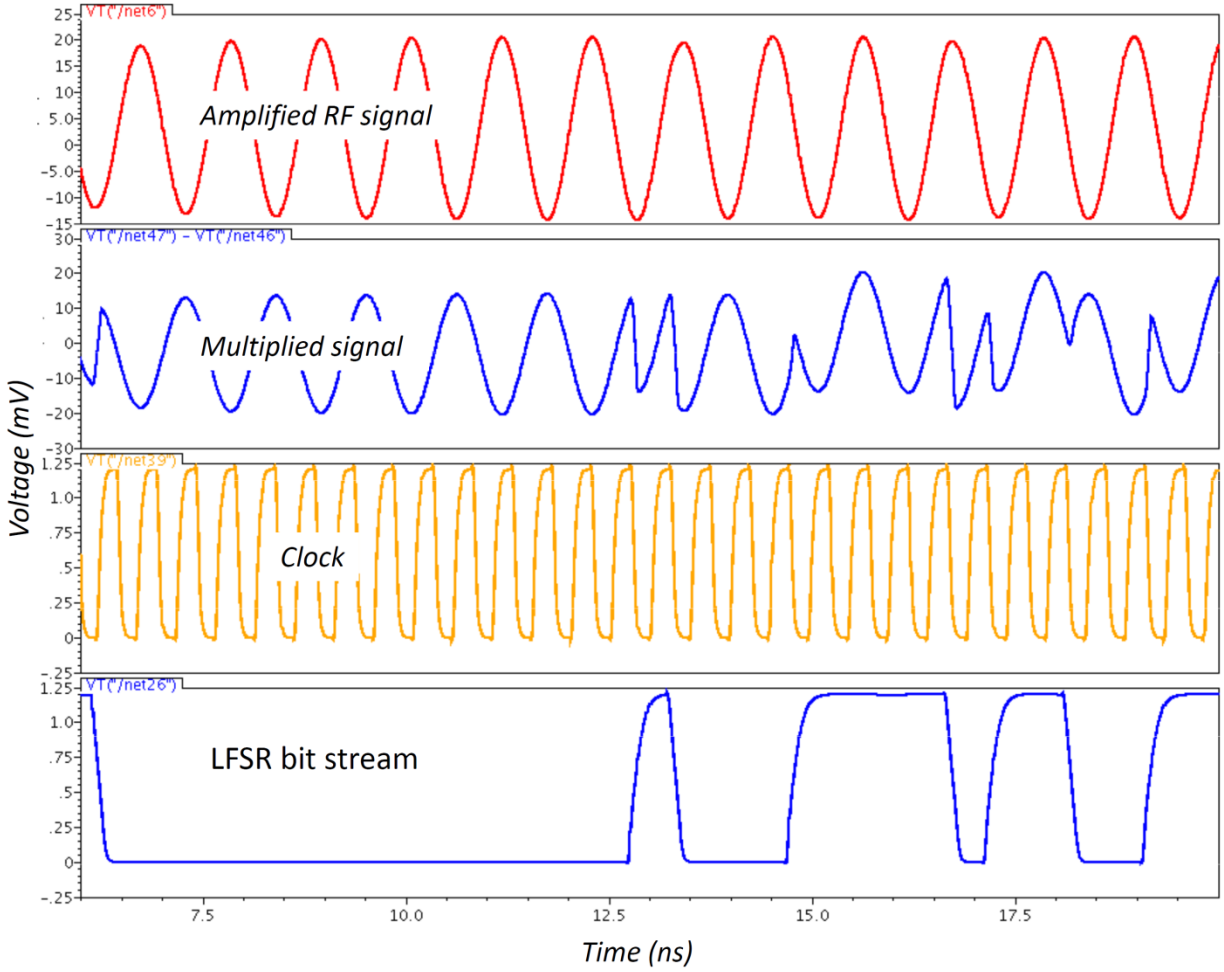


Mixer Specification

- Noise figure is less than 10dB
- Isolation is more than 30dB

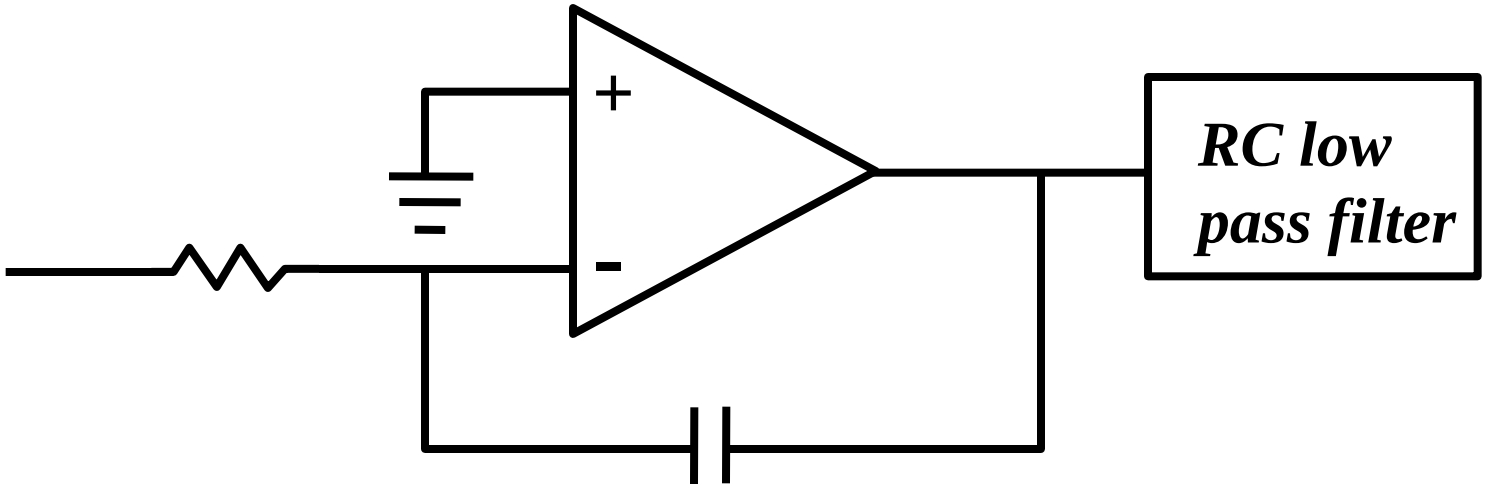


System Response



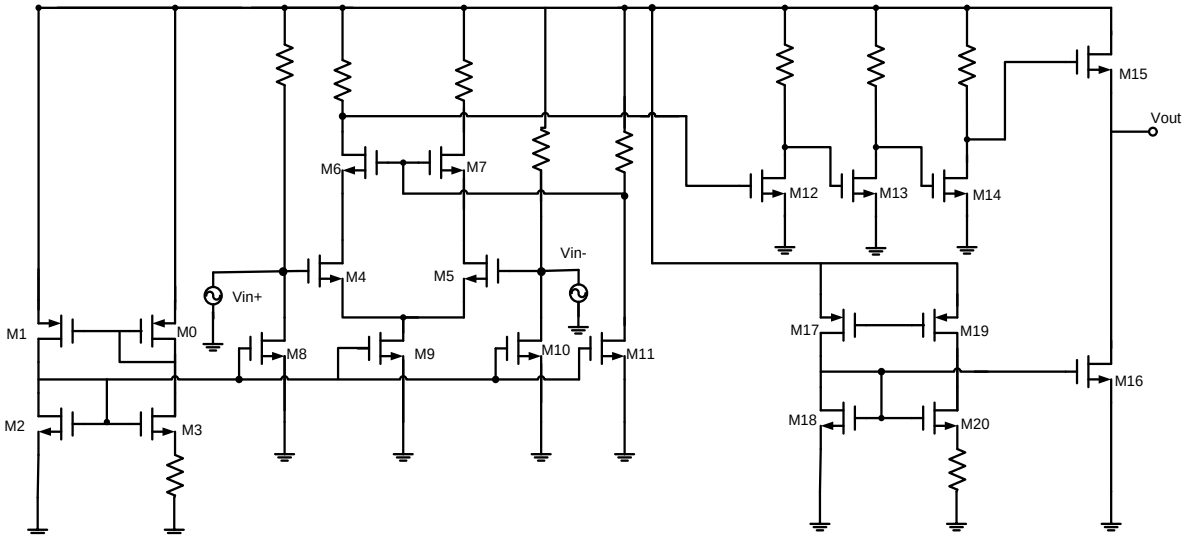
Broadband Integrator

- RC integrator with a broadband amplifier is used
- 10pF coupling caps are used to protect amplifier biasing



A 1.6GHz Broadband CMOS Amplifier

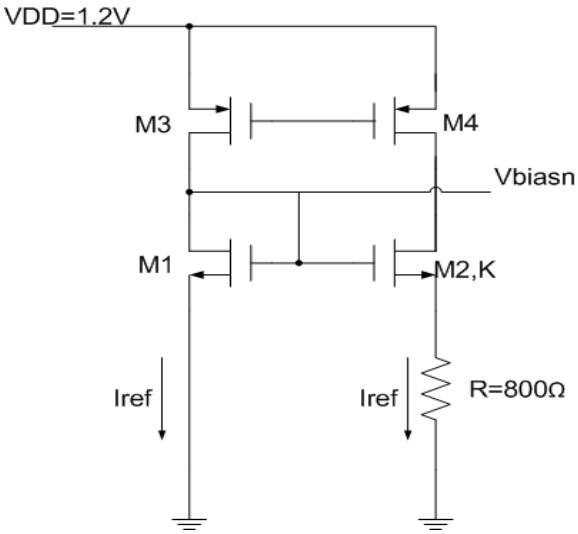
- A cascode differential pair followed by cascaded common-source stages provide the gain of the amplifier
- Three small size source follower stages are used to relax the gain-bandwidth trade off



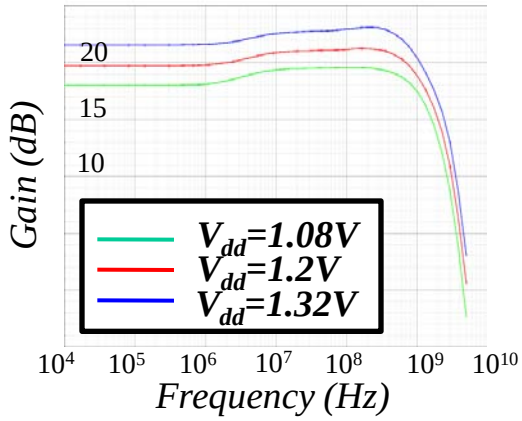
A 1.6GHz Broadband CMOS Amplifier

- Supply independent Beta multiplier current source used

$$I_{ref} = \frac{2}{R^2 k P_n (W/L)_1}\left(1 - \frac{1}{\sqrt{k}}\right)^2$$



Gain vs. Frequency as a function of Temperature



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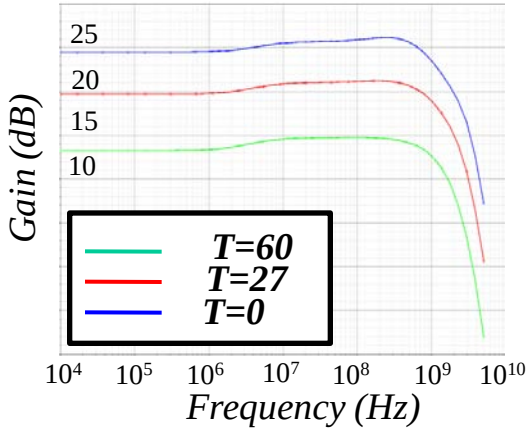
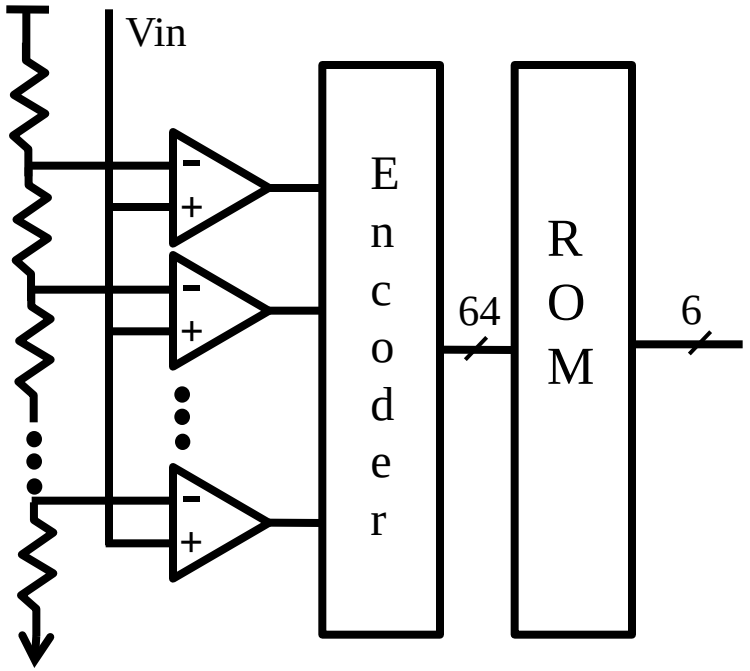


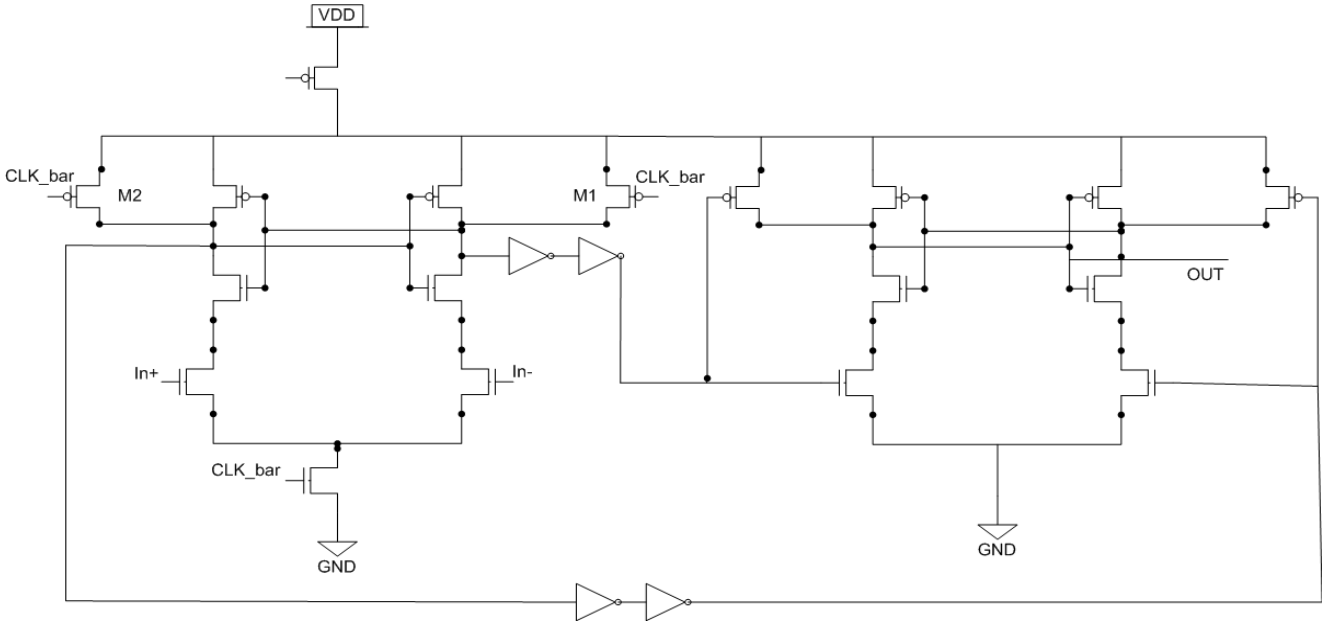
A 2.6mW 200MS/s 6b Flash ADC

- Low performance flash ADC is designed to meet the low power specs
- ROM and encoder designed by hand to reduce the power and area



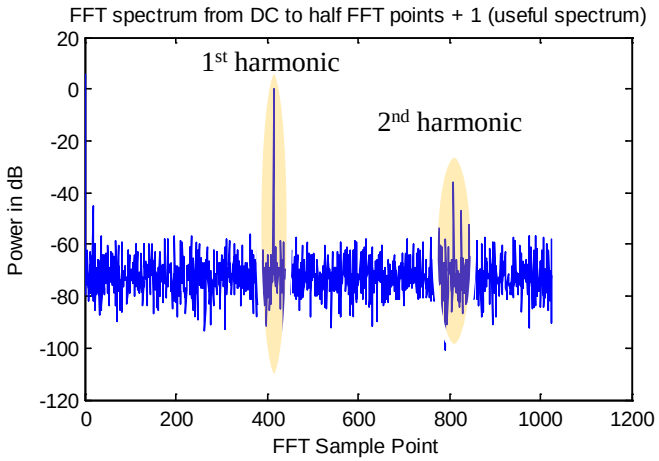
A 2.6mW 200MS/s 6b Flash ADC

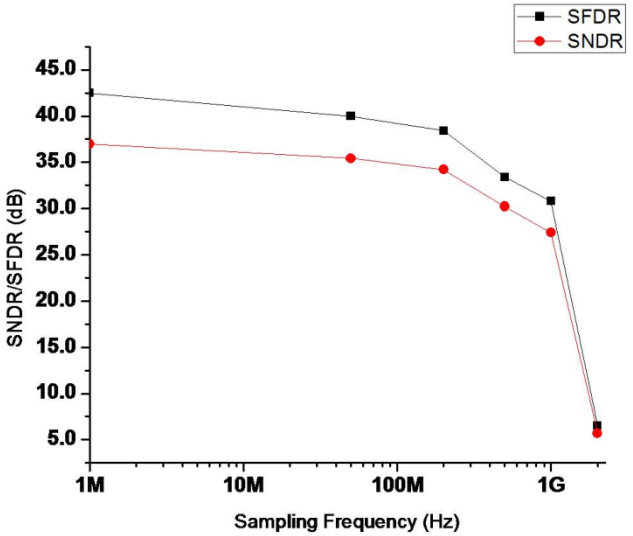
- Low power latched comparators are chosen to reduce the total static power consumption.
- FOM of 80fJ/conversion for each comparator.
- More than 98% success over Monte Carlo simulation

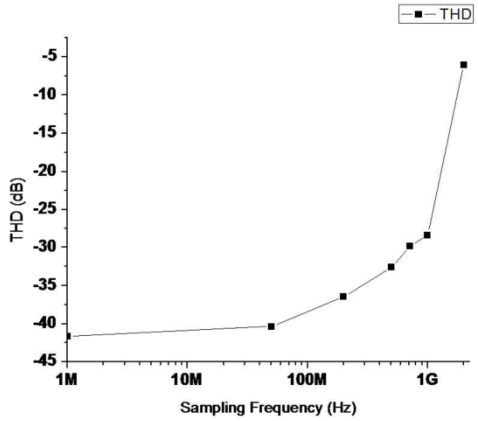


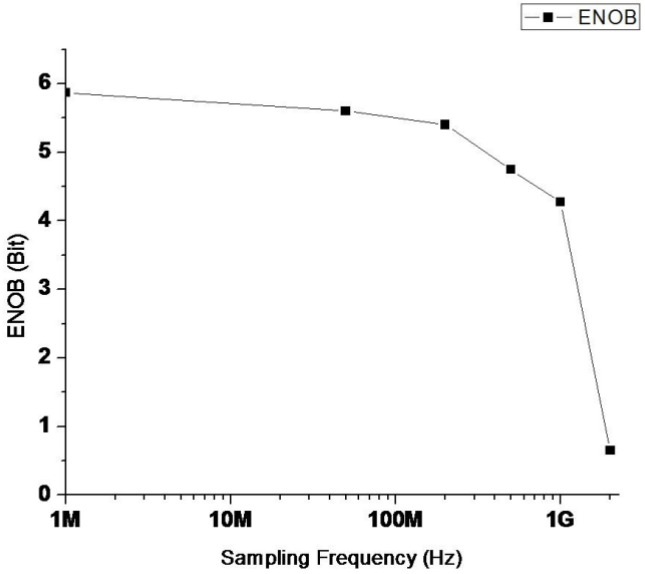
A 2.6mW 200MS/s 6b Flash ADC

- Simulation Results

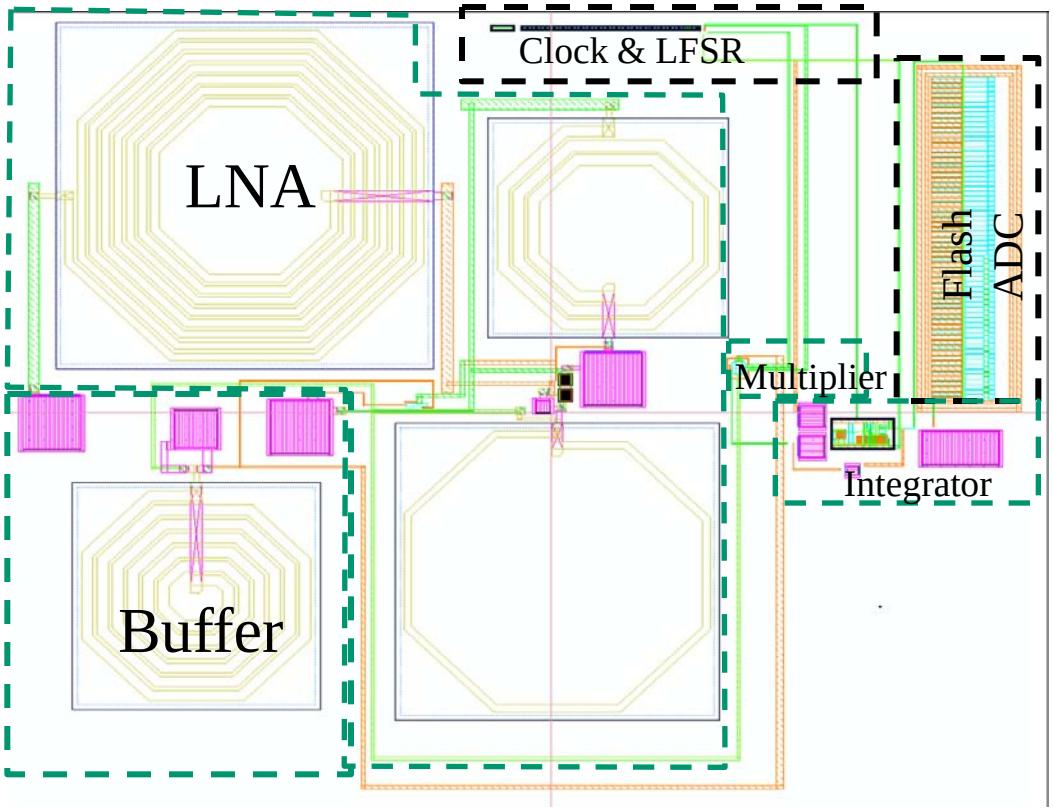






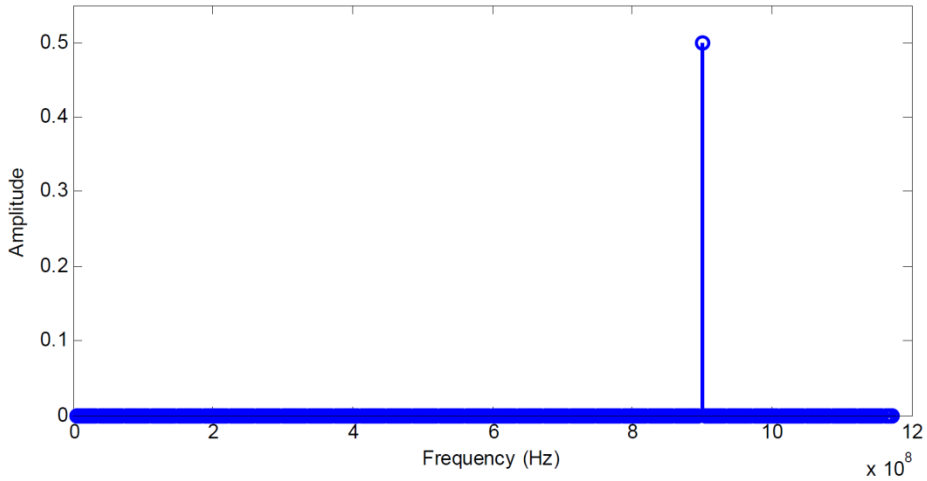


Layout

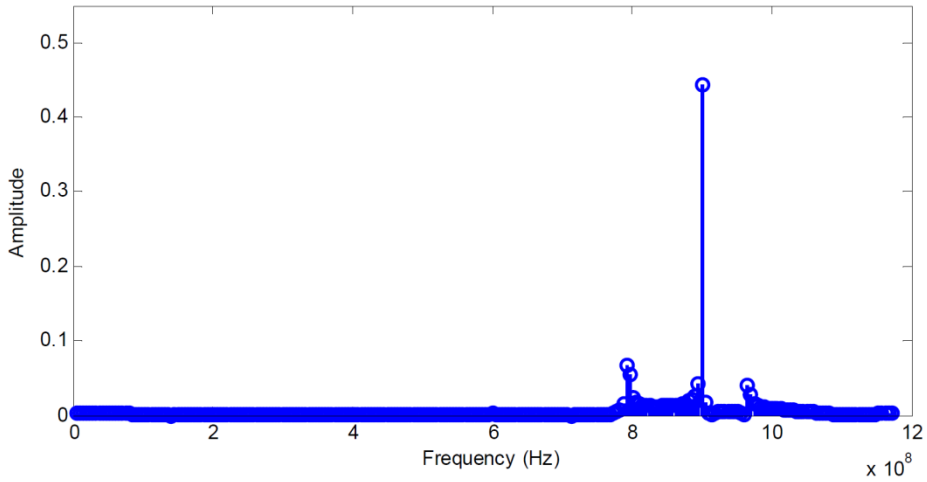


Recovery Algorithm

- Matlab based recovery algorithm



- Ocean-script based code to communicate with Matlab



Final Result

- Usual receiver front ends consume 20-40mW
- The proposed front-end topology consumes less than 10mW/5mW
- Oscillators in general consume more power

Overall system Specification @ 900MHz		
LNA + Buffer	S_{11}	-21dB
	S_{21}	23dB
	S_{12}	-58dB
	S_{22}	-14dB
	Power	4.95mW
	NF	1.2dB
	1dB compression	-12.2dBm
	IIP3	-3.9dBm
Mixer	NF	9.67dB
LFSR + clock	Power	$600\mu W$
	clock	2GHz
Integrator	Power	1.5mW
	3-dB cutoff	12MHz
Flash ADC	Power	2.6mW
	Sampling	200MSps
	SNDR	36.98dB
	ENOB	5.87
	FOM	308fJ/conversion

Acknowledgement

- Special thanks to
  - Professor Wentzloff
  - Kuo-Ken Huang
  - Mohammad Ghahremani

Conclusion

- A complete front end for compressive sensing based recovery has been designed
- Compressive sensing can be utilized in data analysis of the sparse signals
- Compressive sensing based receivers are more power efficient than other receivers
- In the applications that require power efficient topologies, they are a good candidate
- The Oscillator power consumption is much less than the other structures

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