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A MOSFET's Driver Applied to High-frequency Switching with Wide Range of Duty Cycles

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Abstract

A MOSFET's gate driver based on magnetic coupling is investigated. The gate driver can meet the demands in applications for wide range of duty cycles and high frequency. Fully galvanic isolation can be realized, and no auxiliary supply is needed. The driver is insensitive to the leakage inductor of the isolated transformer. No gate resistor is needed to damp the oscillation, and thus the peak output current of the gate driver can be improved. Design of the driving transformer can also be made more flexible, which helps to improve the isolation voltage between the power stage and the control electronics, and aids to enhance the electromagnetic compatibility. The driver's operation principle is analyzed, and the design method for its key parameters is presented. The performance analysis is validated via experiment. The disadvantages of the traditional magnetic coupling and optical coupling have been conquered through the investigated circuit.

Key words: High Frequency, Magnetic Couple, MOSFET's Driver, Wide Range of Duty Cycle

I. INTRODUCTION

MOSFET is the key component in high-frequency power converters, and a well-performing driver is the basic demand and guarantee for its proper and reliable operation [1]-[6]. MOSFETs operate at wide range of duty cycles in various applications, such as inverters and DC-DC converters with wide operating ranges and quick responding capabilities. Meanwhile, isolation between control signals and power circuit is a must in several applications.

MOSFETs' drivers can be classified as optical isolated, magnetic isolated, and special floating drive ICs according to the isolation methods. Level shift and bootstrap are mainly used in high-voltage floating drive ICs to power the drivers, and thus the circuits can be quite simple and reliable. However, these circuits can only be used in bridge series power converters and cannot realize fully galvanic isolation between the control and power circuits [7], [8]. The low-voltage driver ICs are mostly designed for special occasions, such as synchronous rectification circuits. This drawback limits their application. In addition, these circuits cannot guarantee galvanic isolation between the control and power circuits. Isolated driver with optoelectronic isolation can realize isolation for signals with wide range of duty cycles, but auxiliary isolated power supplies are needed. Unfortunately, optical isolation can hardly satisfy the demands for high-frequency power converters because of long transmit time of normal opto-couplers and weak anti-interference capabilities of high-speed opto-couplers [9], [10]. Generally, traditional magnetic isolated drivers can be used in high-frequency switching occasions. However, these drivers are typically limited by the magnetic reset time of coupling transformer [11], [12]; if the power converter operates in a wide range of duty cycles, such as in the case of SPWM inverters where duty cycles range in nearly 0%-100%, then designing proper components and parameters for traditional magnetic isolated drivers is difficult, which limits their utilization in various applications [13]-[15]. A circuit proposed in [16], [17] converts the pulse edges of the driving signal to narrow pulses, magnetically couples them to the secondary side, and the signal is then reconstructed and restored by the circuit on the secondary side. This circuit can sustain a wide range of duty cycles, but complicated circuits and large power loss remain to be solved.

To meet the requirements for the power MOSFETs' driver at high frequency (up to 1 MHz) and both high-voltage and

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low-voltage isolated circumstances, a driver is investigated. The driver's operation principle is analyzed and the key parameters are designed. Finally, the experimental waveforms are presented to verify the feasibility of the driver.

II. Operation Principle and Design Consideration

A. Operation Principle

The basic topology of the investigated driver is shown in Fig. 1. Compared with traditional circuits, the main improvement is that a restore capacitor on the secondary side and an independent floating capacitor are added. The output stage is realized by a totem configuration, which can achieve quick charging and discharging of the gate-source capacitor.

The capacitor C_1 sustains the DC component of the input PWM signal, while the AC component of the input is transmitted to the secondary side of the isolated transformer. The capacitor C_2 and diode D_2 restore the DC level at the secondary side. The capacitor C_3 operates as an independent floating capacitor and supplies current to the totem output. The main operating waveforms are shown in Fig. 2.

The capacitance C_3 is large enough to neglect the pulsation of the voltage across the capacitor C_3. The capacitances of C_1 and C_2 are designed properly to neglect the voltage fluctuation in every switching period. The operating modes below are analyzed based on the aforementioned assumed conditions.

At turn-on, u_p is positive which turns on Q_1, partially discharging C_3 upon C_{GS}, to turn on the MOSFET. The driving current in traditional magnetic isolated driver comes from the primary side of the transformer, and thus the rising rate is limited by the leakage inductor. On the contrary, driving energy comes from the capacitor C_3 in Fig. 1, which enables fast rising of the gate voltage. When the energy storage capacitor C_3 is discharged, this capacitor can be recharged through capacitor C_2 and diode D_1.

At turn-off, u_p is negative, and D_2 is forward biased. C_{GS} is discharged through Q_2, which is saturated, turning off the MOSFET.

The voltage across the blocking capacitor C_1 is the average of the input port voltage U_{in} is as follows:

$$u_{C1} = DU_{in}. \tag{1}$$

where D denotes the duty cycle.

In the analysis below, turns ratio of the transformer is denoted as 1:n, the forward voltage drop is denoted as U_D, the base-emitter voltage of the transistor is denoted as U_{BE}, and the collector-emitter saturation voltage drop is denoted as $U_{CE(sat)}$.

When a high level U_{in} is inputted, the voltage across the primary side of the transformer is as follows:

$$u_p = (1-D)U_{in}. \tag{2}$$

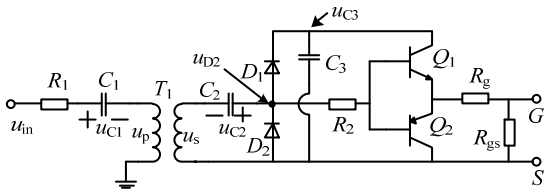


Fig. 1. Basic topology of the driver.

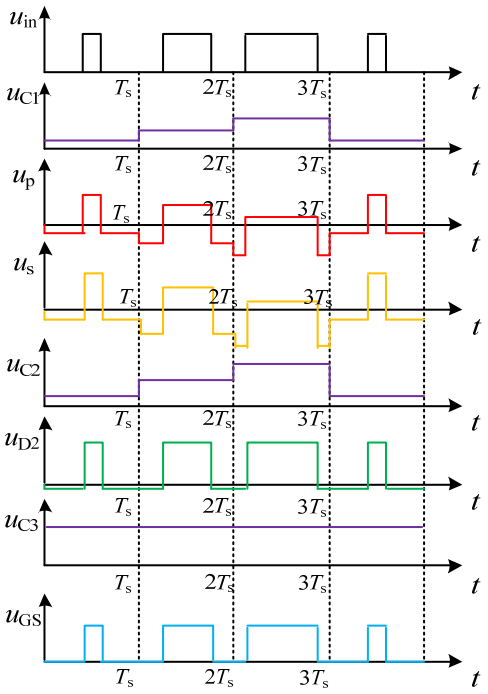


Fig. 2. Key operating waveforms of the driver

The voltage across the secondary side is as follows:

$$u_s = n(1-D)U_{in}. \tag{3}$$

The voltage across the capacitor C_2 is as follows:

$$u_{C2} = nDU_{in}. \tag{4}$$

Thus, the voltage restored by the capacitor C_2 is as follows:

$$u_{D2} = nU_{in}. \tag{5}$$

As a result, the voltage of the floating supply capacitor C_3 is as follows:

$$u_{C3} = nU_{in} - U_D, \tag{6}$$

and the output of the totem is as follows:

$$u_o = nU_{in} - U_D - U_{CE(sat)}. \tag{7}$$

Therefore, the output voltage across the gate-source is as follows:

$$u_{gs} = \frac{R_{gs}}{R_g + R_{gs}} u_o. \tag{8}$$

When a low level 0 V is inputted, the voltage across the primary side of the transformer is as follows:

$$u_p = -DU_{in}. \tag{9}$$

The voltage across the secondary side is as follows:

$$u_s = -nDU_{\text{in}} . \tag{10}$$

Thus, the voltage restored by the capacitor C_2 is as follows:

$$u_{\text{D2}} = -U_{\text{D}} , \tag{11}$$

and the output of the totem configuration is as follows:

$$u_o = U_{\text{CE(sat)}} \approx 0\text{V} . \tag{12}$$

The energy storage capacitor on the secondary side not only simplifies the circuit, but also avoids the resonance of coupling transformer leakage and gate capacitor. Therefore, smaller R_{g} can be used, and thus quick rising and falling edges can be obtained even at high-frequency switching. Meanwhile, the restore capacitor C_2 can stabilize the voltage of C_3 to avoid the influence of duty cycles. This statement can be verified via experiments.

Moreover, the galvanic isolation capability can be improved because of the decrease of the limitation of coupling transformer's leakage inductor. In traditional magnetic coupling drivers, the coiling method of the transformer in Fig. 3(b) is commonly used instead of that in Fig. 3(a) because of the large leakage inductance. However, this large leakage inductance is no longer an issue because of the driver's insensitivity to such leakage inductance. The galvanic isolation in Fig. 3(a) is better than that in Fig. 3(b) because no direct contact occurs between the primary and secondary windings. With this coiling method of the transformer and the insensitivity to the leakage inductance, the proposed scheme has advantages on galvanic isolation.

B. Design Consideration

1) Design for the Coupling Transformers: High permeability ferrite material with no air gap is selected considering high coupling coefficient and no energy storage needed in the transformer. Thus, the maximum magnetic flux density allowed, B_{max}, is determined. Accordingly, the upper limitation of magnetic flux variation ΔB is chosen to be about one-third of B_{max}.

According to Eq. (7), the turn ratio n is mainly decided by the amplitude of the PWM signal U_{in} and the driving voltage of MOSFET. The voltage drop caused by the semiconductor itself should be considered if necessary.

The magnetic core has to be kept unsaturated, and thus the turns should be designed to maintain limited magnetic flux variation ΔB. Then, the limitation can be derived as follows:

$$n_p \geq \frac{(U_{in} - u_{c1})t_{on}}{\Delta B A_e} = \frac{U_{in}(1-D)D}{\Delta B A_e f_s} . \tag{13}$$

This equation illustrates that the lower limit of primary turns n_p is determined by the parameters of input signal (input voltage amplitude U_{in}, frequency f_{s}, and duty cycle D), the magnetic core's effective magnetic flux area A_{e}, and the allowed maximum magnetic flux density B_{max}.

Meanwhile, to reduce the loss of magnetizing current of the transformer, the inductive coefficient A_L of the specific magnetic core can be found in its datasheets, and the loss can be estimated by the following equation:

$$i_m = \frac{U_{in} D(1-D)}{2N_p^2 A_L f_s} . \tag{14}$$

Therefore, the turns n_p and n_{s} can be approximately determined.

2) Design for Capacitors: In terms of designing the capacitor C_1 for blocking DC content of the input signal and capacitor C_2 for level restore, the voltage across the capacitors should be kept almost unchanged per period, while the average voltage should change quickly according to the duty cycle. Thus, the capacitances should be the minimum values that meet the demands. On the contrary, the voltage of floating supply capacitor C_3 should be kept during the whole operating life. Hence, an available maximum value should be better.

The equivalent circuit during turn-on is shown in Fig. 4 (the resistors R_{g} and R_{gs}, gate-source capacitor are neglected).

The parameters in Fig. 4 are all converted to the primary side. With the neglected parasitic resistance R, a simple L short for the leakage inductance of the transformer L_s, the equation can be derived as follows:

$$i(t) = u_i \sqrt{\frac{C}{L}} \sin\left(\frac{1}{\sqrt{LC}} t\right) . \tag{15}$$

Therefore, a new equation can be derived as follows:

$$u_{C1}(t) = \frac{1}{C_1}\int i(t)\,\mathrm{d}t = -\frac{u_i C}{C_1}\cos\left(\frac{1}{\sqrt{LC}} t\right) , \tag{16}$$

where

$$u_i = u_{in} - u_{C1}(0) + u_{C2}'(0) - U_D' - u_{C3}'(0) ,$$

$$C = \frac{C_1 C_2' C_3'}{C_1 C_2' + C_1 C_3' + C_2' C_3'} .$$

Eqs. (17)-(19) calculate the voltage ripples of capacitor C_1, C_2', and C_3'.

$$\left[u_{C1}(t)\right]_{pk} = \frac{2u_i C}{C_1} , \tag{17}$$

(a) Windings on both sides. (b) Windings on one side.

Fig. 3. Two different coiling methods of the transformer.

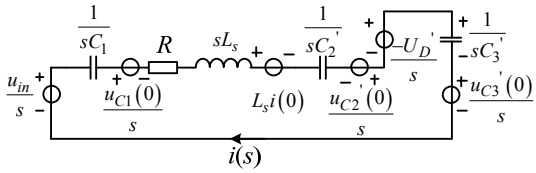


Fig. 4. Equivalent circuit during turn-on.

$$\left[u_{C2}{}'(t)\right]_{pk} = \frac{2u_i C}{C_2}, \tag{18}$$

$$\left[u_{C3}{}'(t)\right]_{pk} = \frac{2u_i C}{C_3}. \tag{19}$$

Oversized voltage ripples of capacitor C_1 and C_2 will unintentionally turn-on and turn-off the MOSFET, and thus the normal operation of totem configuration should be unaffected by the voltage ripples converted to the secondary side.

Notably, the analysis above neglects the effect caused by the magnetizing current. However, when the capacitance is small, the magnetizing current cannot be neglected and becomes the main factor. The voltage changes of capacitor C_1 caused by the magnetizing current can be estimated as follows:

$$\Delta u_{c1\_m} = \frac{i_{m\_ave} D}{C_1 f_s} = \frac{u_{in} D^2 (1-D)}{2 L_m C_1 f_s{}^2}. \tag{20}$$

The selection of capacitor C_1 should consider the two factors mentioned earlier.

To maintain the stable conductive characters of the power switch, the output voltage of the driver should be kept unchanged. In other words, the voltage ripple of the capacitor C_3 should be limited to a certain range.

The voltage drop of capacitor C_3 is determined by the power needed to drive the gate, and can be estimated as follows:

$$\frac{1}{2}C_3 u_{C3}^2 - \frac{1}{2}C_3 (u_{C3} - \Delta u_{C3})^2 = \frac{1}{2}Q_G u_o + \frac{u_o{}^2 D}{(R_g + R_{gs}) f_s}. \tag{21}$$

By solving the equation above, an approximate equation can be derived as follows:

$$\Delta U_{C3} = \frac{Q_g}{2C_3} + \frac{u_{C3} D}{(R_g + R_{gs}) C_3 f_s}, \tag{22}$$

where Q_g denotes the gate charge of the driven power switch.

3) Design for Transistors: If the power supply capacitor C_3 is large enough, then this capacitor can be regarded as an ideal voltage source. At this point, the maximum current at the switch's turn-on and turn-off moment is as follows:

$$i_{g\max} = \frac{u_o}{R_g}. \tag{23}$$

The turn-on and turn-off current of the totem configuration is the same as that of the switch. Thus, the peak current of the transistors should meet or exceed the driver's peak current.

4) Design for Resistors: The resistors R_1 and R_2 (optional) are used to damp the oscillation caused by strap inductance and the gate capacitor. R_1 can be selected according to the energy needed by the driver, and R_g can be chosen according to the required peak current and driving speed.

III. Practical Design

To verify the accurateness of the analysis for the operation principle and design methods mentioned earlier, a practical example is designed based on driving the SiA920DJ type MOSFET by Vishay Corporation. This type contains two N-type MOSFETs, whose key parameters are as follows: $V_{DS(max)}$ = 8V, $V_{GS(max)}$ = 5V, and $V_{GS(th)\_min}$ = 0.35V. This driver can drive both low-voltage and high-voltage MOSFETs where the control and power circuits should be isolated.

In this example, the PWM signal is generated by the digital signal processor. After going through an amplifier, the signal's voltage difference between the high level and the low level is 1.9 V. The frequency ranges from 10 kHz to 1 MHz, and the designed output voltage is 4 V. When designing the parameters, the voltage fluctuation of capacitor C_3 is limited to below 0.5 V, and the voltage fluctuation of capacitor C_1 is limited to below 0.5 V after being converted to the secondary side.

The parameters of the circuit's components are chosen as follows: R_{gs} = 10 kΩ, R_2 = 200 Ω, R_g = 20 Ω, C_1 = 1 μF, C_2 = 0.33 μF, and C_3 = 10 μF. In addition, the transistors use 2SC9013 and 2SC9015 for NPN-type and PNP-type, respectively. The magnetic core used is the type H10/6/5 by Nanjing New Conda Magnetic Industrial Co., Ltd. This core is made up of high permeability ferrite material called HP3. According to its datasheet[18], its inductance coefficient AL equals 5100 nH/N^2 (tolerance ± 30%) under the measuring conditions of 10 kHz, 0.1 V, and 25 °C, and this type is a ring core with no gap. The primary and secondary winding numbers are 20 and 54, respectively. The turn ratio is 1:2.7, and coupling coefficient is about 0.999 that is calculated from the measuring results.

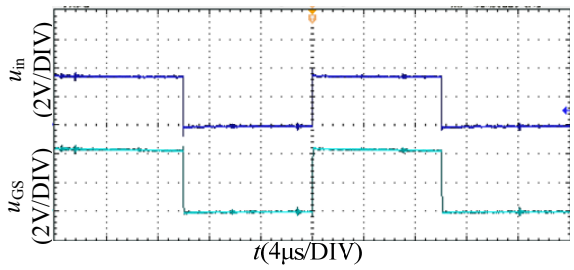
The input and output PWM waveforms at the switching frequencies of 50 kHz, 100 kHz, and 1 MHz are shown in Fig. 5. The rising and falling edges of the output voltage are sharp enough to turn-on and turn-off the MOSFET quickly.

The expanded waveforms embedded in Fig. 5(c) show that even at the frequency of 1 MHz, the turn-on and turn-off propagation delay is about 20 ns, and the rise and fall time is about 30 ns. Therefore, the signal can be transmitted by the circuit with low distortion and accurate duty cycle.

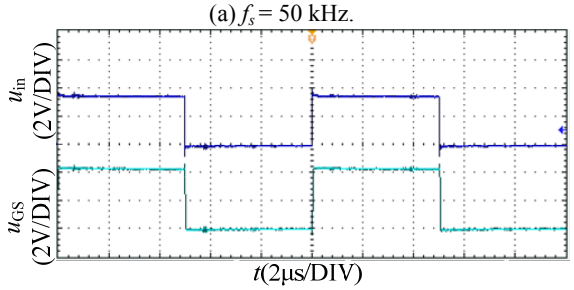
The driving waveforms when the switching frequency reaches 1 MHz and the duty cycles are 0.067 and 0.933 are shown in Fig. 6. This figure illustrates that the driver can truly suit the demands for high frequency and wide range of duty cycles.

The resistor R_g is now replaced with a short wire to ensure the condition R_g = 0. The experimental waveforms are shown in Fig. 7. Zero R_g operation can be achieved, and the driver now performs better than the original driver. The result strongly proves the previous statement.

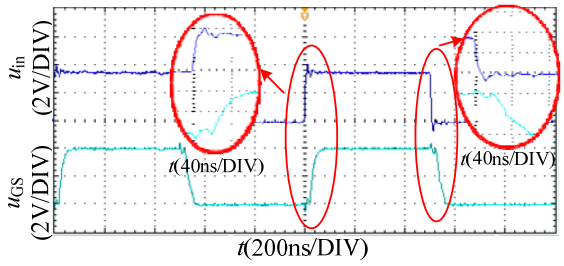
An extra inductor is now added in series with the transformer to simulate a larger leakage inductance. The



(a) f_s = 50 kHz.

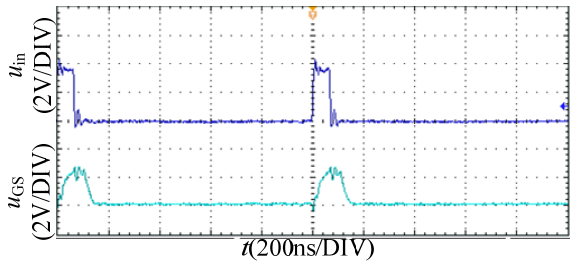


(b) f_s = 100 kHz.

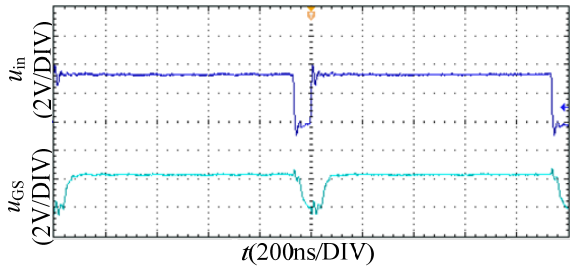


(c) f_s = 1 MHz.

Fig. 5. Waveforms at different frequencies.



(a) D = 0.067.



(b) D = 0.933.

Fig. 6. Waveforms at different duty ratios.

transformer is still the original transformer. The extra inductor is made by two turns of coils with the magnetic core the same as that of the transformer. The inductance is tested to be about 25 μH. The experimental waveforms are shown in Fig. 8. By comparing these waveforms, larger leakage

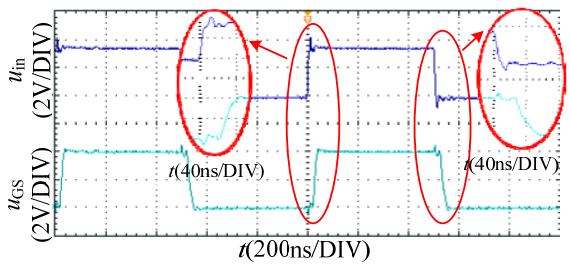
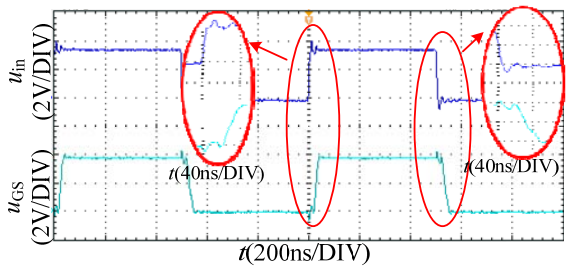
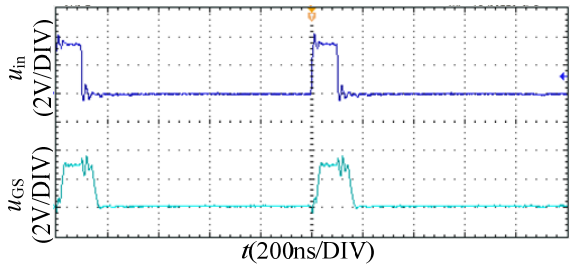


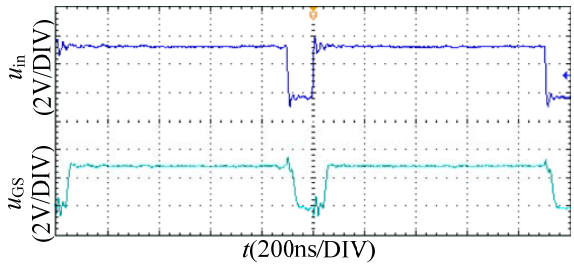
Fig. 7. Waveforms when R_g = 0.



(a) D = 0.5.



(b) D = 0.1.



(c) D = 0.9.

Fig. 8. Waveforms with extra inductance of 25 μH and R_g = 0.

TABLE I
TYPICAL DATA OF THE THREE APPROACHES

Parameters	PX3517 Upper Gate	PX3517 Lower Gate	UCC27 511A -Q1	This driver
Rise time(ns)	10	10	16	20
Fall time(ns)	10	5	7	30
Turn-on propagation(ns)	15	15	15	20
Turn-off propagation(ns)	20	7	19	20

inductance hardly affects the characteristics of the output. This comparison will verify the statement regarding the driver's insensitivity to the leakage inductance.

To realize the comparison with other approaches, two

driver ICs for low-voltage applications are considered. One is the new driver IC PX3517 designed for synchronous rectified buck circuits. According to its datasheet[19], this driver can operate at the maximum switching frequency of 1.2 MHz. Other detailed data regarding this driver are listed in Table I. The other one is UCC27511A-Q1, a single channel, high-speed, low side gate driver IC. The corresponding data regarding this driver according to its datasheet[20] when VDD = 4.5 V are also listed in Table I. Notably, the test conditions vary for different driver ICs and different parameters.

From the comparison results, the preliminary prototype of the driver in the manuscript can perform similar propagation delay and rise and fall time in low-voltage applications. Although the speed-related data of this driver are a little larger than those of commercial ICs, the driver is realized by a printed circuit board with general commercial components.

IV. Conclusion

A MOSFET driver is investigated. The driver's operation principle is analyzed and the design method for its key parameters is presented. The driver can operate at high frequency (up to 1 MHz). Almost full range of duty cycles can be transmitted without distortion.

This driver has several other important advantages. Firstly, fully galvanic isolation can be achieved with no extra floating supplies needed owing to the transformer. Secondly, by avoiding the oscillation in principle, no driving resistor is needed to damp the oscillation. As a result, the change rate of driving current caused by the driving resistor is not limited. Hence, sharp rising and falling edges of the output voltage can be realized. Finally, the design for the transformer can be made more flexible because the driver is insensitive to the leakage inductor of the transformer. Thus, the isolation voltage can be extended and the galvanic isolation performance is better.

Good performance and low power loss are verified via experiments. The isolated circuit is suitable for applications requiring high frequency and wide range of duty cycles.

Acknowledgment

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