# A Novel and High Performance Implementation of 8x8 Multiplier based on Vedic Mathematics using 90nm Hybrid PTL /CMOS Logic

Navya Rajput
Department of Electronics and Communication
Maharaja Surajmal Institute of Technology
New Delhi, India

Ankit Jindal
Department of Electronics and Communication
Maharaja Surajmal Institute of Technology
New Delhi, India

Sahil Saroha
Department of Electronics and Communication
Maharaja Surajmal Institute of Technology
New Delhi, India

Ritesh Kumar
Department of Electronics and Communication
Maharaja Surajmal Institute of Technology
New Delhi, India

Geetanjali Sharma
Department of Electronics and Communication
Maharaja Surajmal Institute of Technology
New Delhi, Ind

## ABSTRACT
Power consumption plays an imperative role specifically in the field of VLSI today, every designer be it an analog circuit or a digital circuit designer is concerned about the amount of power his or her circuit is going to consume in the end. The core of this paper consist of the introduction of a novel and high performance design of an 8x8 multiplier using ancient Indian mathematics called Vedas. This paper presents four different designs which includes 8x8 Vedic multiplier and 8x8 array multiplier implementation using CMOS and Hybrid PTL/ CMOS logic style and finally proved that Hybrid PTL(Pass Transistor Logic)/CMOS design of Vedic Multiplier is the best among all these implementations .The multiplier and the adder-subtractor units used for the implementation of Vedic multiplier are adopted from ancient methodology of India mathematics called as Vedas. The use of Vedas not only abates the carry propagation taking place from LSB to MSB but also produces the partial product and there sums in the same step. Vedic mathematics based multipliers thus causes least delay and consume least power among these four multipliers. The functionality of all the four designs and there PDP and power calculations at three different frequencies and four different voltages were calculated on 90 nm CMOS technology using tanner EDA 13.0v.The proposed Hybrid PTL/CMOS implementation of Vedic multiplier is up to 34.29% power efficient and about 49.82% speedy as compared to the conventional CMOS implementation of array multiplier.

## Keywords
Vedic Mathematics, Multiplier, PDP.

## 1. INTRODUCTION
The use of multipliers is inevitable in almost every field of technology especially in the field of electronics and

communication. Multipliers are widely used for the calculation of Discrete Sine Transform, Discrete Cosine Transform and Discrete Fourier Transform in the field of digital signal processing and image processing, their use is almost unquestionable in the field of communication which involves multiplication of two signals for modulation and demodulation processes. Oodles of transistors are used for the implementation of conventional multipliers in use today [1-10].

As the communication and signal processing industries are proliferating the demand for the multipliers is continuously increasing at a rapid rate. For past quite a lot of time, the invention of high speed and power efficient multipliers has been a grave matter of concern .Most prevalent form of multipliers in use today are array multiplier, booth's multiplier, bit serial implementation of multiplier and algebraic transformational based multipliers but in all of these multipliers there is a common drawback of latency and power consumption. Implementation of all these multipliers involves carry propagation taking place from Least Significant Bit (LSB) to Most Significant Bit (MSB) which is the cause of latency in these circuits and high power consumption results from their inability to produce partial products and sums in the same step [11].Vedic mathematics is a part of four Vedas (books of wisdom) [1], [2]. It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.The word „Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one [5], [10] and [12]. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

This paper deals with various multipliers implemented using CMOS logic style and Hybrid PTL/CMOS logic and their comparative analysis on the basis of power dissipation and PDP (Power delay product). A variety of multipliers have been reported in the literature [6]-[8] but power dissipation and area used by these multiplier circuits are relatively large. This paper propose a high performance and power efficient 8x8 multiplier design based on Vedic mathematics using

Hybrid PTL/CMOS logic style which is proved to be the best among all implemented designs.

This paper is structured as follows. Section II surveys the basic fundamentals of Vedic multiplication techniques. Section III describes array multiplier that is conventional multiplier. Section IV includes the proposed multiplier design. Section V explains the Hybrid PTL/CMOS logic and there importance in the VLSI designs .Finally Section VI contains simulation and results that is the comparison of power consumption and PDP for the four designs. Section VII states the conclusion. References are given at the end of paper in section VIII.

## 2. VEDIC MATHEMATICS AND URDHAV TRIYAGBYAHM RULE

Entire concept of Vedic mathematics was exhumed by Shri Bharati Krishna TirhajiMaharaj. Vedic mathematics involves 16 sutras (formulas)each one of these having their own individual significance. The Ekadhikina Purvena means next is one more than previous, Urdhva-Tiryagbyham means vertically and crosswise, Nikhilam Navatashcaramam Dashatah means all are subtracted from 9 and the last is subtracted from 10, Paraavartya Yojayet means transpose and then adjust, Shunyam Saamyasamuccaye means when the sum is same then that sum is zero,(anurupye) Shunyamanyat means if one is in ratio then other is zero,Puranapuranabyham means completion and non-completion, Chalana-Kalanabyham means differences and similarities,Yaavadunam means whatever the amount of its deficiency,Vyashtisamanstih means part and whole,Shesanyankena Charamena means last digit's remainder, Sopaantyadvayamantyam means the ultimate and twice of the penultimate, Ekanyunena Purvena means by one less than previous one, Gunitasamuchyah means the sum's product is equal to the product's sum, Gunakasamuchyah means the sum's factor is equal to the factor's sum.These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. From the above defined sixteen sutras this paper presents one sutra that is **Urdhva-Tiryagbyham** to implement the Vedic multiplier [10]. **Urdhva-Tiryagbyham** sutra means vertically and crosswise as shown in the Figure 1.It is a rule applicable to all the cases of multiplication.

This rule is based on the concept that produces the sum of the partial products generated during the multiplication of two numbers concurrently that is the concept of producing the partial products and their sumin the same step is provided by Urdhav rule.The algorithm can be generalized for n x n bit number.

**Fig. 1: Urdhav-Triyakbhyamrule**

Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor.

To illustrate the multiplication algorithm, let us consider the multiplication of two numbers N1=41 and N2=32. The process is followed according to the steps shown in Fig. (b).In the first step, multiplication of the unit digit of the two numbers is carried out vertically that is multiplication of 1 and 2 and then place it as the unit digits on the final product. In the second step cross multiply the unit digit of second number to tense digit of first number and unit digit of first to tens digit of second number and then add the results of two cross multiplications, that is addition of 8(product of 4 and 2) and 3(product of 1 and 3) giving 11, place the units digit of this answer (11) as the tense digit of the final answer and the tense digit of the of the answer (11) as carry. In the third step perform vertical multiplication of the tens digits of the two numbers and add the carry produced in the second step to this multiplication giving (12+1=13) thirteen, and place the result as shown in the Figure 2 giving 1312 as the final answer.

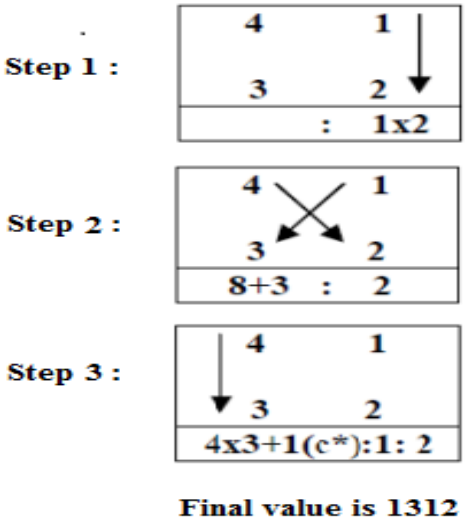


**Fig. 2:Concept of Urdhav rule**

## 3. CONVENTIONAL MULTIPLIER

Array Multiplier is the simplest multiplier. It is a combinational circuit that is used for the multiplication of two number using series connected half and full adders .To understand the functionality of array multiplier Let us consider the multiplication of two numbers A and B, where number A is represented as $a_1a_0$and number B is represented as $b_1$ $b_0$.The number C $_{(0-3)}$ is the product of two numbers A and B given as: - $c_0 = a_0b_0$, c1= $a_1b_0 + a_0b_1$, c2 = $a_1b_1 + co_1$ ($co_1$ is the carry generated during the generation of $c_1$ terms). $c_3 = co_2$ ($co_2$ is the carry generated during the generation of the $c_2$). In the array multiplier the elementary product terms of each partial product term is produced using AND gates and then added using series connected HALF and FULL ADDERS (FA). Figure 3 shows the circuit diagram for implementation of two bit array multiplier where $a_0b_0$, $a_0b_1$, $a_1b_0$ and $a_1b_1$ are the elementary product terms of partial products which are then added using half adders to get the result, So a 2x2 bit array multiplier requires 4 AND gates and 2 HALF ADDERS(HA). Similarly a 4x4 bit array multiplier will require 16 AND gates, 4 HA and 8 FA (total of 12 adders) as shown in Figure 4 and a 8x8 bit array multiplier will require 64 AND gates , 8 HA and 48 FA.

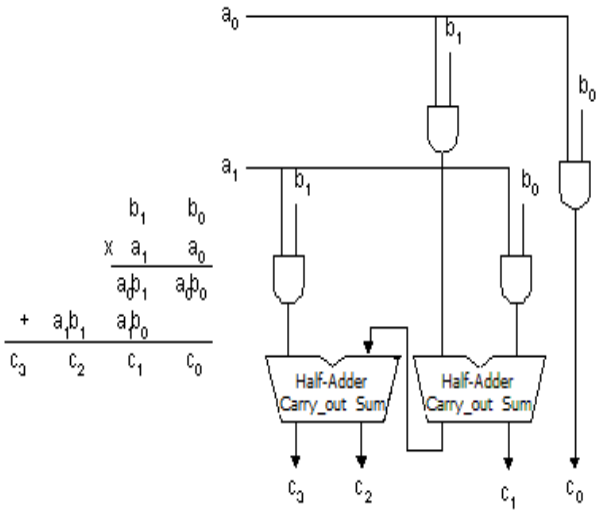


**Fig. 3:2x2 Array multiplier**

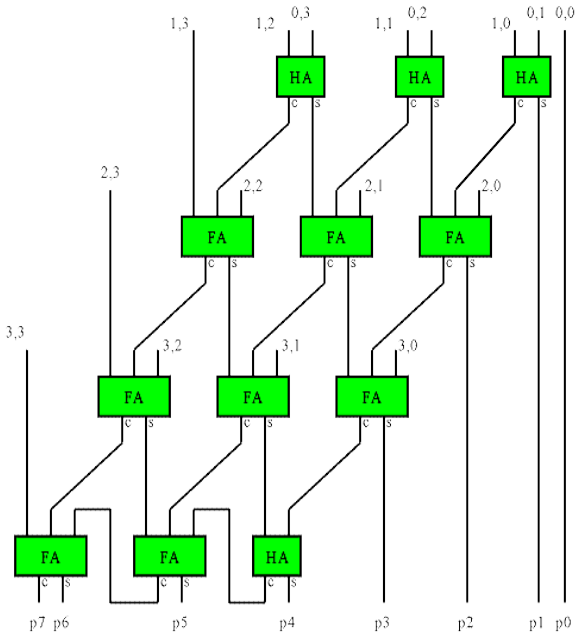


**Fig. 4:4x4 Array multiplier**

## 4. PROPOSED DESIGN USING VEDIC MATHEMATICS

The multiplier using Vedic mathematics is adaptive to parallel processing. The hardware implementations of 2x2, 4x4 and 8x8 Vedic Multiplier are carried out using "Urdhav-Triyakbhyam"(Vertically and Crosswise) sutra for multiplying two binary numbers where both the partial products and their sum are produced concurrently.

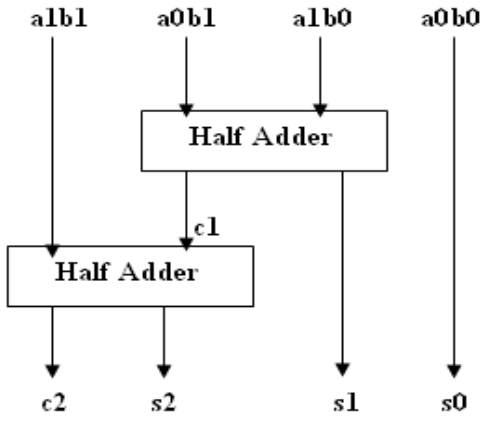


**Fig. 5: 2x2 Vedic multiplier**

The implementation of 2x2-bit Vedic multiplier is structured by using four AND gates and two HA as shown in Figure 5.The 1st HA is used to add outputs of AND gates having input a1b0 & a0b1 and 2nd HA are used to add carry generated from 1st HA and output of AND gate having input a1b1.

Similarly, Consider an example of a 4x4-bit Vedic multiplier unit as shown in Figure 6 which multiplies two 4-bit numbers (A and B), each number can be expressed as ($A_0$–$A_3$, $B_0$–$B_3$); $A_3$ and $B_3$being the most significant inputs.

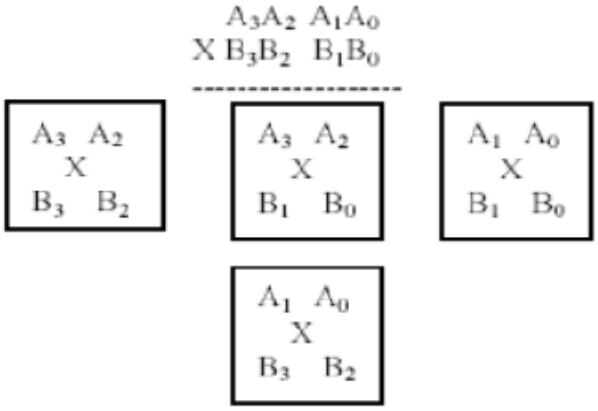


**Fig. 6: 4x4 Vedic multiplier**

Each square shape block in the above figure shows a 2x2 bit Vedic multiplier unit. First 2x2 bit Vedic multiplier has inputs as A1A0 and B1B0. The last block is also 2x2 bit Vedic multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So the final result of multiplication will be of 8 bit as S7S6S5S4S3S2S1S0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Figure 7. To get final product (s7 s6 s5 s4 s3 s2 s1 s0), four 2x2 bit Vedic multipliers and three 4-bit Ripple-Carry (RC) Adders are required.

Analyzing 4X4 multiplications, inputs are a3-a0 and b3-b0 and the output is given by s7 s6 s5 s4 s3 s2 s1 s0.The inputs of 1st 2X2 multiplier are a1a0 and b1b0, 2nd 2X2 multiplier are a1a0 and b3b2, 3rd 2X2 multiplier are a3a2 and b1b0 and that of 4th 2X2 multiplier are a3a2 and b3b2.

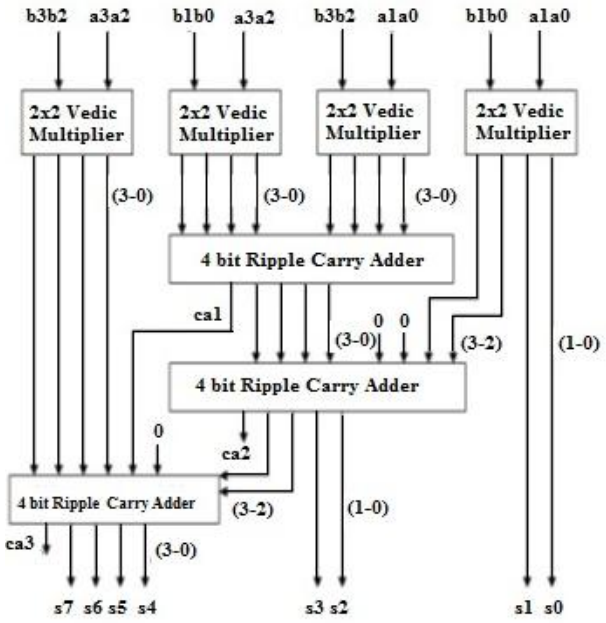


**Fig. 7: Block diagram of 4x4 Vedic Multiplier**

As compared to Array Multiplier, Proposed Vedic Multiplier is efficient in terms of delay and speed. The Proposed Vedic Multiplier can be used to reduce Delay. This 4X4 Multiplier Module is the Basic Building Block of 8X8 Vedic Multiplier.

The module of 8X8 Vedic multiplier shown in Figure 8 can be implemented by using four 4X4 bit Vedic multiplier modules [12]. Analyzing 8X8 multiplications, inputs are a7-a0 and b7-b0 and the multiplication's 16 bits output will be s15-s0.In this , four 4X4 bit Vedic multipliers and three 8 bit RC Adders(having 2 input of 8 bits) are required. Inputs are given to the 4x4 bit Vedic multipliers and the output of multiplier is of 8 bits. Now, the input of the 1st RC Adder is the output of the 2nd and 3rd 4x4 bit multipliers which gives output of 8 bits (7-0) + one carry. The 2nd RC Adder will add the output of 1st RC Adder (7-0) and 4 bits (7-4) output of 1st 4x4 bit Vedic multiplier, other 4bit of are considered as 0.So output is of 8-bits(7-0) and one carry(carry is discarded).The 3rd RC Adder will add the output of 4th 4x4 bit multiplier(7-0) and 4 bits of output of 2nd RC Adder (7-4), other 4 bits are carry of 1st RC Adder and 0.Now ,the output of 8x8 multiplier is s(3-0) output of 1st 4x4 bit multiplier(3-0), s(7-4) is output of 2nd RC Adder (3-0) and s(15-8)=8 is output of 3rd RC Adder(7-0).Thus, implementation of NxN bit Vedic multiplier for N bits. Hence, efficiency and performance can be improved.

## 5. Hybrid PTL/CMOS LOGIC

Pass transistor is the logic design in which the primary inputs drive the gate terminals and source-drain terminals in contrast to static CMOS where primary inputs drive gate terminals. Source side of logic transistor networks is connected to some input signals instead of the power lines. One of the main advantages of this logic style is that only one pass transistor network (either NMOS or PMOS) is sufficient to perform the logic function thereby using PTL one can save on the hardware requirements for the implementation of any circuit. Inverters are usually attached to the gate output to provide acceptable output driving capabilities. To understand the functioning of PTL design consider the implementation of a two input XNOR gate shown in Figure 9,

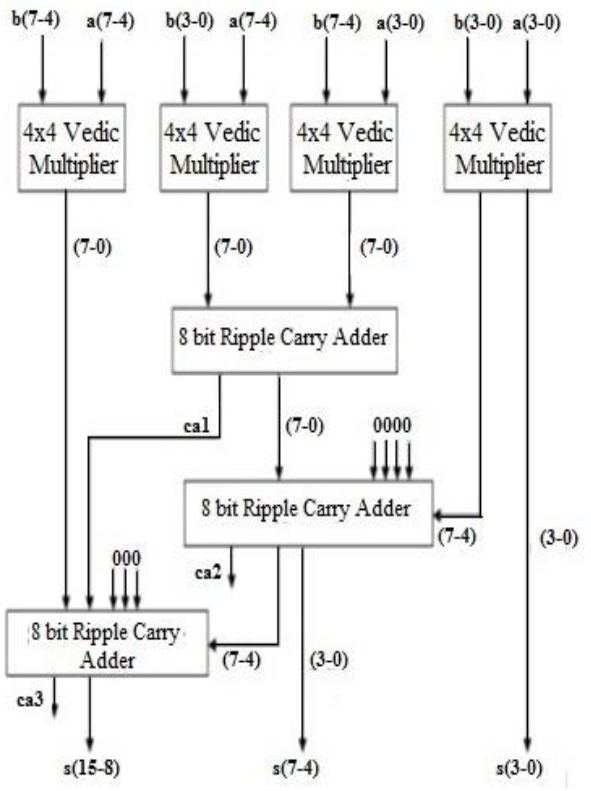


**Fig. 8:Block diagram of 8x8 Vedic Multiplier**

which uses only two NMOS transistors .XNOR gate outputs logic high (1) when the two inputs are same that is logic-1 for inputs 00 and 11 and logic low (0) otherwise. Now when A = 1 then the lower NMOS will function and the upper NMOS will be in off mode and so the input connected to lower NMOS that is B will transfer to the output out. When A= 0 then the upper NMOS is in function and lower NMOS will be in off mode and so the input connected to the upper NMOS will transfer to the output.

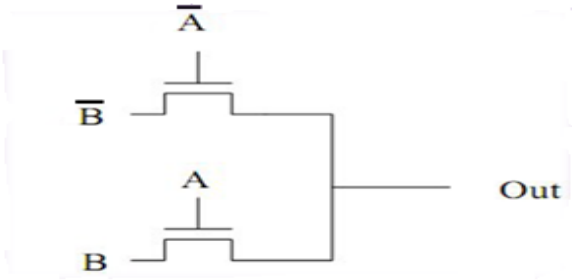


**Fig. 9: XNOR using PTL**

To give an explicit picture of how PTL reduces the number of transistors used in any circuit follow the above stated comparison for PTL implementation of XNOR with CMOS implementation of XNOR which makes use of 3 not gates (boxes) ,4 PMOS and 4 NMOS transistor.

CMOS implementation of XNOR uses 14 transistors adding to the power consumer of the circuit considerably whereas the same function can be implemented using only 2 not and 2 NMOS transistors that is total of 6 transistors by PTL logic Figure 10. Hence PTL logic can not only reduce the hardware requirements for the circuit by reducing the number of

transistors required which intern helps in reducing the power consumption of the circuit.

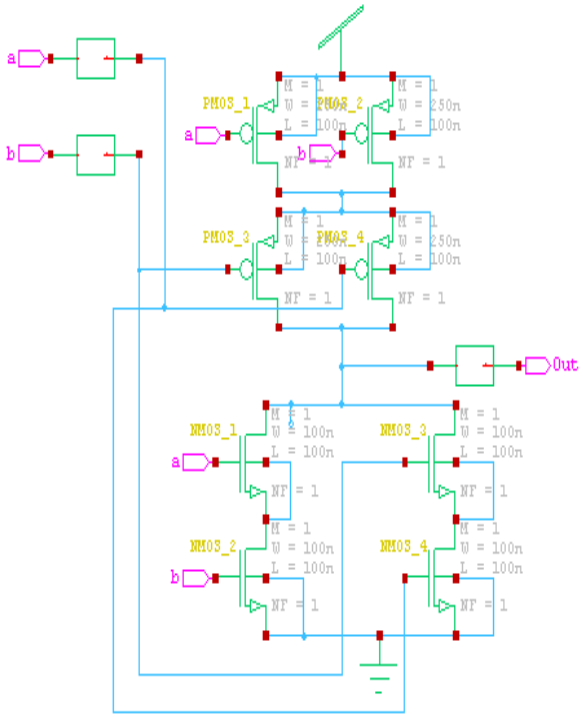


**Fig. 10:XNOR using CMOS**

Though PTL logic style reduces the number of transistors used for the implementation of any logic function it does not give full swing as in the case of CMOS , every PTL logic design must realize a multiplexer structure in addition to these two drawbacks layout designing of PTL logic style is not straight forward and efficient. To overcome these pitfalls in the PTL logic style instead of using purely PTL logic style Hybrid PTL/CMOS logic style is used which incorporates the advantages of both PTL and MOS logic design.

## 6. SIMULATION AND RESULTS

The results simulated for various multipliers which includes Hybrid PTL/CMOS and CMOS design of conventional multiplier and proposed Vedic multiplier were obtained on Tanner EDA Tool 13.0v for various supply voltages and frequencies .Table 1 shows power consumption values for Array multiplier using CMOS logic and Hybrid PTL/CMOS logic, and our proposed design that is Vedic multiplier using Hybrid PTL/CMOS logic for different set of voltages at 100MHZ and 50MHz.

The power consumed by Hybrid PTL/CMOS design of array multiplier at for 2v, 100MHz is 13.29% less as compared to CMOS design of array multiplier and the power consumed by CMOS implementation of Vedic multiplier at 1.5v, 100 MHz is 18.35% less as compared to Hybrid PTL/CMOS design of array multiplier, finally the Hybrid PTL/CMOS design of Vedic multiplier outperforms the CMOS design of Vedic multiplier by showing a power efficiency of 22.22% at 2v and 50 MHz, On comparing the conventional multiplier's CMOS implementation with the Hybrid PTL/CMOS implementation of Vedic multiplier which is proved to be the best multiplier it was noticed that proposed design is 34.29% more power efficient at 2v, 100MHz than the conventional multipliers in use today. Table 2 states the PDP (power delay product) calculations for the four multiplier designs.

The Hybrid PTL/CMOS implementation of array multiplier shows 12.24 % efficiency in terms of PDP over CMOS design of array multiplier at 2v, 50 MHz, CMOS implementation of Vedic multiplier shows 15.5% efficiency over Hybrid PTL/CMOS implementation of array multiplier at 1v, 100 MHz and CMOS implementation of Vedic multiplier is surpassed by Hybrid PTL/CMOS implementation of Vedic multiplier by showing a 11.34% efficiency in terms of PDP at 2v, 100 MHz.

Comparing CMOS implementation of array multiplier and proposed Hybrid PTL/CMOS implementation of Vedic multiplier it was found that proposed design is 49.89% more efficient at 2v100MHz in terms of PDP. The Graphs for the power consumption for four multiplier designs at four different voltages and at 100 MHz and 50 MHz are shown in Figure11 and Figure 12respectively. Similarly the graphs for the PDP (Power Delay Product) calculations for four designs at four voltages and at 100 MHz and 50 MHz are shown in Figure 13 and Figure 14 respectively. These graphs categorically present the Hybrid PTL/CMOS design of Vedic multiplier as the best among all four multipliers.

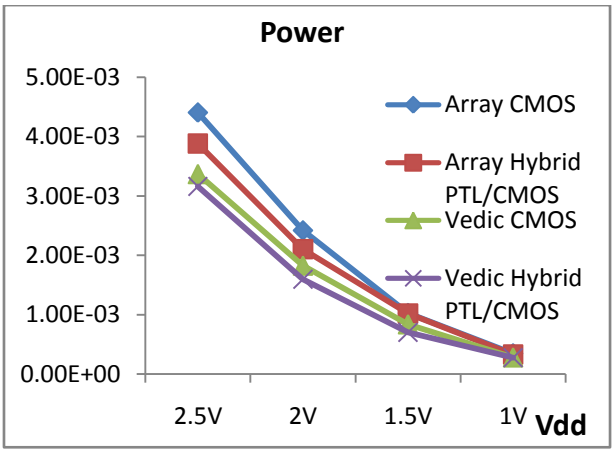


**Fig. 11: Power Consumption vs. Vdd (100MHz)**

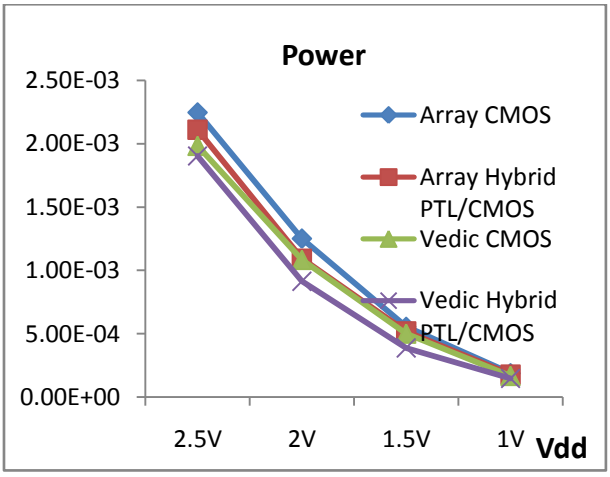


**Fig. 12: Power Consumption vs. Vdd (50 MHz)**

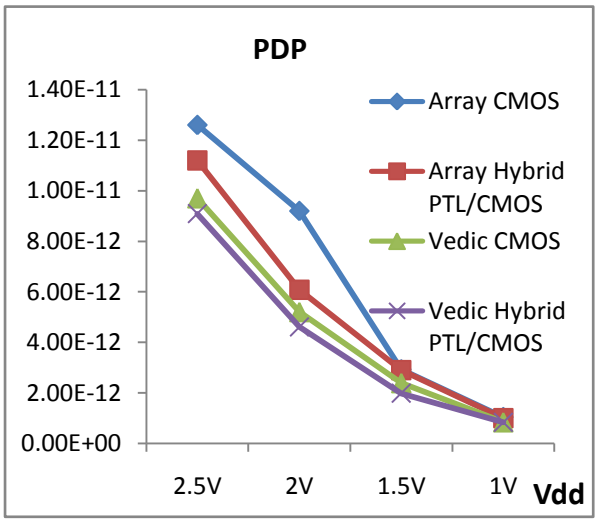


**Fig. 13: Power Delay Product vs. Vdd (100MHz)**

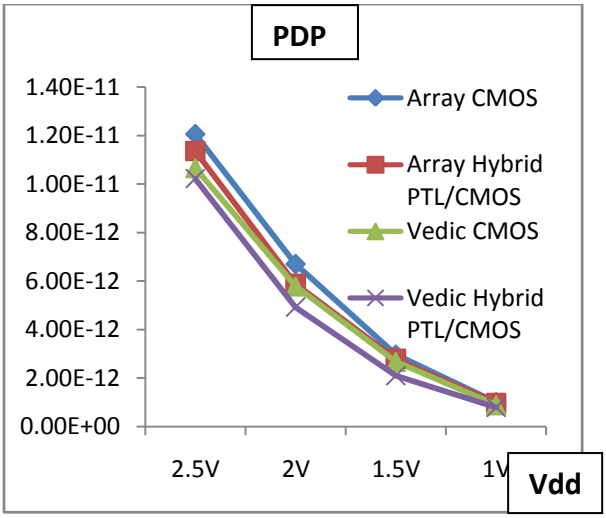


**Fig. 14: Power Delay Product vs. Vdd (50MHz)**

**Table 1 Power Consumption comparison of various Multipliers**

| Design Name | Powers Consumption(mw) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Frequency | | | | | | | |
| | 50 MHz | | | | 100 MHz | | | |
| | Supply Voltage | | | | Supply Voltage | | | |
| | 2.5v | 2v | 1.5v | 1v | 2.5v | 2v | 1.5v | 1v |
| Array CMOS | 2.246 | 2.426 | .556 | .180 | 4.406 | 2.428 | 1.026 | .347 |
| Array Hybrid PTL/CMOS | 2.115 | 1.092 | .518 | .178 | 3.882 | 2.104 | 1.024 | .332 |
| Vedic CMOS | 1.983 | 1.083 | .501 | .167 | 3.373 | 1.829 | 0.838 | .280 |
| Vedic Hybrid PTL/CMOS | 1.900 | 0.914 | .389 | .148 | 3.164 | 1.598 | .702 | .167 |

**Table 2 PDP comparison of various multipliers**

| Design Name | Powers Delay Product | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Frequency | | | | | | | |
| | 50 MHz | | | | 100 MHz | | | |
| | Supply voltage | | | | Supply Voltage | | | |
| | 2.5v | 2v | 1.5v | 1v | 2.5v | 2v | 1.5v | 1v |
| Array CMOS | 12.169 | 6.714 | 2.974 | 1.015 | 12.654 | 9.204 | 2.934 | 1.045 |
| Array Hybrid PTL/CMOS | 11.455 | 5.892 | 2.793 | 0.981 | 11.256 | 6.084 | 2.902 | 0.995 |
| Vedic CMOS | 10.776 | 5.792 | 2.685 | 0.897 | 9.705 | 5.202 | 2.396 | 0.840 |
| Vedic Hybrid PTL/CMOS | 10.278 | 4.932 | 2.107 | 0.799 | 9.096 | 4.618 | 1.985 | 0.835 |

## 7. CONCLUSION

Power consumption, delay, speed, accuracy, hardware requirements, chip area are some the grave concerns in the VLSI industry today .Reduction in the power consumption and delay of a multiplier circuitry is expected to cause a revolution in the field of electronics and communication as these circuits are widely used in every digital and analog system including computers, calculators and other consumer electronics commodities. In this paper the proposed 8x8 Vedic multiplier design using 90nm Hybrid PTL/CMOS logic shows 19.88% to 34.29% power efficiency at 100MHz and 15.17% to 29.90% power efficiency at 50MHz over conventional array multiplier design using 90nm CMOS logic. Thus any system that incorporates this novel design of multiplier will help to curb the power consumption and delay of the systems. The proposed design also shows 15.04% to 26.54% efficiency at 50MHz and 18% to 49.82% at 100MHz in terms of PDP over conventional array multiplier design using 90nm CMOS logic.

## 8. REFERENCES

[1] Jagadguru Swami, Sri Bharati Krisna, Tirthaji Maharaja, "Vedic Mathematics or Sixteen Simple Mathematical Formulae from the Veda, Delhi (1965)", Motilal Banarsidas, Varanasi, India, 1986**.**

[2] Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques", International Conference on Advances in Computational Tools for Engineering Applications (ACTEA) IEEE, pp. 600-603, July 15-17, 2009.

[3] P. K. Saha, A. Banerjee, and A. Dandapat, "High Speed Low Power Complex Multiplier Design Using Parallel Adders and Subtractors, "International Journal on Electronic and Electrical Engineering, (JEEE), Vol 07, no. II, pp. 38-46, Dec. 2009.

[4] S. He, and M. Torkelson, "A pipelined bit-serial complex multiplier using distributed arithmetic," in proceedings IEEE International Symposium on Circuits and Systems, Seattle, W A, April 30-May03,1995,pp. 2313-2316.

[5] P.Mehta and D. Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier." In Proceedings IEEE international conference on Advances in Computing, Control and Telecommunication Technologies. Trivandrum, Kerela, Dec.28-29, 2009, pp.640-642.

[6] C. S. Wallace, "A suggestion for a fast multiplier," IEE Trans. Electronic Computer., vol. EC-13, pp.14-17, Dec.1964.

[7] H. D. Tiwari, G. Gankhuyag, C. M. Kim, and Y. b. Cho,"Multiplier design based in ancient Indian Vedic Mathematics," in Proceeding IEEE International SoC Design Conference, Bussan, Nov. 24-25,2008,pp.65-68.

[8] Z. Huang, and M. D. Ercegovanc, "High-Performance Lox-Power Left-to-Right Array Multiplier Design," IEEE Transactions in computers, vol54,no.3,pp 272-283,March 2005.

[9] T.Aoki ,K.Hoshi, and T. Higuchi, "Redundant complex arithmetic and its application to complex multiplier design ," in proceedings 29th IEEE International symposium on Multiplier-Valued-Logic, Freiburg, May 20-22,1999 , pp.200-207.

[10] S. Vaidya and D. Dandekar,"Delay-Power Performance Comparison of Multipliers in VLSI Circuit Design," in International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

[11] S. He, and M, Torkelson, "A pipelined bit serial complex multiplier using distributed arithmetic," in proceedings IEEE International symposium on circuits and Systems. Seattle, WA, April 20-May-03, 1995, pp.2313-2316.

[12] K.K. Mehta and P.Verma,"Implementation of an efficient Multiplier based on Vedic mathematics using EDA tools, "in International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-5, June 2012.