A PV fed Switched Capacitor Inverter Using Series/Parallel Conversion with Minimum Number of Switches with an Inductive Load

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Abstract— This paper develops a photovoltaic (PV) array fed switched capacitor inverter is proposed. Here the output voltage is larger than the input voltage by switching the capacitors in parallel and in series. Here we don't need any inductors which make the system large. By the usage of capacitors output voltage is boosted. Here photovoltaic (PV) is the main source of supply. By using the H-bridge technique and Marx-inverter structure the harmonics are also reduced by the multi-level output. Here induction motor is connected at output side & the motor will run under critical load also with minimum number of switches. The inverter can be used in hybrid electric vehicles (HEV) and electric vehicles (EV).

Index Terms— Photovoltaic, Multicarrier PWM, Multilevel Inverter, Charge Pump, Switched Capacitor (SC), Filter,Induction Motor**.**

I. INTRODUCTION

Nowadays, there is an increasing demand for ac power supplies. The presence of inductors or transformers in the topology of available DC-AC inverters makes the goal of high power density unachievable. Inductors are bulky elements even in circuits operating at high switching frequency. Inductors and the transformers in the boost converters make the system large because these are having large and heavy magnetic cores to sustain high power. The lack of inductive devices also helps in reducing the EMI problems Due to the continuous power supply reduction, charge pumps circuits are widely used in integrated circuits (ICs) devoted to several kind of applications such as smart power, nonvolatile memories, switched capacitor circuits, Charge Pump (CP) is an electronic circuit that converts the supply voltage *V*DD to a DC output voltage V_{Out} that is several times higher than V_{DD}. (i.e., it is a DC-DC converter whose input voltage is lower than the output one).operational amplifiers, voltage regulators, SRAMs, LCD drivers, piezoelectric actuators, RF antenna switch controllers, etc. Many industrial applications require ac power supplies providing a high-frequency voltage. For example, such inverters are required for supplying gyroscopes, radars, or plasma display panels in the sustaining operation, which are used in high-definition television (HDTV) or high-resolution computer workstation monitors. This is why, the inverter proposed here, both the boost SC active switch and the inverter power switches are operated with a high switching frequency, The main advantage of the solution proposed here is that by adding only a few elements to the SC circuit, a load staircase voltage containing more levels is easily obtained resulting in a staircase load voltage of 25-kHz frequency.

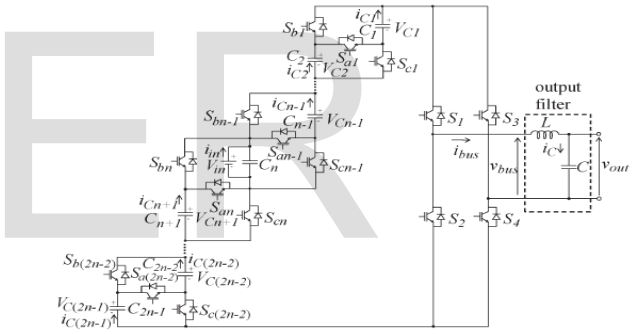

Fig .1.circuit topology of the switched-capacitor inverter using series/parallel conversion

This paper develops A MATLAB/Simulink model of a PV system with switched-capacitor inverter and starts with an introduction of the photovoltaic system for the proposed one as shown in Fig.1. This inverter doesn't require DC to DC boost converter, and this inverter will able to supply high ac current drives Source of this proposed inverter is one of the renewable energy source as PV. The performance of the proposed inverter checked by connecting induction motor as a load. Because induction motor will consume 5 to 6 times rated current at the time of starting, so motor runs in critical load also. the inverter performance and stability are checked by using simulation result applications.

II. MODEL OF PV SYSTEM WITH SWITCHED CAPACITOR BASED INVERTER

The photovoltaic system is shown in fig .2 It contain PV array, switched-capacitor inverter, pulse generator and load.

This system is used for all domestic and industrial single phase high current A.C applications. A solar cell is a solid-state electrical device (P-N junction) that converts the energy of light directly into electricity (DC) using the photovoltaic effect. The process of conversion first requires a material which absorbs the solar energy (photon), and then raises an electron to a higher energy state, and then the flow of this high-energy electron to an external circuit. Silicon is one such material that uses such process.

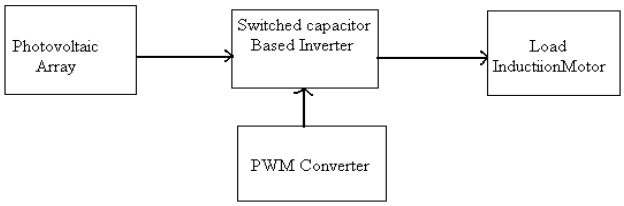

Fig .2.Block diagram of PV system with switched capacitor based inverter

In the existing system, Conventional bridge inverter with source side boost converter and LC filter at output side. For DC to AC step up voltage we need boost converter at dc source side. The boost converter requires additional bulk inductor. The output side LC filter is needed. Source current ripple is very high. Here DC to DC boost converter occupies more space. But in the proposed system PV is connected at the source side. Renewable energy source is utilized effectively. Design calculation is very simple. Here we are not using any type of techniques to photo voltaic. By using the PV there is a Direct step up DC to AC converter and the Harmonics is very low .here LC filter is option able. Renewable energy source is utilized effectively. Design calculation is very simple.

III . OPERATING MODES OF A SWITCHED CAPACITOR BASED INVERTER:

Fig.3, fig .4 and fig.5, shows the current flow of the proposed inverter (n=2) with an inductive load**.** Fig.3 shows all capacitors are connected in parallel whereas shown in Fig. 4 the capacitor C_1 is connected in series and the capacitor C_3 is connected in parallel, and fig.5 shows all capacitors are connected in series.

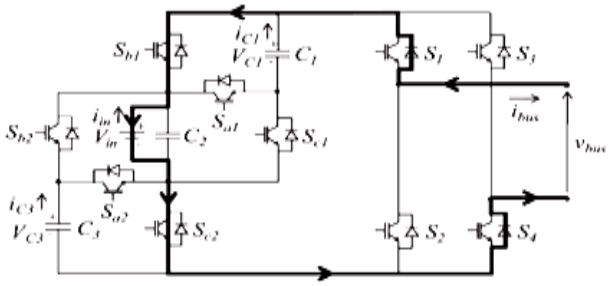

Fig 3.all capacitors are connected in parallel

Fig 3. shows the capacitor C_1 is charged by the current reverse $-i_{C1}$ as shown. Therefore, the proposed inverter can output the bus voltage *Vbus* while the capacitor C_1 is charged. Here switches S_1 and S_4 are switched alternately; the other switches are maintained ON or OFF state. Here C_1 is charged by the current $-I_{c1}$, and here S_{b1}, S_{b2}, S_{c1} is ON remaining switches OFF.

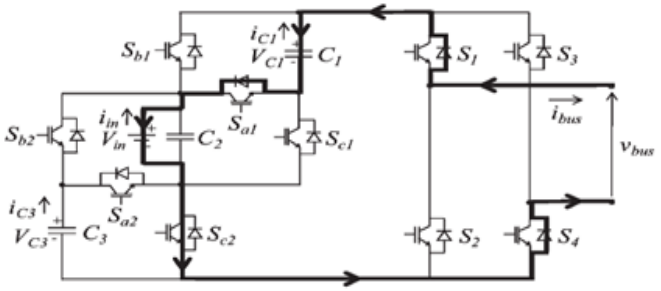

Fig 4: the capacitor C_1 is connected in series and the capacitor C_3 is connected in parallel

Here the capacitor c1 is connected in series and the capacitor c3 is connected in parallel. The capacitor C_3 is charged by the current $-i_{c3}$ and V_{c3} is the voltage of the capacitor C_3 as shown. Here S_{a1}, S_{b2}, S_{c2} is ON state. Remaining switches are OFF state. Switches s_1 and s4 are switched alternately. The bus voltage V_{bus} in the state is

$$\mathbf{V_{bus} = V_{IN} + V_{c1} + V_{c3}}$$

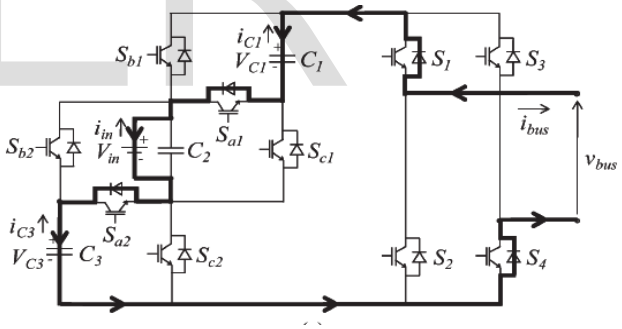

Fig 5: All capacitors are connected in series

Here all capacitors are connected in series. The proposed inverter (n = 2) outputs a 7-level voltage by repeating the three states as shown in Fig.3,Fig.4,Fig.5,Because the driving waveform *vGSa*1 and *vGSa*2 change alternately as shown in Fig. 3, the capacitors *C*1 and *C*3 are equally discharged. Assuming that the number of the capacitors is $2n - 1$, the proposed inverter can outputs $4n - 1$ levels.

DETERMINATION OF CAPACITANCE:

The capacitance C_k can be determined properly by considering the voltage ripple of the capacitors C_k. The smaller voltage ripple of these capacitors leads to the higher efficiency. The capacitance C_k are calculated when the maximum voltage ripple is supposed to be 10% of the maximum voltages of the capacitors.

The capacitors C_k are charged when they are connected in parallel and discharged when they are connected in series. From Fig.3,Fig.5, the switches S_{a1} and S_{a2} of the proposed inverter (n = 2) are symmetrically driven during the half cycle of the reference waveform. Therefore, the voltage ripple of the capacitor C_1 is focused. Assuming that [2] the power factor of the output load cos ϕ = 1, the longest discharging term of the capacitor $C1$ in the proposed inverter (n = 2) is between $t2$ and $t3$. Assuming the Modulation index M = 3, the time $t1$, $t2$ and $t3$.

$$t_1 = \frac{\sin^{-1}(1/3)}{2\pi f_{ref}} \quad \text{……(1)}$$

$$t_2 = \frac{\sin^{-1}(2/3)}{2\pi f_{ref}} \quad \text{……(2)}$$

$$t_3 = \frac{\pi - \sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_{ref}} \quad \text{……(3)}$$

Where frequency *fref* is the of the reference waveform.Therefore, the maximum discharge amount $Q1$ of the capacitor C_1 is

$Q_1=\int_{t2}^{t3} Ibussin\,(2\pi fref\ t\text{-}\phi)\ dt$……..(4)

$C_1>Q_1/0.1V_{in}$……(5)

$I_{c1}=V_{in}-V_{c1}/r_{c1}+2r_{on}$……(6)

The difference of the voltages $V_{in} - V_{c1}$ is small when the capacitance C_1 is large. The capacitor C_1 is charged by the reverse current and the voltage of the capacitor C_1 is increased in the state when C_1 is connected in series as shown in Fig. 4. The charge amount Q_1 of the capacitor C_1 in the state is calculated by

$Q^{-1}=-\int_{t1}^{t2} D_{sat\,(t)}\ Ibus\ sin\ (2\pi\ fref\ t\text{-}\varphi)\ dt$……..(7)

$D_{sa1}\ (t) = 3sin\ (2\pi fref t)\text{-}1$…….. (8)

The maximum discharge amount $Q1$ is larger than the charge amount Q^{-1}. Therefore, the voltage ripple of the capacitor $C1$ is determined by $Q1$ when $0.745 < \cos\phi < 1$. Whether the power factor cos ϕ satisfies cos $\phi \le 0.745$. When the current direction becomes reverse in all states of the switching devices as shown in Fig.(3),(4)and(5). Therefore the maximum discharge amount $Q1$ is calculated by

$Q_1=\int_{\varphi/2\pi fref}^{t3} Ibus\ sin\ (2\pi\ \text{-}fref\ t\text{-}\varphi)\ dt$……(9)

From the equations (4) and (9) the maximum discharge amount Q_1 is reduced. However, Q_1 is larger than the charge amount Q^{-1} because the input current is larger than the reverse current with an inductive load. Therefore, voltage ripple of the capacitor $C1$ is also determined by Q_1 when the power factor cos $\phi \le 0.745$.The maximum discharge amount of Q_1 takes the largest value when cos ϕ = 1 because the peak current is accorded to the peak voltage. Hence, when the capacitance C_k is determined for cos ϕ = 1, the proposed inverter can maintain the output waveform for cosϕ < 1.

CALCULATION OF LOSSES:

Here the power losses of the proposed inverter are calculated. In the calculation, the following losses are considered:

- switching losses.
- Conduction losses of the switches.
- Conduction loss of the output filter.
- Conduction losses and losses caused by the voltage ripple Of the capacitors C_k.

1. SWITCHING LOSSES:

Switching losses are calculated from the charge and the discharge of the parasitic capacitance.From Fig (9) and Fig (10), Switches $S1$ and $S2$ are switched ON/OFF at the carrier frequency f when the reference waveform es satisfies

/es/<1/M A*ref*…… (9)

2. CONDUCTION LOSSES OF THE SWITCHES:

Here all capacitors are connected in series or the state when all capacitors are connected in parallel, the state when one of the capacitors is connected in series. The bus current *ibus* flows in 4 switches on each state as shown in fig.3

$P_{sr}=4.2\pi fref/\pi\int_0^{\frac{\pi}{2\pi fref}} roni^2_{bus}\ dt$…….. (10)

Similarly the current flows in 6 switches in the conventional 7-level CHB inverter because the current flows in 2 switches in each H-bridge. Therefore, the total conduction loss of the switches in the conventional 7-level CHB inverter *PCHB* is calculated as

$Psr=6.2\pi fref/\pi\int_0^{\frac{\pi}{2\pi fref}} roni2bus\ dt$…….. (11)

3. CONDUCTION LOSS OF THE OUTPUT FILTER:

The conduction losses of the filter inductance P_l, *the* filter Capacitances Pc are calculated as the following equations:

$P_l = r_l i^2_{bus}$ ……. (12)

$P_c = r_c i^2 c$……(13)

4. LOSSES OF THE CAPACITORS Ck:

When the capacitors C_k(k _= 2) are connected in parallel, losses occur by the difference between [3] the input voltage *Vin* and the voltages of the capacitors V_{Ck}. The voltage ripple of the capacitors ΔV_k is calculated by

$\Delta V_k=1/Ck\int_{t2}^{t3} ick\ dt$…… (14)

$P_{rip}=\sum_{k=1}^{2n-1} Ck\Delta Vk2\ fref$ …… (15)

From the above two equations the loss P_{rip} is inversely proportional [4] to the capacitance *Ck*, which means the larger

capacitance leads to the higher efficiency. When the capacitors *Ck* are connected in series, the losses occur by the internal resistance *rsc*. The conduction losses of these capacitors *Psc* are calculated by the following equation.

$$Psc=2\pi fref/\pi\sum_{k=1}^{2n-1}\int_{\sin-1(\frac{2}{3})/2\pi fref}^{\pi-\sin-1(\frac{2}{3})/2\pi fref} rsci^2 Ck\,dt \ldots\ldots (16)$$

IV. MATLAB MODEL FOR PROPOSED SYSTEM:

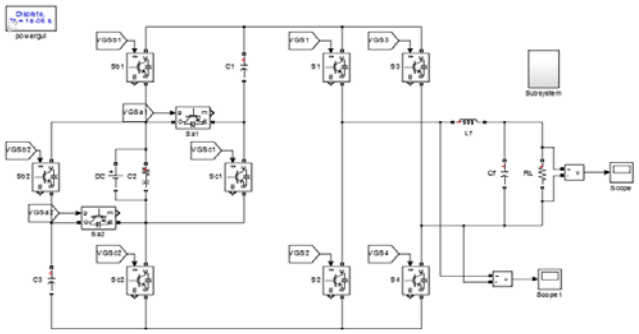

Fig:6. MATLAB model for proposed system

OBSERVED VOLTAGE WAVEFORMS:

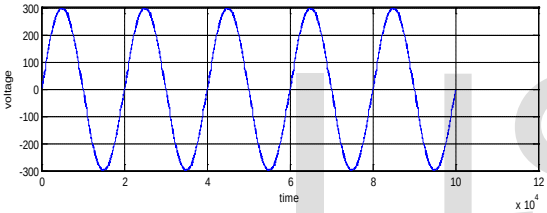

Fig:7.observed output voltage waveform V_{out}

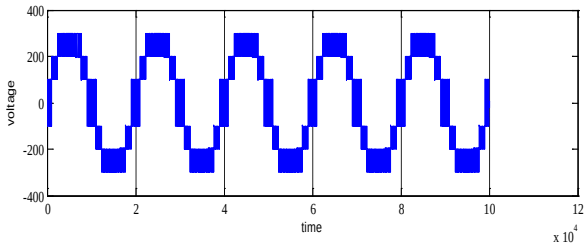

Fig:8.observed bus voltage waveform V_{bus}

The above waveforms are for the proposed system. output voltage waveform vout and the bus voltage waveform vbus are taken.in this project multicarrier PWM is used to see the gate to source voltage levels in MATLAB model subsystem is used to give the pulses for the proposed inverter.here multi multicarrier pwm is taken.for that multicarrier pwm positive and negative pulses are taken.For positive pulses reference wave vref and e1,e2,e3 voltages are taken.

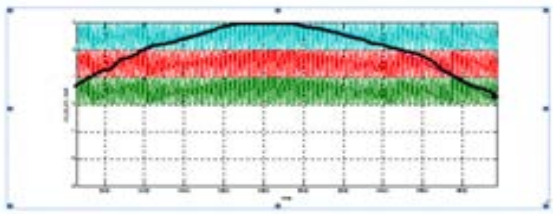

Fig:9.positive pulses for the modulation method for the proposed inverter.

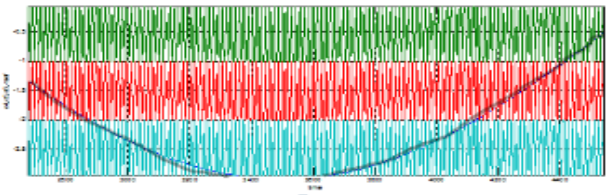

Fig:10. negative pulse for the modulation method for the proposed inverter

For negative peak e4,e5,e6 are taken.The above two waveforms are for the modulation method for the proposed inverter.here reference waves and the carrier wave are taken.when vref>carrier (es) output is 1.otherwise output is 0.

MATLAB MODEL FOR THE EXISTING SYSTEM:

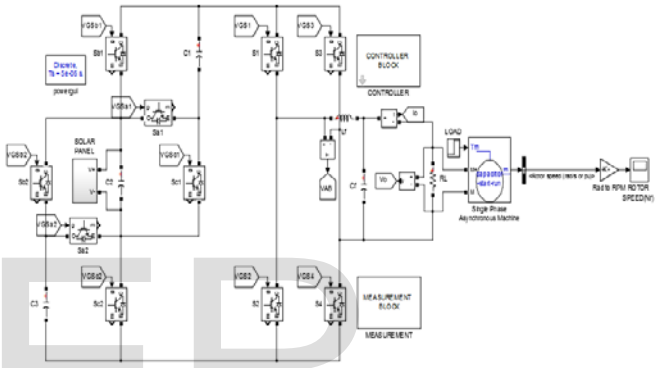

Fig:11. MATLAB model for the existing system connected Pv and the induction motor.

OBSERVED WAVEFORMS FOR THE EXISTING SYSTEM:

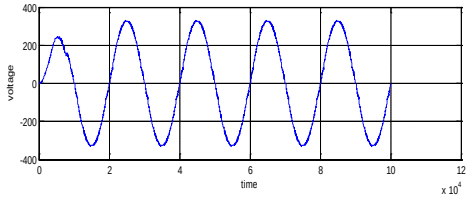

Fig:12. output voltage vo.

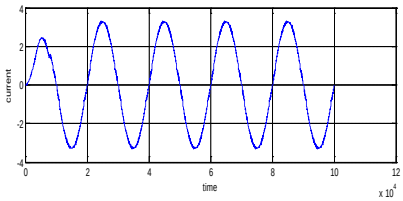

Fig:13. output current (io)

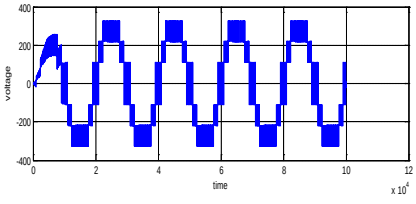

Fig: 14. Voltage across Vab

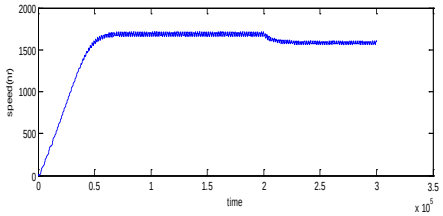

Fig: 15.rotor speed characteristics

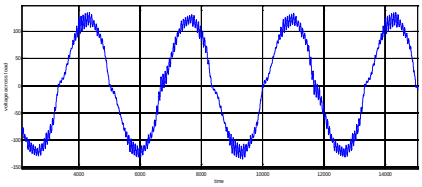

Fig: 16. Voltage under load

The above waveforms are for existing system. Induction motor is connected at load side. here output voltage Vo, output current Io, voltage across Vab, and the rotor speed characteristics, and voltage under load condition. Output voltage increases slowly and maintains constant. Value of output voltage is 300V approximately. And output current also increases slowly and maintains constant. And the value current of output is 3A approximately. Rotor speed characteristics are taken 160rpm approximately. Under critical load conditions motor will run. This is one of the main advantage in existing system.

SIMULINK MODEL OF SOLAR PANEL:

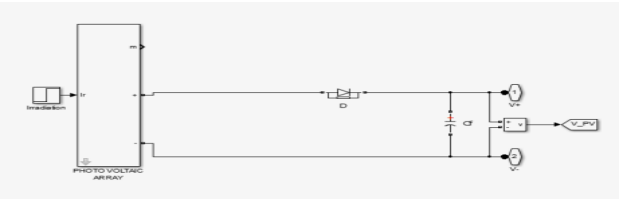

Fig: 17. Simulink model of a solar panel

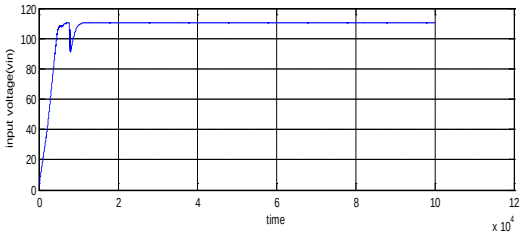

Fig: 18.Input voltage of solar panel

PV ARRAY:

A simple equivalent circuit of the PV array is shown below in fig.10. The dc current source represents the dc photocurrent that is generated from the [7],[8] PV-cell connected in parallel to a diode. The series resistance represents the internal electrical losses. In this circuit, the following equation is derived of Kirchhoff's law.

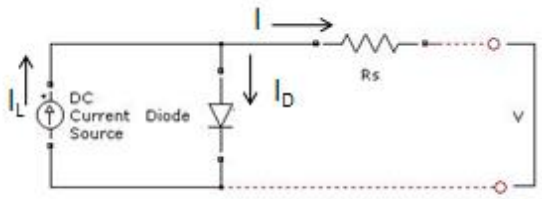

Fig:19. Equivalent electric circuit of a P-V module

The current I_D of the diode is given by the equation

$$I=I_L-I_D \quad (1)$$

$$I_D = I_0[\exp(q(V+IR_sS)/(\gamma kT)_sC)-1] \quad (2)$$

Combining the eq. 1and 2 we have

$$I=I_L - I_0[\exp(q(V-IR_sS)/(\gamma kT)_sC)-1] \quad (3)$$

The eq.4 expresses the voltage:

$$V=\frac{\gamma kT_c}{q}\ln\left(\frac{I_L-I}{I_o}+1\right)-IR_s \quad (4)$$

I_D diode current

I_L photoelectric current related to a given condition of radiation and of temperature

V output voltage

I_o saturation diode current

Γ form factor which represents an index of the cell failing

R_s series resistance of the cell

Q charge (1.602x10-19 C)

K Boltzmann constant (1.381x10-23 J/K)

The above eq. 4 is verified for certain values of temperature and solar irradiance. In case one of these variables differs, the output voltage and current of the P-V module varies from the MPP. In order to calculate [9]the module voltage we have to multiply it by the number of the cells connected in series. The module current is the sum of the cells connected in parallel. When cell temperature or solar irradiance change the PV module is being affected, thus we calculate the output current and voltage from eq. 3, 4.By implementing this mathematical model in MATLAB for different conditions of temperature but in constant solar irradiance, we take the characteristics V-I curve of the PV-cell (fig.20). In this figure we can see the voltage-current characteristics for constant irradiance but for different cell temperatures. As the temperature is rising, the efficiency is falling. The purple line is at 0^0 C, the yellow at 25^0 C, the red at 70^0 C and the blue at 85^0 C. The same behavior appears in many PV cells connected together in order to reach the required power.

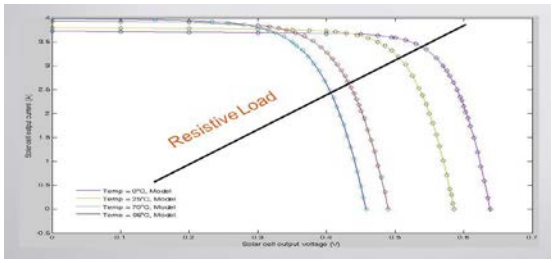

Fig: 20. Module characteristics I-V curves

The straight line represents a simple resistive load. From this figure it is obvious that the power that is generated form this cell and for this load is near the MPP only at the lowest temperature and in the other scenarios there is an amount of energy that cannot be injected to this simple system due to the Ohm's Law and the I-V PV curve. Also we can see that this load is under different voltage and current at different cell temperatures. This indicates the[10],[11] necessity of voltage, or current regulation power electronic circuits, and a system to enable the maximization of the generated power.

V. CONCLUSION:

In this project by using the capacitors in series and in parallel Maximum output voltage is boosted than the input voltage.Total harmonic distortion (THD) is reduced and the THD of the output waveform of the inverter is reduced compared to conventional single phase full bridge inverter as the conventional multilevel inverter. In this project the determination method of capacitance, the modulation method And the losses are calculated .The circuit operation of the proposed inverter was confirmed by the simulation results and examined with an induction motor taking the pv as the main source of supply at source side.

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