

A Simplified Synthesis of Transmission Lines with a Tree Structure

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Abstract. The limiting factor for high-performance systems is being set by interconnection delay rather than transistor switching speed. The advances in circuits speed and density are placing increasing demands on the performance of interconnections, for example chip-to-chip interconnection on multichip modules. To address this extremely important and timely research area, we analyze in this paper the circuit property of a generic distributed *RLC* tree which models interconnections in high-speed IC chips. The presented result can be used to calculate the waveform and delay in an *RLC* tree. The result on the *RLC* tree is then extended to the case of a tree consisting of transmission lines. Based on an analytical approach a two-pole circuit approximation is presented to provide a closed form solution. The approximation reveals the relationship between circuit performance and the design parameters which is essential to IC layout designs. A simplified formula is derived to evaluate the performance of VLSI layout.

1. Introduction

Interconnection design has been a major concern in the design of high-speed systems. The state-of-the-art IC chips are designed to operate at multigigahertz clock rate. In this speed range the traditional *lumped*—*RC* model can no longer provide sufficient modeling information about interconnections. Instead, the effect of inductance must be considered, and, in general, a *distributed* or *transmission line* model need to be used. Research on the evaluation of interconnection performance has been active in several different levels. The most accurate and original method is to solve 3-D (or 2-D) time-variant Maxwell equations [1–2]. The effect of electrical and geometric parameters on the circuit performance can be investigated in great detail. For instance, the scattering of waves at a wire bend (or a discontinuity) can be evaluated. However, due to the complexity of this approach only numerical method is feasible. A general relationship between the circuit performance and design parameters cannot be explicitly established. Furthermore, a practical design tool cannot be developed based on this approach because of its formidable computation time.

A less complicated approach to evaluate interconnection performance considers a 1-D problem, i.e., solves a 1-D *telegraph equation* [3]. Even though the dimension of the problem is reduced only the ideal case, an infinite long line or ideal termination, is analytically solvable [4]. For a generic interconnection structure, for instance, several lines connected into a tree, an exact analytic solution is almost impossible to be obtained because of the irregular boundary conditions encountered in solving the telegraph equation.

The next level to attack the interconnection issue is *circuit simulation*, which is a typical numerical approach. Since circuit simulation is an indispensable step in IC design the research along this line focuses on developing an efficient interconnection model so that it can be easily incorporated into the existing circuit simulator, such as *spice* [5, 6]. Although a simulator in principle can simulate any circuit it has the disadvantage that a general understanding of physical meaning behind the interconnection design is often shaded by the numerical calculation. For instance, a simulator can easily evaluate the performances of the trees of different topologies which implement the same net. It is hard for the simulator to tell why one topology is

better than the others. Even more importantly, it is very difficult to construct a proper interconnection topology using the information provided by the circuit simulation.

A deep understanding of the intrinsic relationship between interconnection performance and interconnection topology and parameters is the starting point for optimal interconnection designs. Such a relationship can only be thoroughly explored from an analytical approach. In this paper we first analyze a generic distributed *RLC-tree* circuit. We shall solve this problem analytically, and then extend the result to the case where the interconnection has a tree structure consisting of transmission lines, which is called *tree-of-transmission-lines*. Based on the analytic solution a lower-order circuit approximation will be presented for developing a closed-form solution. The approximation reveals the interplay between circuit performance and the design parameters which is essential to IC layout design [7, 8]. A simplified formula is consequently derived to guide VLSI performance driven layouts [9–11].

The article is organized as follows. In Section 2 the necessary background and the circuit formulation of interconnections in the high-speed system are introduced. In Section 3 the defined problems, *RLC* tree and *tree-of-transmission-lines*, are analyzed analytically. In Section 4 the approximation technique is discussed and a closed-form solution is presented. In Section 5 some special issues regarding the *tree-of-transmission-lines* are discussed in detail. In Section 6 several design examples are presented and the accuracy of the developed approximation is confirmed by the numerical simulation. Finally, in Section 7 comments are made on the obtained results and on the further research.

2. Preliminaries

Let us consider a circuit layout as illustrated in figure 1 where gate G_0 drives six gates G_i , $i = 1, \dots, 6$ through a net N . The interconnection (net N) has a tree structure. An accurate modeling of this interconnection calls for the consideration of transmission line effect when the circuit intends to operate at very high frequency. That is, each wire segment needs to be treated as a transmission line. Since a net is usually laid out in a tree structure we hence have a tree in which edges are transmission lines. We call it *tree-of-transmission-lines*. Each transmission line in the tree is described by a telegraph equation. Because the telegraph equation considers only 1-D electromagnetical

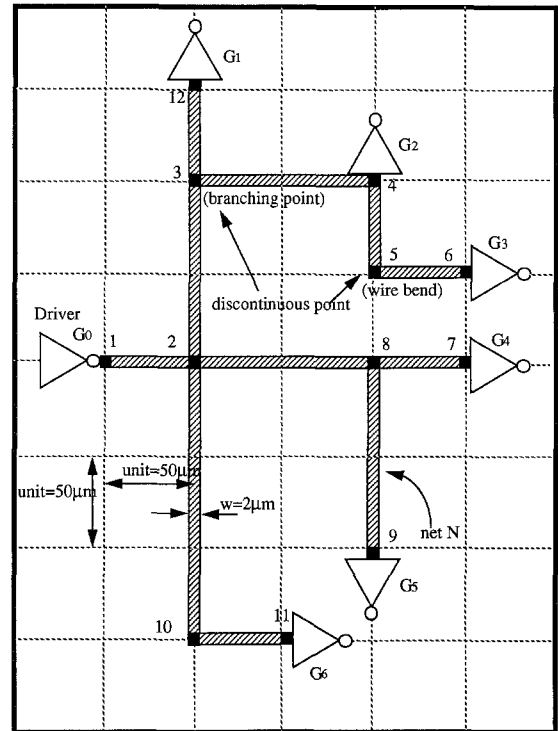


Fig. 1. An illustration of the interconnection layout in IC chips.

field, 2-D field effect is modeled by introducing extra capacitance at the discontinuities of interconnections, such as branching point and wire bend (figure 2). The loading gates also introduce the capacitance or resistance at the nodes of the tree, depending on the technology (MOS or bipolar device). Formally, we define

DEFINITION 1. The topology of the *tree-of-transmission-lines* is a tree. Each edge of the tree is a transmission line. At each node there is a capacitor connected to the ground.

In the following we shall first solve a distributed *RLC* tree circuit and then extend the result to the case of *tree-of-transmission-lines* by taking appropriate limitations. In order to do so we cut each edge of *tree-of-transmission-lines* into many small segments and model each segment by an *RCL* circuit as indicated in figure 2. The resulted circuit is a distributed *RLC* tree. Taking Laplace transform on the *RLC* tree we can introduce a more simple and general notation as illustrated in figure 3, where Z_i , $i = \dots$, represents impedance between two nodes. Notice that the impedance here can represent a much more complicated circuit than just the Laplace transform of a single resistance or capacitance. The analytical approach addressed in the following

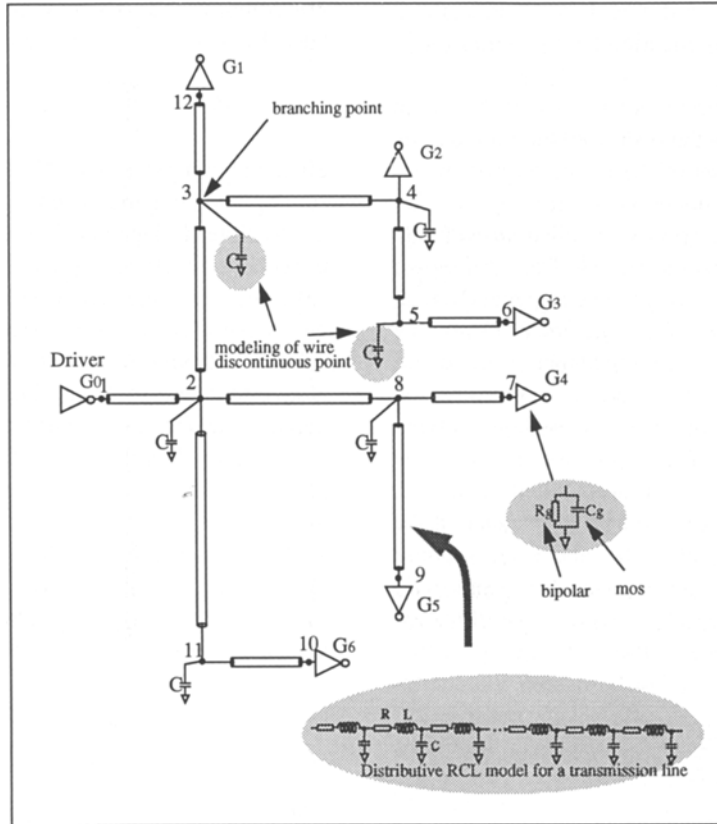


Fig. 2. Tree-of-transmission-lines.

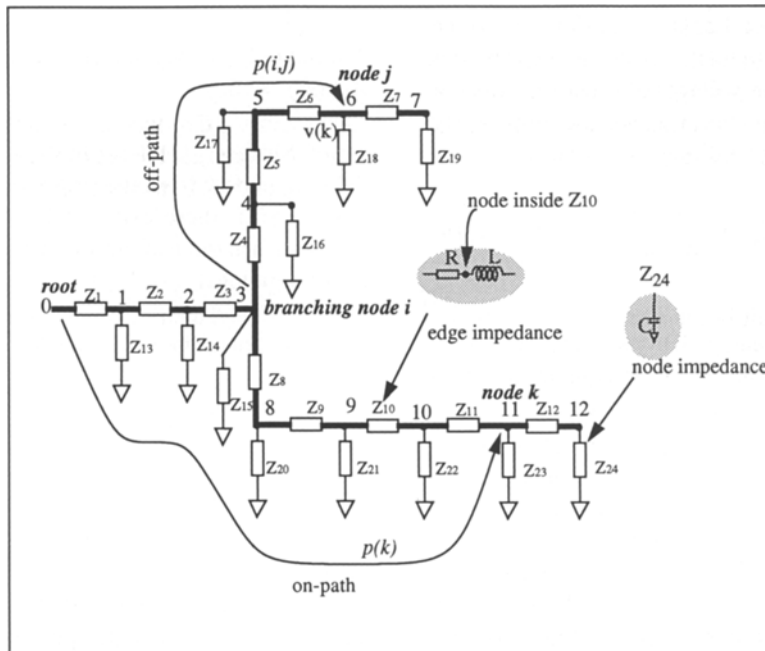


Fig. 3. The distributed RCL tree to model the tree-of-transmission-lines.

sections based on the circuit model shown in figure 3 actually has a broader application than just the simple *RLD* tree.

Let us consider the circuit voltage response v_k at an arbitrary node k . Denote the path from the root to node k by $p(k)$. Denote the set of the nodes on $p(k)$ by A_p and the set of the rest nodes in the tree by \bar{A}_p . The nodes in A_p and \bar{A}_p are respectively called *on-path* and *off-path* nodes with respect to node k . Denote the path from node i to node j by $p(i, j)$. The impedance in an edge of the tree is called *edge impedance*. Denote by $Z_{p(i,j)}(s)$ the sum of the edge impedance of the edges in $p(i, j)$. Call $Z_{p(i,j)}(s)$ *path impedance*. From a node j to ground there is a unique path without passing through the other nodes. The impedance of this unique path is denoted by $Z_{n(j)}(s)$ and called *node impedance*. Denote by $Z_{k,j}(s)$ the path impedance of the common portion of the paths $p(k)$ and $p(j)$. Suppose node i is the branching point between $p(k)$ and $p(j)$. From the definition, $Z_{k,j}(s) = Z_{p(i)}(s)$. We illustrate the above notations and definitions in figure 3 with $k = 11$, $j = 6$ and $i = 3$. We have path impedance $Z_{11,6}(s) = Z_1 + Z_2 + Z_3$, $Z_{p(2,8)}(s) = Z_3 + Z_8$, $Z_{p(6)}(s) = Z_1 + Z_2 + Z_3 + Z_4 + Z_5 + Z_6$, and node impedance $Z_{n(11)}(s) = Z_{23}$.

3. Analytical Theory

Let the input at the root be $f(t)$, and its Laplace transform be $F(s)$. Let Laplace transform of v_k be $V_k(s)$. Suppose there are total m nodes in the tree. For an arbitrary node k the voltage difference between k and the input is the summation of voltage drops along the path $p(k)$ [13]. Accordingly, we have

$$F(s) - V_k(s) = \sum_{j=1}^m Z_{k,j}(s) \frac{V_j(s)}{Z_{n(j)}(s)}, \quad K = 1, \dots, m. \quad (1)$$

This gives a set of linear equations with $V_k(s)$, $k = 1, \dots, m$, as unknowns. We write equation (1) into the matrix form

$$\begin{pmatrix} a_{1,1} & a_{1,2} & \cdots & a_{1,m} \\ a_{2,1} & a_{2,2} & \cdots & a_{2,m} \\ \cdots & \cdots & \cdots & \cdots \\ a_{m,1} & a_{m,2} & \cdots & a_{m,m} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_m \end{pmatrix} = \begin{pmatrix} F_1 \\ F_2 \\ \vdots \\ F_m \end{pmatrix} \quad (2)$$

where $a_{k,j} = Z_{k,j}(s)/Z_{n(j)}(s)$, $k \neq j$, $a_{j,j} = Z_{j,j}(s)/Z_{n(j)}(s) + 1$, and $F_i = F$, $i = 1, \dots, m$. Denote $D(s) = \det A$ and $N_k(s) = \det A_k$, where A_k is the matrix obtained by substituting vector \vec{F} into the

k th column of A . Theoretically, $V_k(s)$ can be calculated by using the following equation.

$$V_k = \frac{N_k(s)}{D(s)}, \quad k = 1, 2, \dots, m. \quad (3)$$

Since the computation of $N_k(s)$ and $D(s)$ is time consuming and, in general, only the numerical solutions are feasible, Pillage and Rohrer [12] proposed an approximation method (AWE) to calculate them. In their AWE method a high-order system is first approximated by a desired lower-order system, and then poles are calculated from the approximated lower-order system. Notice that their method relies on the numerical techniques. The physical meaning of the solution is difficult to be explored explicitly. In the following we will approximate the calculation of system poles by exploiting the property of a linear system, and further develop an analytical closed-form solution.

Let s_k , $k = 1, \dots, m$, be the roots of $D(s) = 0$. From the linear algebra we can calculate the determinant of A by expanding it along the k th row

$$D(s) = \det A = \sum_{j=1}^m a_{k,j} A_{k,j}, \quad (4)$$

where $A_{k,j} = (-1)^{k+j} \det A_{k,j}$ and $\det A_{k,j}$ is the determinant of an $(m-1)$ by $(m-1)$ matrix obtained by deleting the k th row and j th column. $A_{k,j}$ is the cofactor of $a_{k,j}$. We now present a theorem.

THEOREM 1. *There exists at least one pole s_k such that $A_{k,k}(s_k) \neq 0$.*

Proof. Since $A_{k,k}(s)$ describes a subcircuit obtained by deleting node k from the original circuit described by matrix $A(s)$, there exists at least one pole s_k which distinguishes the two circuits when both circuits have a tree topology. \square

From Theorem 1 we can define

$$\theta_{k,j} = \frac{A_{k,j}(s_k)}{A_{k,k}(s_k)}. \quad (5)$$

Equation (4) becomes

$$\begin{aligned} D(s_k) &= \left[\sum_{j=1}^m \theta_{k,j} a_{k,j} \right] A_{k,k}(s_k) \\ &= \left[1 + \sum_{j=1}^m \theta_{k,j} \frac{Z_{k,j}(s_k)}{Z_{n(j)}(s_k)} \right] A_{k,k}(s_k) = 0 \end{aligned} \quad (6)$$

The fact that $A_{k,k}(s_k) \neq 0$ implies that s_k must be the solution of

$$1 + \sum_{j=1}^m \theta_{k,j} \frac{Z_{k,j}(s)}{Z_{n(j)}(s)} = 0 \quad (7)$$

There might be several s_k 's depending on the order of equation (7). Considering the arbitrariness of the choice of row k and repeating the same operation to all rows of $A(s)$ we obtain

$$D(s) = \prod_{k=1}^m \left[1 + \sum_{j=1}^m \theta_{k,j} \frac{Z_{k,j}(s)}{Z_{n(j)}(s)} \right]. \quad (8)$$

We introduce a new parameter γ_k defined as¹

$$\gamma_k = \left[\sum_{j=1}^m \theta_{k,j} \frac{Z_{k,j}(s_k)}{Z_{n(j)}(s_k)} \right]^{-1} \left[\sum_{j=1}^m \frac{Z_{k,j}(s_k)}{Z_{n(j)}(s_k)} \right] \quad (9)$$

Equation (7) becomes

$$\gamma_k + \sum_{j=1}^m \frac{Z_{k,j}(s_k)}{Z_{n(j)}(s_k)} = 0, \quad k = 1, \dots, m. \quad (10)$$

All system poles are then calculated from equation (10). In the rest of this paper we assume that $f(t)$ is a step function.² Writing pole s_j in the form $s_j = -\alpha_j + i\beta_j$ and taking the reverse Laplace transformation we obtain

$$v_k(t) = V_0 - \sum_{j=1}^m \text{Res}(V_k(s_j)) e^{(-\alpha_j + i\beta_j)t}, \quad k = 1, \dots, m, \quad (11)$$

where $\text{Res}(V_k(s_j))$ is the residue of $V_k(s)$ at pole s_j .

4. A Closed-Form Approximation

The primary goal of this paper is to find a causal relationship between circuit response, such as the waveform at a node, and the circuit parameters. A closed form solution is hence preferred since it reveals the physical meanings of the solution. Such a closed-form solution is also critical to the *performance-driven layout* in high-speed IC design as demonstrated later in Section 6. In the previous section we have found a general solution (equations (10) and (11)) to a distributed *RLC* tree circuit. Unfortunately, numeric calculation has to be used to determine those poles and the corresponding residues for any nontrivial problems. This to a certain extent shades the physical meaning of the solution.

Notice that pole s_k is obtained by separating a factor from $\det A(s)$ by expanding $\det A(s)$ along its k th row. Since the k th row of $A(s)$ actually represents the relationship between node k and all the other nodes, we can “consider,” for convenience, s_k as a *pole associated* with node k though we know that a pole is related to a system instead to a node. From equation (6) it is clear that the factor $(1 + \sum_{j=1}^m \theta_{k,j} Z_{k,j}(s_k)/Z_{n(j)}(s_k))$ separated from $\det A(s)$ contains all the information of the relationship between node k and the rest of the circuit, since the other factor $A_{k,k}(s_k)$ does not contain any element connecting node k and the rest of the circuit. Therefore, the poles s_k calculated by setting this factor equal to zero (equation (10)) can be used as the poles of a lower-order approximation. Namely, we use the poles s_k calculated from

$$\gamma_k + \sum_{j=1}^m \frac{Z_{k,j}(s_k)}{Z_{n(j)}(s_k)} = 0. \quad (12)$$

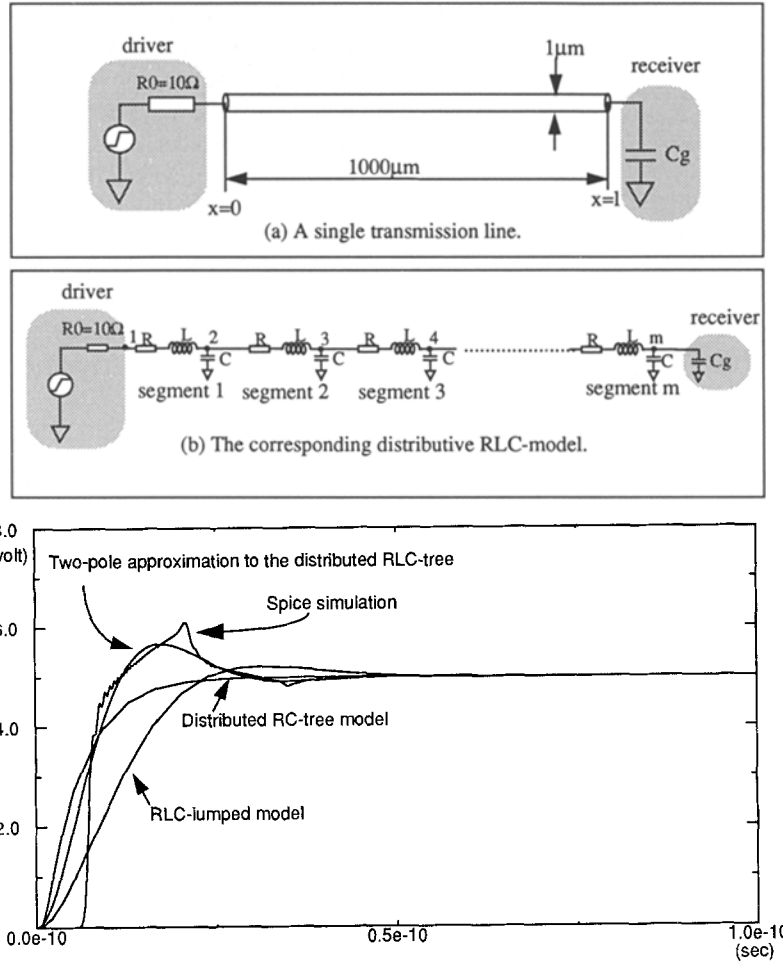
to approximate the response at node k . Suppose the above equation has an order $d(k)$ with respect to s , and $s_{k(1)}, s_{k(2)}, \dots, s_{k(d(k))}$ are its roots. We have the following approximation for the voltage at node k

$$v_k(t) = V_0 - \sum_{j=1}^{d(k)} \text{Res}(V_k(s_{k(j)})) e^{s_{k(j)}t}. \quad (13)$$

equations (12) and (13) are the approximations of equations (10) and (11), and specify a lower-order system which is an approximation of the original one.

It remains to calculate the poles from equation (12) and the corresponding residues. This requires γ be calculated first.³ From the definition of γ (equations (9) and (5)) its value can be calculated if the poles are known. We hence face a *chicken-and-egg* problem here. The purpose of introducing γ is to simplify the calculation of poles. Thus, we shall first calculate poles with γ as a parameter. We then determine γ by considering some special cases where the solutions of poles are known. Namely, by comparing our solution of poles with γ as a parameter to the known poles we can determine the value of γ .

The special case we use to determine γ is shown in figure 4a, where a uniform transmission line is connected to a driver at $x = 0$ and to a capacitor at $x = l$. This is a general interconnection model for CMOS circuits. Zhou, Preparata, and Kang studied the analytic solution of this problem and further suggested to use a two-pole system to approximate the original one [4]. For the considered transmission line let the resistance,



(c) Numerical calculation of the waveform in a single transmission line.

Fig. 4. A single transmission line.

inductance and capacitance of unit length by R , L , and C , respectively. The driver has output impedance R_0 . The load has impedance $1/sC_g$. The poles of their two-pole system are determined by the following equation with the assumption that $Cl \gg C_g$.⁴

$$CLl^2 s^2 + (2R_0Cl + RCl^2 + \frac{\pi}{2}) s + \left(\frac{\pi}{2}\right)^2 = 0 \quad (14)$$

In order to make comparison we apply our result equation (12) to the single transmission line case. We uniformly cut the line into m segments and later let $m \rightarrow \infty$. The nodes are labeled as shown in figure 4b. We calculate the pole associated with node m locating at $x = l$. Since the line is uniformly cut, $Z_{n(j)}(s) = 1/sC_j = m/sCl$, $Z_{m,j}(s) = R_{m,j} + sL_{m,j} = (lR/m + s lL/m)j$, $Z_0(s) = R_0$ and $Z_{n(m)}(s) = 1/sC_g$, where C_g is the gate capacitance. For the discussed circuit equation (12) becomes

$$\left[\frac{LCl^2}{2} + lC_g \right] s^2 + \left[R_0Cl + \frac{RCl^2}{2} + (R_0 + Rl)C_g \right] s + \gamma_m = 0. \quad (15)$$

Using the same assumption that $Cl \gg C_g$ and comparing equations (15) and (14) we find $\gamma_m \approx 1.23$. The response at the receiving end is expressed by

$$V(t) = V_0 - V_0 \left[\frac{s_2}{s_2 - s_1} e^{s_1 t} + \frac{s_1}{s_1 - s_2} e^{s_2 t} \right] \quad (16)$$

where s_1 and s_2 are the solutions of equation (15).

We calculate numerically the waveform of the circuit shown in figure 4a, and the result is shown in figure 4c. A fair match is seen comparing our result to the simulation one. It is also seen that the distributed RC

model [13] and lumped *RLC* model [8] cannot well model the discussed problem at the concerned frequency range.

5. Tree of Transmission Lines

For a tree structure, the response differs from node to node. The response at a particular node can be calculated based on the poles associated with this node as discussed in Section 4. When calculating the response at a given node *k* the main difference between the single line and the tree-of-transmission-lines is the existence of off-path nodes in the later case. In the following we still use equations (12) and (13) as a general solution form and properly introduce a scale factor to reflect the influence of the off-path nodes.

Let us consider the response at an arbitrary node *k*. Suppose node *j* is an off-path node and the branching point between *p(k)* and *p(j)* is node *i*. The path impedance $Z_{p(j)}$ consists of two portions: $Z_{p(i)}$ and $Z_{p(i,j)}$, respectively. Call $Z_{p(i)}$ *on-path impedance*, and $Z_{p(i,j)}$

off-path impedance. Denote them by $Z_{on(k,j)}$ and $Z_{off(k,j)}$, respectively. Figure 5 illustrates the above definitions. Equation (12) can be written as

$$\gamma_k + \sum_{j \in A_p} \frac{Z_{k,j}(s)}{Z_{n(j)}(s)} + \sum_{j \in \bar{A}_p} \frac{Z_{k,j}(s)}{Z_{n(j)}(s)} = 0 \quad (17)$$

where A_p and \bar{A}_p are respectively the sets of on- and off-path nodes as defined in Section 2. If set \bar{A}_p is empty (no off-path nodes) the above equation describes a single transmission line which we have discussed in Section 4. The effect of branching points and off-path nodes is reflected by the last summation $\sum_{j \in \bar{A}_p} Z_{k,j}(s)/Z_{n(j)}(s)$. Notice that this summation originates from charging capacitors at off-path nodes. The following observations are useful for the construction of the scale factor (figure 5).

1. The off-path impedance is zero. The off-path capacitors can be treated as the lumped capacitors at the corresponding branching node. This case can be considered as a single transmission line. Equivalently, the scale factor should be one unit in this case.

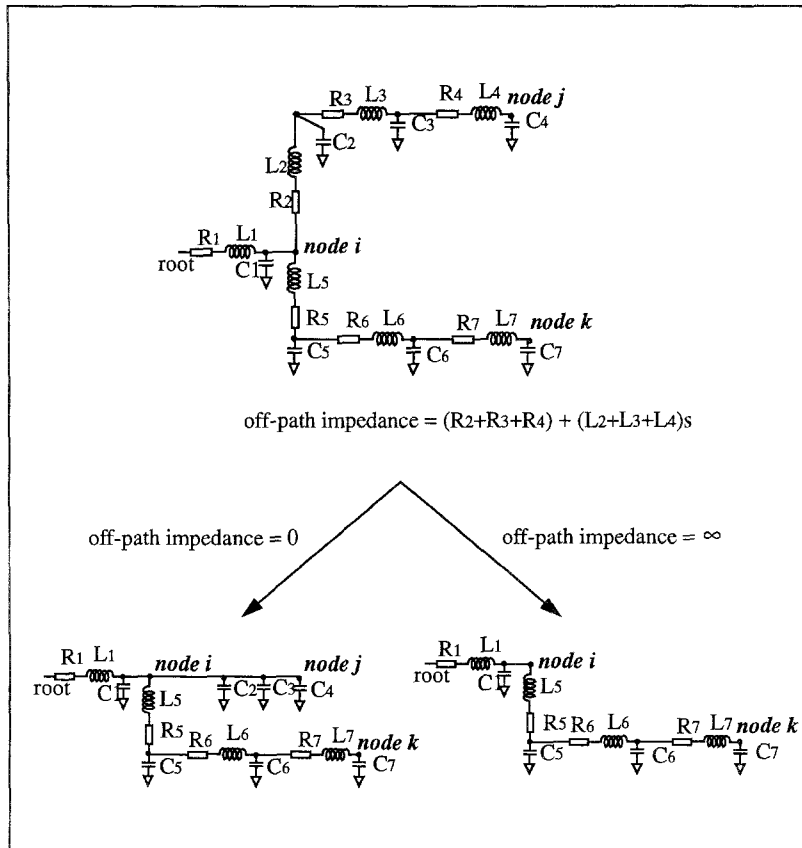


Fig. 5. The effect of charging off-path node capacitors.

2. The off-path impedance is of infinity. There is actually no need to consider charging the off-path node capacitors. The summation term over the off-path nodes should be scaled to zero. That is, the scale factor should be zero.
3. Neither of the above two cases is true. That is, the off-path impedance has a finite value. The scale factor takes the value between 0 and 1.

We introduce a scale factor $1/(1 + Z_{\text{off}(k,j)}) : j \in \bar{A}_p$. We modify equation (17) by⁵

$$1.23 + \sum_{j \in A} \frac{Z_{k,j}(s)}{Z_j(s)} + \sum_{j \in A} \frac{1}{1 + Z_{\text{off}(k,j)}(s)} \frac{Z_{k,j}(s)}{Z_j(s)} = 0 \quad (18)$$

Therefore, the bigger the $z_{\text{off}(k,j)}$ the smaller the effect of charging off-path node j . The introduced scale factor satisfies the requirement at the two extreme situations: either the off-path impedance is zero or infinite. Equation (18) and (13) are the approximations for the tree-of-transmission-lines. Actually, we can conservatively choose the scale factor to be one unit, which leads to an upper bound on the delay estimation since all off-path capacitors are to be charged regardless of the value of off-path impedance. Choosing the scale factor as one unit we can merge equations (18) and (12) and, equivalently, we are no longer to distinguish the case of a single line from that of a tree-of-transmission-lines.

To demonstrate the effectiveness of the two-pole approximation for the case where the original circuit

is a distributed *RLC* tree, figure 6 compares the result by the two-pole approximation with that by *spice* simulation for the routing tree in figure 1. Tree edges are cut into small wire segments of $10 \mu\text{m}$ long and each of them is then modeled by an *RLC* circuit as described before. We calculate the voltage response at node 11. It is seen that the two-pole approximation well captures the main property of the distributed *RLC* circuit. Although the accuracy achieved by the two-pole approximation is inferior to the standard of circuit simulation, it is sufficient to guide the performance-driven layout. As has been shown in [9, 14] that an average up to 67% reduction on the interconnection delay can be obtained based on the presented two-pole approximation, as compared to the traditional lumped *RC* model.

6. Waveform, Delay, and Design Example

In this section we examine the waveform and delay of an interconnection circuit, and then apply the obtained result to an IC design problem. The waveform is important here because, different from the *overdamping* case, oscillations exist in the interconnection circuit as demonstrated in figure 6. Therefore, to properly define the delay of interconnections is not a trivial problem. Actually, it is a rather difficult problem.

One of the traditional definitions of delay is defined as the time period τ in which the node voltage $v_k(t)$ *stably* reaches a given value or high. One choice of this given value usually is $0.9 V_0$, where V_0 is the final value of $v_k(\infty)$.⁶ The stable here means $v_k(t) \geq 0.9 V_0$ as $t \geq \tau$. This definition of delay is popular when

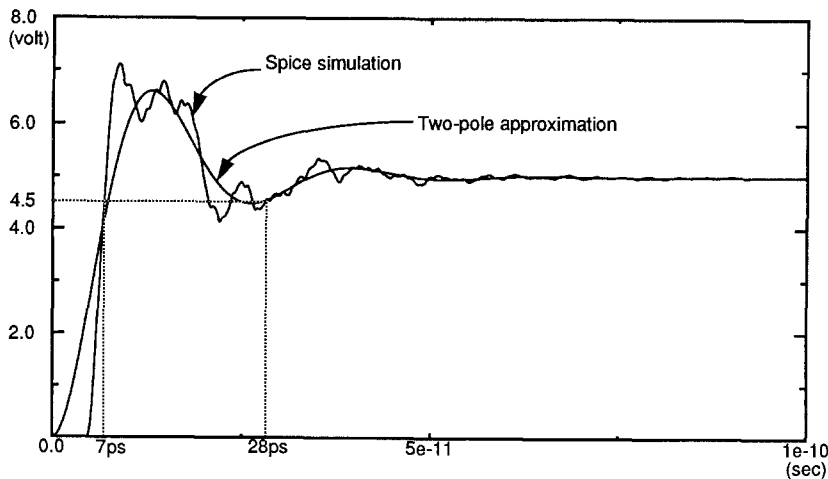


Fig. 6. The effectiveness of two-pole approximation.

the response is *over-* or *critically-damped*. It is not clear whether this definition is still a good one when there exists oscillation. In figure 6 we see $\tau = 27$ ps by this definition. However, the loading gate at node k ($= 11$) may have been permanently turned on at the time $v_k(t)$ first time reaches $0.9 V_0$ ($t = 7$ ps). Notice that different gates may have different threshold voltage and different circuits may have different gate turn-on and turn-off design margin. It is clear that the definition of delay depends on the specific application and the technology.

We now discuss a design example. We construct two different trees to implement the same net in figure 1. The constructed trees are shown in figure 7, where tree1 is a minimum Steiner tree and tree2 is an A-tree [14]. Traditionally, tree1 is considered as the optimal imple-

mentation which provides the minimal delay under the lumped RC model. However, using the distributed RLC model and the two-pole approximation established in the previous section we can construct an A-tree (tree2) which gives a shorter delay and smaller overshooting than that the minimum Steiner tree dose, as demonstrated in figure 8 [9]. In other words, tree2 provides a better performance as compared with tree1. The reason that we are able to construct a better interconnection topology is the availability of a closed-form solution equation 15 based on the second-order approximation [10, 11]. In contrast, a numerical simulator can usually provide the information for a proper choice of interconnection parameters, such as wire size, but hardly provide any information for the choice of the interconnection topology.

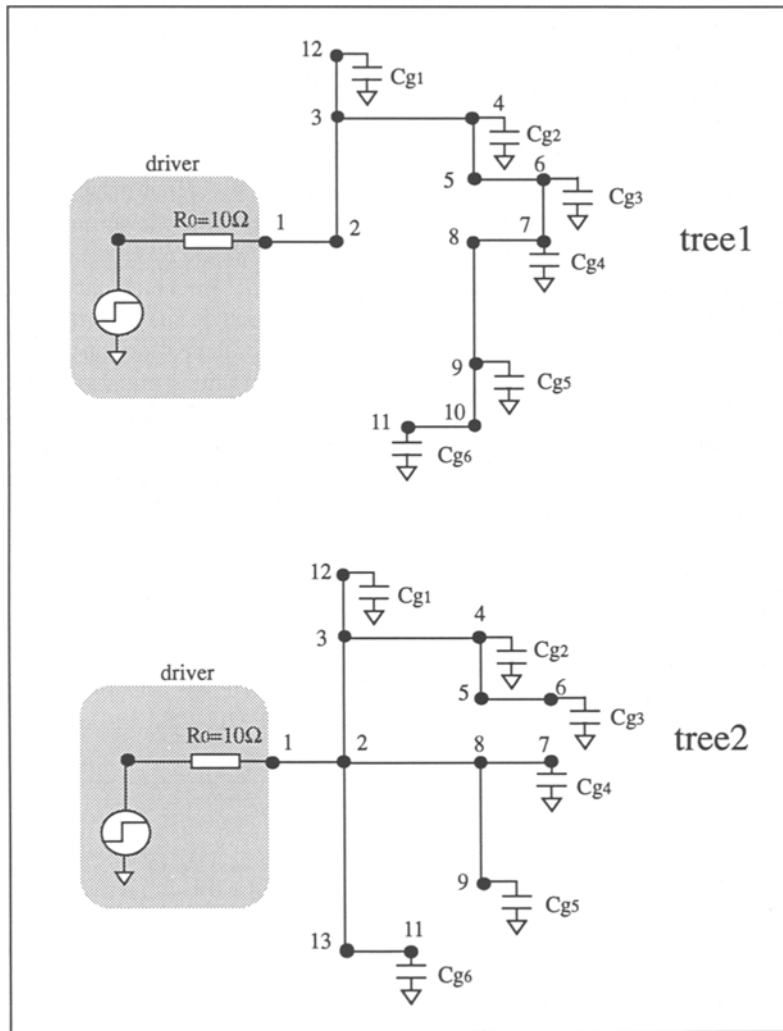


Fig. 7. Two different trees to implement the same net N in figure 1.

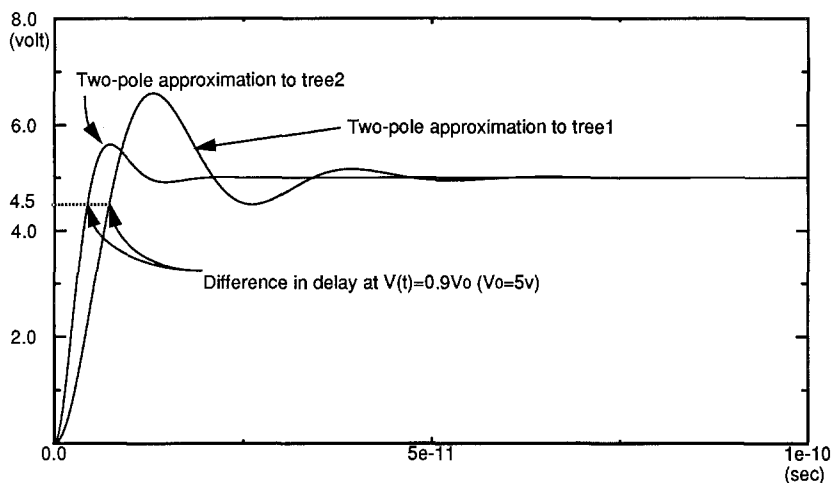


Fig. 8. Waveforms at node 11 of tree1 and tree2.

Note that tree1 is a minimum Steiner tree, but has very long tree radius. Tree2 has a slightly longer total wire length, but much smaller tree radius. It was claimed in [15] that a routing tree with small wire length and small radius is the best in terms of circuit delay. Our work confirms their claim theoretically and experimentally. An efficient algorithm to construct a routing tree with both small radius and small wire length is given in [15]. Furthermore, a minimal delay tree can be constructed based on the analytical solution obtained in this paper [10, 11].

7. Discussion and Conclusion

We have analyzed the distributed *RCL* tree circuit and extended the obtained results to the calculation of the tree-of-transmission-lines. A lower order circuit approximation has been established for developing the closed-form solution. The numerical calculation has shown the validity of the approximation. The obtained results have been applied to the design of IC layouts. We make the following comments on the discussed problem for the future research.

1. When studying the *RLC* system a one-pole circuit approximation will not be sufficient since it cannot model the wave phenomenon. The wave phenomenon is essential in the transmission line analysis. Hence, the approximation circuit should be at least of order 2.
2. Our lower order circuit approximation can be considered as an extension of the result of Rubinstein et al. where they studied an *RC* tree [13]. In fact, by setting inductance equal to zero our result equation (12) will reduce to their result.

3. The definition of delay in a distributed *RLC* circuit (or a tree-of-transmission-lines) is not clear, especially when the transmission line is poorly terminated. As mentioned in the paper this issue is technology dependent. However, a more objective measure on the signal delay needs to be addressed.
4. Our result on the lower-order circuit approximation to a distributed *RLC* tree can be easily incorporated into VLSI layout tools since the result is in an analytical closed form. The result not only provides a means for the performance evaluation of high-speed interconnections, but also establishes the relationship between the circuit response, such as delay, and the interconnection topologies. Recent study has shown that the interconnections constructed based on our two-pole approximation model preserve a high fidelity to the optimal interconnection performance [11].

Acknowledgments

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Notes

1. Notice that s_k is the solution of equation (7).
2. The case of an arbitrary driving function $f(t)$ can be discussed similarly.
3. When context is clear we will omit the subscript of γ .
4. This assumption can be satisfied in most practical interconnection design problems.
5. We suppose that γ keeps the value determined from the single line case.
6. Recall that we have assumed that a step input is applied at the root of the tree.

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