A W-Band Phase-Locked Loop for Millimeter-Wave Applications

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Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

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Abstract

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Recently, systems operating in the millimeter-wave frequency bands are demonstrated and realized for many applications. A W-band phase-locked loop (PLL) is designed for a 94GHz medical imaging system. Four popular frequency synthesizer architectures are discussed and compared. The PLL using a fundamental voltage-controlled oscillator (VCO) is chosen for the synthesizer architecture and realized in 0.13μm SiGe BiCMOS process. The employed fundamental Colpitts VCO achieves a tuning range from 92.5 to 102.5GHz, an output power of 6dBm, and a phase noise of -124.5dBc/Hz at 10MHz offset. The locking range of the PLL is from 92.7 to 100.2GHz, the phase noise is -102dBc/Hz at 1MHz offset, and reference spurs are not observable. This work also compares the figure-of-merit for millimeter-wave VCOs and discusses the LO distribution for millimeter-wave applications.

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Chapter 1

Introduction

1.1 Introduction

Recently, systems operating in the millimeter-wave frequency bands are demonstrated and realized for many applications. For example, the 60GHz transceivers are for high-speed wireless communication [1], [2], 77GHz for automotive radar systems [3], [4], and 94GHz for medical imaging systems [5]–[7]. Additionally, several frequency bands between 70GHz and 100GHz are open for commercial development. Compared to the microwave spectrum, the big advantage of this millimeter-wave range is that the wider bandwidth can be utilized leading to faster communication, and higher radar/imaging resolution resulting from the shorter wavelength. As semiconductor technologies advance, the device cut-off frequencies increase, making these millimeter-wave systems more realizable and more efficient. Moreover, phased-array systems and beamforming techniques have been reported to improve the system

performance.

1.2 LO Generation

In the millimeter-wave systems, the LO part is one of key components, and most of the systems need low LO noise (jitter) and high output power. For example, the phase noise or jitter of the carrier frequency degrades the system accuracy, increasing system errors. Especially, imaging resolution and quality will be degraded due to high phase noise in imaging systems and the SNR improvement will be dampened in the beamforming system. The data acquisition rate can also be reduced significantly due to high jitter. Moreover, if the output power is low, it degrades mixer conversion gain and noise figure, which can only be ameliorated with more buffer stages and increased power consumption. Thus, the overall system performance can be significantly affected by the LO.

To date, various frequency synthesizers have been reported for these frequency bands and several synthesizer architectures have been attempted in order to improve the performance. These architectures are categorized into four groups: PLL using a fundamental VCO, PLL using an N-push VCO, PLL and a frequency multiplier, and finally PLL and an injection-locked oscillator. Each has merits and disadvantages, and will be discussed in chapter 2.

1.3 LO Distribution

The importance of an LO distribution is often neglected in the millimeter-wave systems. Even though the LO signal is generated well, if it is not properly delivered, the overall system performance will be degraded. As such the LO distribution network should be carefully considered even at the initial stages of designing a millimeter-wave transceiver. A VCO is usually placed far from other TX/RX amplifiers to avoid coupling or pulling issues [8]. Accordingly, the length of a routing line increases and becomes comparable to a quarter of the wavelength in the millimeter-wave frequencies. Then these long lines can cause significant attenuation and phase shift. Moreover, as the VCO drives TX, RX, or PLL divider, the signal distribution should be included in the analysis.

1.4 Target Application

This report focuses on demonstrating the LO generation and distribution parts for the 94GHz medical imaging system [5]–[7]. The system is to detect breast cancer cells by exploiting the high contrast between the dielectric constants of cancer tissue and healthy tissue [5]. To overcome high attenuation at 94GHz and to increase the system SNR, the transmitter needs to employ a beamforming system with multiple synchronous carriers, requiring accurate phase and time lock. At the receiver, multiple pulses are averaged to increase the SNR. For these reasons, this imaging system requires a low phase noise synthesizer and a high LO signal power, whereas the power consumption specification is relatively relaxed.

1.5 Outline

The rest of this report is organized as follows. Chapter 2 discusses frequency synthesizer architectures to generate a millimeter-wave frequency and Chapter 3 gives a detailed description of the designed W-band fundamental VCO. Then the PLL and its building blocks are presented in Chapter 4. Chapter 5 discusses the LO distribution. Measurement results for the free-running VCO and the PLL are given in Chapter 6, followed by conclusion in Chapter 7.

Chapter 2

Frequency Synthesizer Architectures

As mentioned in Chapter 1, there are four kinds of frequency synthesizer architectures as shown in Fig. 2.1. In these architectures, the synthesizer takes the same input reference frequency and gives the same output frequency. Here, the output frequency is assumed as 96GHz to make calculations easy because 96 is a multiple of 2, 3 and 4.

2.1 PLL using a Fundamental VCO

The first architecture uses a PLL which employs a fundamental-frequency VCO [9]–[12]. As shown in Fig. 2.1(a), the VCO output and the first-stage divider input are running at 96GHz. Only this architecture requires the 96GHz frequency divider so high-frequency divider design is critical. The fundamental VCO has design challenges arising from the low gain in transistors and low quality factor (Q) in varactors, which limits the tuning range at

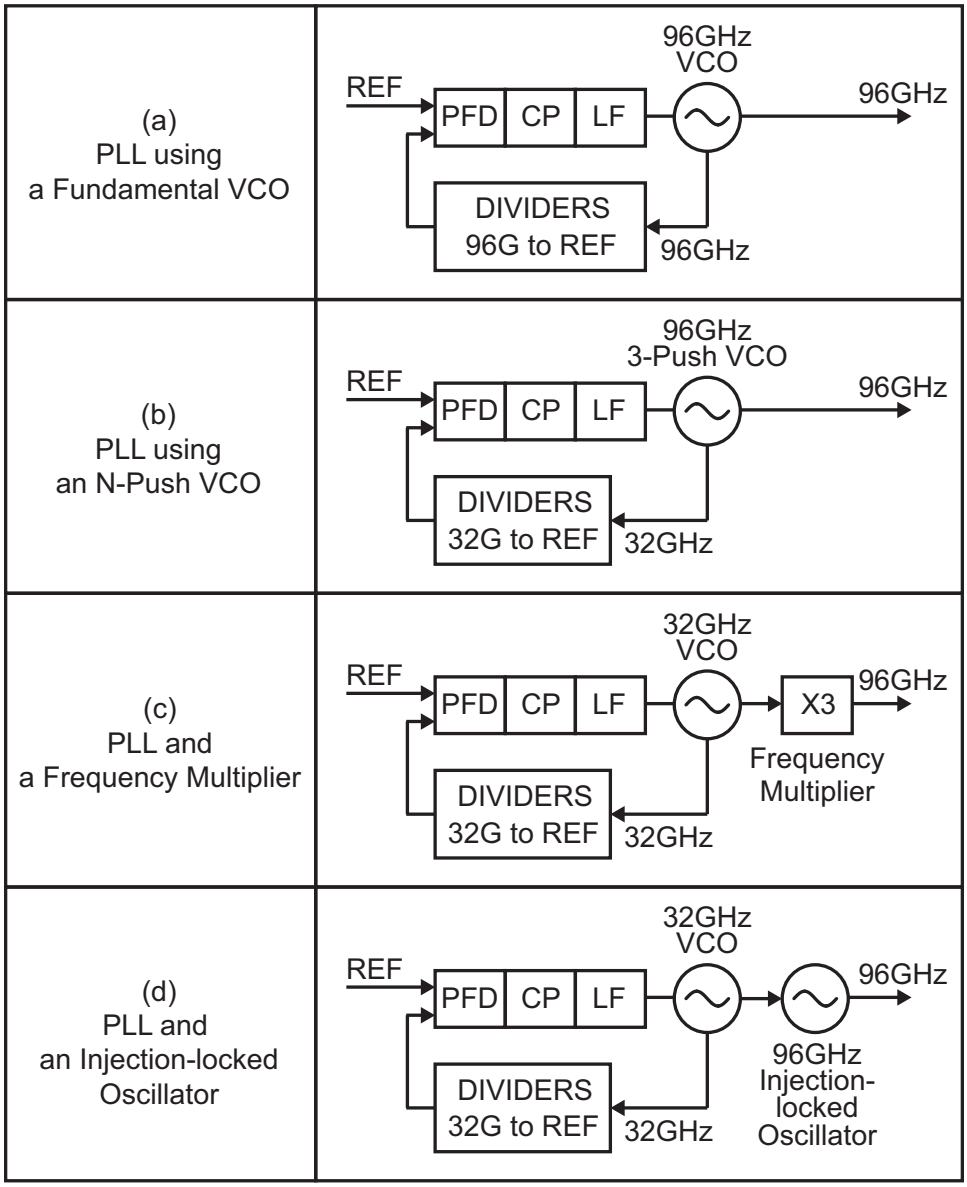


Figure 2.1: Frequency synthesizer architectures. (a) PLL using a Fundamental VCO. (b) PLL using an N-push VCO. (c) PLL with a Frequency Multiplier. (d) PLL with an Injection-locked Oscillator.

the high frequency of 96GHz. For this design, achieving the high LC tank Q, high swing, and low phase noise is challenging, but the VCO can be made very small due to low tank inductance ($\sim$50pH).

2.2 PLL using an N-push VCO

The second architecture uses an N-push VCO instead of the fundamental VCO in the PLL [11], [13], [14]. Fig. 2.1(b) shows only the case of N=3. An advantage is that the first-stage divider does not need to run at 96GHz so the power dissipation of the divider chain can be reduced. Another advantage is that the VCO operates at a lower frequency (48 or 32GHz). Thus, transistors have higher gain and varactors have higher Q compared to the first architecture, so the VCO design can be relaxed depending on the factor of N. However, N-push VCOs suffer from low output power because the output power relies on the non-linearity of devices. If N is 2, two phases are obtained easily from a differential signal, but if N is 3 or more, it requires more phases or more oscillators, causing more power consumption and possibly more complex routings. Also amplitude and phase mismatches reduce the output power. Thus, more buffer stages are needed to generate a desired output power.

2.3 PLL and a Frequency Multiplier

The third architecture uses a low-frequency PLL and an additional frequency multiplier [15], [16]. Here the frequency multiplier is defined as a non-oscillating block (not inside the PLL) that generates an output frequency, a multiple of the input frequency. The multiplication ratio can be 2, 3, or higher. (3 for Fig. 2.1(c)) As the ratio increases, the conversion gain generally decreases, the output power decreases, and the required input power increases.

There are several types of frequency multipliers. One may think that the injection-locked oscillator is a frequency multiplier, but it is categorized into a different group because the non-oscillating multipliers and the oscillators show different characteristics. One typical type is a harmonic generator as described in the previous architecture and has the same problem, high conversion loss. To obtain a high output power, the input power, that is the VCO output power, should be even higher. Also the strong fundamental tone of the VCO can leak through the multiplier and affect the mixer or system performance, so the unwanted tones should be filtered out properly. On the other hand, a big advantage is that the PLL is designed at a lower frequency.

2.4 PLL and an Injection-locked Oscillator

The last architecture is using a low-frequency PLL and an injection-locked oscillator [16], [17]. As shown in Fig. 2.1(d), this architecture is similar to the previous one, but this requires a 96GHz oscillator and uses the injection locking technique, which is widely used to improve the phase noise. The oscillator should have a wide locking range to ensure the injection locking over PVT variations. The oscillator does not need a varactor for fine tuning but should have some switched capacitors to compensate for the frequency shift due to variations. If the oscillator fails to be locked by the low-frequency oscillator, then it shows pulling effects and contaminates the spectral purity, leading to a system misbehavior. Therefore, more design margins should be included to guarantee the injection locking. To

Table 2.1: Comparison of the Frequency Synthesizer Architectures

Architecture	Required Blocks	Advantages	Disadvantages
(a) PLL using a Fundamental VCO	Fundamental VCO, High-frequency Divider	Low complexity Small area	High-frequency Divider Low varactor Q/tuning range
(b) PLL using an N-push VCO	N-push VCO	Low division ratio Wide tuning range	Low output power Many oscillators (N>2)
(c) PLL and a Frequency Multiplier	Low-frequency VCO, A Frequency Multiplier	Low division ratio Wide tuning range	Low output power Output harmonics
(d) PLL and an Injection-locked OSC	Low-frequency VCO, An Injection-locked OSC	Low division ratio Better phase noise	Injection pulling issue Narrow locking range

get a wide locking range, it requires low Q and strong injection [8] but the low Q raises power dissipation and phase noise. Moreover, the input injection signal is generated as a harmonic of the low-frequency VCO and so the VCO output power should be high, as in the third architecture.

2.5 Design Considerations

Table 2.1 summarizes the above synthesizer architectures. All the architectures can be a good option that designers can choose depending on the system requirements. Designers should first consider what blocks need the LO signal, how much output power and phase noise the blocks want, and whether the blocks require multiple phases like the I/Q mixer. Also designers should check the process technology (device characteristics, transmission line performance, etc.). Next, the chip floorplan should be considered. For example, the PLL location, the distance between the VCO and mixers/buffers, and the number of routings needed. Designers cannot know or estimate everything at the initial design time, but the

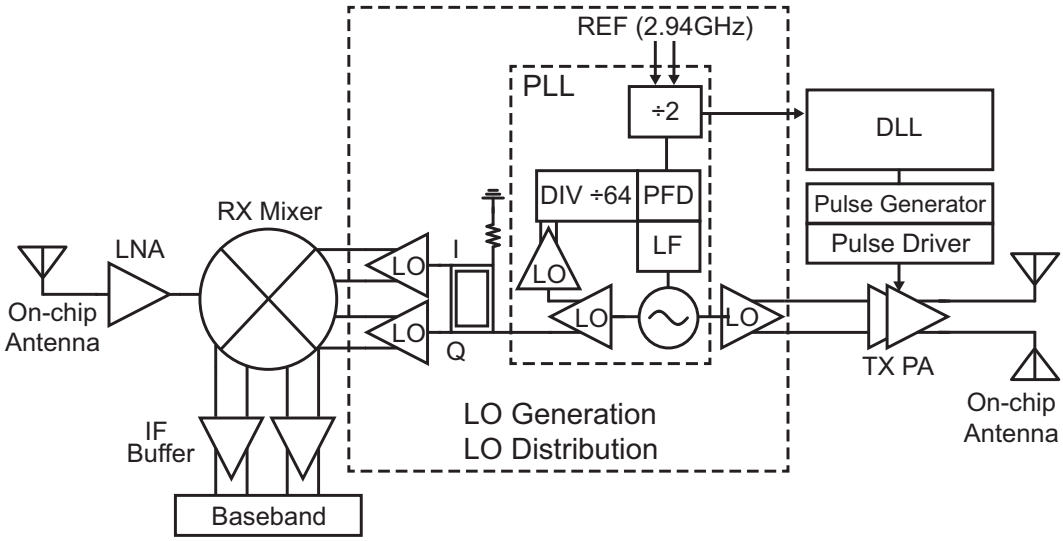


Figure 2.2: Block diagram of the targeted medical imaging system.

above information helps in the architecture selection.

As mentioned in Chapter 1, this work is mainly for the 94GHz medical imaging system and the system block diagram is illustrated in Fig. 2.2 [6], [7]. Several considerations drove the selection of the final synthesizer architecture. First, as the LO is shared between the TX PA and the RX I/Q mixers and all the aforementioned blocks require low phase noise and high LO power (>0dBm). The next consideration is the process selection, in this case a 0.13μm SiGe BiCMOS process [18] (f_T is around 230GHz). As the second and third architectures have inherently lower output power, amplification of the VCO to achieve the requisite high power requires several buffer stages, burning more power, which occupies a larger area. The required power gain increases faster than linearly as a function of N (number of stages combined or the N'th harmonic in the multiplier) since the harmonic powers drop due to the non-linear nature of the frequency multiplication or generation. While the first

and fourth architectures both need a 96GHz fundamental oscillator, the first one needs a 96GHz divider and the fourth one needs a low-frequency VCO. With the given process, the 96GHz Miller divider can be implemented with wide frequency range and small area. Also, the injection locking scheme is avoided because TX, RX, DLL, and PLL are integrated on the same chip and the pulling effect can be a problem [8]. Given all of these factors, the PLL using a fundamental VCO is chosen for the frequency synthesizer architecture in this work.

Chapter 3

W-band Fundamental VCO

3.1 VCO Design Considerations

At the millimeter-wave frequencies, two topologies (cross-coupled VCO and Colpitts VCO) are widely used. But it is well known that the maximum oscillation frequency of the Colpitts VCO is higher than that of the cross-coupled VCOs [4]. So the Colpitts VCO can achieve relatively lower phase noise and wider tuning range. Thus a 96GHz fundamental Colpitts VCO is designed and implemented in this work [9]. The schematic of the VCO is shown in Fig. 3.1 [19], [20] and the parameters are in Table 3.1. The transistor bias points are set by optimizing the gain performance (f_T, f_{max}) and the current consumption. The device size is determined by the tank loss [21]. Since the transistor capacitance is in series with the varactor in the Colpitts VCO, the change of the device size does not significantly cause a frequency shift or a tuning range degradation so the device size can be decided independently

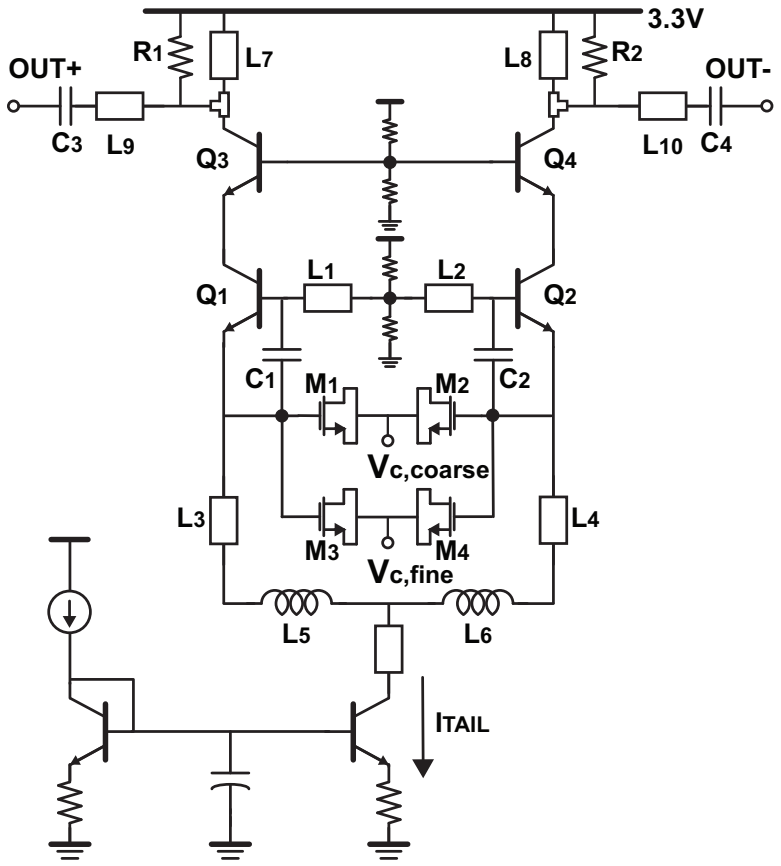


Figure 3.1: Schematic of the W-band fundamental Colpitts VCO.

of the varactor size ($C_\pi + C_{1,2} \gg C_{var}$). Also, the external capacitors (C_1 and C_2) are added and adjusted between the base and the emitter in order to linearize the transistor capacitance and increase the tuning range. Moreover, to save the power consumption, the output buffer (Q_3 and Q_4) is stacked on top of the VCO tank circuit, so the buffer and the tank core share the DC current. Therefore additional buffers are not needed for tank isolation due to the cascode-style isolation of the LC tank [20] and this technique also reduces the die area. Specifically, the impedance looking into the emitter of Q_3 or Q_4 should be small to sustain the oscillation. And the impedance looking into the collector of Q_3 or Q_4 can be potentially

Table 3.1: VCO Parameters

Devices	Size
Q_1, Q_2	$L_E = 5 \times 1.6\mu m$
Q_3, Q_4	$L_E = 5 \times 2.4\mu m$
M_1, M_2	$2.25\mu m \times 0.13\mu m \times 10 \times 3$
M_3, M_4	$3.40\mu m \times 0.13\mu m \times 10 \times 1$
R_1, R_2	150Ω
C_1, C_2	$50fF$
C_3, C_4	$80fF$
L_1, L_2	Microstip Line $5\mu m \times 63\mu m$
L_3, L_4	Microstip Line $3\mu m \times 84\mu m$
L_5, L_6	Spiral Inductor $180pH$
L_7, L_8	Microstip Line $3.6\mu m \times 99\mu m$
L_9, L_{10}	Microstip Line $3.6\mu m \times 18\mu m$
I_{tail}	24mA

negative around the oscillation frequency so the load resistors (R_1 and R_2) make the output resistance positive over all the frequencies. An LC matching network is used to match to 50Ω.

The tank Q is one of the most important parameters in LC VCOs. The Q affects most of VCO properties such as the overall tank loss, the power dissipation, the tank swing, and phase noise. In the low frequency bands (<10GHz), the tank Q is dominated by that of the inductor. But, as frequency increases higher than 30GHz, the Q of varactors is degraded significantly. So the varactor Q determines the overall tank Q at the millimeter-wave frequencies. At the same time, the tuning range is also set by the varactor size. Thus it is critical to obtain high-Q and large-ratio (C_{max}/C_{min}) varactors to achieve better VCO performance. However, the Q and the capacitance ratio are in a trade-off as described in Fig. 3.2. For example, for MOS varactors if the channel length is chosen as the minimum,

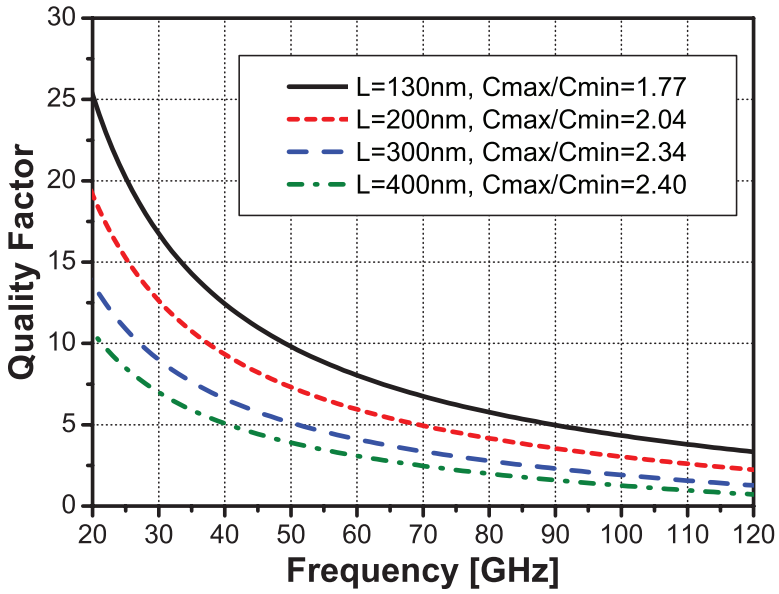
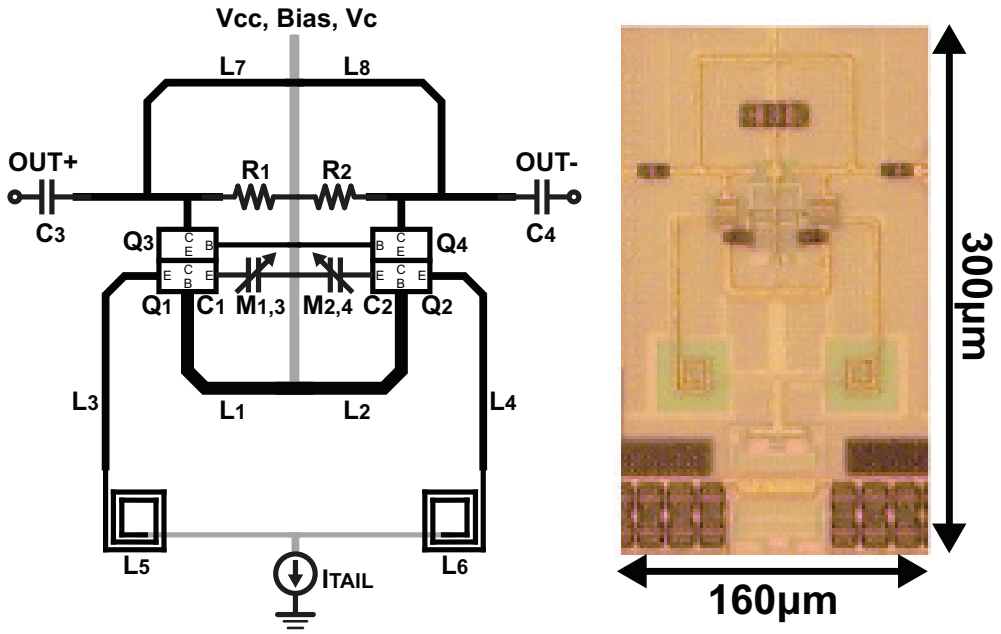


Figure 3.2: Quality factors of the accumulation-mode MOS varactors of the 0.13μm process (post-layout simulation).

the Q can be maximized but the capacitance ratio is minimized. On the contrary, if the length is increased, then the capacitance ratio increases but the Q decreases. Additionally, if the minimum width is used and the finger number is increased, then parasitic capacitance is increased so the Q can be increased but the capacitance ratio is degraded due to the parasitic capacitance. Therefore, there is an optimum point (length, width, finger number) in the varactor design. Definitely, the varactor layout is important to reduce parasitics. In this work, the minimum length (0.13μm) and 2.25μm of the width are chosen to balance the Q and the capacitance ratio. Four devices are used and each has ten fingers. For a desired K_{VCO} in the PLL, the width of one device is increased to 3.40μm, as shown in Table 3.1. As a result, the varactor Q is 4.9, C_{max} is 67fF, and C_{min} is 39fF. In order for this VCO to be employed in a PLL and to realize a desirable K_{VCO}, the varactors are divided into two



(a) (b)

Figure 3.3: Layout and implementation of the VCO. (a) VCO floorplan (not to scale). (b) Micrograph.

parallel banks and tuned by two analog control voltages, $V_{c,coarse}$ and $V_{c,fine}$, as shown in Fig. 3.1.

The inductors are realized by microstrip lines which consist of top-layer thick metal (M6) and two-bottom-layer ground plane (M1 and M2). The tank inductance is about 50pH ($L_1 = L_2 \approx 25$pH) from an EM simulation. Spiral inductors (L_5 and L_6) are used to increase the inductance of the emitter chokes, which block the noise from the tail current source. The tail bias circuit makes a high impedance at twice the oscillation frequency and reduces the phase noise of the fundamental oscillator [22]. The floorplan of the VCO is shown in Fig. 3.3(a) and its die photo is in Fig. 3.3(b). The VCO occupies a small area of $160\mu m \times 300\mu m$ (including the output buffer and biasing circuit). Since three different inductors are located

in the compact area, so the mutual coupling can cause appreciable changes in the inductance values. The coupling coefficient, as well as the direction of the current, need to be taken into account. The entire structure is simulated using HFSS to accurately capture these effects. The above techniques are used to trade-off and produce the best compromise between low phase noise, wide tuning range, and high power efficiency.

3.2 Design Procedure

The design procedure of the Colpitts VCO is described below. This procedure can be applied to cross-coupled VCOs as well.

1. Make a unit cell of the transistor and extract parasitics. Find the optimum bias points depending on the gain performance (f_T, f_{max}) and the current consumption.

2. Check the quality factor and the capacitance ratio (C_{max}/C_{min}) of varactors with post-layout simulations. They depend on the length, width, and finger number of the varactors. Choose the inductor architecture (microstrip line, coplanar waveguide, etc.) and find the inductance and quality factor with EM simulations.

3. Based on the performance of transistor, varactor, and inductor, scale up the transistor and choose an optimum varactor size and an inductance value based on the desired quality factor, the target tuning range, and estimated transistor and parasitic capaci-

tance. The negative resistance should be enough to compensate the tank loss. (This step requires an iteration.)

4. The varactor and inductor (LC tank) should be laid-out in a compact area to reduce parasitics. Then, place transistors, considering the VCO floorplan. Extract and check if the transistor performance and parasitics match with those of the previous step. If not, go to the previous step and update estimates.

5. Simulate the overall performance and adjust sizes or parameters.

6. Add other components such as choke, biasing circuits, and output matching circuits. Consider mutual inductances among EM structures and check if the mutual inductance causes a frequency shift or any unwanted problems.

In practice, designers face difficulties in simulating millimeter-wave circuits. Simulations should be carefully set up because parasitics are hard to capture accurately at these frequencies. RF designers separately use a parasitic extractor (for transistors or capacitors) and an EM simulator (for inductors, transformers, or transmission lines). Because parasitic (mutual) inductances cannot be extracted without defining return paths, the result of the layout extraction cannot include all the parasitics correctly. Thus, the boundary between post-layout extraction and EM simulation should be properly defined to include parasitics. If possible, replace all active devices with ports and extract the entire EM structure. When performing post-layout extraction of the parasitic capacitance and resistance, only include

the transistors to avoid double counting the parasitics. This can be done by defining the layout as a black box and then replacing it with the EM simulation results. Most simulators can read in S-parameters directly, but for improved convergence, it may be necessary to convert the S-parameters to an equivalent circuit model.

3.3 Discussion on Figure-of-Merit

The important properties of VCO are the VCO frequency (f_{osc}), phase noise ($L\{f_{offset}\}$) measured at an offset of f_{offset}, output power (P_{out}), power dissipation (P_{diss}), and tuning range ($TR(\%)$), realized by varying the control voltage over the a given range (V_{tune}). In order to fairly compare the VCOs reported in the literature, several versions of figure-of-merit (FoM) have been developed. The FoM has become so important for for VCO publications that a FoM comparison table is now standard practice. However, several different versions of FoM can be found in the literature.

$$FoM_1 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{1mW}{P_{diss}} \tag{3.1}$$

$$FoM_2 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{P_{out}}{P_{diss}} \tag{3.2}$$

$$FoM_3 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{1mW}{P_{diss}} \cdot \left(\frac{TR(\%)}{V_{tune}}\right) \tag{3.3}$$

$$FoM_4 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{1mW}{P_{diss}} \cdot \left(\frac{TR(\%)}{10}\right)^2 \tag{3.4}$$

$$FoM_5 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{P_{out}}{P_{diss}} \cdot \left(\frac{TR(\%)}{10}\right)^2 \tag{3.5}$$

FoM_1 is the most widely used but it excludes the output power [23]. So, even if a VCO generates very little output power, it does not affect the FoM_1. It may be told that the output power is already considered in the phase noise, but the phase noise is determined by the LC tank swing, which should be distinguished with the output power. Although the tank swing is large, if the output buffer is improperly designed, the output power can be low. In addition, if the output power is low, then it needs more buffers and more power dissipation to meet system specifications because mixers, for example, require large LO power. Therefore, the output power (P_{out}) should be included.

Most VCO papers talk about power consumption of only the core LC tank. But the VCO is for both generating AC power and delivering it to other blocks. Thus, the P_{diss} should be the dissipation of the core and the buffer both. And the output power of the buffer should be P_{out} in the FoM. Thus the buffer design is also critical.

Lastly, the tuning range is one of the most important properties in VCO. Even though some systems do not need a wide range or only need to hit a single frequency, a

reasonable tuning range is still required because of large variation due to parasitics at the millimeter-wave frequencies. The tuning range is in a direct trade-off with other properties as mentioned earlier. $FoM_3 - FoM_5$ include the tuning range (TR) and FoM_3 even takes V_{tune} into account [24]. But the control voltage range (V_{tune}) is not in a direct trade-off relationship as other parameters and so FoM_5 is chosen for this work.

Chapter 4

W-Band Phase-locked Loop

The frequency synthesizer architecture is selected as the PLL using a fundamental VCO in Chapter 2. The fundamental VCO is discussed in the previous chapter. This chapter describes the PLL architecture and the building blocks [9]. The PLL uses a traditional third-order loop filter and an integer-N divider chain as shown in Fig. 4.1. Generally a crystal oscillator is used for the reference input, but in this work it is assumed that an off-chip 3GHz frequency synthesizer is available in the imaging system. A higher reference frequency is preferred in order to attenuate reference spurs and to reduce the number of dividers. Also, to sharpen the clock transition, an input divider is put before the phase detector (PD) and frequency detector (FD). As such, the reference input frequency of the PLL is 1.5GHz and the division ratio (N) is 64.

As mentioned in the previous chapter, the VCO varactors are partitioned into two banks which are driven by two analog control voltages, $V_{c,coarse}$ and $V_{c,fine}$, respectively. The

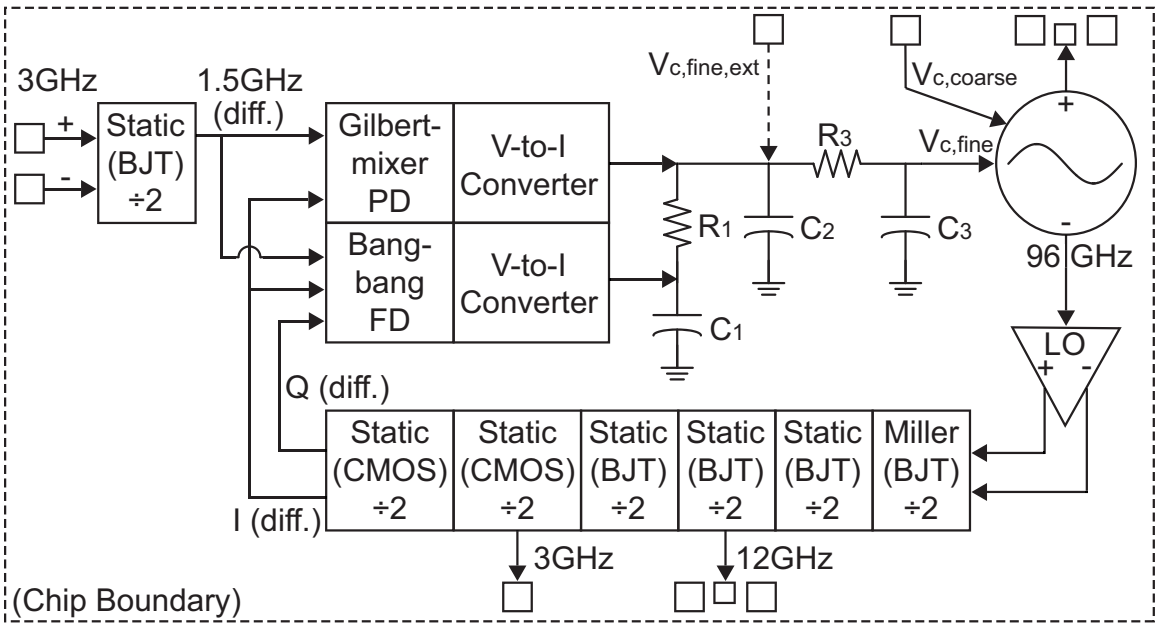
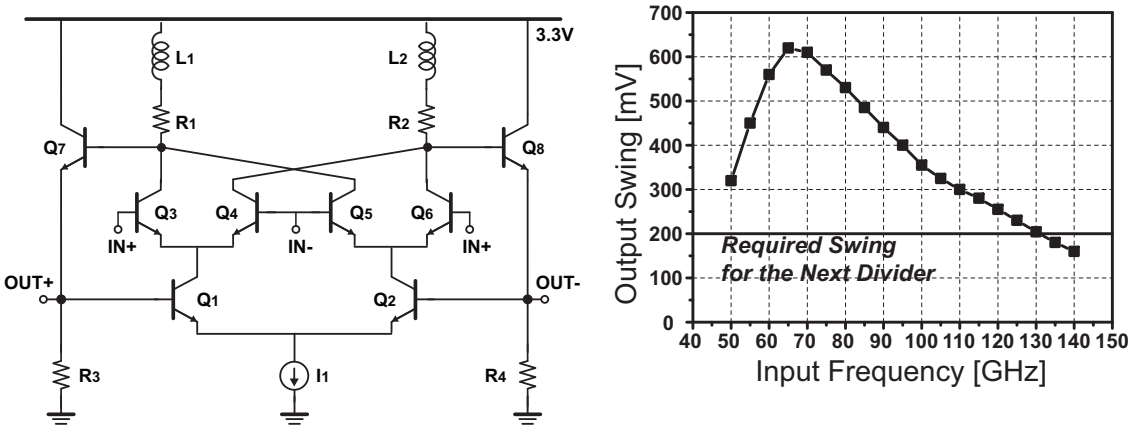


Figure 4.1: Block diagram of the stand-alone phase-locked loop.

$V_{c,fine}$ comes from the loop filter or from the outside, and the $V_{c,coarse}$ is externally set for the frequency band. In this way, the free-running VCO can also be measured with the same chip by turning off the PD and FD and by driving the two control voltages externally. For testing, the three outputs are brought to pads, f_{VCO}(96GHz), $f_{VCO}/8$(12GHz), $f_{VCO}/32$(3GHz). The RF GSG pads are used for 96GHz and 12GHz outputs and can be probed on wafer directly.

4.1 Divider Chain

The frequency architecture chosen in Chapter 2 requires the first-stage frequency divider running at the VCO frequency. It is also challenging to make a frequency divider at such high frequencies efficiently and reliably. At the millimeter-wave frequencies, three popular



(a) (b)

Figure 4.2: Miller divider. (a) Schematic. (b) Simulated output swing and the input frequency (with an input power of −1dBm.

divider topologies are the injection-locked divider, the Miller divider, and the static CML divider [10]. It is known that the injection-locked divider can operate at the highest frequency among them. But the locking range is generally narrow and the frequency band should be switched depending on variations. In addition, the static divider can achieve a wide operating range but it is power-hungry at 96GHz. For these reasons in this work, a W-band and wide-range Miller divider is implemented. Fig. 4.2(a) displays the schematic of the Miller divider. The input clock feeds the top transistors ($Q_3 - Q_6$) to reduce the input capacitance and shunt-peaking inductors (L_1 and L_2) are used to enhance the operation range of the divider. As shown in Fig. 4.2(b), from 50GHz to 130GHz with −1dBm input differential power, the divider can generate a worst case output swing of 200mV, enough to drive the next-stage divider in post-layout simulation. This is sufficient to cover the whole W-band frequencies ($75 - 110$GHz). Also this divider occupies a small area of $110\mu m \times 40\mu m$. The divider chain

is composed of six stages including the first-stage Miller divider as in the PLL block diagram (Fig. 4.1). The static CML BJT dividers are used for the next three stages, and static CML CMOS dividers are used for the last two stages.

4.2 Phase Detector

A Gilbert-mixer analog PD is selected to attenuate reference spurs and to solve the dead-zone problem [10], [25], [26]. The gain of this analog PD is high and linear in the vicinity of locking. Also, the output current of the V-to-I converter is continuous and no pulse is generated at the reference clock rate. Thus, the dead-zone problem does not occur. Moreover, when locked, the PD output is ideally at twice the reference frequency only. This can be rejected by the loop filter and reference spurs can be significantly suppressed. On the contrary, the standard XOR PD generates a reference spur because the XOR PD output has a strong reference component (also at the second harmonic) which leaks into the loop filter and the VCO control voltage. To reject the reference spur, the loop bandwidth should be lowered, but doing so significantly increases the noise contribution of the VCO.

The schematic of the mixer-type PD is illustrated in Fig. 4.3(a) and that of the unit V-to-I converter is in Fig. 4.3(b). The nominal K_{PD} is about 2mA/rad and can be varied by changing both the PD output swing and the transconductance of V-to-I converter. Note that the V-to-I converter remains on when the loop is locked, which results in higher noise contribution to PLL in-band noise. To reduce such noise contribution, a PMOS with larger

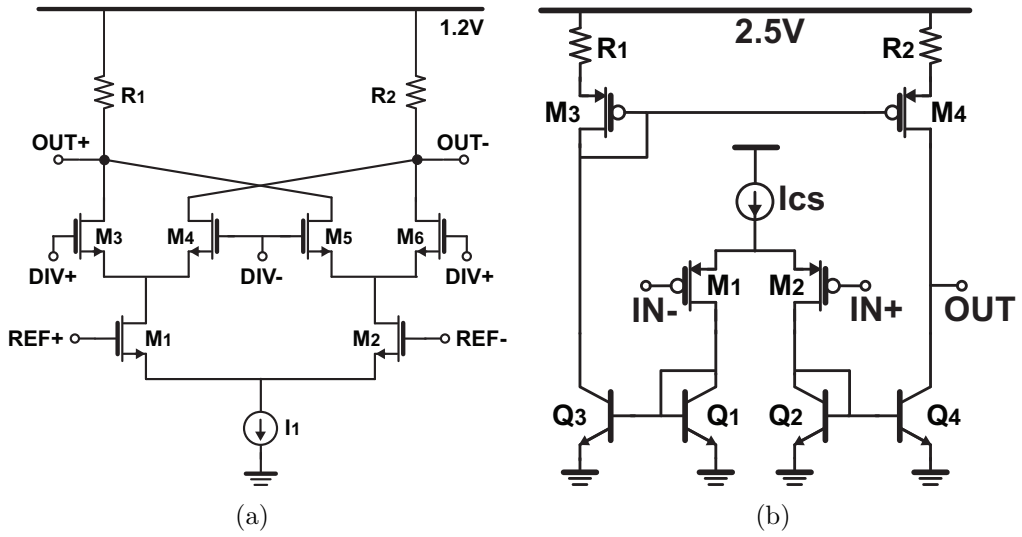


Figure 4.3: (a) Schematic of the phase detector (PD). (b) Schematic of the unit V-to-I converter of the PD.

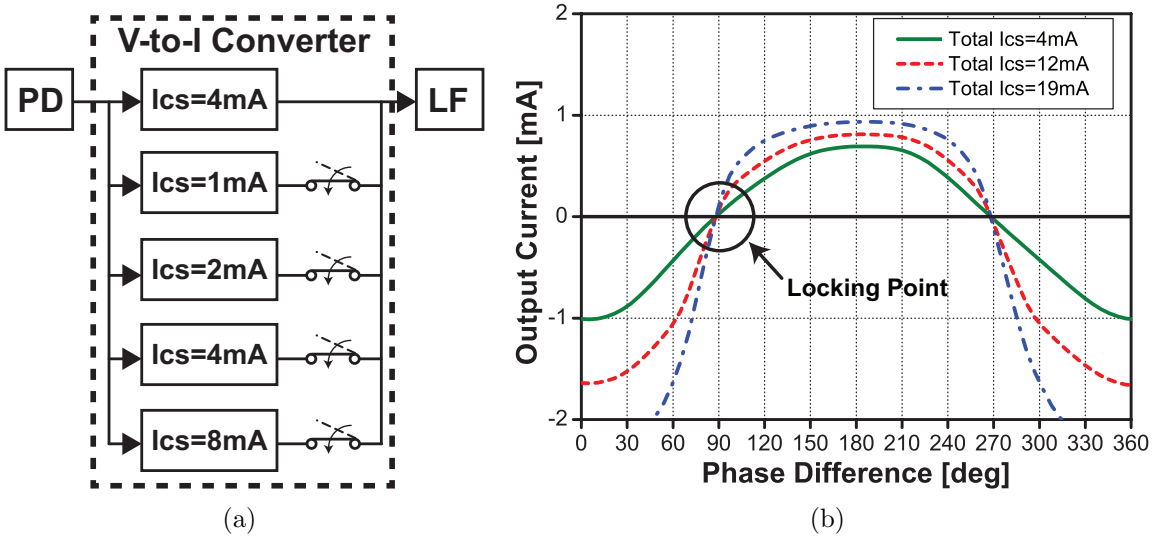


Figure 4.4: (a) Structure of the PD and V-to-I converter. (b) Simulated K_{PD}.

channel length and NPN bipolar transistors are used in the V-to-I converter. To increase the output impedance and to reduce the noise contribution, the degeneration resistor is used in the PMOS side. Fig. 4.4(a) shows how the K_{PD} can be adjusted to change the overall loop

gain and phase margin. The five scaled blocks are connected in parallel and the switches turn off blocks selectively, allowing the source current (I_{cs}) of the V-to-I converter to vary from 4mA to 19mA. The output current of the V-to-I converter is simulated with different source currents as shown in Fig. 4.4(b), showing that K_{PD} can be varied from 0.8 to 3.5mA/rad.

4.3 Frequency Detector

The frequency detector is used to widen the frequency acquisition range of the PLL. If the divided frequency is the same as the reference frequency, then this FD should be turned off and it does not disturb the phase locking behavior. In this PLL, the bang-bang FD is employed and schematically shown in Fig. 4.5(a) [26]. The corresponding V-to-I converter is shown in Fig. 4.5(b). Both the FD and the converter are completely off when the frequency is locked.

4.4 Loop Parameters

The component values of the loop filter are $R_1 = 500\Omega$, $C_1 = 150pF$, $C_2 = 7.2pF$, $R_3 = 1k\Omega$, and $C_3 \approx 100fF$ in Fig. 4.1. The zero frequency is about 2MHz and the pole frequency is 46MHz so the loop bandwidth is around 20MHz. With $N = 64$ and $K_{VCO} = 2.5GHz/V$ from simulation, K_{PD} can be adjusted to ensure the loop stability as shown in 4.4(b).

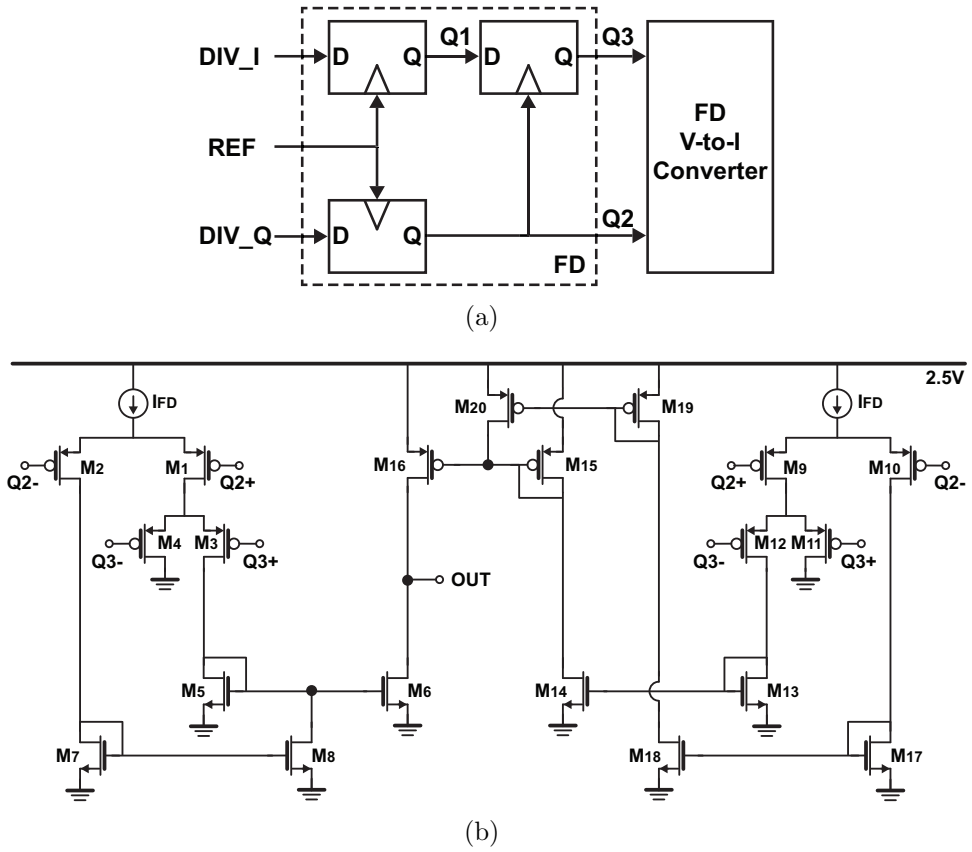


Figure 4.5: (a) Schematic of the bang-bang frequency detector (FD). (b) Schematic of the V-to-I converter of the FD.

4.5 LO Buffer

In Fig. 4.1, there is a single-to-differential buffer between the VCO and the first-stage divider. While a passive balun is enough to drive the Miller divider, the LO buffer is used for signal distribution of the system as shown in Fig. 2.2. This LO buffer is composed of an input passive balun and a following differential cascode amplifier as described in Fig. 4.6. Its simulation results are in Fig. 4.7, the small-signal gain is about 10dB and OP_{1dB} is 2dBm in simulation. Its input is matched to 50Ω and its output impedance is differentially 100Ω

(Each output is 50Ω.). Since other blocks can have the same characteristic impedance (for example, 50Ω), this LO buffer can be useful for LO distribution.

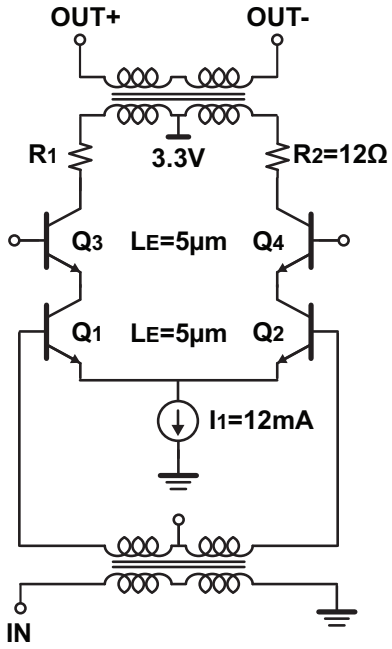
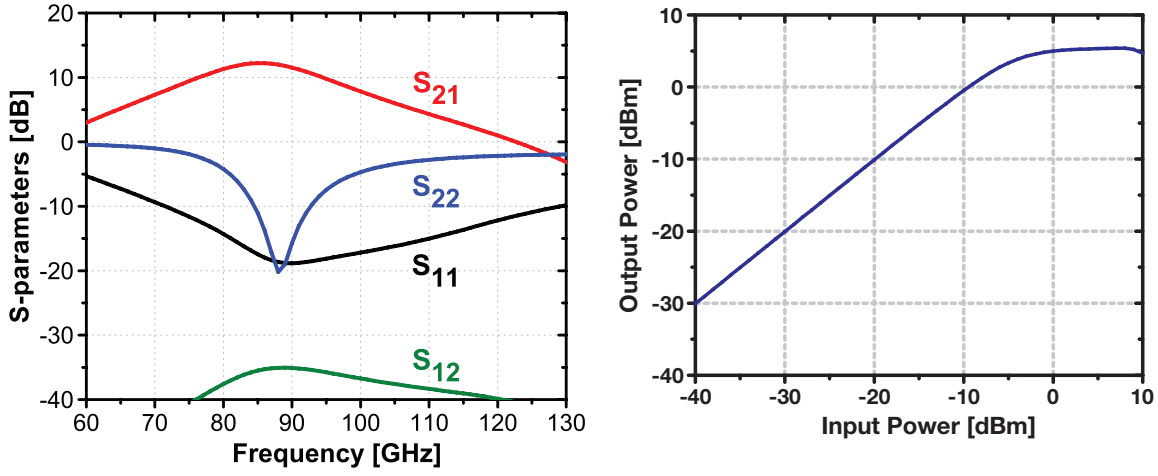


Figure 4.6: Schematic of the LO buffer.



(a) (b)

Figure 4.7: Simulation results of the LO buffer. (a) S-parameters. (b) Large signal simulation.

Chapter 5

LO Distribution

In the millimeter-wave circuit design, the chip floorplan can significantly affect the layout and design of sub-blocks. Especially, LO distribution part is usually implemented after other parts (TX and RX) are designed because it depends on the VCO output power, the power required by TX or RX, and how many blocks need the LO signal. Sometimes LO distribution blocks may burn more DC power than the power budget to meet the power requirements. Thus it is important to know the performance of the LO distribution components and to apply it into the high-level design. There are several components which are widely used for the LO distribution.

1. Transmission line: Typically implemented lines on silicon are the microstrip line, coplanar waveguide, and so on. Each transmission line is characterized by the four parameters (Z, λ, Q_L, Q_C) depending on the geometry [27], but in a high-level design it

is sufficient to have the characteristic impedance (Z) and the line loss (dB/100μm). From the chip floorplan, the length of the transmission line can be estimated, and the loss should be taken into account properly.

2. Power divider: It is useful to split one LO signal and to deliver the LO to many other blocks. For example, the Wilkinson divider is used to split the LO signal in phase and to isolate two outputs in the phased-array system [2]. The divider loss is around 1dB (technology dependent).

3. Passive balun: Often employed for the conversion from a single-ended signal to a differential signal or vice versa. The transformer can be made small with one turn at millimeter-wave frequencies. But it should be matched or loaded well to balance the differential output. Typical insertion loss is roughly 1dB (technology dependent).

4. Active balun: Used to amplify the input signal and to convert it to the differential output. There is no loss, but it needs the DC power and the linearity can be an issue. The input LO signal is a large signal, hence the second harmonic and the third harmonic can be generated through the active balun. If these harmonics affect the mixer performance or the overall system performance, then those harmonics should be attenuated and an additional filter may be required.

5. Quadrature hybrid: Commonly used in systems needing quadrature up/down conversion. There is a trade-off between using a QVCO and using a quadrature hybrid, and

the trade-off is well described in [17]. For the hybrid on silicon, using transmission lines and lumped capacitors is typical for area reduction, and lumped transformer based hybrids are even smaller [2].

If all the above blocks have the same impedance, then the LO distribution will be like assembling blocks. The VCO output power and the LO signal power required by TX or RX as well as the gains or losses of the distribution components are given by circuit simulations. Also it is important to know performance changes due to PVT variations and mismatch. Then it is straightforward to design and implement the LO distribution part. In this work, all the single-ended input/output impedances of the VCO, LO buffer, and the first-stage divider are matched to 50Ω and so the LO distribution can be scalable with 50Ω transmission lines. The choice of transmission line impedance is discussed in more detail in [1]. In Fig. 2.2, the input and output impedance of the hybrid are 50Ω, and TX PA input and RX mixer LO input are matched to 50Ω, thus making the LO distribution simple and easy.

Chapter 6

Experimental Results

The prototype PLL is fully integrated in 0.13μm SiGe BiCMOS process [18]. The die photo is shown in Fig. 6.1 [9]. The PLL occupies $0.85mm \times 1.1mm$ including pads, the VCO and loop filter occupy $160\mu m \times 300\mu m$ and $240\mu m \times 180\mu m$ respectively, and the actual area of the PLL is about $0.3mm^2$. Fig. 6.2 illustrates the measurement setup. On-wafer probing can be performed with a chip-on-board assembly setup. When the VCO output is measured, the output GSG pad is probed on wafer with a W-band probe, down-converted by an external mixer (Millitech MXP-10), and then measured with the Agilent E4440A spectrum analyzer or the Agilent 86100C sampling oscilloscope. For the 12GHz output, a V-band probe is used and the external mixer is not needed. The PLL reference clock is fed by the Agilent E8267D signal generator. Batteries and off-chip regulators are used for low noise supplies.

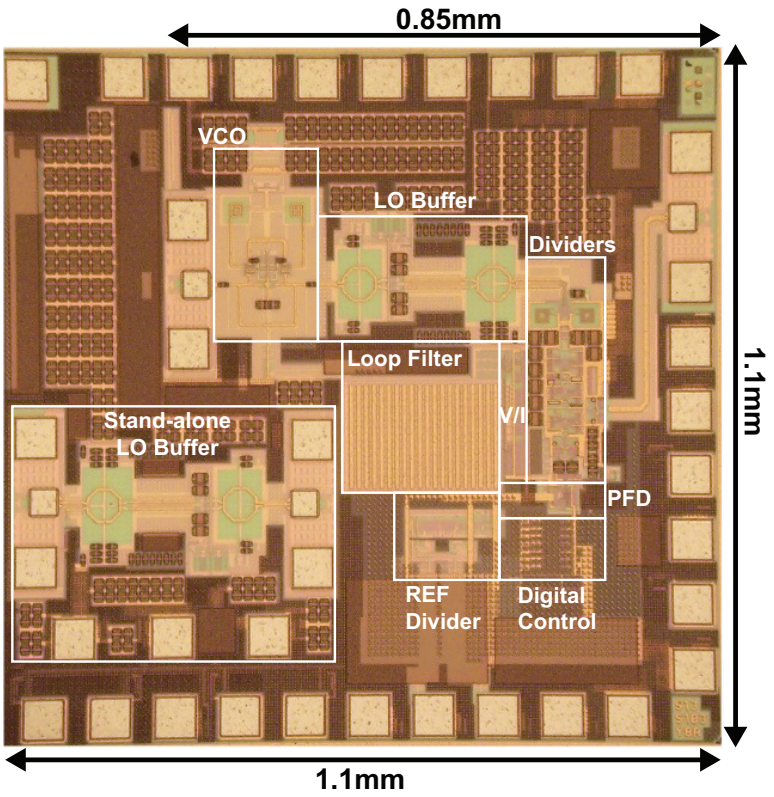


Figure 6.1: Die photo of the PLL chip.

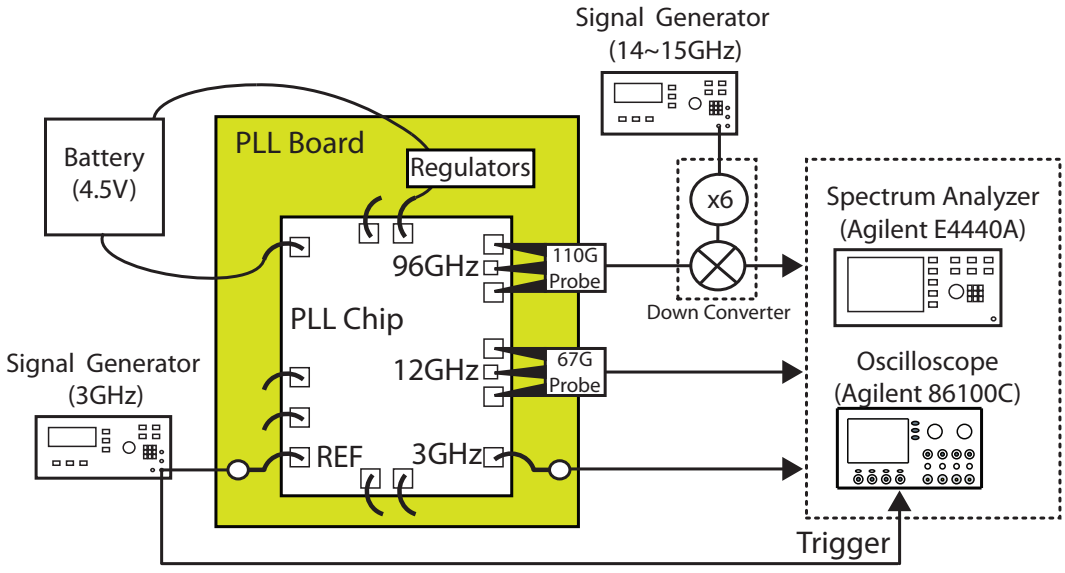


Figure 6.2: Setup for measuring the output spectrum and jitter.

6.1 Free-Running VCO

Fig. 6.3 and 6.4 shows the measurement results of the free-running VCO [9]. The VCO frequency ranges from 92.5 to 100.5GHz by tuning both the two control voltages, $V_{c,coarse}$ and $V_{c,fine}$, without altering the supply voltage or bias points. This indicates that the VCO tuning range is about 8.3%. The whole frequency range is overlapped by changing the $V_{c,coarse}$ because the varactor size connected to $V_{c,coarse}$ is twice larger than that connected to $V_{c,fine}$ as in Table 3.1. From Fig. 6.3, the K_{VCO} is about 2.5GHz/V when $V_{c,fine}$ is 1.25V. The VCO (pre-calibrated) single-ended output power is -12dBm at 92.7GHz as shown in Fig. 6.4. After the overall loss of a W-band probe, W-band cables, waveguides, and the down-converter are calibrated, the (post-calibrated) single-ended output power is 3dBm. At the maximum frequency, 100.5GHz, the single-ended output power is about 0dBm. The phase noise of the free-running VCO measured at 92.7GHz is -102dBc/Hz at 1MHz offset and -124.5dBc/Hz at 10MHz as shown in Fig. 6.4. The tail current is 24mA and the resistor bias current is 3.3mA with 3.3V supply voltage, consuming a DC power of 90mW. Moreover, the output buffer and the VCO core share the same current so additional power consumption is not required. The performance of this VCO is summarized and compared with those of published $90-100$GHz VCOs in Table 6.1. For fair comparison, Equations 3.2 and 3.5 are used, as discussed in Chapter 3. This VCO has the highest FoM among $90-100$GHz VCOs, while the tuning range is 8.3% so it shows a record phase noise performance. As expected, the FoM including tuning range (FoM_5) shows this design to be favorable.

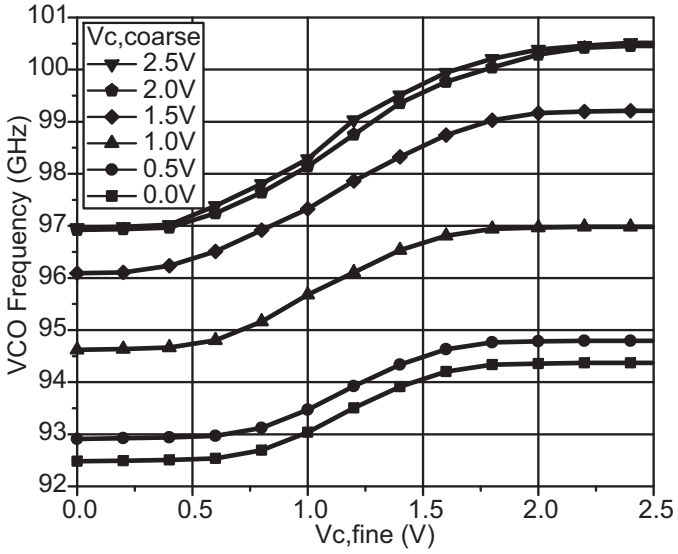


Figure 6.3: Measured tuning range of the free-running VCO.

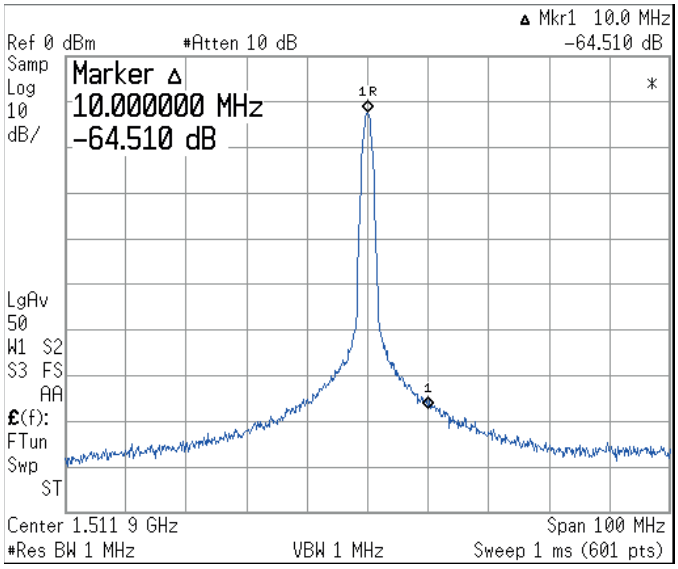


Figure 6.4: Measured output spectrum of the free-running VCO (indicating the phase noise of -124.5dBc/Hz at 10MHz offset).

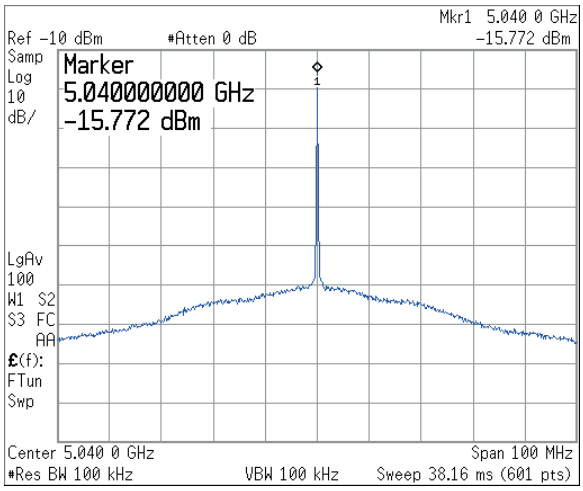
Table 6.1: VCO Performance Summary and Comparison

	[28]	[23]	[20]	This Work
Technology	0.18μm SiGe	0.13μm SiGe	0.35μm SiGe	0.13μm SiGe
Frequency [GHz]	$95.2 - 98.4$	$104 - 108$	$69 - 92$	$92.5 - 100.5$
Tuning Range (TR) [%]	3.3	4	29	8.3
V_{tune} [V]	$-5 \sim 0$	$0 \sim 2.5$	$1 \sim 9$	$0 \sim 2.5$
Phase Noise @1MHz [dBc/Hz]	-85	-101.3	-97	-102
Phase Noise @10MHz [dBc/Hz]	-	-	-	-124.5
Differential Output Power [dBm]	-5.6	2.5	12	6
Power Consumption [mW]	61	133	244	90
Supply Voltage [V]	-5	2.5	5	3.3
Area [mm^2]	0.55×0.45	0.1×0.1	-	0.16×0.3
FoM_2 [dBc/Hz]	161.4	182.9	183.3	190.3
FoM_5 [dBc/Hz]	151.8	174.9	192.6	188.7
$FoM_2 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{P_{out}}{P_{diss}}$ $FoM_5 = \left(\frac{f_{osc}}{f_{offset}}\right)^2 \cdot \frac{1}{L\{f_{offset}\}} \cdot \frac{P_{out}}{P_{diss}} \cdot \left(\frac{TR(\%)}{10}\right)^2$				

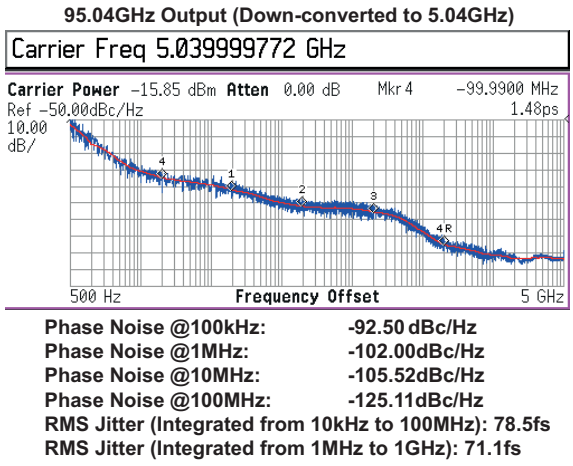
6.2 PLL

The total locking range of this PLL is from 92.7 to 100.2GHz with varying $V_{c,coarse}$ continuously, without changing bias points of the building blocks [9]. If the bias points of the VCO are adjusted, then the range can be shifted up or down by over 1GHz. The locking range is slightly narrower than the tuning range of the free-running VCO because the PLL fails to lock in low-K_{VCO} regions. The locking range is 1.7GHz when the $V_{c,coarse}$ is fixed at 0V and 3GHz when the $V_{c,coarse}$ is fixed at 2.5V. The PLL output power is larger than 0dBm over all the locking range. The output spectrum of the VCO output (95.04GHz, down-converted to 5.04GHz) is shown in Fig. 6.5(a). These plots reveal that the loop bandwidth is about 20MHz and that reference spurs are not observable ($<-60dBc$). The PLL output phase noise values are −92.5dBc/Hz, −102dBc/Hz, −105.5dBc/Hz, and −125dBc/Hz at 100kHz, 1MHz, 10MHz, and 100MHz offset frequencies respectively as in Fig. 6.5(b). The spectrum of the PLL divider output (95.04GHz/8=11.88GHz) is shown in Fig. 6.6(a). These plots also reveal that the loop bandwidth is about 20MHz and that reference spurs are not observable. The PLL divider output phase noise values are −110dBc/Hz, −119.7dBc/Hz, −119.5dBc/Hz, and −131dBc/Hz at 100kHz, 1MHz, 10MHz, and 100MHz offset frequencies respectively as in Fig. 6.6(b). There is about 18dB (=20log8) difference between the 95.04GHz spectrum and the 11.88GHz spectrum as expected. From the measured spectrum, the RMS jitter (integrated from 1MHz to 1GHz) of the 95.04GHz output is 71fs and that of the 11.88GHz output is 192fs. Fig. 6.7 shows the RMS jitter of the 11.88GHz output is

805fs, measured over one minute with the Agilent 86100C sampling oscilloscope. The total DC power consumption is 469.3mW and the power consumption of each building block is shown in Table 6.2. Table 6.3 summarizes the PLL performance and compares it with other similar works. To date, this is the highest frequency fundamental-mode PLL and the lowest phase noise fully integrated millimeter-wave PLL realized in silicon technology.

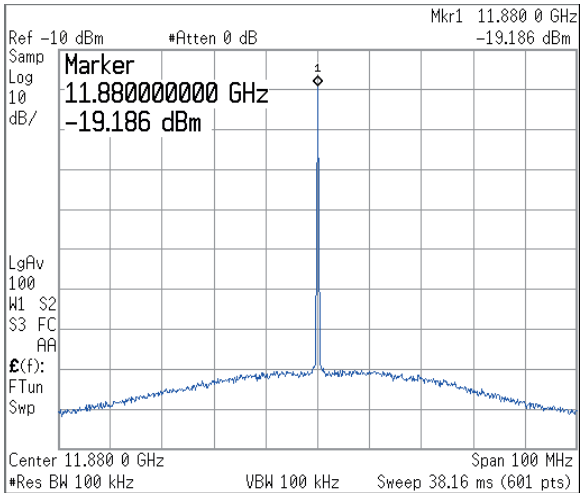


(a)

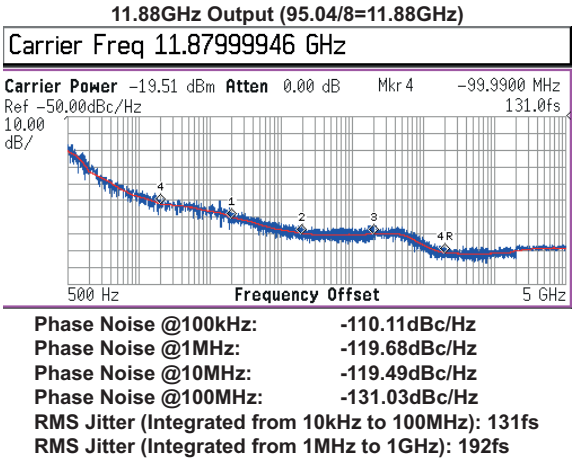


(b)

Figure 6.5: Measured output spectra of the PLL (95.04GHz is down-converted to 5.04GHz). (a) The spectrum. (b) Phase noise values.



(a)



(b)

Figure 6.6: Measured output spectra of the PLL divider (95.04GHz/8=11.88GHz). (a) The spectrum. (b) Phase noise values.

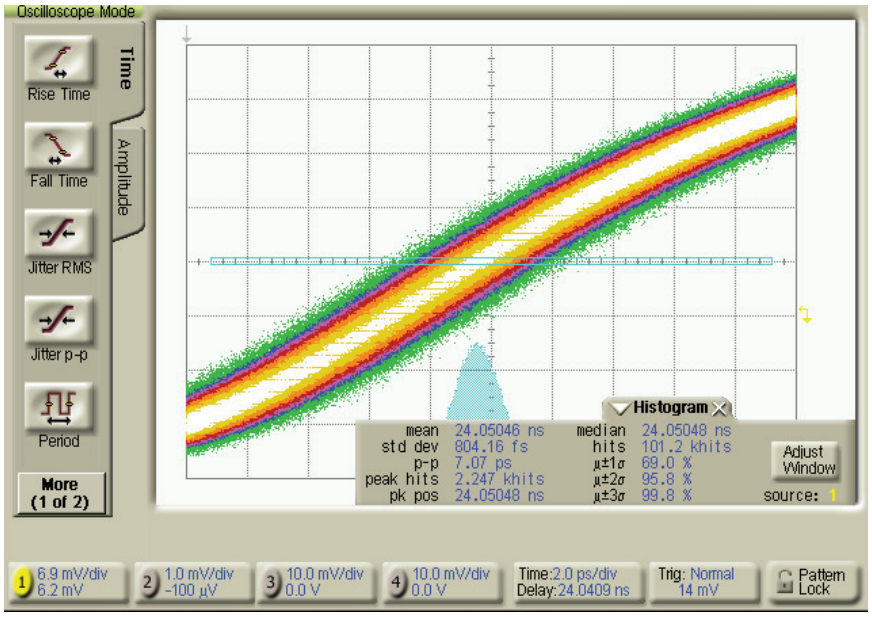


Figure 6.7: Measured jitter of the PLL divider output (11.88GHz).

Table 6.2: Power Breakdown of the PLL

	Supply Voltage	Current (including biasing)	Power Dissipation	Percentage
VCO	3.3V	27.3mA	90.1mW	19.2%
LO Buffer	3.3V	14mA	46.2mW	9.8%
Miller Divider	3.3V	21mA	69.3mW	14.8%
BJT Dividers and Buffers	3.3V	58mA	191.4mW	40.8%
CMOS Dividers and Buffers	1.2V	3mA	3.6mW	0.8%
PD	1.2V	2.5mA	3.0mW	0.6%
V-to-I Converter (PD)	2.5V	10mA	25.0mW	5.3%
FD	1.2V	1mA	1.2mW	0.3%
V-to-I Converter (FD)	2.5V	1mA	2.5mW	0.5%
Input Divider and Buffer	2.5V	10mA	25.0mW	5.3%
Other Biasing Circuits	1.2V	10mA	12.0mW	2.6%
Total			469.3mW	100%

Table 6.3: PLL Performance Summary and Comparison

	This Work	[11]	[12]	[14]	[16]	[16]
Architecture	A (Fig. 2.1(a))	A (Fig. 2.1(a))	A (Fig. 2.1(a))	B (Fig. 2.1(b))	C (Fig. 2.1(c))	D (Fig. 2.1(d))
Technology	0.13μm SiGe	0.13μm SiGe	65nm CMOS	0.13μm CMOS	0.18μm SiGe	0.18μm SiGe
Frequency [GHz]	92.7–100.2	86–92	95.1–96.5	91.8–101	90.9–101.4	92.8–98.1
Locking Range [%]	7.8	6.7	1.5	9.5	10.9	5.5
Phase Noise @1MHz	−102dBc/Hz	−100dBc/Hz	−76dBc/Hz	−72dBc/Hz	−92dBc/Hz	−93dBc/Hz
RMS Jitter [fs]	71.1(2.4°) (1)	119(4.3°) (1)	-	-	159(5.5°) (2)	156(5.4°) (2)
Reference Spur [dBc]	< -60	-	−51.8	$-40 \sim -27$	−52	−54
Output Power [dBm]	3	−3	−26.8	$-31 \sim -22$	−11	−7
DC Power [mW]	469.3	1150	43.7	57	140	140
Supply Voltage [V]	3.3, 2.5, 1.2	2.5, 1.8	1.3, 1.2	1.5, 0.8	2.5, 1.8	2.5, 1.8
Division Ratio	64	16	256	512	256	256
Area [mm^2]	0.93	1.87	0.7	0.87	1.9	1.8

(1) Integrated from 1MHz to 1GHz

(2) Integrated from 100kHz to 100MHz

Chapter 7

Conclusion

It is challenging for an on-chip frequency synthesizer to have high power efficiency, spectral purity, and frequency tunability, especially at the millimeter-wave frequencies. This report presented design considerations and architectures pertinent to millimeter-wave frequency synthesizers. The design and requirements of the LO generation and distribution have also been highlighted. While the four discussed synthesizer architectures are all widely used in millimeter-wave systems, the VCO/divider selection is guided by system specifications and process technology. In this work, a PLL using a fundamental VCO is chosen for the medical imaging system and is fully implemented in silicon. The fundamental VCO achieved a tuning range of 8.3%, an output power of 6dBm, and a phase noise of -124.5dBc/Hz at 10MHz offset. The PLL can be locked from a range of $92.7 - 100.2$GHz and realizes a phase noise of -102dBc/Hz at 1MHz offset and a single-ended output power of 3dBm. Finally, this report contributes some insight to the design of the millimeter-wave LO generation and distribution.

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