

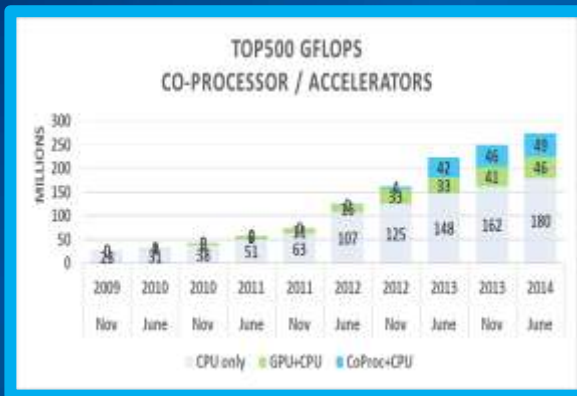
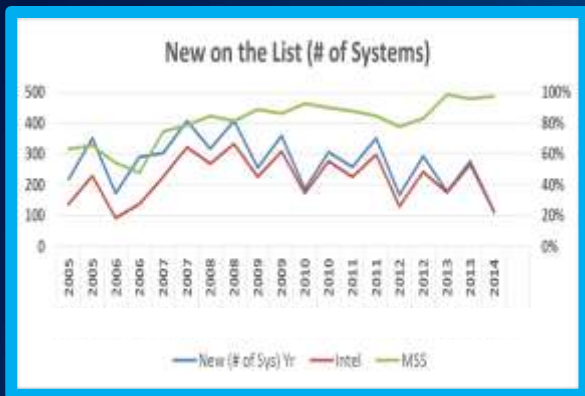
Accelerating Insights... **In the Technical Computing Transformation**

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June 2014



TOP500 Highlights



Intel® Xeon Phi™
in Jun'14 list

#1—TOP500 system

#1—Intel® Xeon Phi™ Total
Rmax > GPU's Total
Rmax

427 of 500 (85%) of all systems
111 of 114 (97%) of new systems

Use Intel processors

PRACE ISC Award—2014

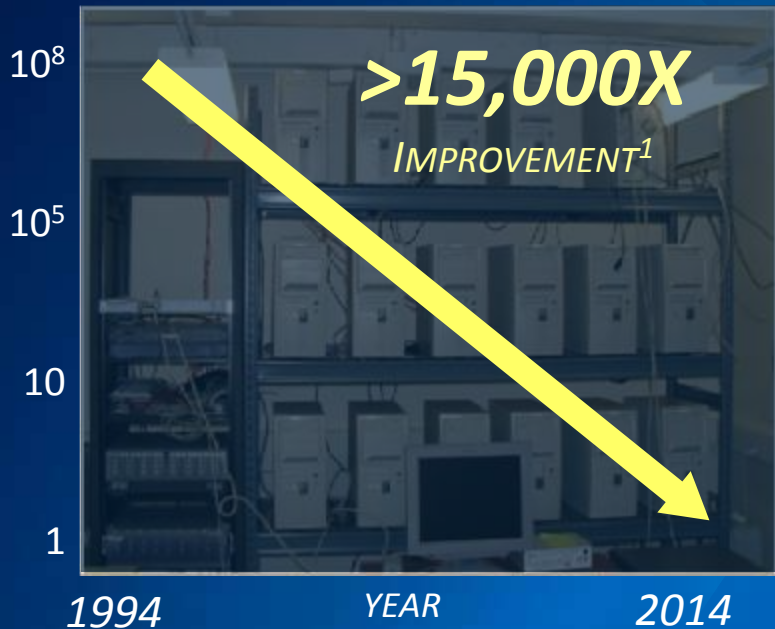
1st Sustained 1PFlop Real Science Performance on an IA-based System



The Democratization of HPC...

A 20 Year Retrospective

$\$/\text{FLOP}$



\uparrow **Beowulf Cluster**



Pioneering Science

High ROI Industry Innovations

¹Source: Intel per socket estimate comparing Intel DX4™ processor (Beowulf) versus Intel® Xeon Phi™ (Knights Corner)
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HPC's Next Stage

New Usages



3D Printing

New Access



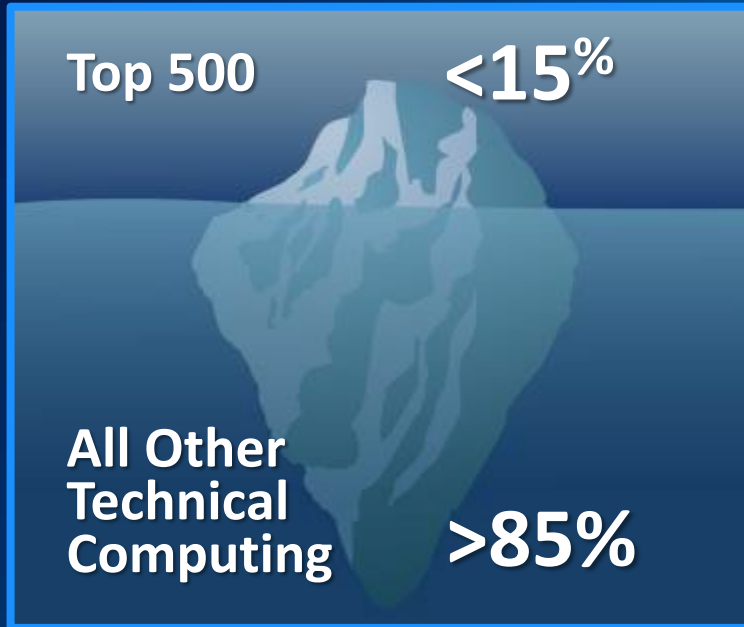
HPC Cloud Service

New Models



Crowdfunding

Technology Waterfalls from the Top



% of sockets sold

*Performance Waterfall**
#1 Top500 System to Single Socket

6-8 years

#1 to #500

~9 years

#500 to Single Socket

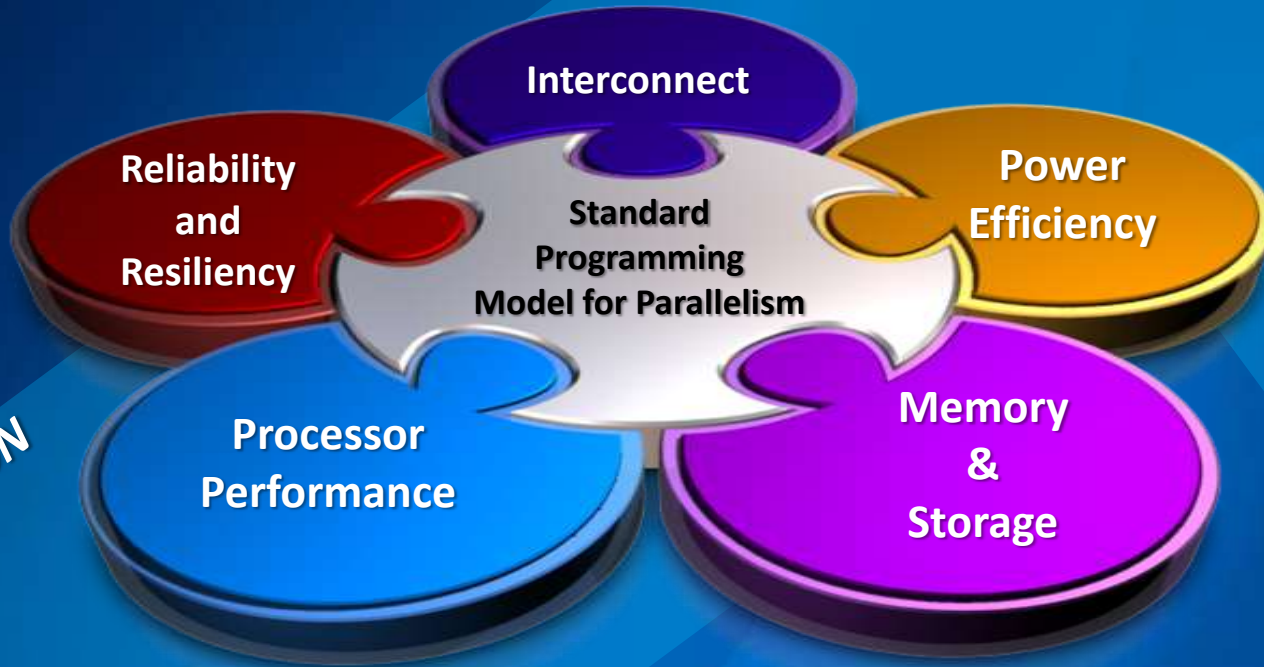
**plus.....similar waterfalls for other capabilities in areas like fabrics, storage, software, ...*

Source: Top500.org and Intel Estimate of Top500 sockets as % of sum of analysts reports of HPC and branded Workstations sockets. Performance waterfall timelines based on TOP500.org statistics (#1-#500) and Intel estimate (#500 to projected Intel Knights Landing)
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Unabated System Innovation ~~At~~ The Top

from



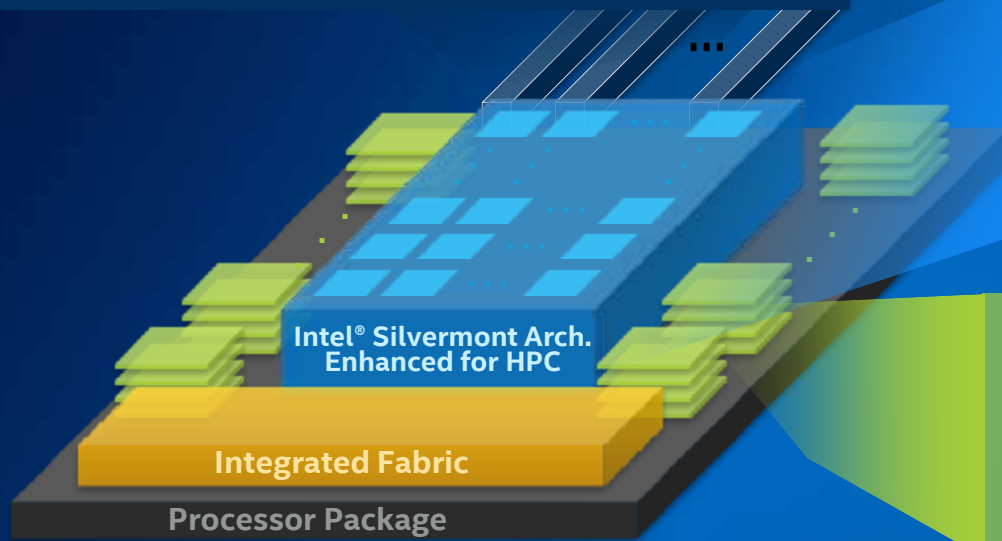
Unveiling Details of Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

★ 2nd half '15
1st commercial systems

★ 3+ TFLOPS¹
In One Package
Parallel Performance & Density

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors



Compute: Energy-efficient IA cores²

- Microarchitecture enhanced for HPC³
- **3X** Single Thread Performance vs Knights Corner⁴
- Intel Xeon Processor Binary Compatible⁵

On-Package Memory:

- up to **16GB** at launch
- **1/3X** the Space⁶
- **5X** Bandwidth vs DDR4⁷
- **5X** Power Efficiency⁶

Jointly Developed with Micron Technology

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. ¹Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle. FLOPS = cores x clock frequency x floating-point operations per second per cycle. ²Modified version of Intel® Silvermont microarchitecture currently found in Intel® Atom™ processors. ³Modifications include AVX512 and 4 threads/core support. ⁴Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner). ⁵Binary Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX). ⁶Projected results based on internal Intel analysis of Knights Landing memory vs Knights Corner (GDDR5). ⁷Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.



Conceptual—Not Actual Package Layout

Announcing

Intel® Omni Scale—The Next-Generation Fabric

- Designed for Maximum Scalability
- Rich Set of Programming Models
- Flexible Configurations
- End-to-End Solution

INTEGRATION

Intel® Omni
Scale Fabric



Starting with
Knights Landing

Intel® Omni
Scale Fabric



Future 14nm
generation

★ Coming in '15

✓ PCIe
Adapters

✓ Edge
Switches

✓ Director
Systems

✓ Intel Silicon
Photonics



✓ Open
Software
Tools*

Intel® True Scale
Fabric Upgrade
Program *Helps Your
Transition*

*OpenFabrics Alliance
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The Future Is Here

Knights Landing Supercomputer...the 1st of Many

**Announced
April '14**



System name: **Cori**

>9300 *Knights Landing nodes*



Next Generation Intel®
Xeon Phi™ Products
(Knights Landing)

“..a significant step in advancing supercomputing design toward *the kinds of computing systems we expect to see in the next decade as we advance to exascale.*”

Steve Binkley

*Associate Director of the Office of Advanced Scientific
Computing Research*

“Cori will provide a significant increase in capability for our users and *will provide a platform for transitioning our very broad user community to many core architectures.*”

*Sudip Dosanjh
NERSC Director*



AMBER WRF VISIT VASP UTBENCH SU2 SG++ SeisSol, GADGET, SG++ ROTOR SIM R Quantum Espresso Optimized integral OPENMP/ MPI Openflow NWChem

AVBP
(Large Eddy)

NEMO5

MPAS

Blast

Mardyn

BUDE

MACPO

CAM-5

Ls1

CASTEP

Harmonie

Castep

GTC

CESM

GS2

CFSv2

Gromacs

CIRCAC

GPAW

Modernizing Community Codes...*Together*

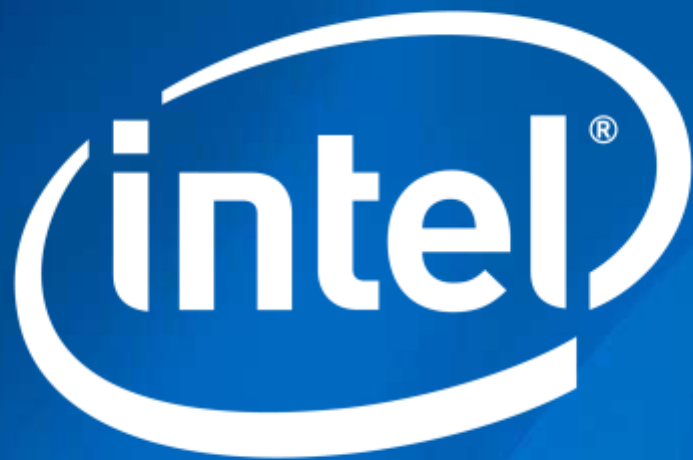
Intel® Parallel Computing Centers

CLiPhi
(COSMOS)

COSA Cosmos codes DL-MESO DL-Poly ECHAM6 Elmer FrontFlow/Blue Code GADGET GAMESS-US

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*Intel® Advanced Vector Extensions refers to Intel® AVX, Intel® AVX2 or Intel® AVX-512. For more information on Intel® Turbo Boost Technology 2.0, visit <http://www.intel.com/go/turbo>

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