ADF4351 uWave Local Oscillator

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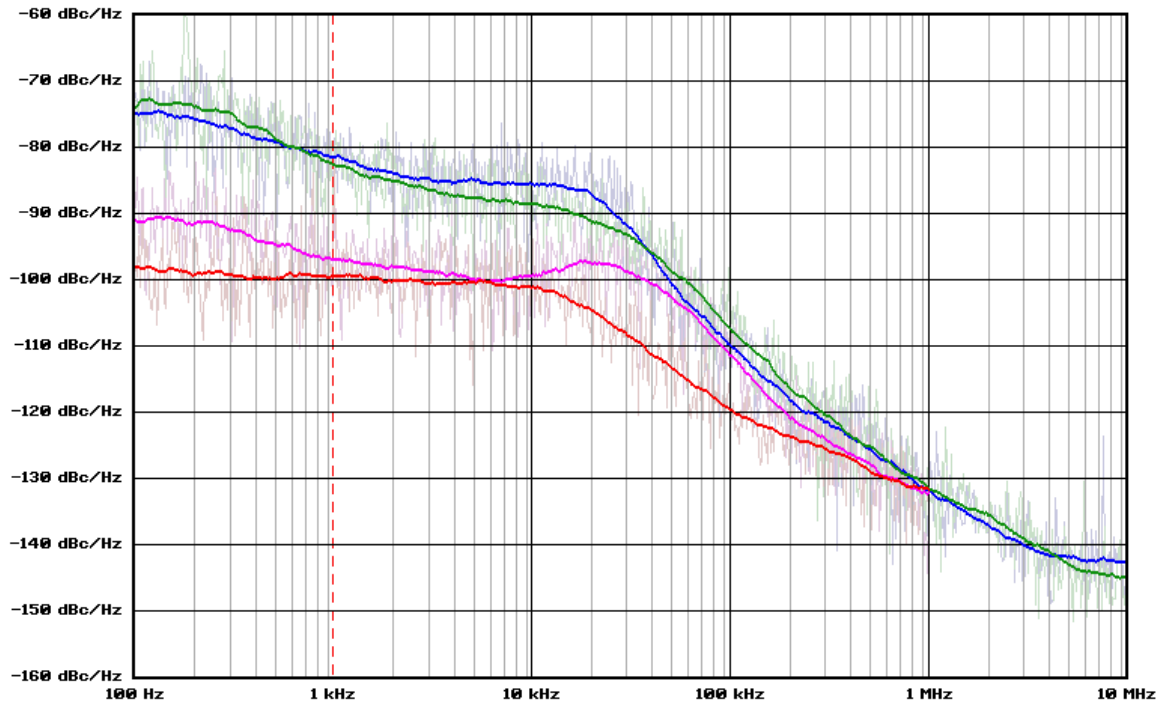
2 Specifications

Power Supply	+8v to +15v @ 200mA
Frequency Range	2200MHz to 4400MHz (fundamental) 31MHz to 2200MHz
Frequency Resolution	2200-4400MHz: 25 kHz 1100-2200MHz: 12.5 kHz 550-1100MHz: 6.25 kHz 275-550MHz: 3.125 kHz ...
Output Level	4 levels software selectable in 2dB steps: +5dBm, +3dBm, +1dBm, -1dBm
Size	65mm x 50mm
Stability	Internal Reference after 30 minute warmup: 1×10^{-10} External Reference: As per specification for external reference
Additional Features	Frequency Sweep @500 points/sec
Reference	• Internal 26MHz OCXO • External reference • Auto Selected reference

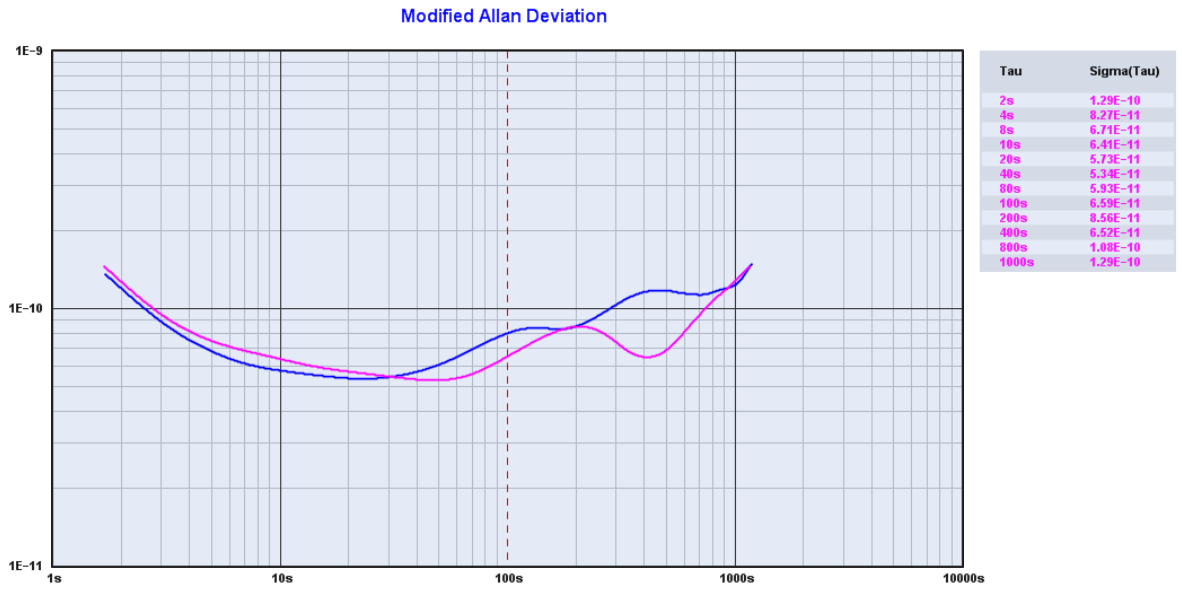
3 Performance

3.1 Phase Noise



Trace	Carrier Hz	Carrier dBm	dBc/Hz at 1000 Hz	RF Atten dB	Instrument
VK3XDK Agile PLL Ref=8566B 10MHz@1.8dBm	1 242 000 000	-2.50	-81.5	0	HP8566B
ADF4350 @1242MHz Fpd=26MHz	1 242 000 000	4.90	-96.8	0	HP8566B
ZL2BKC PLLv2 RF Port (RF1)	1 242 000 000	-1.10	-82.7	0	HP8566B
PN Baseline	100 000 000	-10.00	-99.4	0	HP8566B

3.2 Stability



Trace	Notes	Input Freq	Sample Interval	MDEV at 100s	Duration	Acquired	Instrument	Imported From
ZL2BKC PLLv3 vs 10811A Ref		4399.999988 MHz	1.690 s	8.08E-11	1h 0m 0s	2130 pts	HP5343A	
ZL2BKC PLLv3 vs 10811A Ref	Run 2	4399.999994999999 MHz	1.660 s	6.59E-11	1h 0m 1s	2169 pts	HP5343A	

4 Special Notes

For reliable operation both outputs need to be correctly terminated into 50Ω loads, otherwise instability can be experienced with certain frequencies. If an externbal load is not available the

supplied 50Ω 0603 resistor can be installed in location R2 or R18, and the corresponding 0Ω jumper in location LPF1 and LPF2 should also be removed.

It should also be noted that some from Chinese origins have been measured with a return loss of only 2dB at 3GHz!!!

5 Features

5.1 Frequency Multiplier Correction

When the LO is followed by a frequency multiplier, in particular when multiplying by an odd number, the resulting frequency may suffer from rounding errors resulting in a small frequency error in the final frequency.

In order to prevent oddball frequencies (eg with 0.3333333 MHz re-occurring) the correct procedure is to set the 'M' multiplier value to 3 and then program in desired frequency for the 3rd harmonic.

Example: Generate a Frequency of 10368.270 MHz for a beacon using the 3rd Harmonic

```
M 3
N 0.01
F 10368.280
S 0
```

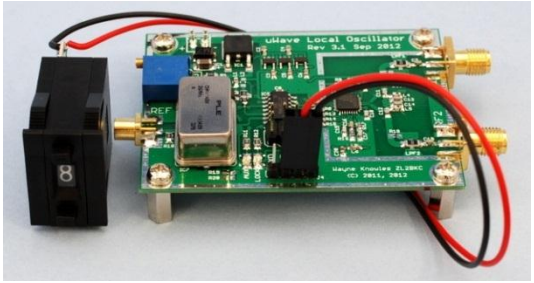
Without the multiplier setting the resulting frequency will be 20kHz higher.

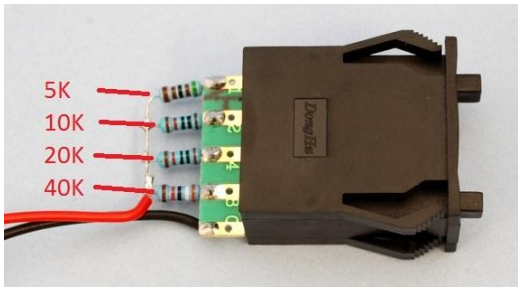
5.2 Channel Interface

A single wire interface is provided to switch between 16 preprogrammed channels (10 with a BCD thumbwheel).

The interface consists of a R ladder using 5k, 10k and 20k resistors. 5k is connected to the binary 1 leg of the BCD thumbwheel, 10k to the binary 2 and 20k to the binary 4 switch. See the photo below for the connections.

The thumbwheel is connected between ground and the CHAN port on connector J4. As an extra precaution it is recommended that a single ferrite bead be placed on the CHAN signal near the PCB to avoid any RF pickup that could lead to erroneous channel changes.





5.3 Programming

Programming can be done by connecting a **TTL** level RS232 interface onto the following pins of J4:

RXD, TXD, and GND

Baud rate: 9600 8 bits No Parity 1 stop bit

The interface levels are 3.3V but the protection circuits allow for 5V levels to also be connected without damage.

A suitable interface is a PL2303 based USB to RS232 converter, or a programming cable for a Yaesu FT8x7 transceiver.

The labeling of the pins on J4 assumes a DCE interface, thus the RXD pin is an input, and TXD is an output.

Use any terminal program, either TeraTerm, Putty or Hyperterm can be used.

```
uLO Universal Local Oscillator Rev3.1
(C)2012 W. Knowles, ZL2BKC
d
RF= 1152.000, L=3
Ref=   26.000, N=    0.025
ExtRef=   10.000
Params=23, CP=7

0 RF= 1152.000, L=3
1 RF= 1296.050, L=3
2 RF= 2400.050, L=3
3 RF= 3400.050, L=3
4 RF= 5760.050, L=3, M=3
5 RF=10368.050, L=3, M=3
6 RF=      NAN, L=3, M=63
7 RF= 1242.000, L=3
8 RF= 4400.000, L=3
9 RF=      NAN, L=3, M=63
10 RF=      NAN, L=3, M=63
11 RF=      NAN, L=3, M=63
```

```
12 RF=      NAN, L=3, M=63
13 RF=      NAN, L=3, M=63
14 RF=      NAN, L=3, M=63
15 RF=      NAN, L=3, M=63
```

5.4 Command Reference

Command	Units	
A 0		Enable onboard oscillator and select Internal frequency reference using the value set by the 'R' command.
A 1		External frequency reference as set by the 'E' command. Note: The internal reference oscillator is powered down
A 2		Force external reference. This option is available for > 20MHz reference or for low level reference that does not auto detect.
C *n*		Load frequency settings for channel *n*
D		Display frequency and channel settings
E *n*	MHz	External reference frequency in MHz
F *n*		Set Frequency
I *n*	MHz	Step size for sweep and increment functions
L *n*		Set output level L0 = -1 dBm L1 = +1 dBm L2 = +3 dBm L3 = +5 dBm
M *n*		Frequency Multiplier
N *n*	MHz	Synthesizer frequency resolution in MHz for the fundamental band.
P *n*		Set PLL parameters (see section below)
R *n*	MHz	Internal Reference frequency in MHz
S *n*		Save frequency, Multiplier and Level settings into channel n (N=0-15)
+		Add step (as set in S) to current frequency
-		Subtract step (as set in S) from current frequency

5.5 PLL Parameters

The 'P' command is used to override the PLL programming parameters.

The default value of 23 sets the correct charge pump current and ensures the LO is muted until it is fully locked. These parameters should not require changing under normal use.

Bits	Decimal	Purpose
0:3	7	Charge pump current (normally 7)

4	16	0 = Output always on 1 = Mute to Lock Detect
5	32	0 = Low Phase Noise mode 1 = Low Spur Mode
6	64	0 = Enable reference doubler for frequencies < 16MHz 1 = Disable reference doubler

6 Special Applications

6.1 Sweep Generator Mode

For experimental applications the PLL can be programmed to perform a frequency sweep with synthesizer accuracy. The ADF4350 is capable of moderately fast sweep speeds but the firmware currently forces a VCO calibration for each frequency change which currently limits the sweep speed to around 800 points per second.

Sweep operation starts when the following parameters are loaded: F (Start Frequency), G (End Frequency), I (Frequency Step) and T (Time per point in ms)

For example the following starts a sweep for tuning a 2 GHz filter:

```
F2200
G2500
I5
T1
```

At the start of each sweep the "CHAN" signal on J1 is toggled low at the start of the sweep, thus a scalar network analyzer can be realized by triggering an oscilloscope using this trigger signal and a diode detector can be connected to the A channel input.

Note: The sweep parameters cannot be saved permanently.

6.2 TX Offset

For some applications the LO frequency needs to be changed during transmit, for example generating a 20MHz repeater offset for a 1296 to 144MHz transverter.

When the TX line (shared with RS232 input) is pulled low the channel number is automatically increased by 8, or decreased by 8 for channels above 8.

6.3 Sharing LO between 2 Tranverters

In order to reduce construction costs and maximise the use of space many constructors opt to share a single LO across multiple bands. Given the PLL board contains 2 LO outputs there is a natural instinct to use these for driving multiple transverters

If the LO frequency requirement is different for each transverter the TX input can be dropped to a logic LOW which results in 8 being added to the channel number, where the different LO frequency has been setup.

Note: The interface is 3.3V logic with a pull-up to logic 1. In most cases a suitable interface circuit may need to be added externally using a NPN transistor or similar.

7 Experimental Options

7.1 Low Frequency operation

The ADF4350 and ADF4351 datasheets recommend different output inductors depending on frequency range. If you require a few more dB of output on the lower frequencies then the inductors L4 and L5 can be changed as follows:

Frequency Range	L4 and L5 Inductor Values
137 to 500MHz	100nH
500 to 1000MHz	47nH
1000 to 2000MHz	7.5nH
2000 to 4400MHz	3.9nH

As supplied a 3.9nH inductor is installed suitable for > 2000 operation, and replacement inductors are supplied if more output power is required on lower frequencies.

7.2 10MHz Filter Option

The external reference input at the PLL is a high impedance and extremely sensitive to external noise, or aliasing used on DDS reference. An optional 10MHz Xtal can be installed in location X1 if more filtering is required.

Note that the input resistor R10, 49.9Ω may be removed if a higher reference level is required and the reference is located nearby.

7.3 Low Pass Filter

When driving a frequency multiplier the LO harmonics generated are critical for producing a large signal after multiplication. However there are design applications where no multiplication is required and if there is insufficient filtering before the mixer this can result in unwanted images. For such applications a Minicircuits LFCN series Low Pass filter can be substituted with the 0Ω 1206 jumper installed in location LPF1 and LPF2.

7.4 Internal Oscillator Powerdown

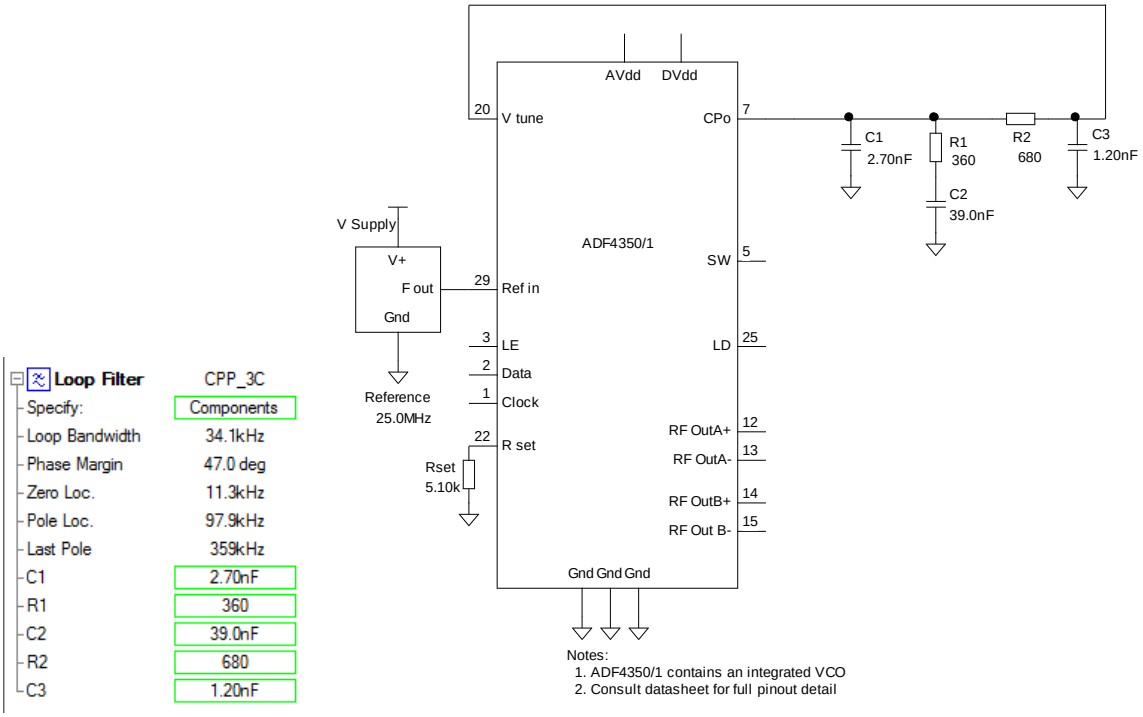
When an external reference is detected the internal oscillator is powered down for 2 reasons:

1. Power Reduction (saving approx. 50mA)
2. Reduce cross talk from internal oscillator which causes unwanted spurs

When the external oscillator is removed the internal reference needs starts from cold again and requires several minutes to warm-up (and 30 minutes to be completely stable). By installing a 0Ω jumper in location R6 the internal reference is never powered off.

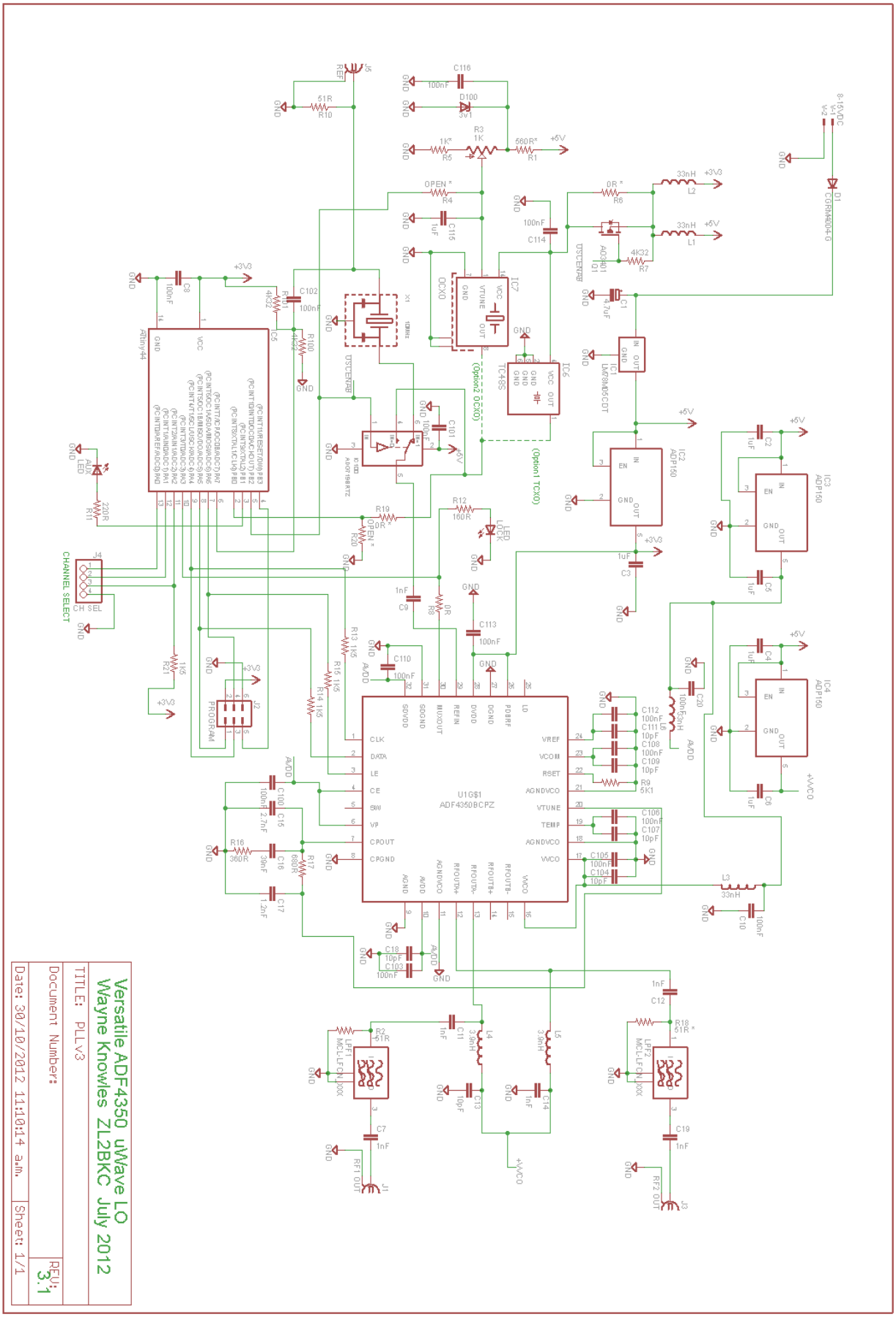
7.5 Loop Filter

The standard loop filter design has a bandwidth of 34kHz which offers a good compromise with phase noise, adjacent channel power and lock time. ADIsimPLL can be used to design alternative loop filters if one is willing to experiment using the following parameters as a starting point:



Loop Filter	CPP_3C
Specify:	Components
Loop Bandwidth	34.1kHz
Phase Margin	47.0 deg
Zero Loc.	11.3kHz
Pole Loc.	97.9kHz
Last Pole	359kHz
C1	2.70nF
R1	360
C2	39.0nF
R2	680
C3	1.20nF

8 Schematic


Versatile ADF4350 uWave LO
Wayne Knowles ZL2BKC July 2012
TITLE: PLLv3
Document Number:
REV: 3.1
Date: 30/10/2012 11:10:14 a.m.
Sheet: 1/1
ADF4350BCPZ
ATtiny44
DCXO
TCXO
CHANNEL SELECT
PROGRAM
LED LOCK
AUX LED