Adiabatic Technique for Energy Efficient Logic Circuits Design

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***Abstract*— The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation. With the help of TSPICE simulations, the energy consumption is analyzed by variation of parameter. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and 2:1 multiplexer circuits. It is find that adiabatic technique is good choice for low power application in specified frequency range.**

***Index Terms*— Adiabatic switching, energy dissipation, power clock, equivalent model.**

I. Introduction

THE term "adiabatic" describe the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event [1, 2].

Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component [1-5].

In conventional CMOS logic circuits (Fig.1), from 0 to V_{DD} transition of the output node, the total output energy $C_L V_{DD}^2$ is drawn from power supply. At the end of transition, only $\frac{1}{2} C_L V_{DD}^2$ energy is stored at the load capacitance. The half of drawn energy from power supply is dissipated in PMOS network (F). From V_{DD} to 0 transition of the output node, energy stored in the load capacitance is dissipated in the NMOS network (/F) [1].

Adiabatic logic circuits reduce the energy dissipation during switching process, and reuse the some of energy by recycling from the load capacitance [1, 2]. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal [6] or sinusoidal power supply voltage [7].

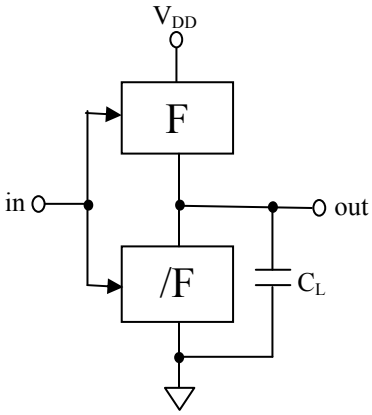

Fig.1 Conventional CMOS logic circuit with pull-up (F) and pull-down (/F) networks.

II. Dissipation Mechanisms in Adiabatic Logic Circuits

Fig.2 shows, the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, C_L is the load capacitance [1].

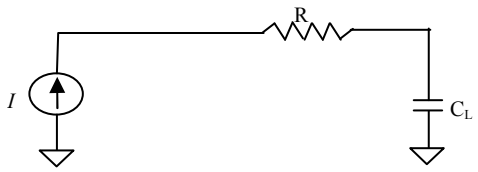

Fig.2 Equivalent model during charging process in adiabatic circuits.

Energy dissipation in resistance R is [1],

$$E_{diss} = I^2.R.T = \left(\frac{C_L V_{DD}}{T}\right)^2.R.T = \left(\frac{RC_L}{T}\right).C_L V_{DD}^2$$

Since E_{diss} depends upon R, so by reducing the on resistance of PMOS network the energy dissipation can be minimized. The on resistance of the MOSFET is given by the first order approximation is [3-5],

$$R = \left[\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})\right]^{-1}$$

Where μ is the mobility, C_{OX} is the specific oxide capacitance, V_{GS} is the gate source voltage, W is the width, L is the length and V_{th} is the threshold voltage.

E_{diss} also depends upon the charging time T, If T>> 2RC then energy dissipation will be smaller than the conventional CMOS [1].

The energy stored at output can be retrieved by the reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction [1, 2].

III. Adiabatic Logic Families

There are the many adiabatic logic design technique [8-18] are given in literature but here two of them are chosen ECRL [10] and PFAL [11], which shows the good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation.

A. Efficient Charge Recovery Logic (ECRL)

The schematic and simulated waveform of the ECRL inverter gate is shown in Fig.3 and Fig.4 respectively. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to $V_{DD,}$ since F is on so output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered.

ECRL uses four phase clocking rule to efficiently recover the charge delivered by pck. For detailed study follow the reference [10].

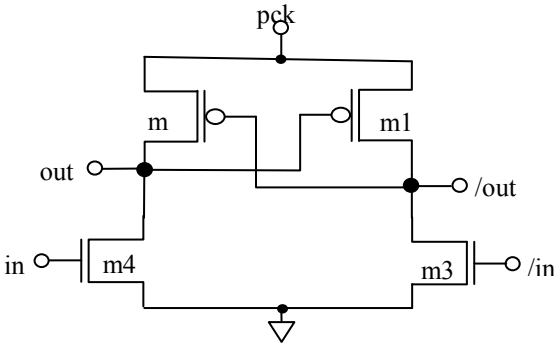

Fig.3 Schematic of ECRL inverter.

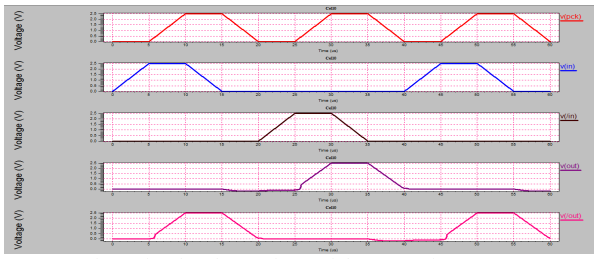

Fig.4 Simulated waveform of the ECRL inverter gate.

The schematic and simulated waveform of the ECRL 2:1 Multiplexer is shown in Fig.5 and Fig.6 respectively. Initially, select input 's' is high and power clock (pck) rises from zero to $V_{DD,}$ output 'out' will select the input 'b'. If select input 's' is low and power clock (pck) rises from zero to $V_{DD,}$ output 'out' will select the input 'a'. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic values. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, high outputs return its energy to pck hence delivered charge is recovered.

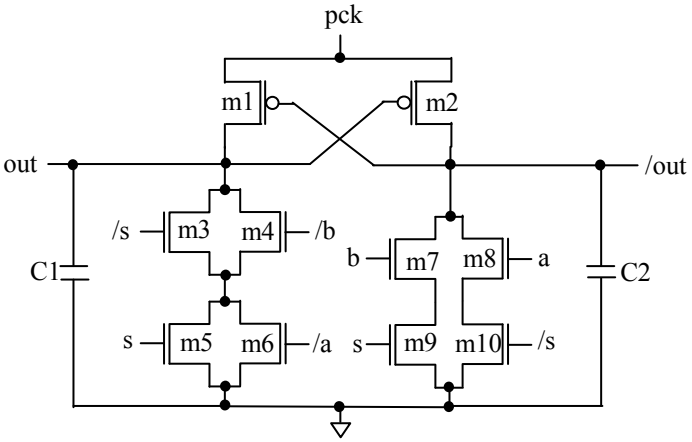

Fig.5 Schematic of ECRL 2:1 Multiplexer.

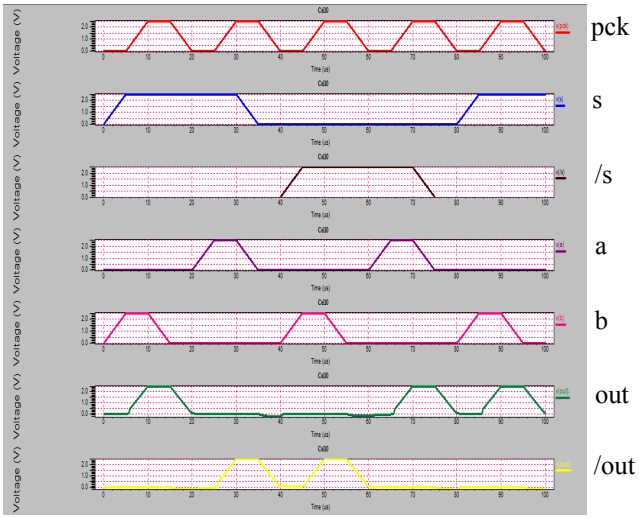

Fig.6 Simulated waveform of the ECRL 2:1 Multiplexer.

B. Positive Feedback Adiabatic Logic (PFAL)

The schematic and simulated waveform of the PFAL inverter gate is shown in Fig.7 and Fig.8 respectively. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to $V_{DD,}$ since F and m4 are on so output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered. PFAL uses four phase clocking rule to efficiently recover the charge delivered by pck. For detailed study follow the reference [11, 13].

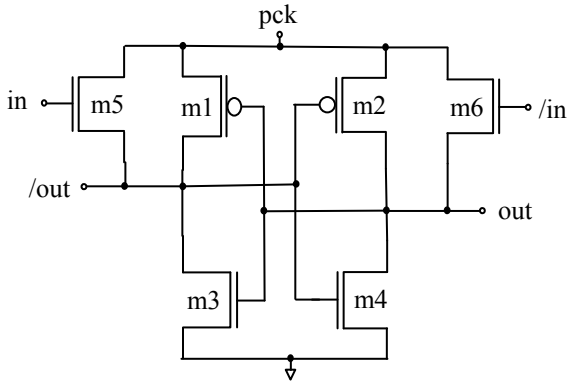

Fig.7 Schematic of PFAL inverter

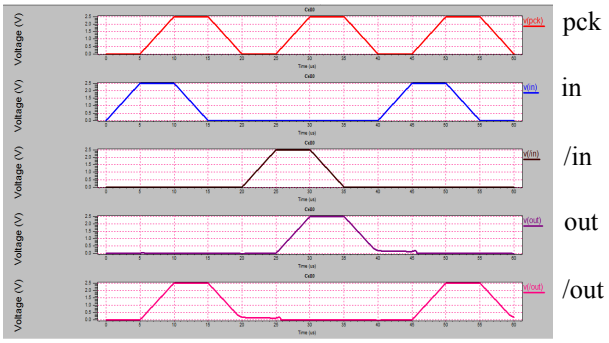

Fig.8 Simulated waveform of the PFAL inverter gate

The schematic and simulated waveform of the PFAL 2:1 Multiplexer is shown in Fig.9 and Fig.10 respectively. Initially, select input 's' is high and power clock (pck) rises from zero to $V_{DD,}$ output 'out' will select the input 'b'. If select input 's' is low and power clock (pck) rises from zero to $V_{DD,}$ output 'out' will select the input 'a'. When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic values. This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, high outputs return its energy to pck hence delivered charge is recovered.

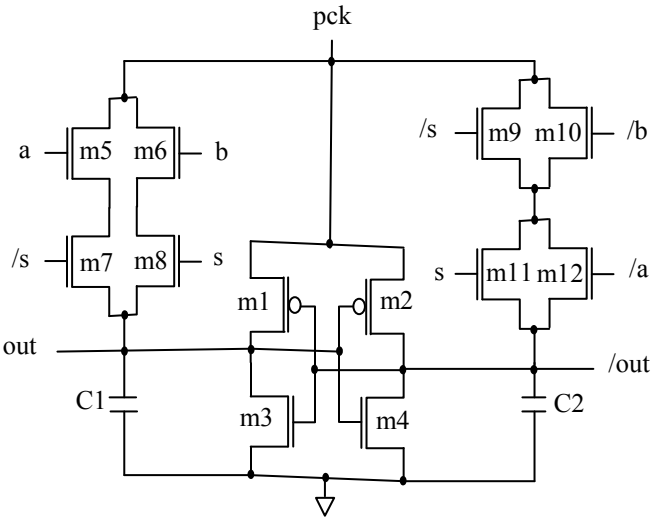

Fig.9 Schematic of PFAL 2:1 Multiplexer

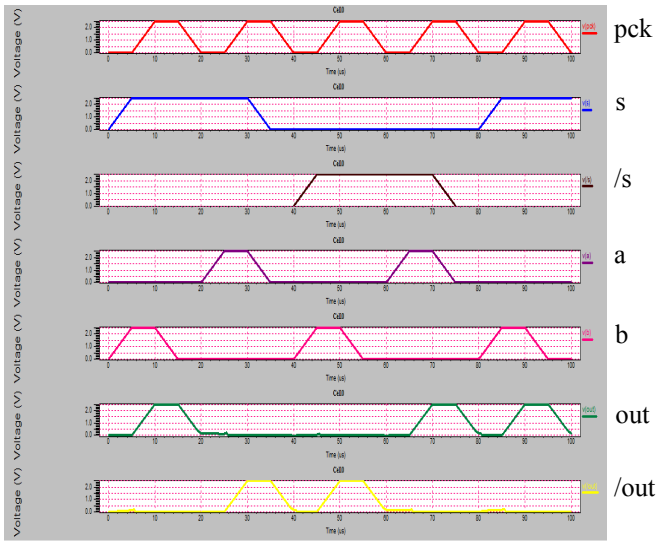

Fig.10 Simulated waveform of the PFAL 2:1 Multiplexer

IV. Impact of Parameter Variations on The Energy Consumption

Energy consumption in adiabatic circuits strongly depend on the parameter variations [19-21]. The impact of parameter variations on the energy consumption for the two logic families is investigated with respect of CMOS logic circuit, by means of TSPICE simulations. Simulations are carried out at 250nm technology node. The W/L ratio of the PMOS and

NMOS are taken as $9\lambda/2\lambda$ and $3\lambda/2\lambda$ respectively, where $\lambda = 125\,nm$.

A. Transition Frequency Variation

Fig.11 shows the energy dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the inverter logic. Fig.12 shows the energy dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the 2:1 multiplexer. It is seen that for high frequency the behavior is no more adiabatic and therefore the energy dissipation increases. At low frequencies the dissipation energy will increase for both CMOS and adiabatic logic due to the leakage currents of the transistors. Thus the simulations are carried out only at useful range of the frequencies to show better result with respect to CMOS.

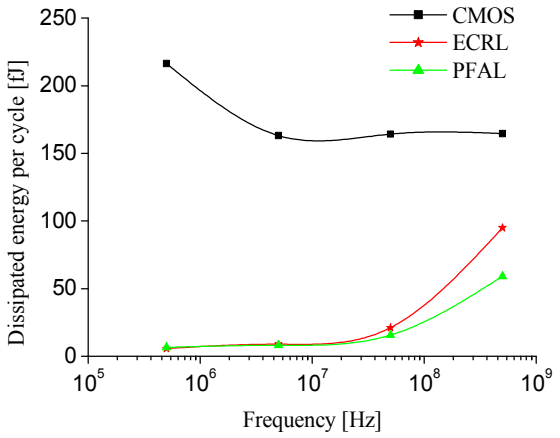

Fig.11 Energy consumption per cycle versus frequency for an inverter at V_{DD} = 2.5V and load capacitance = 20fF.

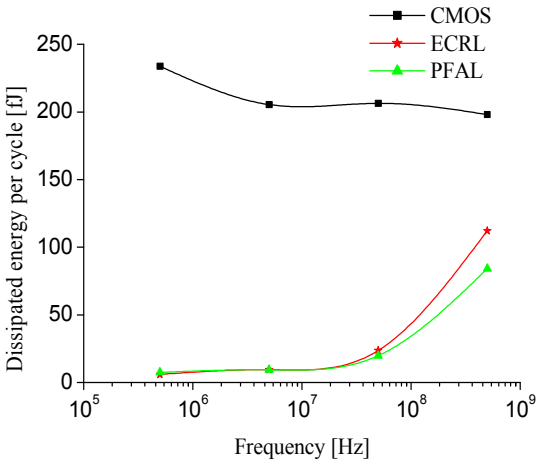

Fig.12 Energy consumption per cycle versus frequency for a 2:1 multiplexer at V_{DD} = 2.5V and load capacitance = 20fF.

B. Load Capacitance Variation

Fig.13 shows the energy dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the inverter logic. Fig.14 shows the energy dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the 2:1 multiplexer. The Figures show that adiabatic logic families having better energy savings than CMOS logic over wide range of load capacitances. PFAL shows better energy shavings than ECRL at high load capacitance.

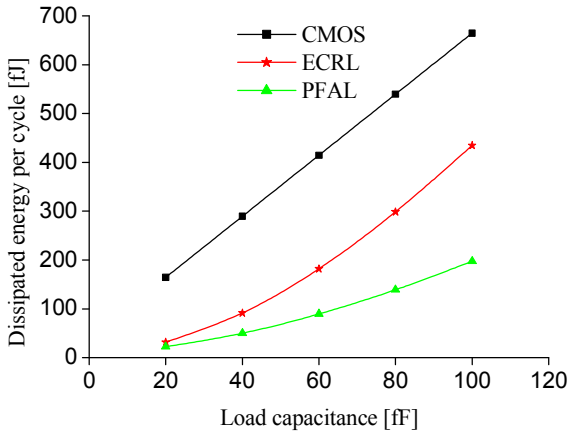

Fig.13 Energy consumption per cycle versus load capacitance for an inverter at V_{DD} = 2.5V and frequency = 100 MHz.

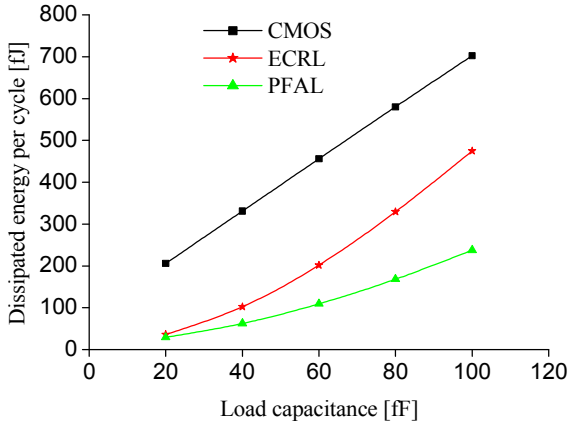

Fig.14 Energy consumption per cycle versus load capacitance for a 2:1 multiplexer at V_{DD} = 2.5V and frequency = 100 MHz.

C. Supply Voltage Variation

Fig.15 shows the energy dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the inverter logic. Fig. 16 shows the energy dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the 2:1 multiplexer. It is seen that supply voltage decreases, the gap between CMOS and logic families is reduced. But ECRL and PFAL still shows large energy savings over wide range of supply voltage.

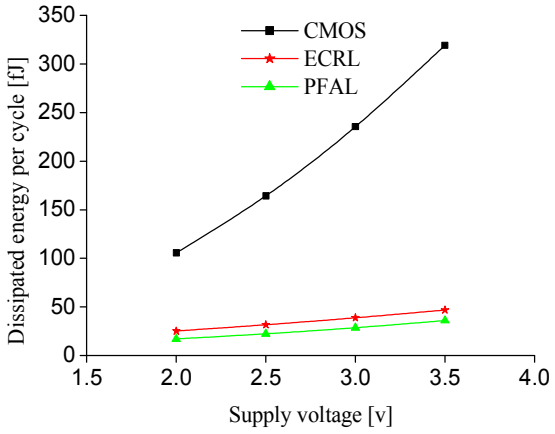

Fig.15 Energy consumption per cycle versus supply voltage for an inverter at load capacitance = 20fF and frequency = 100 MHz.

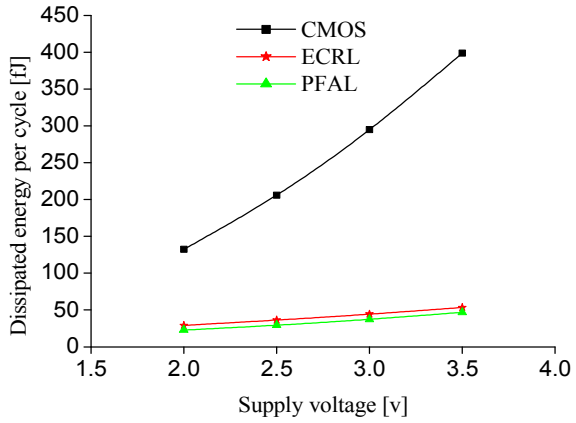

Fig.16 Energy consumption per cycle versus supply voltage for a 2:1 multiplexer at load capacitance = 20fF and frequency = 100 MHz..

V. Conclusion

The different parameter variations against adiabatic logic families are investigated, which shows that adiabatic logic families highly depend upon its. But less energy consumption in adiabatic logic families can be still achieved than CMOS logic over the wide range of parameter variations. PFAL shows better energy shavings than ECRL at the high frequency and high load capacitance. Hence adiabatic logic families can be used for low power application over the wide range of parameter variations.

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