SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY

(A Constituent College of Sri Siddhartha Academy of Higher Education)

Master of Technology in VLSI & EMBEDDED SYSTEMS
2018-19

I Semester

Subject Code	Subject	L – T – P – C	Marks for		
			CIE	SEE	Total
18MVES11	VLSI Technology	4 - 0 - 0 - 4	50	100	150
18MVES12	Digital Signal Processing for VLSI design	4 - 0 - 0 - 4	50	100	150
18MVES13	CMOS VLSI Design	4 - 0 - 0 - 4	50	100	150
18MVES14	Advanced Embedded Systems	4 - 0 - 0 - 4	50	100	150
18MVES15x	Elective-I	4 - 0 - 0 - 4	50	100	150
18MVES16	Technical Seminar -I	0 - 0 - 0 - 2	50	--	50
18MVESL17	VLSI Lab	0 - 0 - 3 - 1	50	--	50
	Total Credits	**20 -0 – 3 - 23**	**350**	**500**	**850**

Elective-I

18MVES151	Nano electronics
18MVES152	ASIC Design
18MVES153	SOC Design

II Semester

Subject Code	Subject	L – T – P – C	Marks for		
			CIE	SEE	Total
18MVES21	Analog CMOS VLSI Design	4 - 0 - 0 - 4	50	100	150
18MVES22	Low Power VLSI Design	4 - 0 - 0 - 4	50	100	150
18MVES23	Digital System Design Using Verilog	4 - 0 - 0 - 4	50	100	150
18MVES24	Advances in VLSI Design	4 - 0 - 0 - 4	50	100	150
18MVES25x	Elective-II	4 - 0 - 0 - 4	50	100	150
18MVES26	Technical Seminar -II	0 - 0 - 0 - 2	50	--	50
18MVESL27	Digital System Design using Verilog Lab	0 - 0 - 3 - 1	50	--	50
	Total Credits	**20 -0 – 3 - 23**	**350**	**500**	**850**

Elective – II

18MVES251	Solar Cells and Thin Film Technologies
18MVES252	RF VLSI Design

III Semester

Subject Code	Subject	L – T – P – C	Marks for		
			CIE	SEE	Total
18MVES31	Internship	0 - 0 - 0 - 10	100	---	100
18MVES32	Project Work Phase-I	0 - 0 - 0 - 9	50	--	50
	Total Credits	**0 -0 – 0 - 19**	**150**	**---**	**150**

Note:

- Internship: Report evaluation on Internship (50 Marks)
  Viva – Voce and Evaluation of Internship (50 Marks)
- Project Work Phase-I: Literature Survey/Visit Industry to finalize the topic of the project and presentation of the same (50 Marks)

IV Semester

Subject Code	Subject	L – T – P – C	Marks for		
			CIE	SEE	Total
18MVES41X	Elective-III	4 - 0 - 0 - 4	50	100	150
18MVES42X	Elective –IV	4 - 0 - 0 - 4	50	100	150
18MVES43	Project Work Phase-II	0 - 0 - 0 - 15	100	200	300
	Total Credits	**8 -0 – 0 – 23**	**200**	**400**	**600**

Elective – III

18MVES411 Testing of VLSI Circuits
18MVES412 Design of Semi Conductor Memories
18MVES413 VLSI interconnects and design techniques

Elective – IV

18MVES421 Computational Aspects of VLSI
18MVES422 VLSI Design Automation
18MVES423 CMOS Mixed Signal Circuit Design

Note:

- Project Work Phase-II:
  1. Project work Seminar – I: Presentation of the project work carried out for the first six weeks (50 Marks)
  2. Project work Seminar – II: Presentation of the project work carried out for the next eight weeks (50 Marks)
  3. Project work evaluation taken up at the end of the IV semester.
     - Report Evaluation: Average of the marks evaluated by internal and external examiners (125 Marks)
     - Viva- Voce: Conducted and evaluated jointly by internal and external examiners (75 Marks)

Total Credits (I to IV Semester)	**88**
Total Marks (I to IV Semester)	**2450**

VLSI TECHNOLOGY

Subject Code: 18MVES11 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Environment for VLSI Technology: Clean room and safety requirements, wafer cleaning processes and wet chemical etching techniques. **7Hrs**

Impurity incorporation: Solid state diffusion modelling and technology, Ion Implantation modelling technology and damage annealing, characterization of impurity profiles. **7Hrs**

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI, characterization of oxide films, high k and low k dielectrics for ULSI. **9Hrs**

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI,mask generation. **9Hrs**

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, epitaxial growth of silicon, modelling and technology.
Metal film deposition: Evaporation and sputtering techniques, failure mechanisms in metal interconnects, multi-level metallization schemes. **11Hrs**

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI. process integration for NMOS, CMOS and Bipolar circuits, advanced MOS technologies. **9Hrs**

TEXT BOOKS:

1. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S.K. Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York.
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
4. James D. plummer, Michael D. Deal, peter B.Griffin, “Silicon VLSI Technology,” prentice Hall,2000.

REFERENCES:

1. Stephena, Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition, Oxford University Press, 2005
2. Yuan Taur, Tak. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 2003.

DIGITAL SIGNAL PROCESSING FOR VLSI DESIGN

Subject Code: 18MVES12 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Introduction to Digital Signal Processing : Linear System Theory- Convolution- Correlation - DFT-FFT- Basic concepts in FIR Filters and IIR Filters - Filter Realizations. Representation of DSP Algorithms - Block diagram-SFG-DFG. **12Hrs**

Iteration Bound, Pipelining and Parallel Processing of FIR Filter: Iteration Bound: Data-Flow Graph Representations- Loop Bound and Iteration Bound- Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power. Retiming: Definitions, Properties and problems- Solving Systems of Inequalities. **10Hrs**

Fast Convolution and Arithmetic Strength Reduction in Filters : Fast Convolution: Cook-Toom Algorithm, Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters, Fast FIR algorithms, Two parallel and three parallel. Parallel architectures for Rank Order filters, Odd Even Merge sort architecture, Rank Order filter architecture, Parallel Rank Order filters, Running Order Merge Order Sorter, Low power Rank Order filter. **10 Hrs**

Pipelined and Parallel Recursive Filters: Pipeline Interleaving in Digital Filters, Pipelining in 1st Order IIR Digital Filters, Pipelining in Higher, Order IIR Filters, Clustered Look ahead and Stable Clustered Look ahead, Parallel Processing for IIR Filters and Problems. **10 Hrs**

Scaling and Round off Noise: Scaling and Round off Noise, State Variable Description of Digital Filters, Scaling and Round off Noise Computation, Round Off Noise Computation Using State Variable Description, Slow-Down Retiming and Pipelining. **10 Hrs**

TEXT BOOK:

1. K.K Parhi, "VLSI Digital Signal processing", John-Wiley, 1999.

REFERENCE:

1. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1995.

VLSI LAB

Sub Code: 18MVESL17 **0 – 0 – 3 – 1**

L – T – P – C

Design and verify the following by schematic simulation and layout simulation:

1. Inverter using MOSFET.
2. Two input NAND, NOR, XOR and realization of Boolean Expressions.
3. D, T, JK, JK Master Slave flip-flops.
4. Adders, MUX and shift registers.
    a. Serial adder and 2-bit parallel adder.
    b. 4:1 Multiplexer.
    c. A serial register capable of holding and shifting 4-bit words
5. Design a basic differential amplifier circuit.
6. Use the op-amp available from the library of tools to convert a sinusoidal wave into square waves by using Schmitt trigger. Design the Schmitt trigger circuit in such a way that UTP=4.5V and LTP= 2.0V.Plot V_o versus V_i.
7. Asynchronous and synchronous 4-bit counters.

CMOS VLSI DESIGN

Subject Code: 18MVES13 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter. **(Text1)** **11Hrs**

CMOS Process Technology Silicon Semiconductor technology: an overview, basic CMOS technology. A basic n-well CMOS process, The p-well process, twin tub process, silicon on insulator **CMOS process enhancements:** Interconnect, circuit elements; Resistors, Capacitors, bipolar transistors, Thin film transistors,3DCMOS**(Text1)** **6Hrs**

MOS Design Processes: MOS layers, stick diagrams, design rules and layout, symbolic diagrams. **Basic circuit concepts:** Sheet resistance ,standard unit of capacitance concepts, delay unit time inverter delays ,driving capacitive loads, propagation delays, scaling of MOS circuits**(Text4)** **9Hrs**

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, MOS logic circuits with depletion Nmos load, CMOS logic circuits, complex logic circuits, CMOS Transmission Gate. **(Text2)** **8Hrs**

Sequential MOS logic Circuits - Introduction, Behavior of bi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop **(Text2)**. **5Hrs**

Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques**(Text2)** **5Hrs**

CMOS Analog Design: MOS Small-Signal Amplifier, common source amplifiers, CMOS inverter as an amplifier, current mirrors, Differential pairs, simple CMOS operational amplifier **(Text3) (11.6.1 to 11.6.6)** **3Hrs**

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology' CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.(**Text5**) **5Hrs**

TEXT BOOKS:

1. Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspective**," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2. Sung Mo Kang & Yosuf Lederabic Law, "**CMOS Digital Integrated Circuits: Analysis and Design**",
3. CMOS VLSI Design: A Circuits and System perspective, Neil H E Weste, David Haris,Ayan, Pearson Education, III Edition.
4. Douglas A Pucknell & Kamran Eshragian , "**Basic VLSI Design**" PHI 3rd Edition (original Edition –1994).
5. Eugene D Fabricius, Introduction to VLSI Design, Mc Graw Hill, International Edition (Original Edition 1990).

REFERENCE: Wayne, Wolf, "**Modern VLSI design: System on Silicon" Pearson Education**", Second Edition.

ADVANCED EMBEDDED SYSTEMS

Subject Code: 18MVES14 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. Characteristics and Quality Attributes of Embedded Systems. **8Hrs**

Hardware Software Co-Design and Program Modelling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modelling Language, Hardware Software Trade-offs. **8Hrs**

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages. **8Hrs**

Real-Time Operating System (RTOS) based Embedded System Design:
Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS**.** **10Hrs**

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler / Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan**.** **10Hrs**

Trends in the Embedded Industry: Processor Trends in Embedded System, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks. **8Hrs**

TEXT BOOK:

1. Introduction to Embedded Systems**,** Shibu K V, Tata McGraw Hill Education Private Limited, 2009

REFERENCE:

1. Embedded Systems – A contemporary Design Tool, James K Peckol, John Weily, 2008.

ELECTIVE – I

NANO ELECTRONICS

Subject Code: 18MVES151 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Shrink-down Approaches: Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs **10Hrs**

Limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunneling Transistors, Single electron transistors, new storage, optoelectronic, and spintronics devices**.** **16hrs**

Atoms-up Approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures **10Hrs**

Molecular systems as alternatives to conventional electronics, molecular interconnects; Carbon nanotube electronics, band structure & transport, devices, applications. **16hrs**

TEXT BOOKS:

1. C.P. Poole Jr., F.J. Owens, "**Introduction to Nanotechnology**", Wiley (2003).
2. Waser Ranier, "**Nanoelectronics and Information Technology**" (Advanced Electronic Materials and Novel Devices), Wiley-VCH (2003)

REFERENCES:

1. K.E. Drexler, "**Nano systems**", Wiley (1992)
2. John H. Davies, "**The Physics of Low-Dimensional Semiconductors**", Cambridge University Press, 1998 **.**

ASIC Design

Subject Code: 18MVES152 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Introduction: Full Custom with ASIC, Semi custom ASICS, standard Cell based ASIC, gate array based ASIC, channelled gate array, channel less gate array, structured gate array, Programmable logic device, FPGA Design flow, ASIC Cell Libraries. **8Hrs**

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers. **8Hrs**

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design. **6Hrs**

Low-level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation. **6Hrs**

Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell , a brief Introduction to Low Level Design Language: An introduction to EDIF, PLA Tools and introduction to CFI designs representation, half gate ASIC, introduction to synthesis and simulation. **6Hrs**

ASIC Construction Floor Planning, Placement and Routing: Physical Design, CAD Tools, system Partitioning, estimating ASIC size, partitioning methods, floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, time driven placement methods, physical design flow - global Routing, local Routing, detail Routing, special Routing, circuit Extraction and DRC. **18Hrs**

Note: All Designs Will Be Based On VHDL.

TEXT BOOKS:

1. M.J.S .Smith, "Application - Specific Integrated Circuits**",** Pearson Education, 2003.
2. Jose E.France, YannisTsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication andSignal Processing", Prentice Hall, 1994.

REFERENCES:

1. Malcolm R.Haskard; Lan. C. May, "Analog VLSI Design - NMOS and CMOS**",** Prentice Hall, 1998.
2. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing**"**, McGraw Hill, 1994.

SoC Design

Subject Code: 18MVES153 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Motivation for SoC Design : Review of Moore's law and CMOS scaling, benefits of System-on-Chip integration in terms of cost, power, and performance, comparison of System-on-Board, System-on-Chip, and System-in-Package, typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization, productivity gap issues and the ways to improve the gap – IP based design and design reuse. **6Hrs**

Embedded Processors :Microprocessors, Microcontrollers, DSP and their selection criteria, review of RISC and CISC instruction sets, Von-Neumann and Harward architectures and interrupt architectures. **5Hrs**

Embedded Memories : Scratchpad memories, Cache memories, Flash memories, Embedded DRAM, topics related to cache memories, Cache coherence, MESI protocol and Directory-based coherence. **7Hrs**

Hardware Accelerators in an SOC : Comparison on hardware accelerators and General-purpose CPU, accelerators for graphics and image processing, typical peripherals in an SoC – DMA controller, USB controller. **10Hrs**

Interconnect architectures for SoC : Bus architecture and its limitations, Network on Chip (NoC) topologies, Mesh-based NoC, routing in an NoC, packet switching and wormhole routing. **9Hrs**

Mixed Signal and RF components in an SoC : Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits. **9Hrs**

SoC Design Flow : IP design, verification and integration, hardware software co-design, power management problems and packaging related problems. **6Hrs**

TEXT BOOKS:

1. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.

2. Henry Chang et al., "Surviving the SOC revolution: a guide to platform-based design", Kluwer (Springer), 1999.

REFERENCES:

1. Frank Ghenassia, "Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems", Springer © 2005, ISBN:9780387262321.

2. Luca Benini and Giovanni De Micheli, "Networks on Chips: Technology and Tools", Morgan Kaufmann Publishers © 2006 (408 pages), ISBN:9780123705211.

II SEMESTER

ANALOG CMOS VLSI DESIGN

Subject Code: 18MVES21 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Analog CMOS sub-circuits: Introduction to analog design, Passive and active current mirrors, band-gap references, Switched Capacitor circuits - basic principles, sampling switches, switched capacitor integrator, switched capacitor amplifier, simulation of CMOS sub circuits using SPICE. **12Hrs**

CMOS Single Stage Amplifiers: Common-Source stage (with resistive load, diode connected load, current-source load, triode load, source degeneration), source follower, common-gate stage, cascode stage, folded cascode stage. Frequency responses of CS stage, CD stage, CG stage, cascode stage, simulation of CMOS amplifiers using SPICE. **10Hrs**

Differential Amplifier & Operational Amplifiers: Single-ended and differential operation, basic differential pair – qualitative and quantitative analyses, common-mode response, differential pair with MOS loads, Performance parameters of op-amp, one stage op-amp, two-stage CMOS op-amp, Gain boosting, slew rate, power supply rejection, Simulation of differential amplifiers using SPICE.
1**1Hrs**

Oscillators: General considerations, Ring oscillators, LC oscillators – cross-coupled oscillators, Colpitts oscillator, One-port oscillator, and voltage controlled oscillators. Simulation of oscillators using SPICE. **10Hrs**

Noise Characteristics: Statistical characteristics of noise, Types of noise - thermal noise, flicker noise, Representation of noise in circuits, noise in single-stage amplifiers (CS, CD and CG stages), noise bandwidth. **9Hrs**

TEXT BOOK:

1. Razavi, "**Design of analog CMOS integrated circuits**", McGraw Hill, Edition 2002.

REFERENCES:

1 Gray, Meyer, Lewis, Hurst, "**Analysis and design of Analog Integrated Circuits**", Willey International, 4th Edition, 2002.
2 Allen, Holberg, "**CMOS analog circuit design**", Oxford University Press, 2nd Edition, 2012.

LOW POWER VLSI DESIGN

Subject Code : 18MVES22	**IA Marks : 50**
No. Of Lecture Hours/Week: 04	**Exam Hours : 03**
Total No. Of Lecture Hours: 52	**Exam Marks : 100**

Introduction to Low Power VLSI design and analysis: Introduction to low power VLSI design, Need for low power-CMOS leakage current-static current, Basic principles of low power design, probabilistic power analysis, random logic signal, probability and frequency, power analysis techniques, signal entropy. **12Hrs**

Circuit level and Logic level design techniques: Circuit, transistor and gate sizing, pin ordering, network restructuring and reorganization, adjustable threshold voltages, logic-signal gating, logic encoding, Pre-computation logic. **10Hrs**

Special low power VLSI design techniques: Power reduction in clock networks, CMOS floating node, delay balancing Switching activity reduction, parallel voltage reduction, operator reduction, adiabatic computation, pass transistor logic. **11Hrs**

Low voltage Low Power memories: Basics of SRAM, Memory cell, Pre-charge and equalization circuit decoder, ATD Sense amplifier, Output latch, Low power SRAM technologies, types of DRAM, Basics of DRAM, Cell refresh circuit. **10Hrs**

Software design and Power estimation: Low power circuit design style, Software power estimation - co design, for low power. **9Hrs**

TEXT BOOKS:

1. Gary Yeap “Practical Low Power Digital VLSI Design”, Springer US, Kluwer Academic Publishers, 2002.
2. Kaushik Roy, Sharat C. Prasad, “Low power CMOS VLSI circuit design”, Wiley Inter science Publications",1987. 21

REFERENCE:

1. Kiat-Seng Yeo, Kaushik Roy, “Low Voltage Low Power VLSI Subsystems”, Tata Mc-Graw Hill, 2009.

Digital System Design using Verilog

Subject Code: 18MVES23 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Introduction and Methodology: Digital Systems and Embedded Systems, Binary Circuit Elements, Real-World Circuits, Models, Design Methodology. **6Hrs**
Combinational Basics: Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits. **6Hrs**

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **6Hrs**
Sequential Basics: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology. 6**Hrs**

Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **7Hrs**

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **5Hrs**
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **6Hrs**

Accelerators: Concepts, case study, Verification of accelerators. **5Hrs**
Design Methodology: Design flow, Design optimization, Design for test. **5Hrs**

TEXT BOOKS:

1. Peter J. Ashenden, **"Digital Design: An Embedded Ssytems Approach Using VERILOG",** Elesvier, 2010.

REFERENCES:

1. J. Bhasker, **"A Verilog HDL Primer",** Second Edition, Star Galaxy, 2005.
2. J. Bhasker, **"A Verilog Synthesis: A Practical Primer",** Star Galaxy, 1998

ADVANCES IN VLSI DESIGN

Subject Code: 18MVES24 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS. **3Hrs**

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS. **5Hrs**

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. **6Hrs**

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization **6Hrs**

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic, Defect tolerant computing. **7Hrs**

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks. **9Hrs**

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out. **8Hrs**

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design. **8Hrs**

TEXT BOOKS:

1. Kevin F Brennan "**Introduction to Semi Conductor Device**", Cambridge publications.
2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications.

REFERENCES:

1. D.A Pucknell "**Basic VLSI Design**", PHI Publication
2. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition , 2002

Digital System Design using Verilog Lab

Sub Code: 18MVESL27 **0 – 0 – 3 – 1**
L – T – P – C

Verilog Lab Experiments:

Design and simulate using Modelsim/Xilinx-Verilog language

1. Design and verify an 8 to 3 Programmable priority encoder.
2. Design and verify 3-bit Arbitrary counter and repeat the given sequence.
3. Design and verify BCD adder and Subtractor.
4. Design and verify a Sequential block to generate a sequence using appropriate FSM.
5. Design and verify 8-bit Ripple carry adder and Carry skip adder.
6. Design and verify a Linear feedback shift register based on given polynomial expressions.
7. Design and verify the following 8bit Multipliers. Also report on area delay trade off

   i)Serial Multiplier. Ii) Parallel Multiplier.
8. Design and verify a parameterized FIFO.
9. Design and verify register file which has 32 entry 3 ports having explicit address decoder. The ports are dedicated for read and write and will take one clock cycle for read or write operation.

ELECTIVE – II

SOLAR CELLS AND THIN FILM TECHNOLOGIES

Subject Code: 18MVES251 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

SOLAR IRRADIANCE:
Basics of light: properties of light, energy of photon, photon flux, spectral irradiance, radiant power density, black body radiation, sun radiation.
Solar Radiation: The Sun, solar radiation in space, solar radiation outside the earth's atmosphere, terrestrial solar radiation, solar radiation at the earth's surface, atmospheric effects, air mass, motion of the sun, solar time, declined ion angle, elevation angle, azimuth angle, the sun's position, solar radiation on a tilted surface , arbitrary orientation and tilt, calculation of solar insulation, measurement of solar radiation. **12Hrs**

PN JUNCTION
Basics: Semiconductor materials, semiconductor structure, conduction in semiconductor, band gap, intrinsic carrier concentration, doping, and equilibrium carrier concentration.
Generation: Absorption of light, absorption coefficient, absorption depth, generation rate.
Recombination: Types of recombination, life time, diffusion length, surface recombination.
Carrier Transport: Movements of carriers in semiconductor, diffusion, drift.
PN Junction: Formation of a PN junction, PN junction diode, bias of PN junctions, diode equations, diode equation for PV, ideal diode equation derivation, basic equations, applying basic equations to a PN junction, solving for depletion region and quasi-neutral regions, finding total current. **12Hrs**

SOLAR CELLS:
Principles of solar cell operation: Electrical characteristics, optical properties, typical solar cell structures, ideal efficiencies.
Crystalline silicon solar cells: Manufacturing and properties of Crystalline silicon, high-efficiency laboratory cells, screen-printed cells, laser-processed cells, HIT cell, rear-contacted cells, thin silicon solar cells – light trapping, voltage enhancements, silicon deposition and crystal growth. **10Hrs**

THIN-FILM SILICON SOLAR CELLS: Hydrogenated amorphous silicon (a-Si:H) layers , hydrogenated microcrystalline silicon (μSi:H) layers, p-i-n and n-i-p structures, tandem and multi-junction solar cells. **9Hrs**

RECENT ADVANCES IN THIN-FILM SOLAR CELLS: CdTe based thin film solar cells, uInSe2 (CIS) based thin-film solar cells, thin-film GaAs solar cells, Chalcopyrite Based Solar Cells, concentrator silicon solar cells, dye-sensitized thin-film solar cells, organic solar cells **9Hrs**

TEXT BOOKS:

1. Adrian Kitai, "Principles of Solar Cells, LEDs and Diodes: The role of the PN junction", John Wiley & Sons, 2011.
2. Augustin McEvoy, L. Castaner, Tom Markvart, "Solar Cells: Materials, Manufacture and Operation", 2ndedition, Newnes, 2012.

REFERENCES:

1. Arvind Shah, "Thin-Film Silicon Solar Cells", Illustrated edition, EPFL Press, 2010.
2. I. M. Dharmadasa, "Advances in Thin-Film Solar Cells", Illustrated edition, CRC Press, 2012.

RF VLSI DESIGN

Subject Code: 18MVES252 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Performance parameters of RF circuits: Gain parameters, non-linearity parameters, Noise figure, phase noise, dynamic range, RF front end performance parameters, and performance trade-offs in an RF circuit. **12Hrs**

Filter design: Modern filter design, frequency and impedance scaling, high pass filter design, band pass filter design, band reject filter design, effects of finite Q. **10Hrs**

High Frequency amplifier design: Zeros as Bandwidth enhances, shunt-series amplifier, bandwidth enhancement with frequency doublers, tuned amplifiers, neutralization and unilateralization, cascaded amplifiers, LNA topologies. **09Hrs**

Mixers and Oscillators: Mixer fundamentals, nonlinear systems as linear mixers, multiplier based mixers, sub sampling mixers. problems with purely linear oscillators, tuned oscillator, negative resistance oscillators, frequency synthesis. **11Hrs**

RF power amplifiers: General considerations, Class A, AB, B & C power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF power amplifier design examples. **10Hrs**

TEXT BOOKS:

1. Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "**Adaptive Low Power Circuits for Wireless Communications (Analog Circuits and Signal Processing series)**", Springer, 1st Edition, 2006.
2. Chris Bowick with John blyler and Cheryl ajluni, "RF Circuit design", 2nd Edition, 2000.

REFERENCE:

1. Thomas.H. Lee, "**The design of CMOS Radio-Frequency Integrated Circuits**", Cambridge University Press, 2nd Edition, 2004.

HIGH SPEED VLSI DESIGN

Subject Code: 18MVES253 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Clocked Logic Styles: Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families. **12Hrs**

Circuit design margining and design variability: Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise. **11Hrs**

Latching strategies: Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques. **10Hrs**

Interface Techniques: Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design. **10Hrs**

Clocking Styles: Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques. **9Hrs**

TEXT BOOK:

1. Kerry Bernstein, Keith M. Carrig, "High Speed CMOS Design Styles", Kluwer Academic Publishers, 2002.

REFERENCES:

1. Evan Sutherland, Bob Stroll, David Harris, "Logical Efforts, Designing Fast CMOS Circuits", Kluwer Academic Publishers, 1999
2. David Harris, "Skew Tolerant Domino Design", IEEE Journal of Solid State Circuits, 2001.

ELECTIVE – III

Testing of VLSI circuits

Subject Code: 18MVES411 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Basics of testing and fault modelling: Introduction to Testing - Faults in digital circuits - Modelling of faults - Logical Fault Models – Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation. **8Hrs**

Test generation for combinational and Sequential Circuit: Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. **12Hrs**

Design for testability: Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches. **12Hrs**

Self-test and test algorithms: Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures – Testable Memory Design - Test algorithms - Test generation for Embedded RAMs. **12Hrs**

Fault Diagnosis: Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis. **8Hrs**

TEXT BOOKS:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.

REFERENCES:

1. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
2. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International.
3. N.K. Jha and S.G. Gupta, “Testing of Digital Systems”, Cambridge University Press, 2003.
4. Zainalabe Navabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer, 2010.

Design of Semiconductor Memories

Subject Code: 18MVES412 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

RAM: SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit Operation, Bipolar SRAM Technologies, Silicon On Insulator (SOl) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

DRAM Technology Development, CMOS DRAM, DRAM Cell Theory and Advanced Cell Structures, BiCMOS, Soft Error Failures in DRAM, Advanced DRAM Designs and Architecture, Application Specific DRAM. **8Hrs**

Non-volatile Memories: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read-Only Memories (PROM), Bipolar PROM, CMOS PROM, Erasable (UV) - Programmable Road-Only Memories (EPROM), Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROM, Electrically Erasable PROM (EEPROM), EEPROM Technology And Architecture, Non-volatile SRAM-Flash Memories (EPROM or EEPROM), Advanced Flash Memory Architecture. **10Hrs**

Memory Fault modelling and testing: RAM Fault Modelling, Electrical Testing, Peusdo Random Testing-Megabit DRAM TestingNon-volatile Memory Modelling and Testing-IDDQ Fault Modelling and Testing-Application Specific Memory Testing **10Hrs**

Semiconductor Memory reliability: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory. Reliability: Reliability Modelling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification. **12Hrs**

Advanced memory technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto-resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions. **12Hrs**

TEXT BOOKS:

1. Ashok K. Sharma, “Semiconductor Memories”, Two-Volume Set, Wiley-IEEE Press, 2003.
2. Betty Prince, “High Performance Memories: New Architecture DRAMs and SRAMs - Evolution and Function”, Wiley, Revised Edition, 1999.

REFERENCE:

1. Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, “DRAM Circuit Design : Fundamental and High Speed Topics”, Wiley-IEEE Press, 2nd Edition, 2008.

VLSI Interconnects & Design Techniques

Subject Code: 18MVES413 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Preliminary concepts of VLSI interconnects: Interconnects for VLSI applications-copper interconnections –method of images- method of moments- even and odd capacitances- transmission line equations- miller's theorem- Resistive interconnects as ladder network- Propagation modes in micro strip interconnects- slow wave propagations- Propagation delay. **10Hrs**

Parasitic resistance, Capacitance and Inductance: Parasitic resistances, capacitances and inductances- approximate formulas for inductances- green's function method: using method of images and Fourier integral approach- network Analog method- Inductance extraction using fast Henry-copper interconnections for resistance modelling . **10Hrs**

Interconnection delays: :Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections- transmission line analysis for parallel multilevel interconnections-analysis of crossing interconnections- parallel interconnection models for micro strip line- modelling of lossy parallel and crossing interconnects- high frequency losses in micro strip line- Expressions for interconnection delays- Active interconnects. **14hrs**

Cross talk analysis: Lumped capacitance approximation- coupled multi conductor MIS micro strip line model for single level interconnects- frequency domain level for single level interconnects-transmission line level analysis of parallel multi level interconnections. **10Hrs**

Novel solutions for problems in interconnect: Optical interconnects – carbon Nano tubes/ Graphenes vs. Copper wires. **8Hrs**

TEXT BOOKS:

1. H B Bakog Lu, Circuits, "Interconnections and packaging for VLSI", Addison Wesley publishing company.
2. J A Davis, J D Meindl, "Interconnect technology and design for Gigascale integration", Kluwer academic publishers.

REFERENCES:

1. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, "Interconnect Centric deisgn for advanced SOC and NOC", Springer.
2. C K Cheng, J Lillis, S Lin, N Chang, "Interconnect analysis and synthesis", Wiley interscience. 5. Hall S H, G W Hall and J McCall, High speed digital system design, Wiley inter-science
3. Askok K Goel, "High speed VLSI interconnections", Wiley inter-science, second edition, 2007.

ELECTIVE – IV

Computational Aspects of VLSI

Subject Code: 18MVES421 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Analysis and design of Algorithms: Abstract Data Types - Time and Space Analysis of Algorithms - Big Oh and Theta Notations - Average, best and worst case analysis - Simple recurrence relations and use in algorithms – Mappings. Algorithms Analysis - Sorting - Searching - Design Techniques- Greedy Methods - Dynamic Programming - Divide and Conquer - Back Tracking –Applications. **12Hrs**

VLSI models: Integrated circuits and the mead Conway rules-VLSI implementation of logic-Abstraction of VLSI circuits. Lower bounds on area and time: Introduction to lower bound arguments-information and crossing sequence- probabilistic circuits and algorithms – circuits with repetitive inputs. **10Hrs**

Algorithm for VLSI Design: Algorithms for layout –organization with high area- Compilation and optimization algorithms. **10Hrs**

Overview of VLSI design systems: Design languages- CIF –CHISEL –ESIM –LGEN- LAVA-SLIM- A regular expression language. **10Hrs**

Algorithms for VLSI design tools: Reporting Intersections of Rectangles-Circuit Extraction Algorithms-Design Rule Checking-An Algorithm for Simulation of Switch Circuits-The PI Placement and Routing System-Optimal Routing. **10Hrs**

TEXT BOOK:

1. Jeffrey D. Ullman, “Computational aspects of VLSI”, Computer Science Press (1984).

REFERENCE:

2. Alfred .V. Aho, John .E. Hop croft, Jeffrey .D. Ullman, "Data Structures and Algorithms", Addison-Wesley Publications.,1985

VLSI DESIGN AUTOMATION

Subject Code: 18MVES422 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Data structures and Basic Algorithms: Basic terminology, Complexity Issues and NP-Hardness: algorithms for NP-hard problems. Basic algorithms: Graph algorithms, computational Geometry algorithms- Basic data structures Graph algorithms for physical design: classes of graphs in physical design, relationship between graph classes, graph problems in physical design, algorithms for Interval graphs, permutation graphs and circle graphs. **10Hrs**

Partitioning and Clustering: Partitioning and Clustering Metrics, Move-Based Partitioning Methods, Mathematical Partitioning, Formulations. Clustering: Hierarchical Clustering, Agglomerative Clustering, Multilevel Partitioning. **10Hrs**

Floor planning and Placement: Floor planning: Early research-Slicing floor plan - Floor plan representation-Packaging floor plan representation-Recent advances in floor planning. Placement-Introduction- Problem formulation- Simulation based placement algorithms- Partitioning based placement algorithms-cluster growth-Quadratic assignment-resistive network optimization. **12Hrs**

Routing and Compaction: Global Routing- Detailed routing- Over the cell routing and via minimization- clock and power routing. Problem Formulation - Classification of Compaction algorithms- 3/2 dimensional compaction-2D compaction- Hierarchical compaction- Recent trends in Compaction. **12Hrs**

Issues on Interconnects: Timing driven Interconnect synthesis-Buffer insertion basics-Generalised buffer insertionBuffering in layout environment-Global interconnect planning. Introduction to physical design for 3D circuits. **8Hrs**

TEXT BOOKS:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2008. For I", Kluwer Academic Publisher,2002

REFERENCES:

1. Sung Kyu Lim, "Practice Problems in VLSI physical design Automation", Springer, 2008.
2. charles J . Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar ,"Hand book of algorithms of Physical design Automation ", CRC press, 2009.
3. Jeffrey D Ullman, "Computational aspects of VLSI", Computer Science Press, 1984.
4. Sadiq M .Sait, Habib Youssef, "VLSI Physical design automation theory and Practice", World Scientific Publishing, 1999.

CMOS Mixed Signal Circuit Design

Subject Code: 18MVES423 **IA Marks: 50**
No. Of Lecture Hours/Week: 04 **Exam Hours: 03**
Total No. Of Lecture Hours: 52 **Exam Marks: 100**

Phase Locked Loop: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL. **10Hrs**

Sampling Circuits: Basic sampling circuits for Analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures, Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture. **11Hrs**

D/A Converter Architectures: Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, , switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, Current steering architectures. **11Hrs**

A/D Converter Architectures: Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures. **10Hrs**

Integrator Based Filters: Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-c integrator, and discrete time integrators. Filtering topologies, bilinear transfer function and biquadratic transfer function. **10Hrs**

TEXT BOOKS:

1. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, Edition 2002.
2. Razavi, “Principles of data conversion system design”, Wiley IEEE Press, 1st Edition, 1994.
3. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2009.

REFERENCE:

1. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 1986. 5. Baker, Li, Boyce, “CMOS: Circuit Design, layout and Simulation”, PHI, 2000.