Advanced FinFET Process Technology

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   - Merits and Issues of FinFET
2. Advanced FinFET Process Technology
   - Vth Tuning
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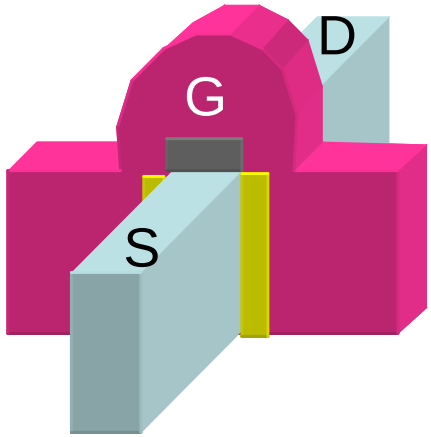
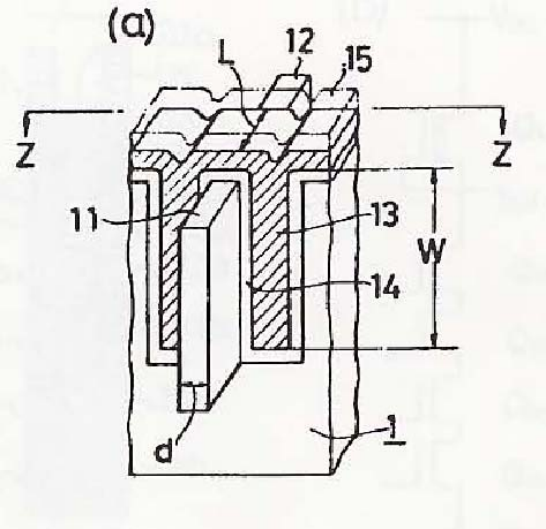
3. Summary

Multi-Gate FinFETs



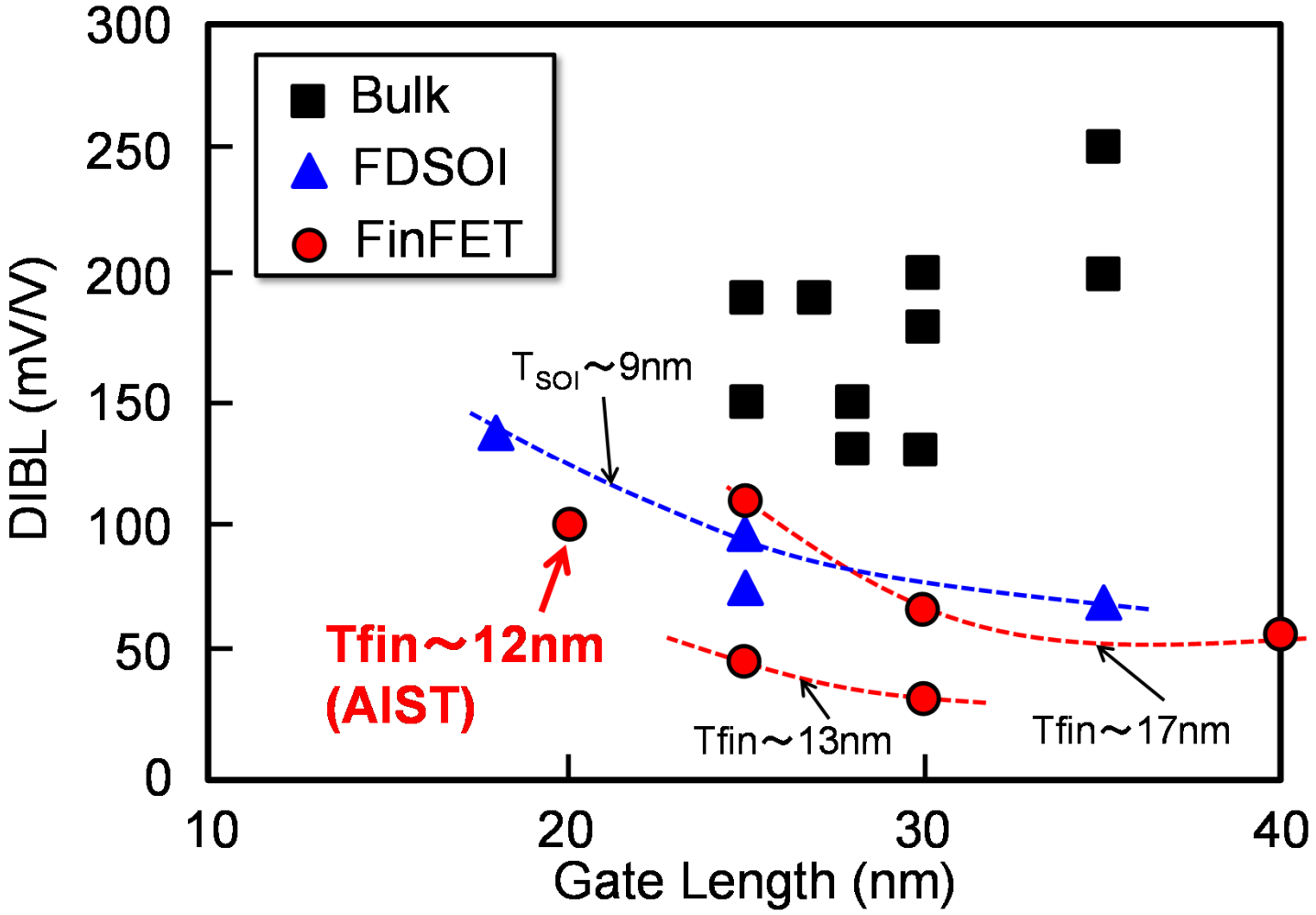
FinFET



1st FinFET Patent
in 1980 from AIST

- ✓Proposed by AIST in 1980 (named “FinFET” by UCB in 1999)
- ✓Ultrathin and undoped channel and self-aligned double gate
- ✓Extremely high short channel effect (SCE) immunity

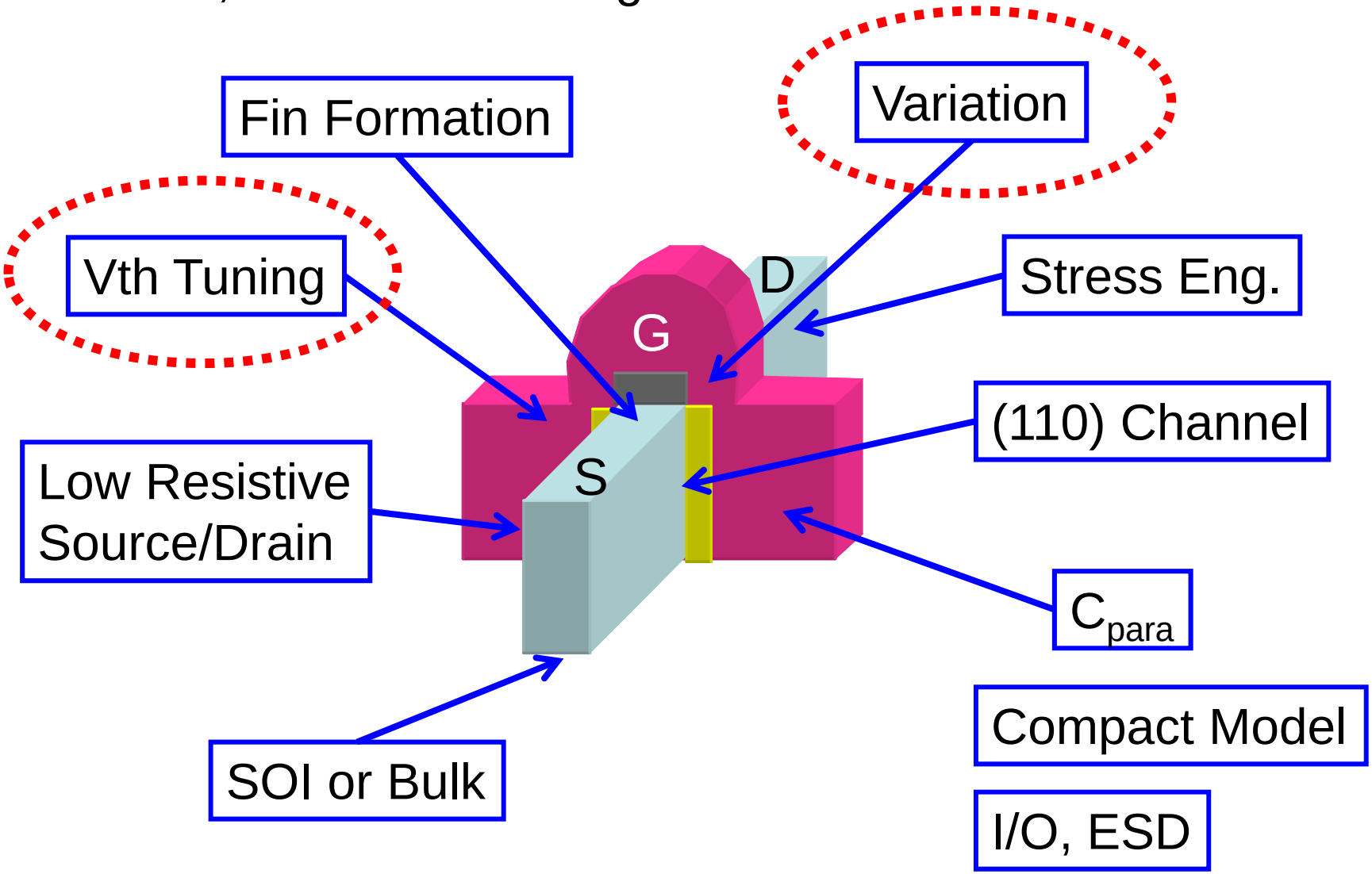
DIBL Benchmark



✓FinFETs show the smallest DIBL (=highest SCE immunity)

Issues for Advanced FinFET

✓ However, several technological issues still exist…



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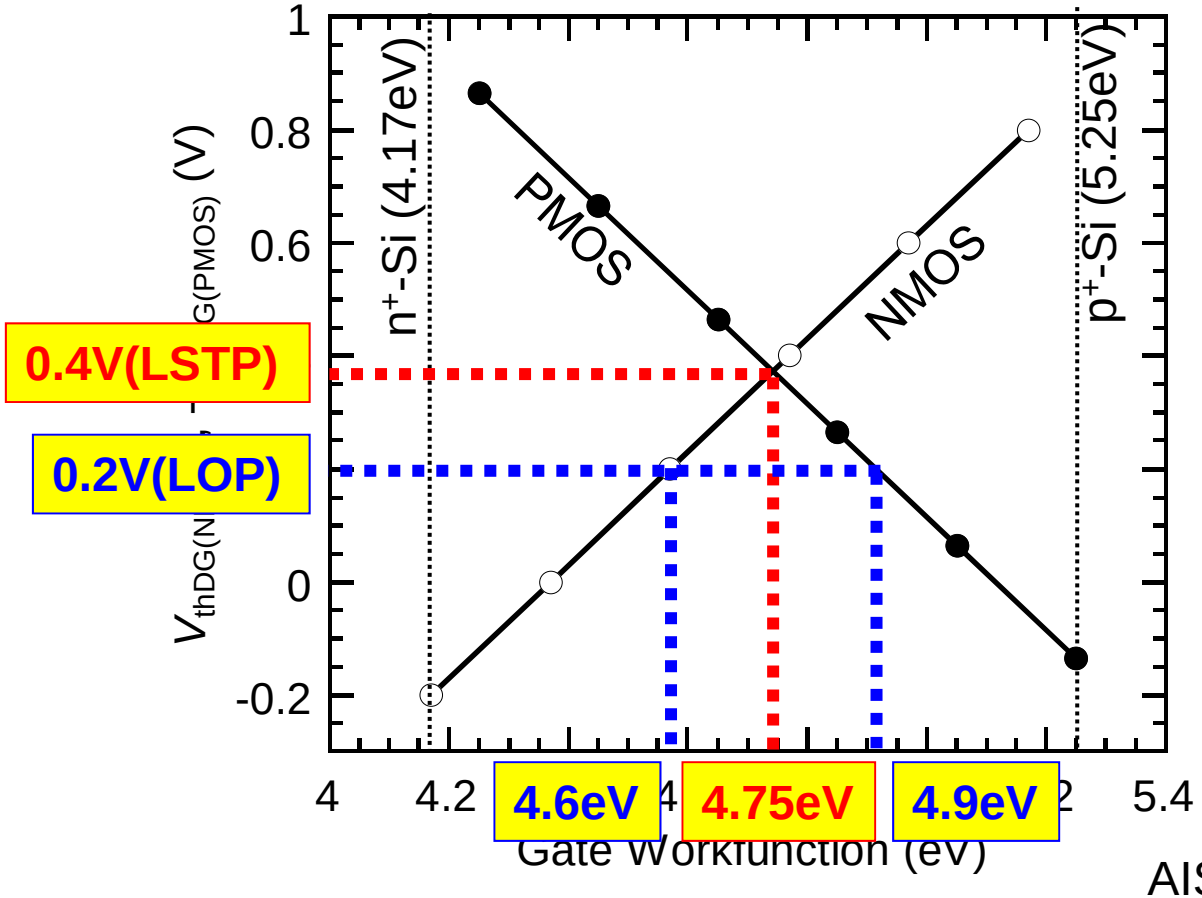
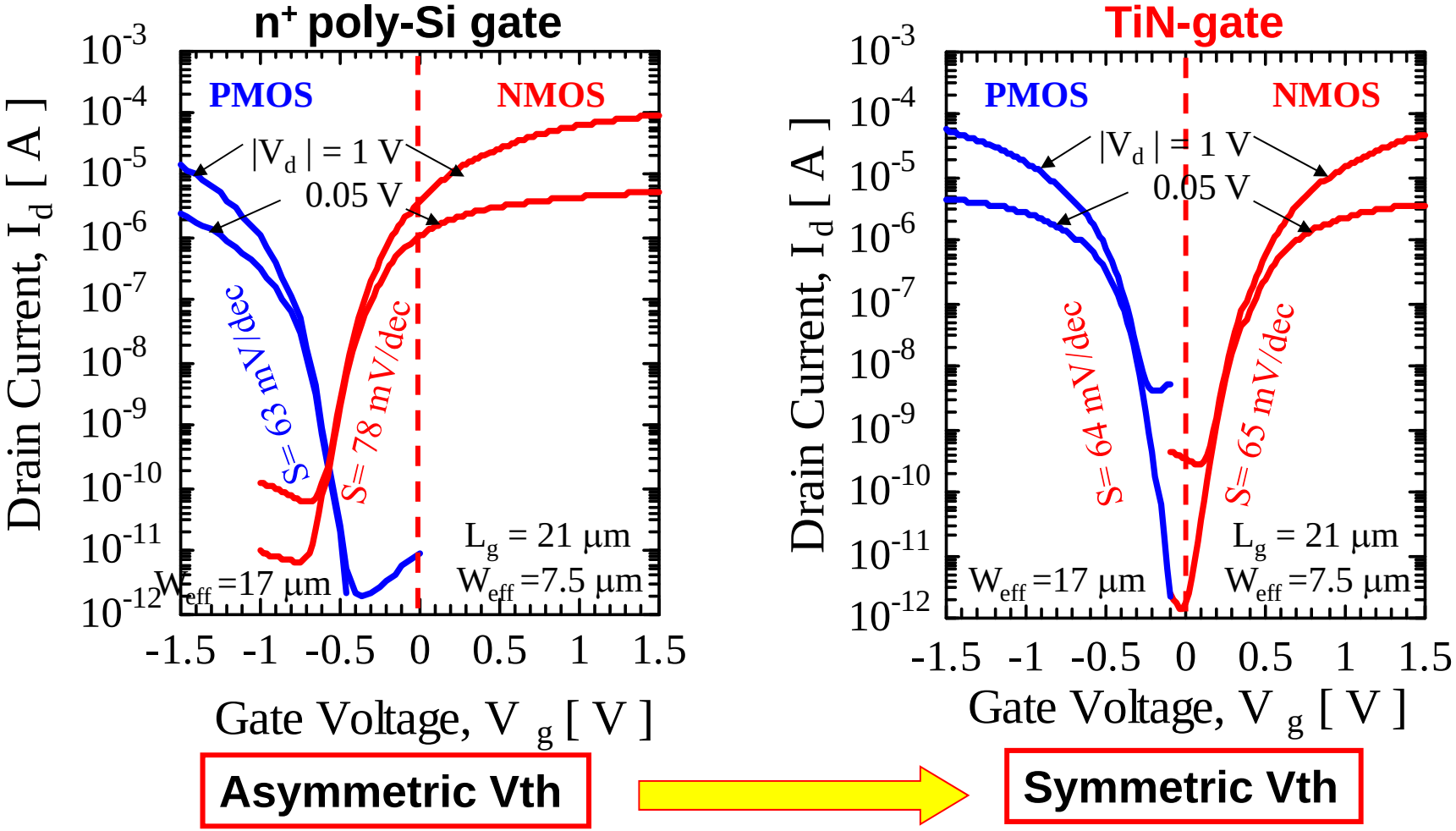
V_{th} for FinFETs



AIST, IEEE TED 2007

- ✓ V_{th} has a linear relationship with Gate Workfunction
- ✓ For low V_{th}, dual metal gate (dual WF) is needed

I_d-V_g for Poly- and TiN-Gate FinFET



Asymmetric Vth → **Symmetric Vth**

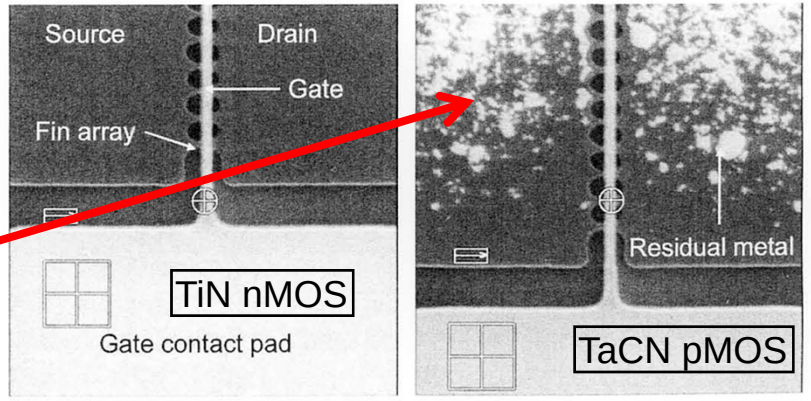
- ✓ Almost symmetrical Vth's (normally off) are obtained thanks to the midgap work function of TiN (4.75 eV)

Dual Metal Gate Integration

General approach:

"Deposition and etching"

Integration of TiN and TaCN gate FinFETs



Etching residue

Ref. M.M.Hussain et al., ESSDERC2007, p.207

This work :

"Metal Inter-diffusion"

For PMOS

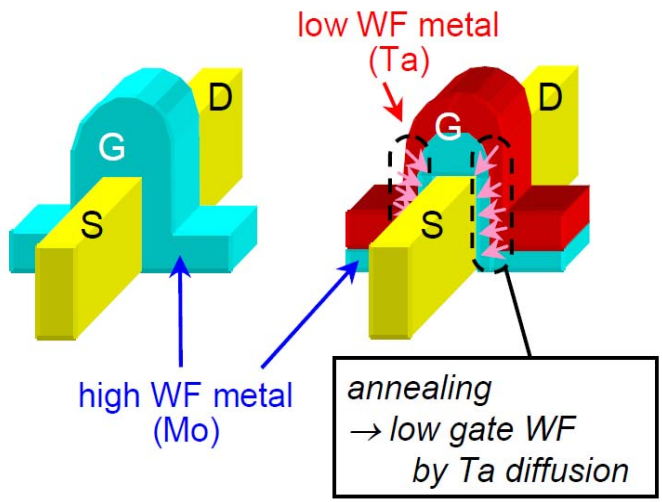
→ **Mo(4.95 eV)**

For NMOS

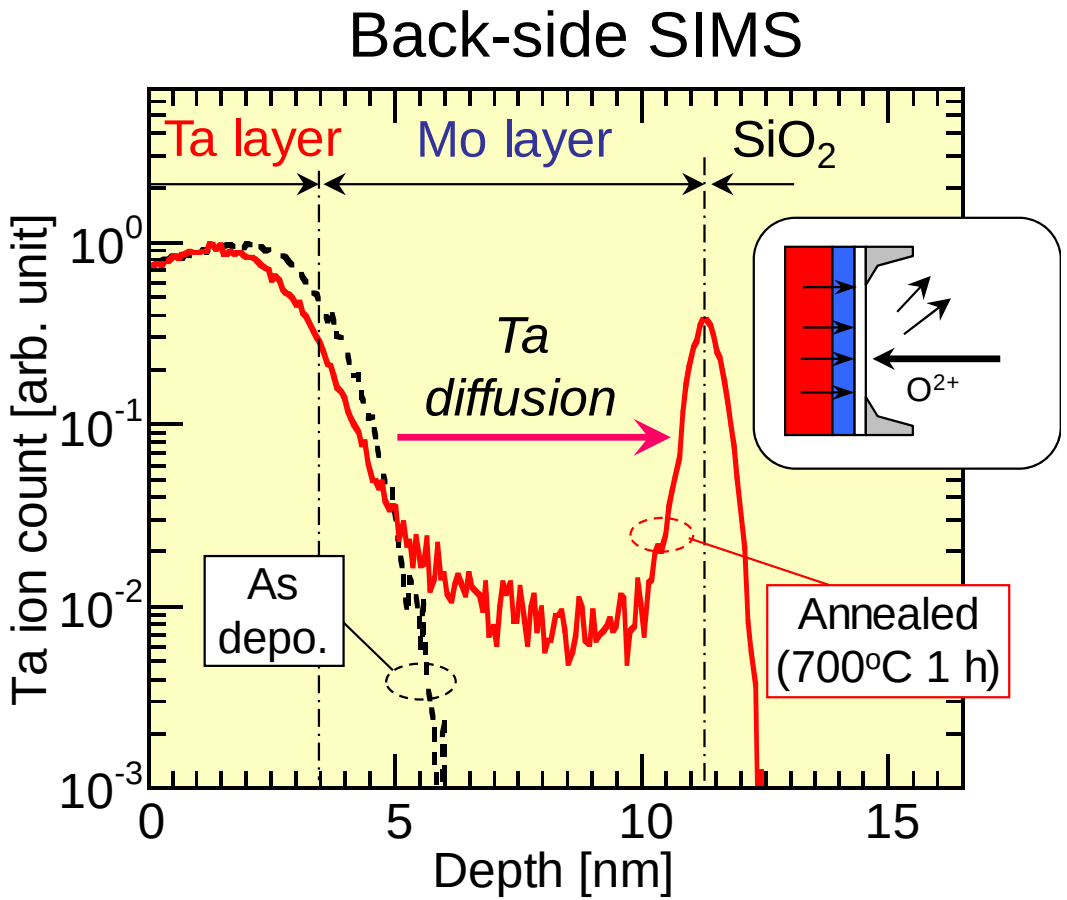
→**Ta(4.25 eV)/Mo stack**

→**Ta Inter-diffusion in Mo**

(No metal etching)



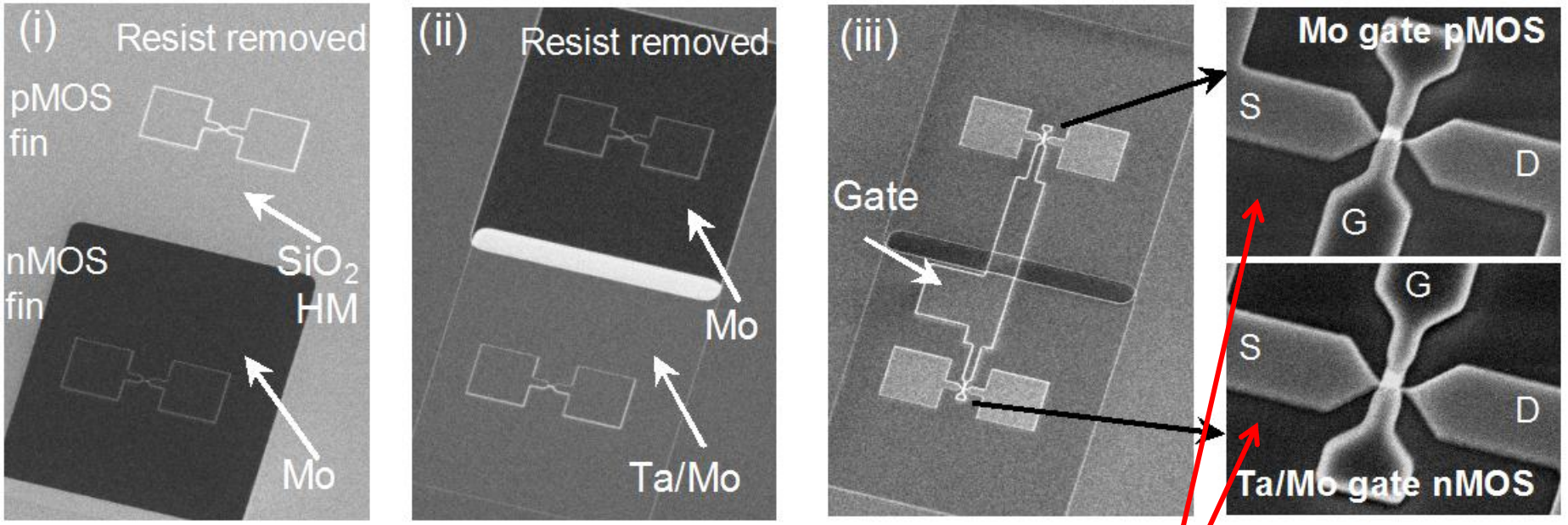
Ta diffusion in Mo



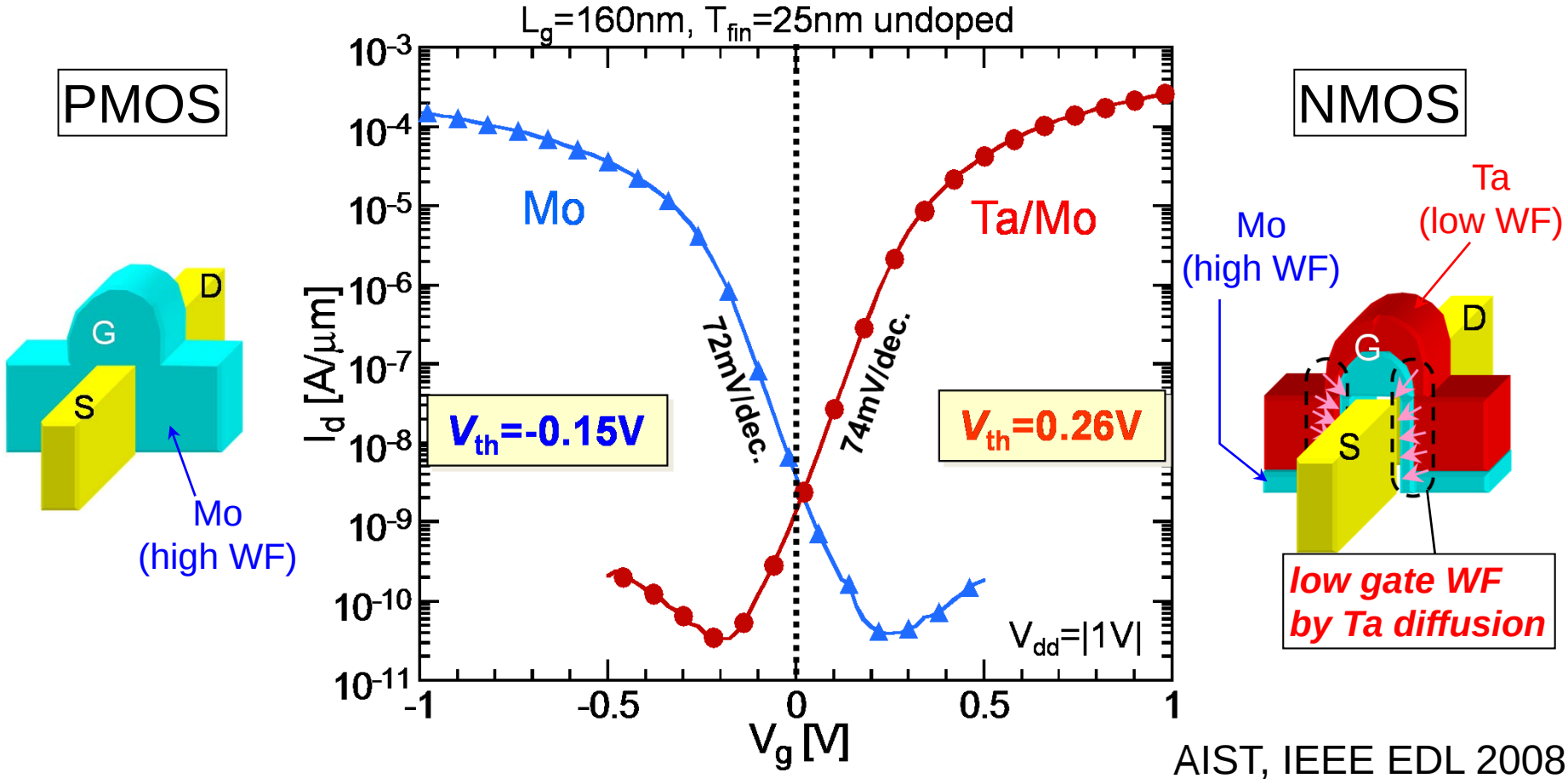
- ✓ Ta diffuses in Mo and piles-up at Mo/SiO_2 interface after annealing
- ✓ Thus WF for NMOS is determined by Ta (4.25eV)

Features of Dual MG FinFETs

SiO_2 HM etchback in nMOS region → Ta and SiO_2 HM etchback in pMOS region → Patterning of Mo and Ta/Mo gates



I-V for Mo and Ta/Mo FinFETs

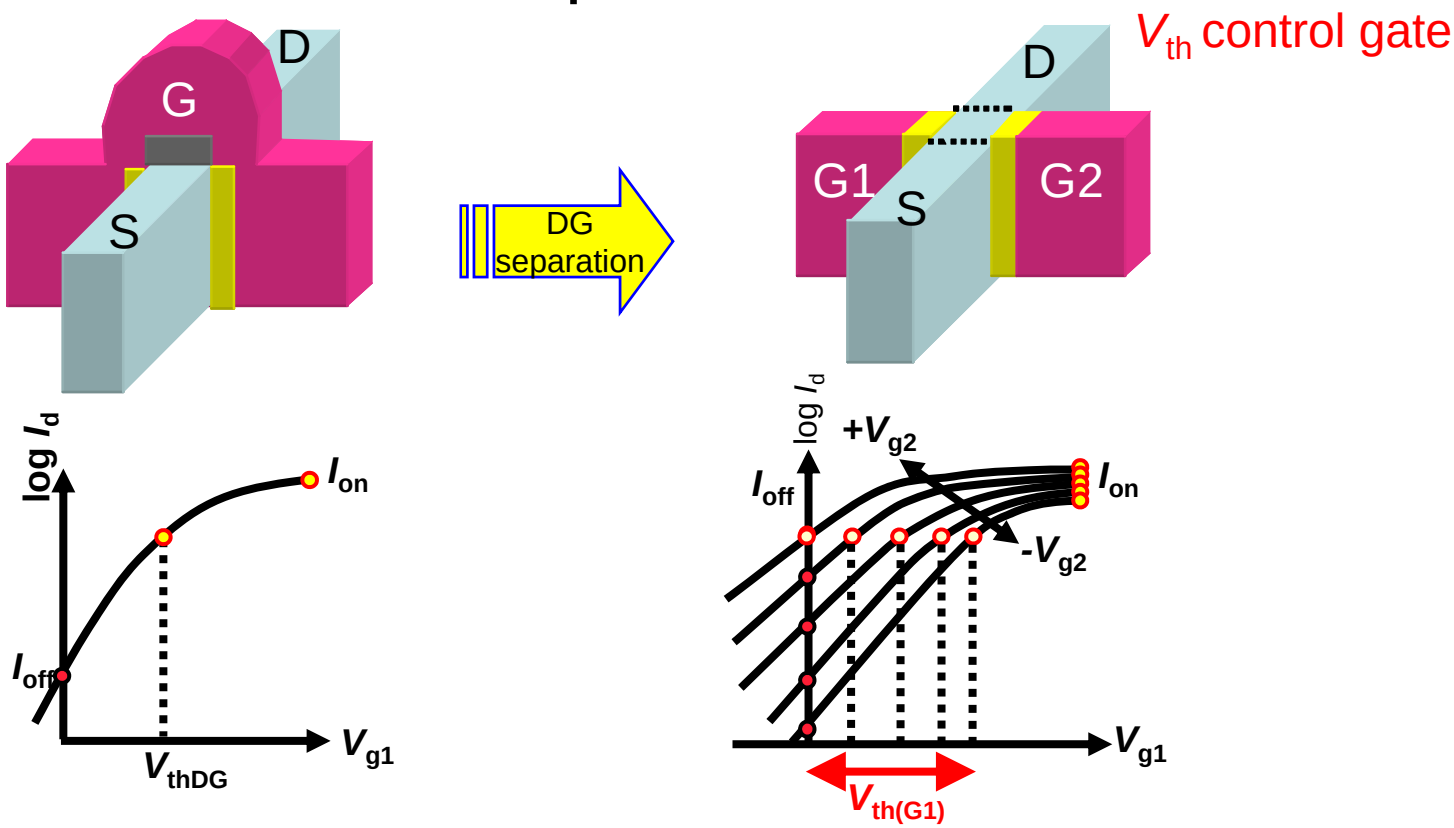


AIST, IEEE EDL 2008

- ✓ For NMOS, low V_{th} can be achieved by Ta diffusion in Mo
- ✓ For PMOS, low V_{th} can be achieved by Mo
- ✓ Off leakage → Negligible

Four-Terminal FinFET

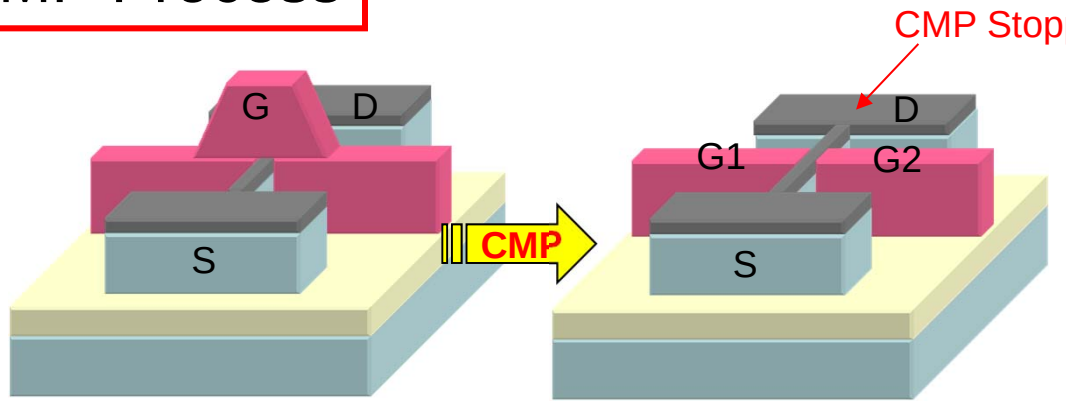
4T-FinFET = Independent DG FinFET



✓Vth for FinFET can be controlled flexibly and individually by separating the DG

DG Separation

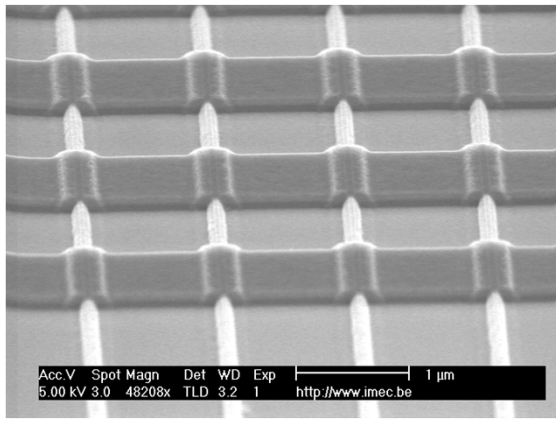
CMP Process



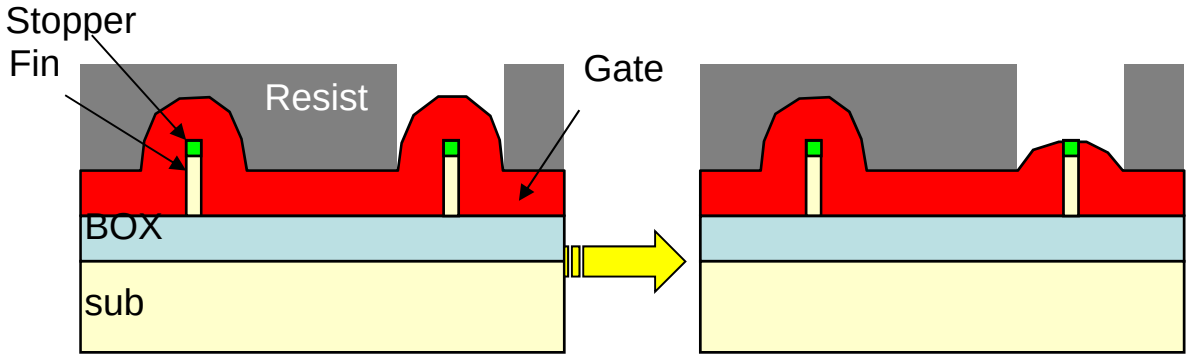
FinFET Formation

DG Separation by CMP

SEM Image after CMP

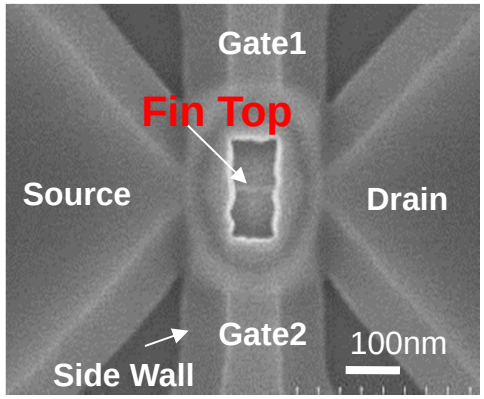


Local Etch-back Process

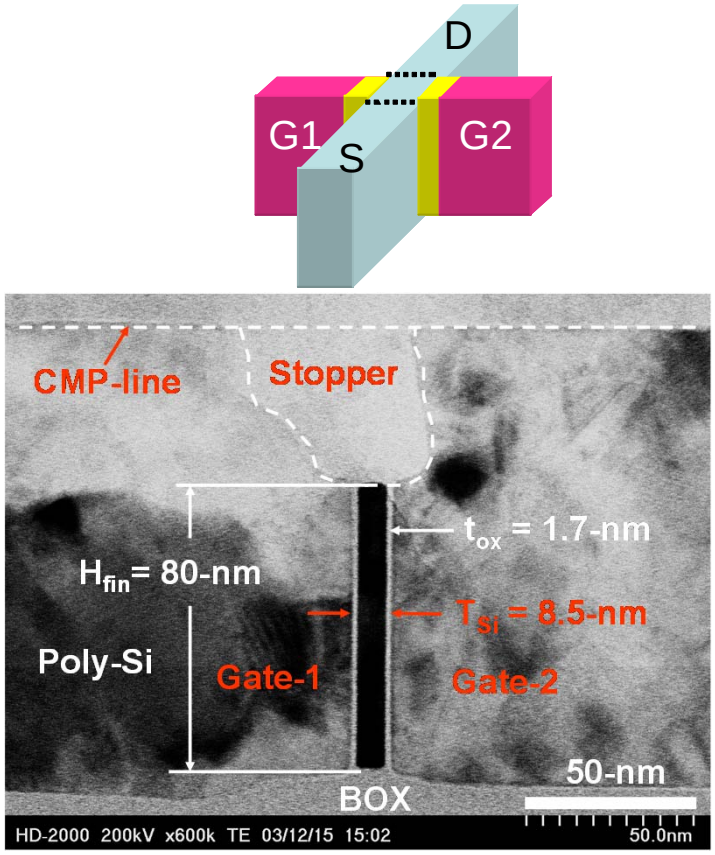


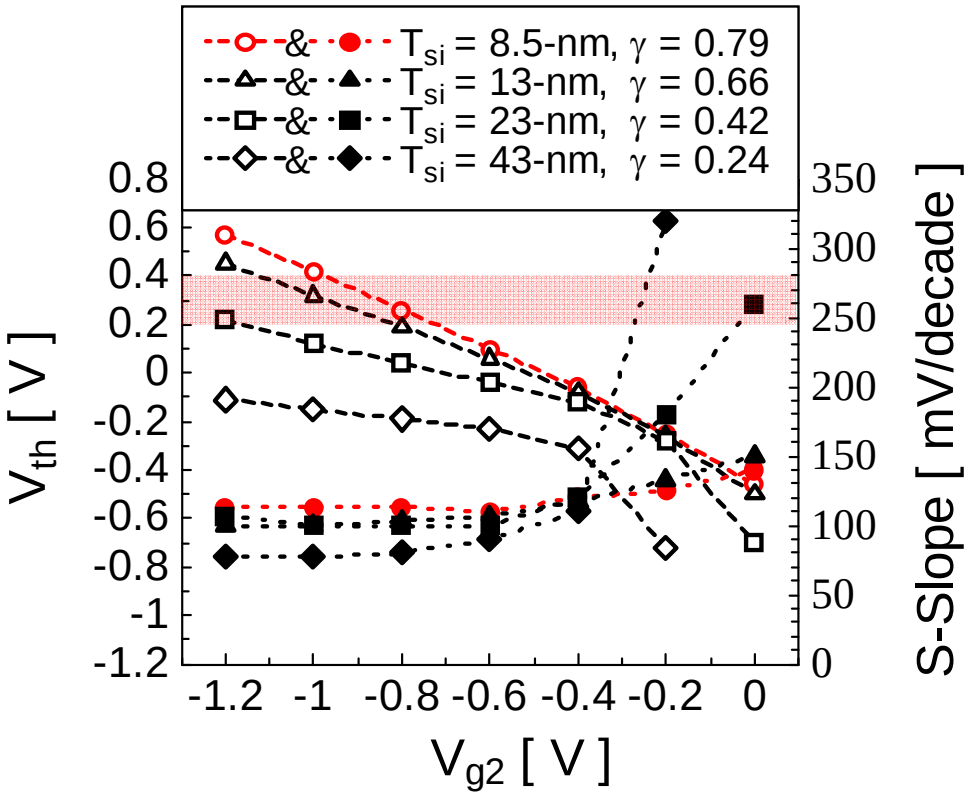
FinFET Formation and Lithography

DG Separation by LEB



Vth Tuning by Controlling Vg2





✓Vth can be tuned from LSTP to HP flexibly by selecting a proper Vg2 (The Second Gate)

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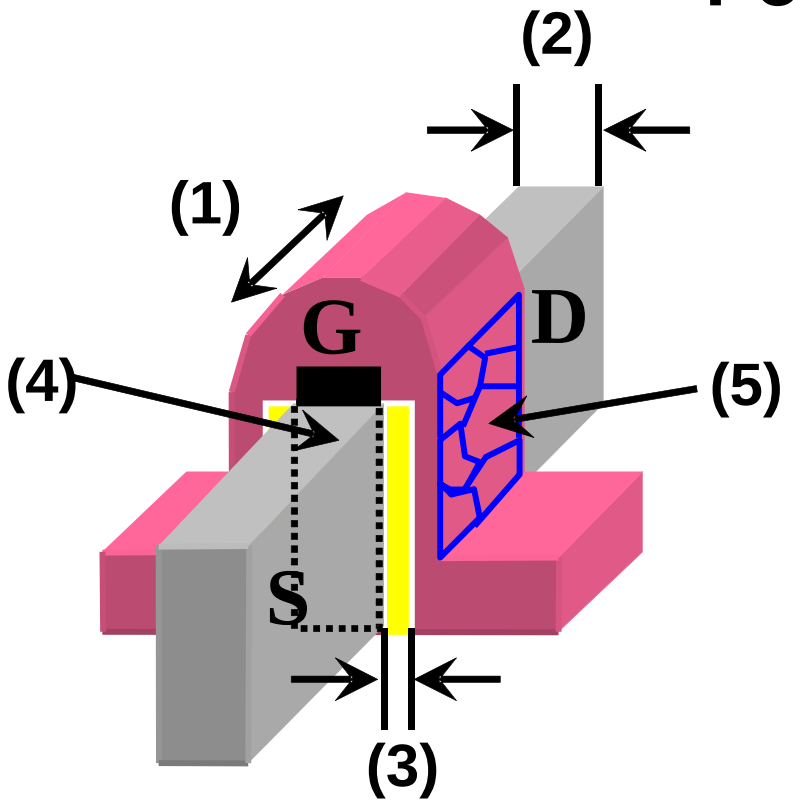
V_{th} Variation for MG FinFETs



Possible V_{th} Variation Sources

(1) Gate Length (L_g)

(2) Fin Thickness (T_{Si})

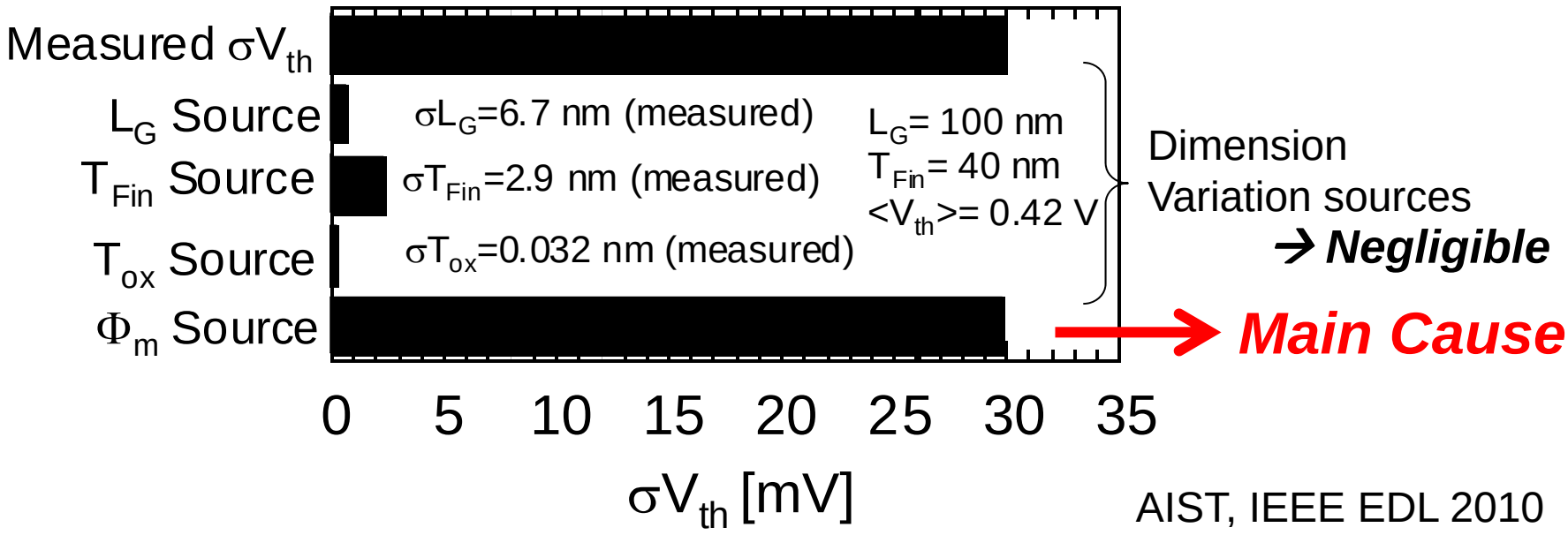
(3) Oxide Thickness (T_{ox})

(4) RDF

(5) Work Function WFV (Φ_m)

✓ FinFET variability sources were systematically analyzed

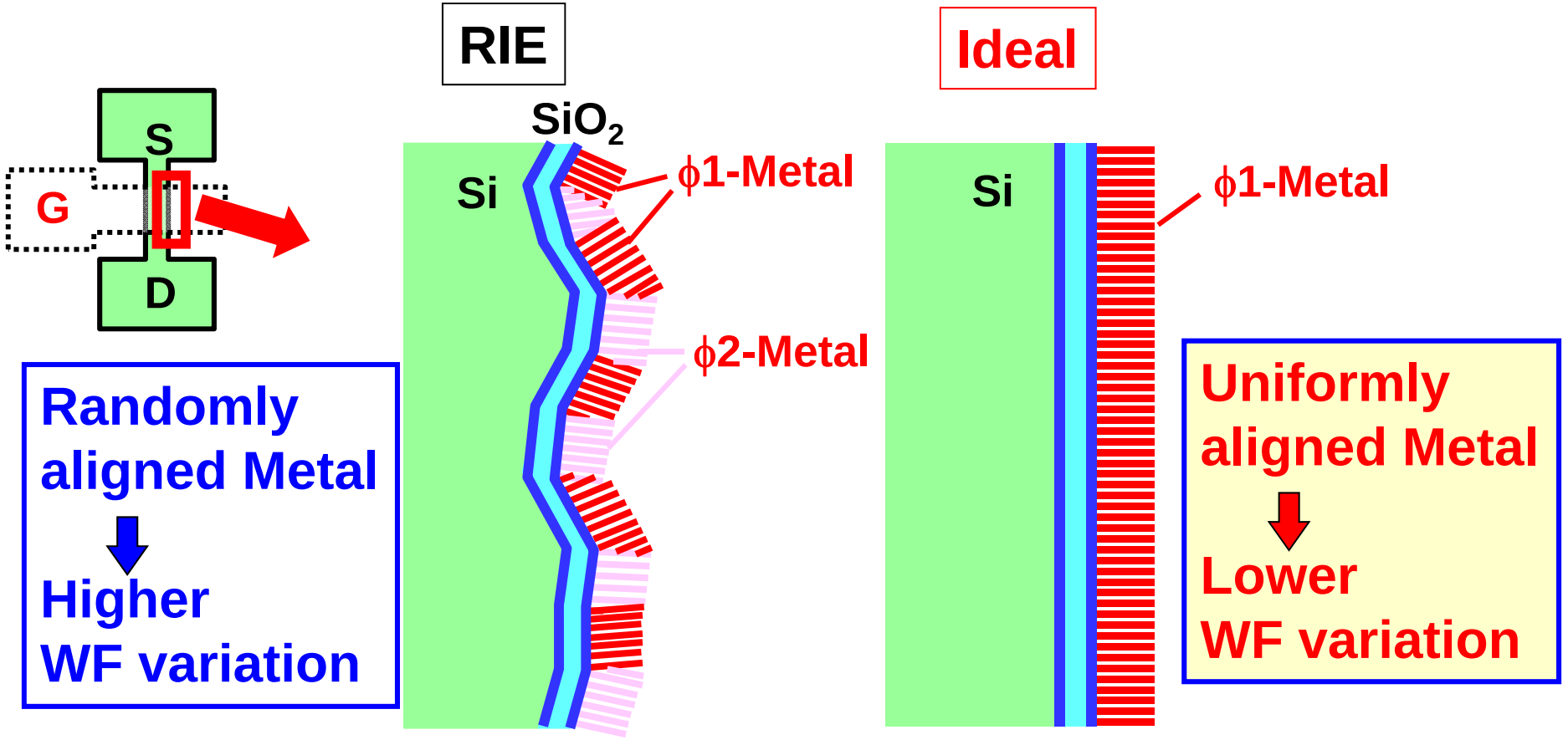
Main Cause of Vth Variation



AIST, IEEE EDL 2010

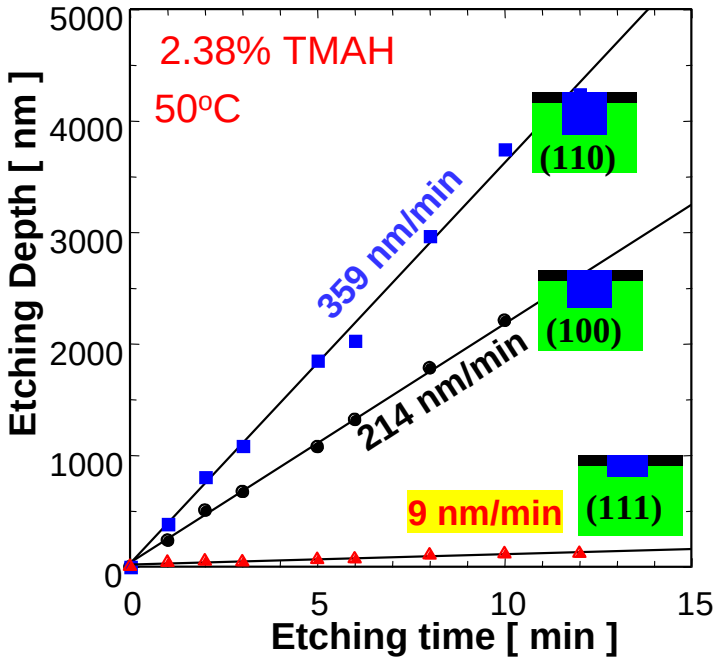
- ✓ Dimension variation sources are negligible
- ✓ Main cause of the V_{th} variation is the Workfunction Variation

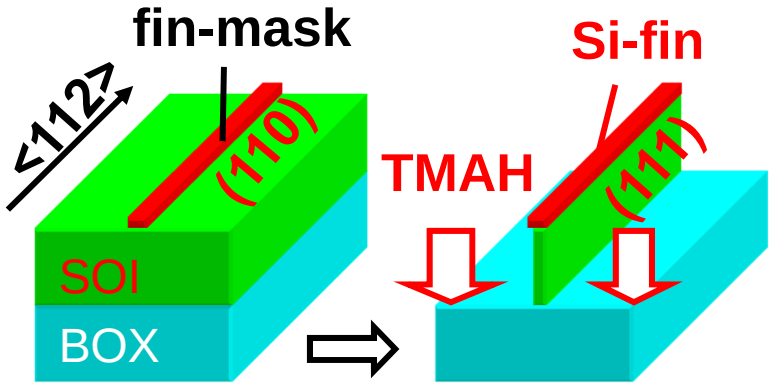
Workfunction Variation



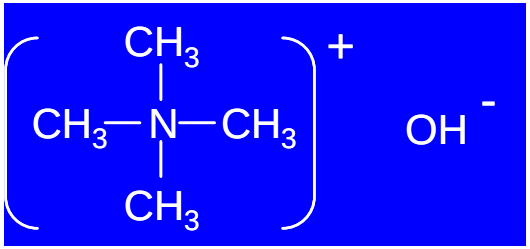
- ✓ Rough etched side wall causes randomly aligned metal grain and thus higher WF variation
- ✓ If side wall is flat, uniformly aligned metal grain and thus lower WF variation can be expected

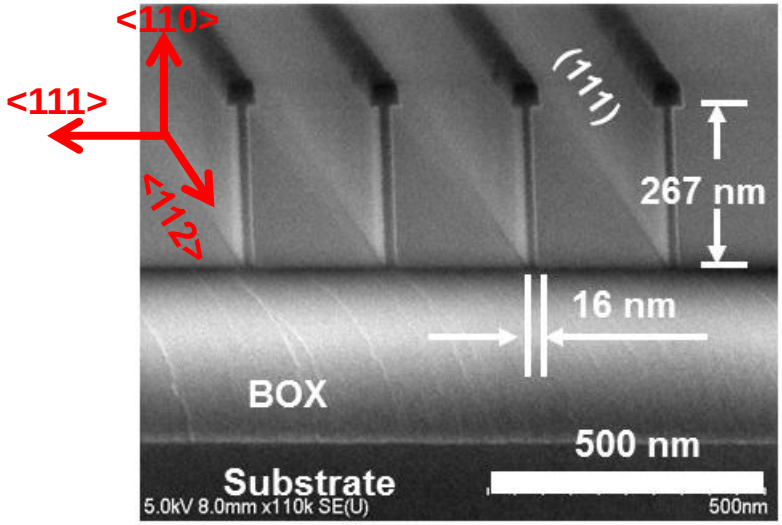
Nano-Wet Etching Process





Etchant:
2.38% TMAH (Resist Developer)
(Tetramethylammonium hydroxide)



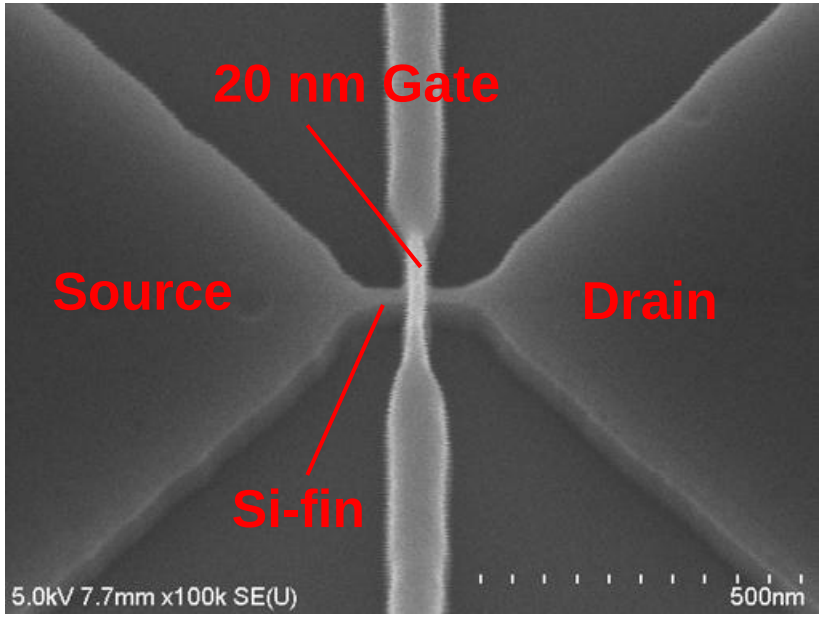


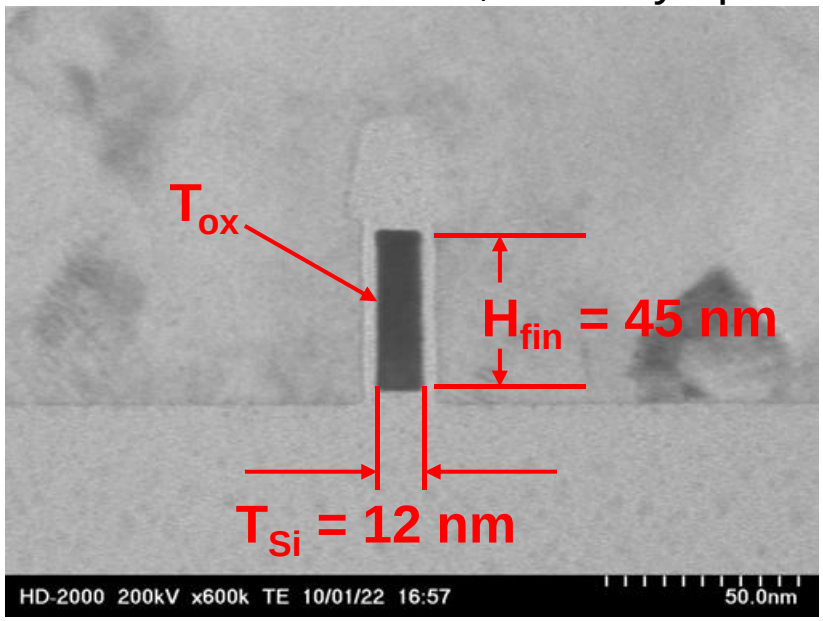
AIST, IEDM 2006

✓Extremely low ER of (111) in TMAH → Flat (111) side wall

SEM and STEM images of FinFET

AIST, VLSI Symp. 2010

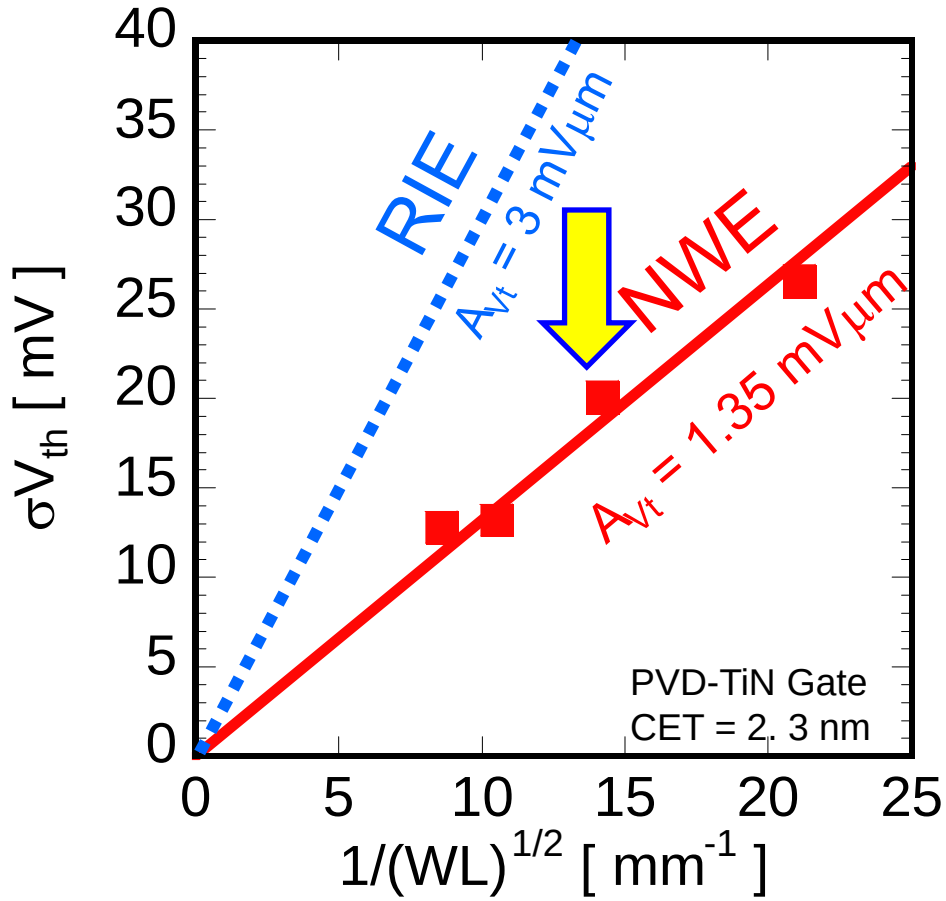




- ✓ Min.L_g = 20 nm, T_{Si} = 17.8 nm, H_{Si} = 45 nm
- ✓ Nano-Wet-Etched FinFET
- ✓ Undoped channel
- ✓ T_{ox}(CET) = 2.3 nm by C-V
- ✓ Gate Stack : PVD-TiN/SiO_2

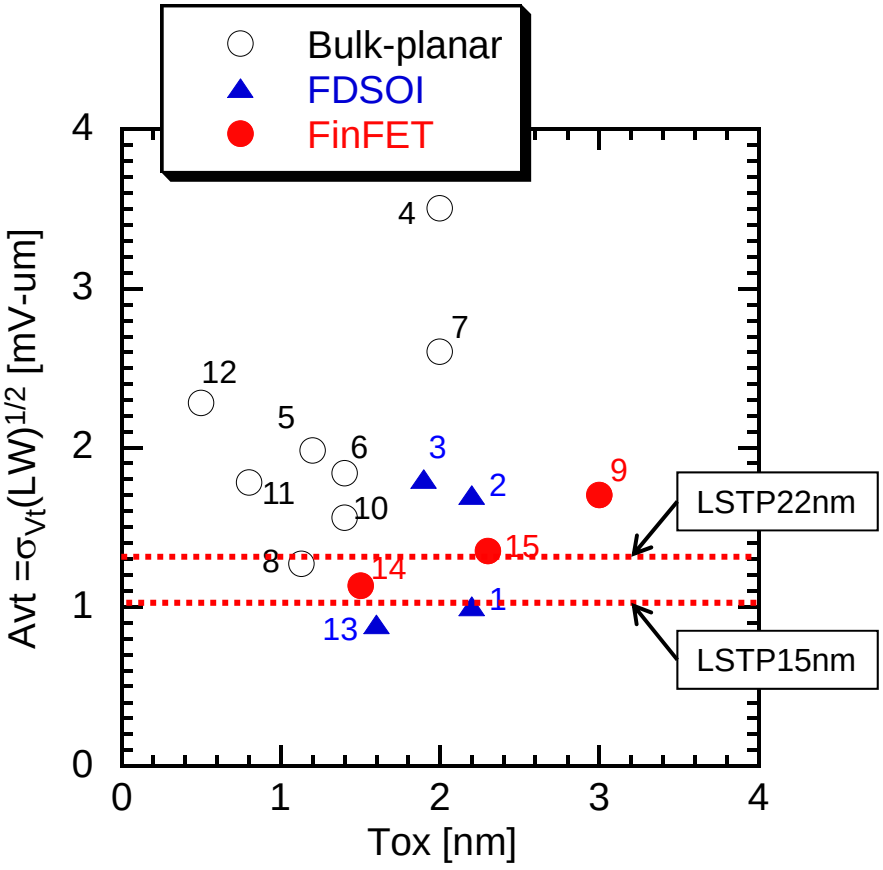
Measured σV_{th} for Nano-Wet-Etched FinFET

AIST, VLSI Symp. 2010



✓ A_{Vt} was significantly lowered by flattening the side channel

Avt Benchmark



List of reported A_{Vt} values

Ref. #	Device Structure	Gate Stack	Author.	Organi-zation	Reference
1	FDSOI	Poly/SiO2	A.Cathignol	ST	ESSDERC2006
2	FDSOI	TiN/HfO2	C. Fenouillet-Beranger	ST	IEDM2007
3	FDSOI (SOTB)	NiSi/	Y.Morita	Hitachi	VLSI2008
4	Bulk-planar	Poly/SiON	T.Tsunomura	Selete	VLSI2008
5	Bulk-planar	MG/HK	F.Arnaud	ST	IEDM2008
6	Bulk-planar	MG/HK	S.Hasegawa	Toshiba	IEDM2008
7	Bulk-planar	s-Si/SiON	H.Fukutome	Fujitsu	IEDM2009
8	Bulk-planar	HK/MG	M.Goto	Toshiba	VLSI2009
9	FinFET	Mo/SiO2	T.Matsukawa	AIST	VLSI2009
10	Bulk-planar	MG/HK	F.Arnaud	ST	IEDM2009
11	Bulk-planar	MG/HK	L.A.Ragnarsson	IMEC	IEDM2009
12	Bulk-planar	MG/HK	L.A.Ragnarsson	IMEC	IEDM2009
13	FDSOI	MG/HK	K.Cheng	IBM	IEDM2009
14	FinFET	TiN/HfSiO	T.Chiarella	IMEC	ESSDERC2009
15	FinFET	TiN/SiO2	Y.Liu	AIST	VLSI2010

T. Matsukawa, et al., (AIST.) SOI Conf, 2011, 7.1.

- ✓ Obtained Avt meets 22-nm-node SRAM requirement
- ✓ For 15nm and beyond, Avt should be further reduced

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Summary

- By introducing Ta/Mo dual metal gate technology, low V_{th} ($\pm$0.2V) can be obtained for CMOS FinFETs.
- By separating the DG, Vth can be tuned from 0.2V to 0.4V flexibly.
- Flattening of Si-fin sidewall channel is very promising for reducing Vth variations.

This work was supported in part by NEDO