Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications

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Editors

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ISBN 978-0-387-95867-5 e-ISBN 978-0-387-95868-2
DOI 10.1007/978-0-387-95868-2
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2009934298

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Printed on acid-free paper

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This book is dedicated to my wife Anat for all her support and patience.

Preface

In **Advanced ULSI interconnects – fundamentals and applications** we bring a comprehensive description of copper-based interconnect technology for ultra-large-scale integration (ULSI) technology for integrated circuit (IC) application. Integrated circuit technology is the base for all modern electronics systems. You can find electronics systems today everywhere: from toys and home appliances to airplanes and space shuttles. Electronics systems form the hardware that together with software are the bases of the modern information society. The rapid growth and vast exploitation of modern electronics system create a strong demand for new and improved electronic circuits as demonstrated by the amazing progress in the field of ULSI technology. This progress is well described by the famous “Moore’s law” which states, in its most general form, that all the metrics that describe integrated circuit performance (e.g., speed, number of devices, chip area) improve exponentially as a function of time. For example, the number of components per chip doubles every 18 months and the critical dimension on a chip has shrunk by 50% every 2 years on average in the last 30 years. This rapid growth in integrated circuits technology results in highly complex integrated circuits with an increasing number of interconnects on chips and between the chip and its package. The complexity of the interconnect network on chips involves an increasing number of metal lines per interconnect level, more interconnect levels, and at the same time a reduction in the interconnect line critical dimensions.

The continuous shrinkage in metal line critical dimension forced the transition from aluminum-based interconnect technology, that was dominant from the early days of modern microelectronics, to copper-based metallization that became the dominant technology in recent years. As interconnect critical dimensions shrank to the nano-scale range (below 100 nm) more aggressive interconnect designs on smaller scale became possible, thus keeping “Moore’s law” on pace. In addition to the introduction of copper as the main conducting material, it was clear that new dielectric materials, with low dielectric constant (“low-*k*” materials), should replace the conventional silicon dioxide interlevel dielectric (ILD). Thus the overall technology shift is from “aluminum–silicon dioxide” ULSI interconnect technology to “copper-low-*k*” technology. The Cu-low-*k* technology allows patterning of 45 nm wide interconnects in mass production and will probably allow further shrinkage in patterning of 15–22 nm lines in the next 10 years.

Copper metallization is achieved by electrochemical processing or processes that involve electrochemistry. The metal deposition is done by electrochemical deposition and its top surface is planarized (i.e., made flat or planar in the industry jargon) by chemical mechanical polishing (CMP). Electroplating is an ancient technique for metal deposition. Its application to ULSI technology with nano-scale patterning was a major challenge to scientists and engineers in the last 20 years. The success in the introduction of copper metallization so that it became the leading technology demonstrated the capability and compatibility of electrochemical processing in the nano-scale regime. In this book we will review the basic technologies that are used today for copper metallization for ULSI applications: deposition and planarization. We will describe the materials that are used, their properties, and the way they are all integrated. We will describe the copper integration processes and a mathematical model for the electrochemical processes in the nano-scale regime. We will present the way we characterize and measure the various conducting and insulating thin films that are used to build the copper interconnect multilayer structures using the "damascene" (embedded metallization) process. We will also present various novel nano-scale technologies that will link modern nano-scale electronics to future nano-scale-based systems.

Following this preface we bring an introduction where we bring the fundamentals of Cu electroplating for ULSI – when electrochemistry meets electrical engineering.

In Part II we give a historical review describing interconnect technology from the early days of modern microelectronics until today. It describes materials, technology, and process integration overview that brings into perspective the ways metallization is accomplished today. Further understanding of the scaling laws is presented next. Both semiconductor and interconnect progress are described, since they are interwoven into each other. Progress in interconnects always follows progress in transistor science and technologies. Although this book focuses on interconnect technology it should be clear that interconnects link transistors and the overall circuit operation is achieved by combined interaction of a highly complex network. The basic role of interconnects in such networks and how interconnects performance is linked to overall circuit performance are discussed next. One of the key issues in the increasing complex system is whether there are also other paradigms. One such paradigm is the 3D integration of ULSI components, also known as "3D integration."

In Part III we present a detailed review of interconnect materials. There is no doubt that the advancement in materials science and technology in recent years was the key to the advances in the ULSI technology. There are few groups of materials in ULSI interconnects: conductors (e.g., copper, silicides), barrier layers (e.g., Ta/TaN, TiN, WC), capping layers (dielectrics such as nitride-doped amorphous silicon or silicon nitride or electroless CoWP), and dielectrics with a dielectric constant less than that of silicon dioxide (i.e., low-k materials). We dedicate a special part to the material properties of silicides (metal–silicon compounds) that are used as the conducting interfacing material between the metallic interconnect network and the semiconductor transistors. The following parts bring an intensive review of low-k materials. They pose a major challenge since they should compete with

the conventional silicon dioxide that, although its dielectric constant is higher, has excellent electrical and mechanical properties and whose process technology is well established and entrenched in the industry and research communities.

In Part IV we focus on the actual electrochemical processes that are used for ULSI interconnect applications. We will first present the copper plating principles and their application to sub-micron patterning. Additives will be described in light of their role in the fully planar embedded metallization technology (i.e., the damascene process). In addition to conventional process we also mention some novel processes. Among them, the atomic layer deposition is the most promising and is under intensive investigation due to its ability to form ultra-thin seed layers with excellent uniformity and step coverage. Other interesting nano-scale processes are the deposition of nano particles, either inorganic or organic, that yield nano-scale metal lines that may, one day, be used for nano-electronics applications.

A common approach that links basic modeling to actual structure is the use of computer-aided design (CAD) simulating the desired structure based on the fundamental physical and chemical models of the process. For example, the use of electrochemical deposition onto narrow features with critical dimensions below 100 nm and with aspect ratio (i.e., the ratio of height to width) more than 2 to 1 requires a special process that is called "superfilling." In such a process, the filling of the bottom of the feature is much faster than the deposition on its upper "shoulders." Rapid deposition and full deposition onto the feature is achieved without defects (e.g., voids, seams) and with relatively thin metal on the shoulders that can be reliably removed in the ensuing chemical mechanical polishing planarization step. The discovery of the "superfilling" process was a major breakthrough in the initial stages of the introduction of copper metallization. In Part V we give a detailed description of such modeling of copper metallization using electrochemical processes for nano-scale metallization.

Part VI links all the previous parts together and describes the actual fully planar embedded metal process that is known as the damascene process. Following a detailed description of the various damascene concepts and its associated process steps we discuss the process integration issues. The integration involves linking all the various components: starting at the lithography level, patterning the wafer, deposition of the barrier and seed layers followed by the copper plating and its chemical mechanical polish (CMP) planarization, and ending with capping layer deposition. In this part we focus on the basic roles of each one of the components in the overall integration issue and on the way we put them all together.

Part VII describes the basic principles of the tools that are used for the copper metallization. There are two families of tools that we describe here – tools for deposition and tools for chemical mechanical polishing (CMP). Plating tools, both for electroplating and for electroless plating, are described in detail emphasizing their relation to the damascene process as applied for ULSI applications, i.e., material properties and integration in the manufacturing line.

Another family of tools is the one used for metrology and inspection. We present in Part VIII the innovative and advanced tools that are being used for Cu nanotechnology. One of the most promising tools is the use of X-ray technology, especially

X-ray reflection (XRR), which has proven to be the only method suitable for ultra-thin barrier layers and for porous materials that are used for low dielectric constant insulators. Another interesting development in modern planarization technology is the capability for in-line metrology. We present recent innovations in this field using optical metrology that is integrated with chemical mechanical polishing processes.

Finally, in Part IX we present a full and comprehensive review of the most promising interconnect technologies for future nanotechnology. This part includes a complete review of novel nanotechnologies such as bio-templating and nano-bio interfacing. Another key issue is the role of interconnect with future computation and storage technology. In this part we review the role of interconnect and 3D hyper integration, spintronics, and moletronics. In summary this part and the following prolog lay forth the reasons why electroplating is considered as the key technology for nano-circuits interconnects.

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Acknowledgments

We would like to thank all the contributors to this book. Each one of them is a leader in his field and the contributions are highly appreciated.

We also would like to thank Dr. Ragini Raj Singh and Ms. Rakefet Ofek-Almog from Tel Aviv University for the tedious work of editing, formatting, and communicating with the various authors. The devoted work of Dr. Singh allowed the successful completion of this book.

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Part I
Introduction

Chapter 1
Challenges in ULSI Interconnects – Introduction to the Book

Y. Shacham-Diamand

Ultra large-scale integration (ULSI) technology is one of the most dominant and important technologies of the 21st century. It is the base for the global electronics system industry.

Our current information society is based on information technologies that have been developed in the last decade. Information technologies emerged as a result of developments in silicon-based integrated circuits (ICs) that are the "engines" that collect, process, and distribute information (Fig. 1.1). The rapid development in highly complex hardware, allowing both digital and analog signal processing, conditioning, and dissemination, was accompanied by developments in software allowing better command and control of the hardware. All of this became possible due to the invention of the integrated circuit, first on germanium (Kilby 1958) [1] and next on silicon (Noyce 1959) [1], and the rapid development toward ultra large-scale integration (ULSI) using complementary metal oxide semiconductor (silicon) (CMOS) technology.

The integration of few devices on chip was started as small-scale integration (SSI), followed by medium-scale integration (MSI), large-scale integration (LSI), very large-scale integration (VLSI), and finally ultra large-scale integration (ULSI). The integrated circuit includes transistors as the switching devices and interconnects that interface the switches between themselves and the external world. Typical integrated circuit (IC) dimensions are between few millimeters (length or width) and few centimeters. It is laid on a thin (slightly less than 1 mm) single-crystal silicon wafer forming arrays of chips. The chips are separated by narrow scribing lanes that define boundaries along them; the chips are later separated and packaged. For a detailed description of the ULSI processing the reader is referred, for example, to references [2] and [3].

The term ULSI was coined when the critical dimension of the patterns within the micro-chips reached the range of 0.25 μm. Current ULSI circuits have features with dimensions in the nanoscale region (smaller than ∼100 nm). This reflects the transition from the era of micron-scale electronics into the nanoscale era. The

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Y. Shacham-Diamand et al. (eds.), *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications*, DOI 10.1007/978-0-387-95868-2_1,
© Springer Science+Business Media, LLC 2009

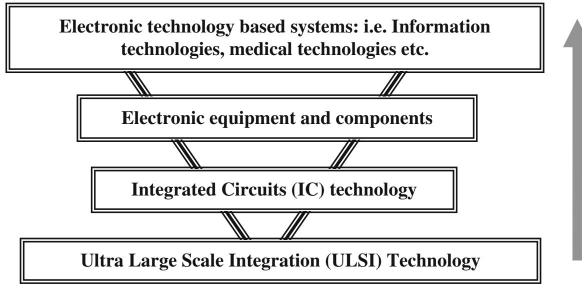

Fig. 1.1 The electronic technology-based hierarchy – from ULSI technology up to electronic technology-based systems

technology that is currently used for ULSI manufacturing is a "top-down" manufacturing, i.e., alternating patterning using optical lithography and ULSI process modules for removing materials (i.e., etching), adding materials (i.e., deposition, growing), or modifying materials (i.e., doping, silicidation). For a detailed description of ULSI technology status and forecast the reader is referred to the International Technology Roadmap for Semiconductors (ITRS) [4].

According to the ITRS 2006 report on interconnects [4], the most difficult and challenging issues for near future interconnects manufactured with dimensions of 32 nm and above are the following:

- Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity.
- Engineering manufacturable interconnect structures compatible with new materials and processes.
- Achieving necessary reliability.
- Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.
- Manufacturability and defect management that meet overall cost/performance requirements.

Along with those specific issues there are always the issues of patterning, cleaning, filling at the nanoscale dimensions, integration of new processes and structures, and mitigating size effects. The challenges refer to both local interconnects and global wiring scaling issues which may affect circuit layouts and architecture to accommodate higher clock rate and better thermal engineering.

The ITRS 2006 report on interconnects [4] forecast for the year 2013 is that interconnect ½ pitch will be 32 nm for both memories and processing circuits. The total interconnect length will be up to 3125 m/cm^2 with 13 metallization levels and 4 optional levels for ground planes and capacitors. The metallization pitch of 64 nm

will be with Cu lines with aspect ratio of 1.9 (height/width) for micro processor units (MPUs) that can carry a maximum current density of 8.08×10^6 A/cm^2. The contact aspect ratio is expected to be up to 20 for dynamic random access memories (DRAM) which have more regular and, hence, denser layouts than MPUs. The delay of such Cu lines depends on their length, their driving circuit, and the capacitive load for both their sides and at their end. For a 1 mm long line the delay of a minimum size wire will be ~3.45 ns assuming that the effective specific resistance of such lines will be in the range of 4.83 μΩ·cm.

Longer term forecast for the year 2020 assumes 28 nm pitch for the metallization, 14 metal layers, total interconnect length of 7243 m/cm^2, aspect ratio of 2 (height/width), maximum current density of 2.74×10^7 A/cm^2, and an RC delay for a 1 mm long line of ~23.4 ns, assuming that the effective specific resistance of such lines will be in the range of 8.2 μΩ·cm. Note that one of the key problems that will limit Cu interconnects in the far future is the rapid increase in the line-specific resistivity due to size-dependent scattering and the effect of barriers that reduces the effective cross section of the Cu lines.

1.1 Material Issues in Cu Interconnects

One of the key challenges for ULSI interconnect technology is related to the materials that are used for manufacturing the ULSI ICs. In Table 1.1 we summarize the most important conducting materials and some of the most important properties.

We classified the materials according to their main applications:

a. Conductors – used as conductors. The most common conductor for ULSI ICs today is copper, the main topic of this book.
b. Silicides – mainly used for contacts; however, they can also be used for local interconnect applications [5].
c. Barrier layers – used to protect the silicon and the interlevel dielectrics (ILD) from the hazardous effects of Cu [6]. They are also used to protect Cu against corrosion due to the interaction with air or with the following deposition processing steps.

One key problem in copper metallization is the effect of scaling on the resistivity. The effect of scaling becomes noticeable when the vertical and lateral dimensions of the lines become comparable to the electrons' mean free path (Table 1.2) in the metal [7].

The size effect also depends on the quality of the metal interface which affects the nature of the scattering, i.e., specular vs. diffusive. Improving the interface smoothness at the atomic level and reduction of surface defects may assist in keeping the effective resistivity and its distribution in a useable range. Otherwise, the line

Table 1.1 ULSI material properties (* – thin film)

	Resistivity (μΩ·cm)	Young's modulus (GPa)	TCR (%/°C)	Thermal conductivity (W/cm/°C)	CTE (ppm/°C)	Corrosion resistance in air	Melting point (°C)
Conductor							
Cu	*1.7–2.2	130	0.43	3.98	16.5	Poor	1084
Ag	1.59	83	0.41	4.25	19.1	Poor	
Au	2.35	78	0.4	3.15	14.2	Excellent	
Al	*2.7–3.0	70	0.45	2.38	23.5	Good	660
W	*8–15	411	0.48	1.74	4.5	Good	3410
Silicide							
PtSi	28–33					Excellent	1229
$TiSi_2$	13–16					Excellent	1540
WSi_2	30–70					Excellent	2165
$CoSi_2$	15–20					Excellent	1326
NiSi	14–20					Excellent	992
Poly Si (heavily doped)	500–1000					Excellent	1410
Barriers							
TiN	50–150					Excellent	2950
$Ti_{0.3}W_{0.7}$	75–200					Excellent	2200
TaN	>150					Excellent	
CoWP	25–80					Excellent	

Table 1.2 Electron mean free path in the conducting metals [7]

Metal	Mean free path, λ (nm)
Tungsten	14.2
Aluminum	14.9
Gold	35.5
Copper	39.3
Silver	52.7

resistance will be too high and circuits will not be able to operate at high enough frequency.

The second family of materials are the insulators that isolate between the interconnect materials. The most common material that is being used is the silicon dioxide that is deposited by chemical vapor deposition (CVD), which is typically enhanced by plasma (plasma-enhanced CVD – PECVD) allowing deposition at low temperatures (below 400°C). Silicon dioxide has excellent mechanical and electrical properties; it is compatible with CMOS processing and can be deposited with a very low defect density. However, as the critical dimension of interconnects had been scaled to the range of 90 nm and below the issue of interconnect delay became the limiting factor of the whole integrated circuit.

1.2 Interconnect Performance Issues

Interconnect affects the performance of the circuit. Here is a short list of the main performance variables that characterize ULSI ICs:

- Speed – it depends on the delay due to the loading of the parasitic capacitances of the lines and the series resistance of the conducting lines (interconnects) and the switching devices. We refer to this as "RC delays."
- Power dissipation – the dynamic power dissipation is proportional to the parasitic capacitance, to the power supply squared, and to the clock frequency. There is also some utilization factor that may take into consideration the average actual transition rate between logical states per unit time, which is only a fraction of the clock frequency that describes the maximum possible transition rates between logic states.
- Cost – interconnects define a significant part of the chip and they affect its area, thus the number of chips per wafer, and the wafer yield; both factors that affect cost. Interconnects also require many lithography and patterning steps that are a significant factor of the overall cost of manufacturing.
- Defect density – there are many interconnect layers and each one has a large number of components. Therefore, significant number of defects, such as shorts and opens, are related to the interconnect process. It also definitely affects the cost of manufacturing.

Lowering the RC delay is possible by one of the following ways:

a. reducing the interconnect resistance – reducing the metal-specific resistance;
b. reducing the parasitic capacitance – lowering the dielectric constant of the inter-level dielectrics;
c. optimizing the interconnect geometry – optimizing the aspect ratio, improved layout on critical points;
d. improved device properties – higher current-driving capabilities;
e. improved circuit design – adding repeaters, use of transmission lines [8, 7].

Note that all of the above are a subset of the overall requirements which also include requirements for manufacturability, cost performance, and thermal management.

Reducing the interconnect resistance was achieved by the transition from aluminum to copper metallization. Improving the copper-effective resistance is achieved by lowering its barrier layer thickness and improving its interface properties. Lowering the parasitic capacitance is possible by using dielectric materials with a lower dielectric constant – low-*k* dielectrics. Intensive study of both organic and organic dielectrics with low dielectric constant has been underway and it yields few interesting materials that are considered as candidates to replace silicon dioxide. Low-*k* materials are classified as solid and porous

materials, where the porous materials offer lower dielectric constant; however, their porosity generates some major processing challenges.

The absolute value of resistance and capacitance is also determined by the lines' actual dimensions. Therefore, the overall interconnects' layout plays an important role on the chip performance. Due to the high complexity of current ULSI chips, which may contain $>10^8$–10^9 devices and interconnects, it is difficult to simulate the overall chip performance. Therefore, although there are current "known best methods" for layout the problem is far from being solved and there is a dire need for better algorithms improving the layout and achieving better performance.

Improving the device properties has been achieved recently by the following ways:

a. Using bipolar devices with the CMOS circuits – this technology, known as BiCMOS, includes bipolar devices which have better current-driving capabilities than MOS transistors. It is used for driving high capacitive loads such as long buses and interfacing pads.
b. The introduction of silicon on insulator technology – lowering the source/drain parasitic capacitances eliminates significance of the devices' parasitic capacitance, therefore allowing better performance, i.e., higher speed at lower dissipated power.
c. The successful implementation of SiGe (Silicon–germanium) technologies. There are few possibilities that are being explored:
    c.1. p-type MOS transistors with improved current-driving capabilities and
    c.2. strained silicon transistors where the conduction is in single crystal silicon and the SiGe technology is used to apply the stress.

The last option improving interconnect performance is by improving the circuit design, for example, adding repeaters and choosing logic design with the least number of transitions between stages for the given application if possible (for reviews of on-chip interconnect the reader is referred to references [8, 7, 9]).

1.3 Interconnect Process Issues

A key development in modern ULSI manufacturing was the introduction of the Damascene process by P. Andricacos and his colleagues from IBM in 1998 [10]. The transition from the old aluminum process, which uses negative lithography, to the new Cu process (see Fig. 1.2), using positive lithography, revolutionized the industry.

Altogether Al-negative patterning was well established and yielded excellent results; it was impossible to apply it to copper patterning because Cu has no volatile species in conventional plasma etch processes; therefore, it was impossible to use conventional photoresist-based lithography for Cu patterning. In addition to this the transition to deep lithography preferred planar surface since the depth of focus

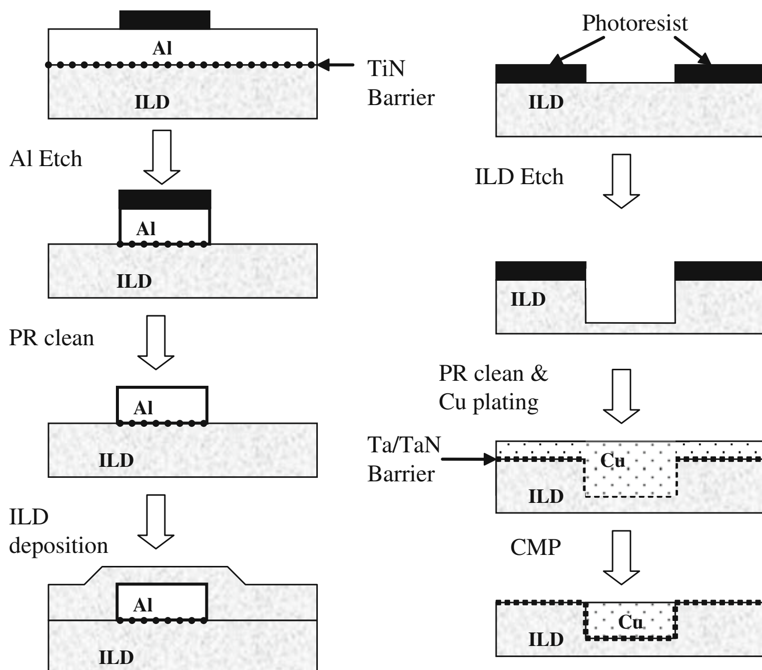

Fig. 1.2 The "old" Al-negative patterning (*left*) vs. the "new" single Damascene-positive patterning (*right*)

became comparable to the thin film thickness. This requirement leads to an additional planarization step of the interlevel dielectric.

Another issue that gave advantage to the fully planar Cu process was the ability to apply the Damascene process for both the lines and the contacts. This process is called "dual Damascene" where the lines and the contacts are etched first and the metal is deposited only once onto the whole metal level before it is planarized by chemical mechanical polishing (CMP). Compare this to standard Al process where the contact requires an additional tungsten deposition step followed by a planarization step. We summarize the Cu Damascene process on the conventional Al process in Table 1.3.

The need to use positive patterning for copper yielded a better process than Al patterning with superior resolution and less processing steps. This allowed lowering the cost of the metallization process which is a significant part of the overall cost of manufacturing since there many metallization levels require many tools and manufacturing facilities. Since the equipment cost and building are a major part of IC manufacturing, no wonder that the industry adopted the copper dual Damascene process although it was a new and immature process compared to the well-established and mature Al processing. This was at the end of the 1990s, while today most of the problems in the dual Damascene have been solved and it is the dominant Cu patterning technology.

Table 1.3 The advantage of the Cu dual Damascene process

	Cu dual Damascene	Al lithography
Lithography	Normally fully planar→ • better resolution	Requires an additional ILD planarization step to achieve full resolution
Etching	ILD etch→ • Only one material • Better process control	Etching two materials→ • Metal etch: Al and barrier • ILD etch: via definition process
Contacts	Cu contacts→ • Same material • Same deposition step	W contacts→ • Additional deposition step • Additional planarization step • Additional interface between the Al wire and the W plug
Planarization	One planarization step	Two planarization steps
Deposition	• One metal deposition step • One barrier deposition step • One ILD deposition step	• Two metal deposition steps: Al and W • One barrier deposition step • Two ILD deposition steps
Metal deposition	• Cu electroplating • Barrier sputtering • Capping layer by sputtering or electroless plating	• Al sputtering • W chemical vapor deposition

Among the few issues debated in the 1990s regarding the application of the dual Damascene process was the method of deposition of Cu. There were few possible options:

a. physical deposition – either by evaporation or sputtering;
b. chemical vapor deposition – CVD or PECVD;
c. electrochemical deposition methods – electroplating (EPD or ECD) and electroless plating (ELP).

Electrochemical deposition (ECD) emerged as the winning technology due to its superior filling capabilities of narrow trenches with high aspect ratio [10]. This was achieved due to the "superfilling" phenomena that were intensively investigated by many researchers. Commercial tools for Cu electroplating for ULSI metallization were conceived in the 1990s and became available recently along with high-quality deposition solution that contained Cu ions and additives allowing good superfilling [12]. The availability of sub-100 nm Cu nano-wires using electroplating for ULSI application was the result of efforts of many people, research institutes, and companies. It depicted the highlight of using electrochemical processes for nano-technologies applications. There are still many problems in process [11] and equipment [12]; however, it seems that scaling to 32 nm interconnect is possible. Recently few other methods have been introduced such as atomic layer deposition (ALD) of barriers [13, 14] and Cu seed layers [15] that may significantly improve Cu nano-wire processing for ULSI.

In this book we cover the latest issues in Cu nano interconnect technology for ULSI applications. We focus on the electrochemical issues related to Cu nano-wires applications. In this book the issues that are briefly described in this introduction are outlined one by one. While the majority of the Cu nano-technology issues are related to ULSI application, there are possible other applications. Therefore, we present in the last chapter a brief review and forecast of some promising electrochemical-based nano-scale metallization schemes for various applications mostly related to electronics.

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Part II
Technology Background

Part II presents the technological background for interconnect in ULSI systems. It includes detailed description of MOS device and interconnects scaling physics (Chapter 2). Chapter 3 is about electrical performance of Cu interconnects for ULSI applications. It is well known that the steady growth in complexity of integrated electronic systems requires a growing number of metal interconnect layers in ULSI chips. The role of interconnects in integrated electronic systems is described in this chapter: Metrics for evaluating the quality of signal interconnections are presented, and simple electrical circuit models for interconnects are introduced. In light of these models, the fundamental problem of interconnect scaling is presented and design approaches for addressing the problem are briefly surveyed. As there are lots of deposition techniques, either electroless or electrodeposition, available elsewhere Chapter 4 presented a brief description of electrodeposition process and a focused discussion of copper electrodeposition for chip interconnects. It must be emphasized that different chip manufacturers have their unique combination of electrodeposition tools, proprietary tailored bath, and integration scheme for copper chip interconnects. Successful implementation of the copper electrodeposition process in high-volume chip manufacturing involves equal attention to metrology, process integration, and reliability issues. Besides void-free deposition of interconnect structures, selection of a reliable CMP process, excellent adherence of copper lines/vias to the dielectric, low resistivity, and resistance to electromigration are some of the key requirements for a high-yielding, reliable interconnect electrodeposition process. All these aspects are addressed in greater detail in different chapters of this book. Along with this Chapter 5, "Electrophorectic Deposition," defined the process of electrophoretic depositionand the process is summarized. The limitations of the process are explained and potential applications in the microelectronics sector are identified. Three areas in which industrial feasibility has been explored are then described in more detail. In addition to deposition technologies, proper device integration technology is important. As wafer-level 3D integration (i.e., 3D stacking prior to singulation of wafers into individual chips) has become an increasingly active research topic, without any large-scale IC manufacturing, Chapter 6 "Wafer Level 3D Integration for ULSI Interconnects" presents types of 3D integration, BEOL-based wafer-level 3D processing and wafer-level 3D design opportunities. Wafer-level interconnectivity is extended to multiple device levels.

Chapter 2
MOS Device and Interconnects Scaling Physics

Marc Van Rossum

2.1 Device Fundamentals

2.1.1 The MOSFET Transistor

2.1.1.1 Basic Device Physics

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most common active device in today's integrated circuits. Its basic structure consists of a doped silicon well, with at the opposite ends two highly doped contact regions (the source and drain junctions) allowing the current to pass close to the well surface (Fig. 2.1). In an n-type MOSFET, the well region is p-type doped and the source and drain are n+ doped, whereas the reverse polarity scheme applies for p-type devices. CMOS circuits contain both n-MOS and p-MOS transistors combined to form various logic gates. The transistor body is electrically isolated from the surrounding circuitry by a thick "field" oxide. A third electrode (the gate), to which the input signal is applied, is sitting on top of the well. It consists of an electrical contact layer (usually heavily doped polysilicon with a metallic top layer) separated from the silicon substrate by a thin insulator film made of thermally grown silicon dioxide. The substrate is thus capacitively coupled to the gate electrode, making the MOSFET a nearly ideal switch element due to the high isolation between input and output.

The output signal modulation takes place by varying the potential of the gate with respect to the substrate, which affects the charging of the MOS capacitor. In an n-MOSFET for instance, a negative gate voltage induces a positive (hole) charge accumulation region under the gate insulator. At positive gate voltages, holes are repelled into the substrate, creating a depletion region with fixed negative charges due to the ionized acceptor ions. At even more positive voltages, a negative charge

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Y. Shacham-Diamand et al. (eds.), *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications*, DOI 10.1007/978-0-387-95868-2_2,
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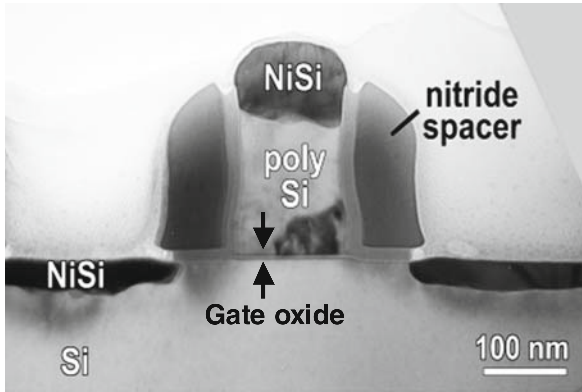

Fig. 2.1 The MOSFET transistor (IMEC)

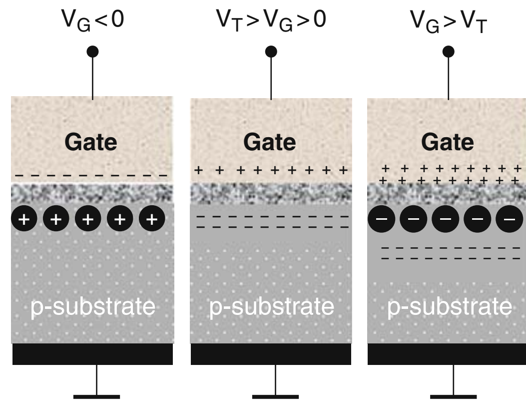

Fig. 2.2 Charge regimes of a MOS capacitor in n-MOSFET

inversion layer (i.e., with a negative charge imbalance) starts forming at the top of the depletion region by the minority carriers (electrons) that are attracted to the surface. The gate voltage that corresponds with the transition between the depletion and the inversion regime is called the threshold voltage V_T (Fig. 2.2).

According to the MOS capacitor model, the charge density Q_S induced into the substrate per unit area is linearly proportional to the applied gate voltage V_G:

$$Q_S = -(V_G - \psi_S)C_{ox} \tag{2.1}$$

where ψ_S is the band bending potential at the silicon surface and C_{ox} is the gate oxide capacitance expressed as

$$C_{ox} = \frac{\varepsilon}{t_{ox}} \tag{2.2}$$

with ε as the dielectric constant of the gate insulator and t_{ox} its physical thickness.