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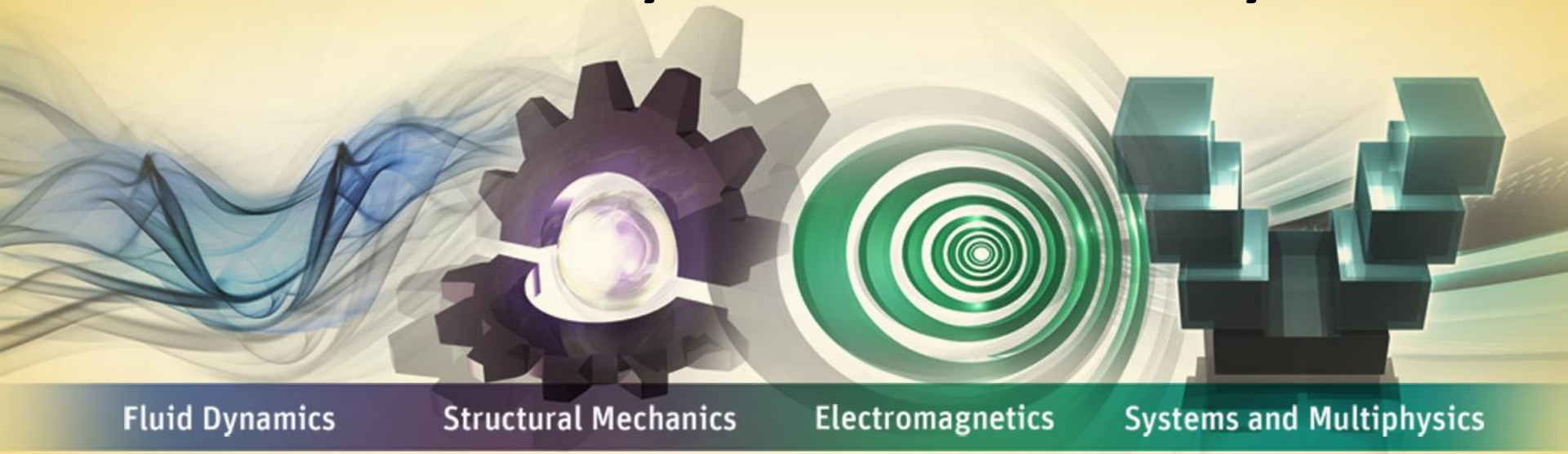
Advanced SI Analysis – Layout Driven Assembly



Tom MacDonald

RF/SI Applications Engineer II

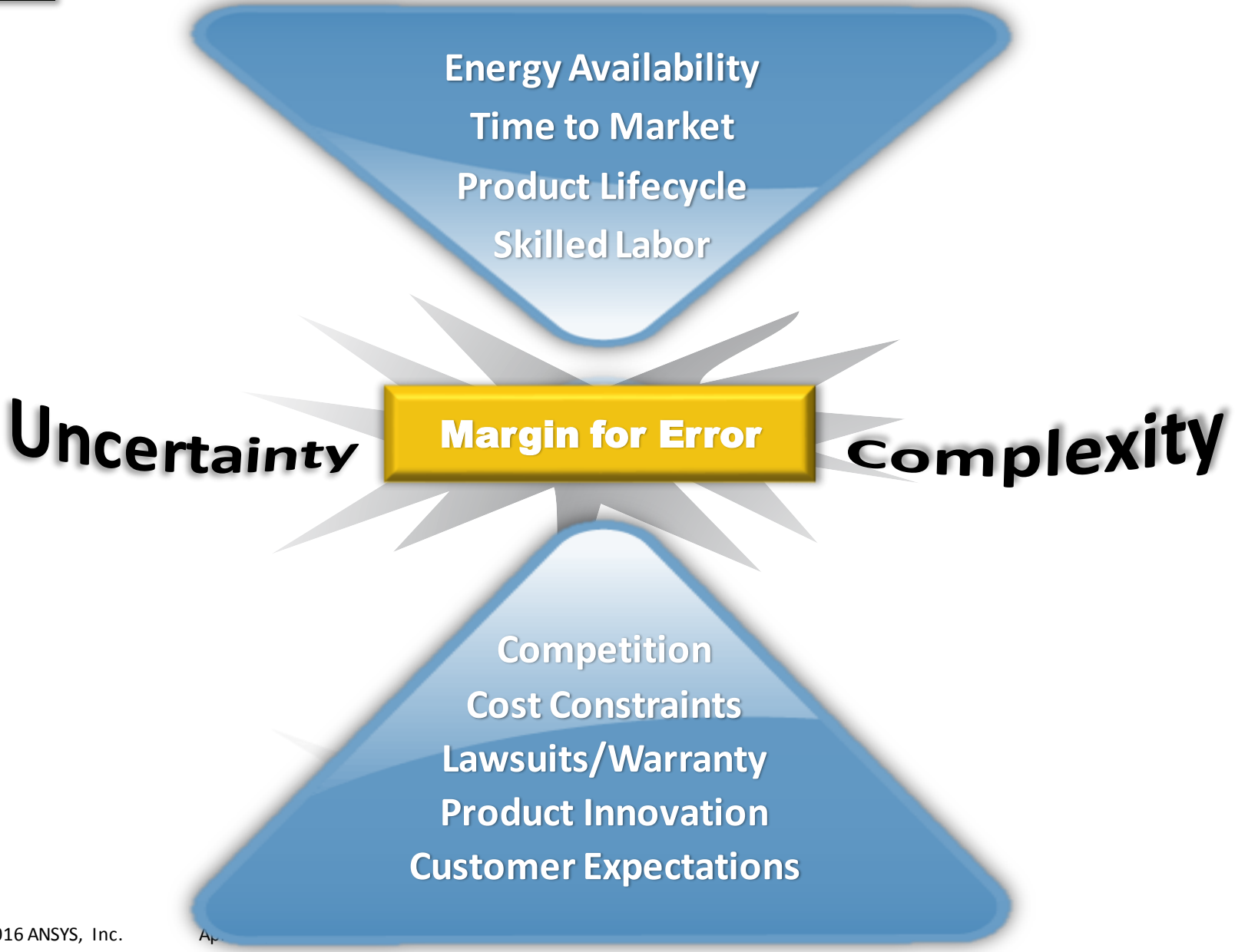
Abstract

As the voracious appetite for technology continually grows, so too does the need for fast turn around times and efficient techniques for characterization. To improve timeliness of turns, ANSYS SI product suite offers new functionality to enhance the user experience with layout driven assembly. By combining HFSS for connectors and HFSS 3D Layout for boards, this methodology allows us to apply current best solving techniques to our problems for optimal turnaround time and accuracy.

Agenda

- Design Pressures
- Layout Driven Assembly
- Multiphyics Board Analysis
- SIwave Workflow Enhancements
- Q & A

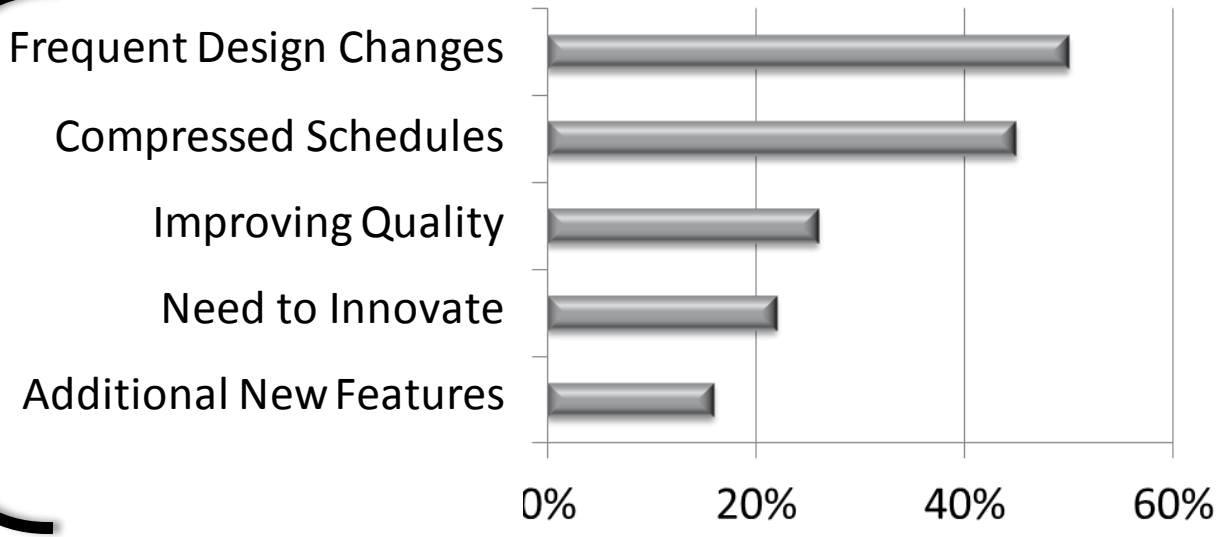
Customer Pressures



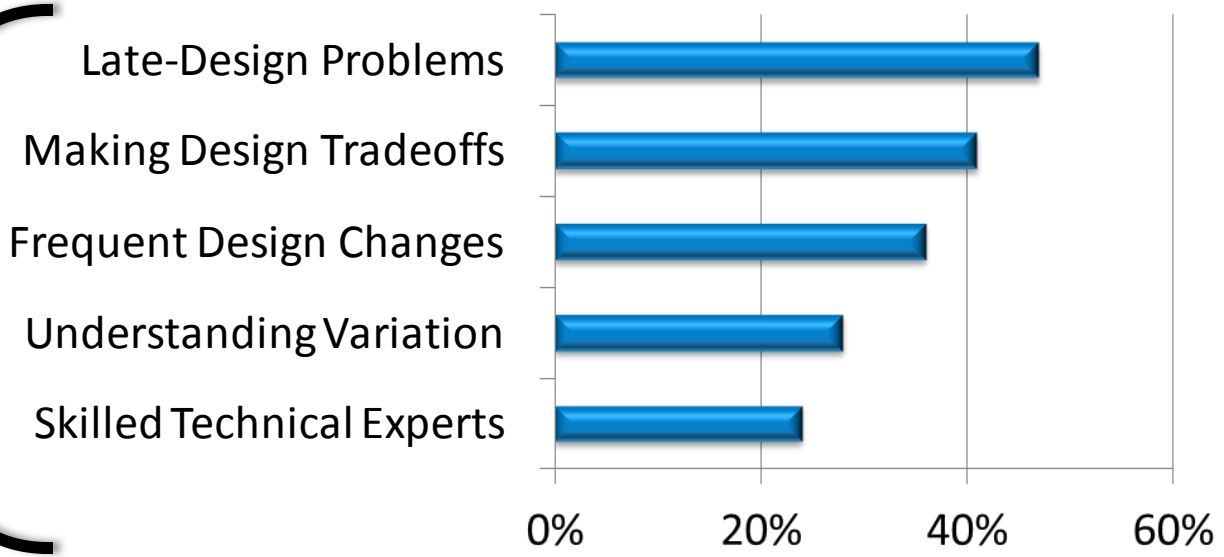
Getting Product Designs Right

Top Business Pressures Driving Product Design Improvement

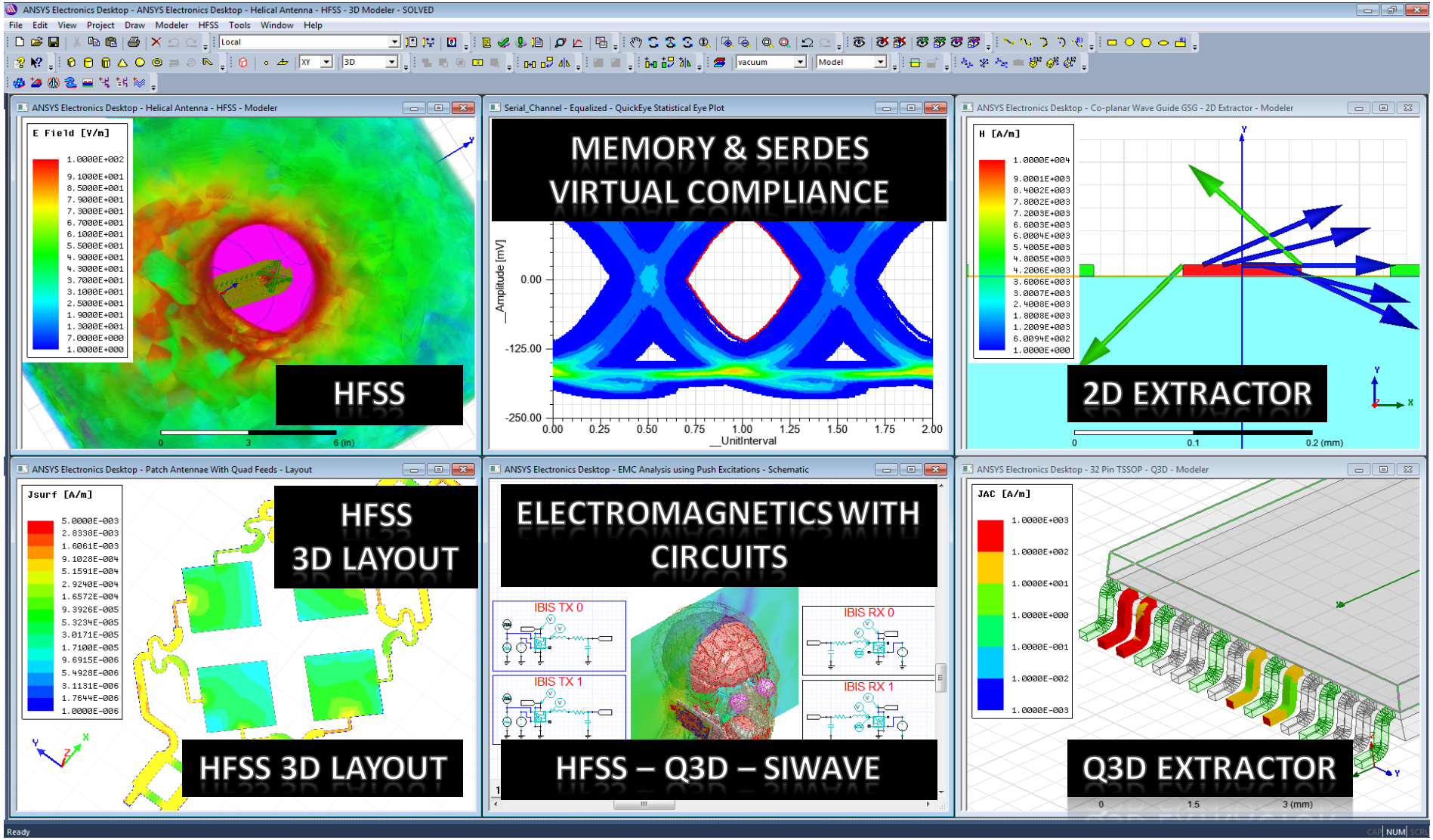
Source: Aberdeen Group, April 2011



Biggest Hurdles for Product Design



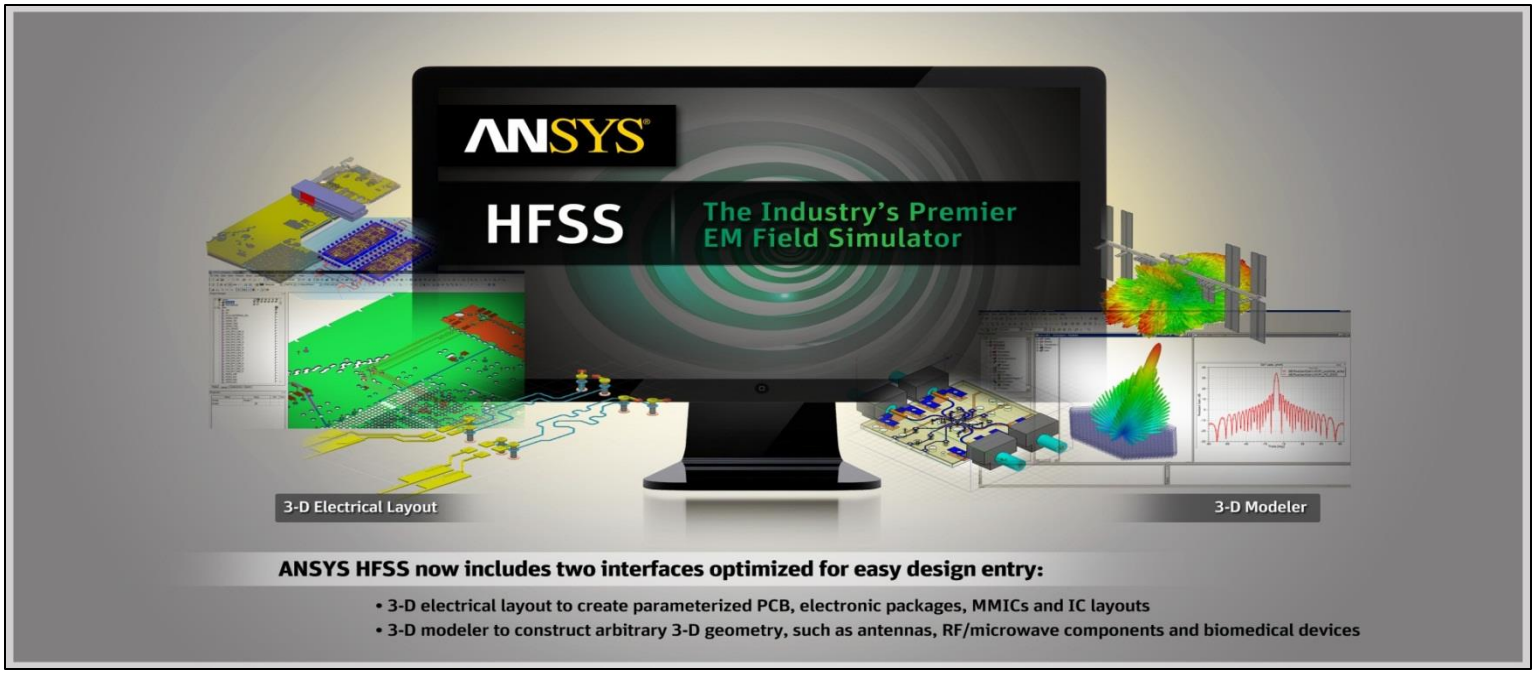
ANSYS Electronics Desktop



HFSS 3D Layout

HFSS interface optimized for layout designs

- Stackup editor
- Trace, pads, vias bond wires, solder bumps and balls
- Same 3D accuracy of HFSS in automated design flow



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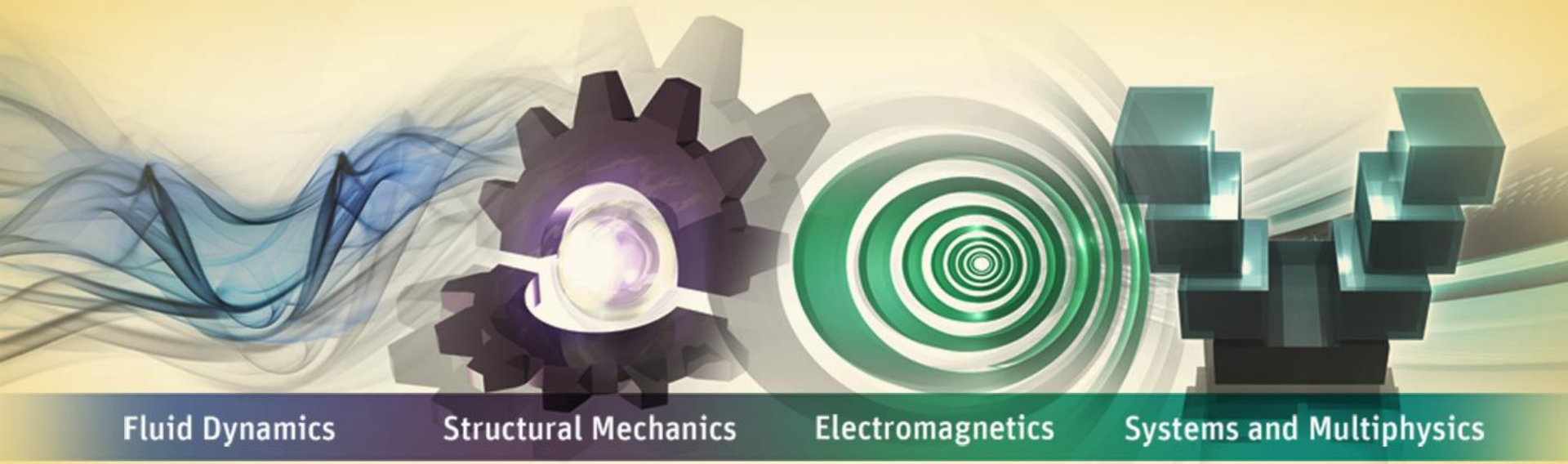
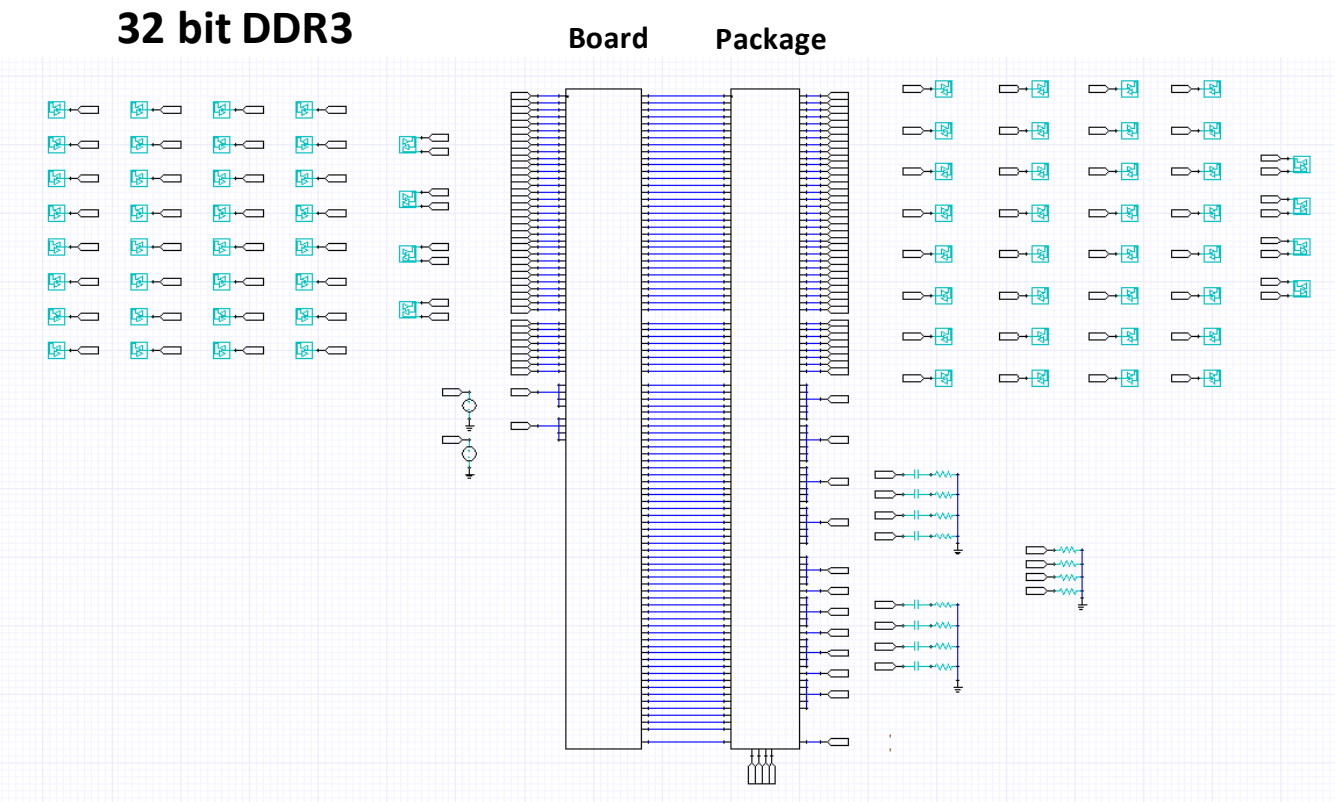
Layout Driven Assembly



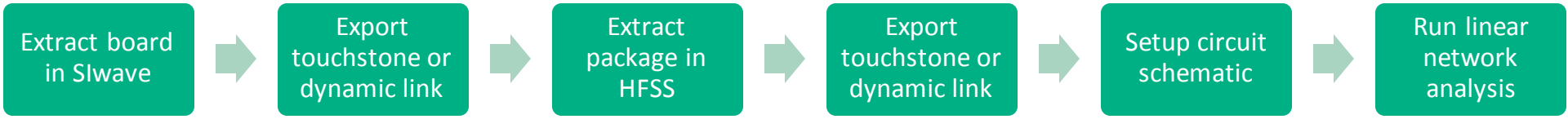
From Schematic Capture to Layout Driven Assembly

The old way of analyzing a package system plus a board



Package on Board Example

Last year…



Challenge: requires the use of 2-3 software packages

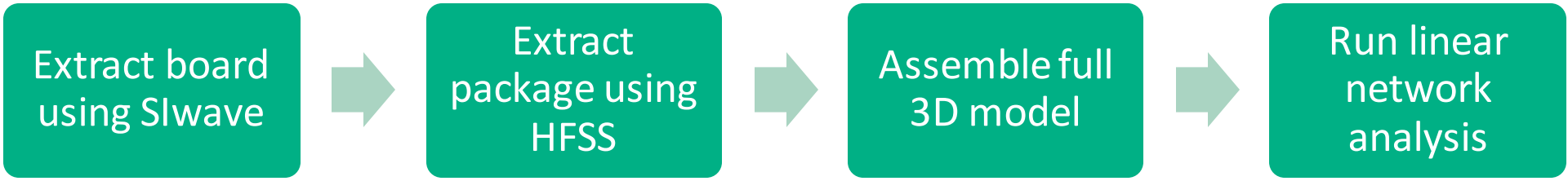
Next step: make a design change

Next step challenges:

- Keep track of touchstone revs
- Making changes to SIwave design (no variables)

Package on Board Example

Present Day…



Benefit: requires the use 1 software package (Electronics Desktop)

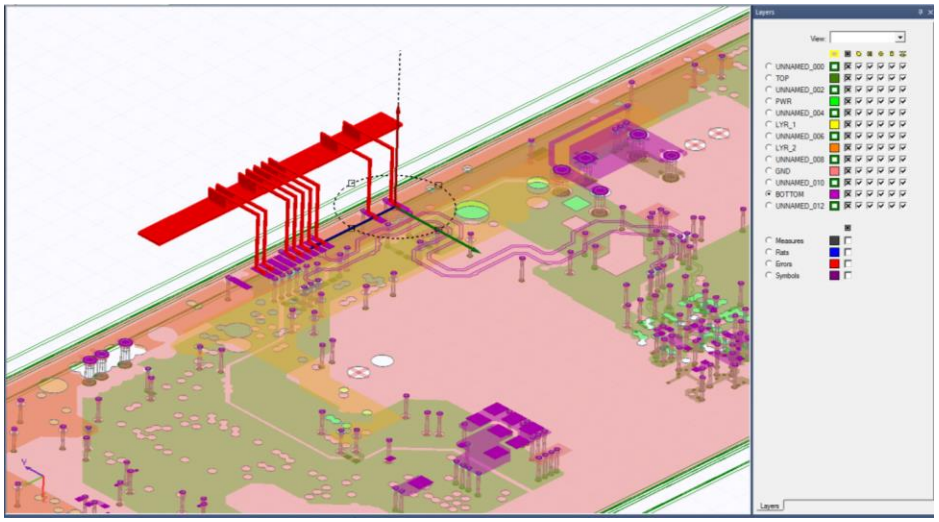
Next step: make a design change

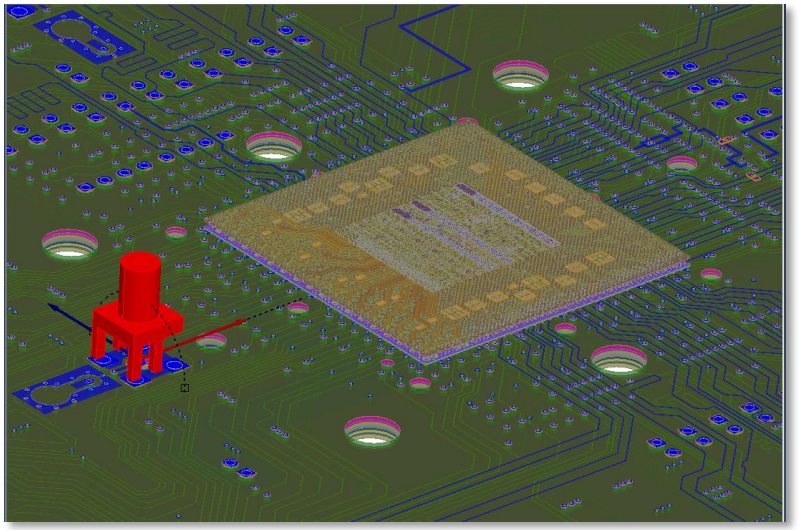
Benefits:

- **No need to keep track of touchstone revs**
- **Layout interface enables parametric SIwave designs**

System Verification

Layout-Driven Assembly in ANSYS Electronics Desktop





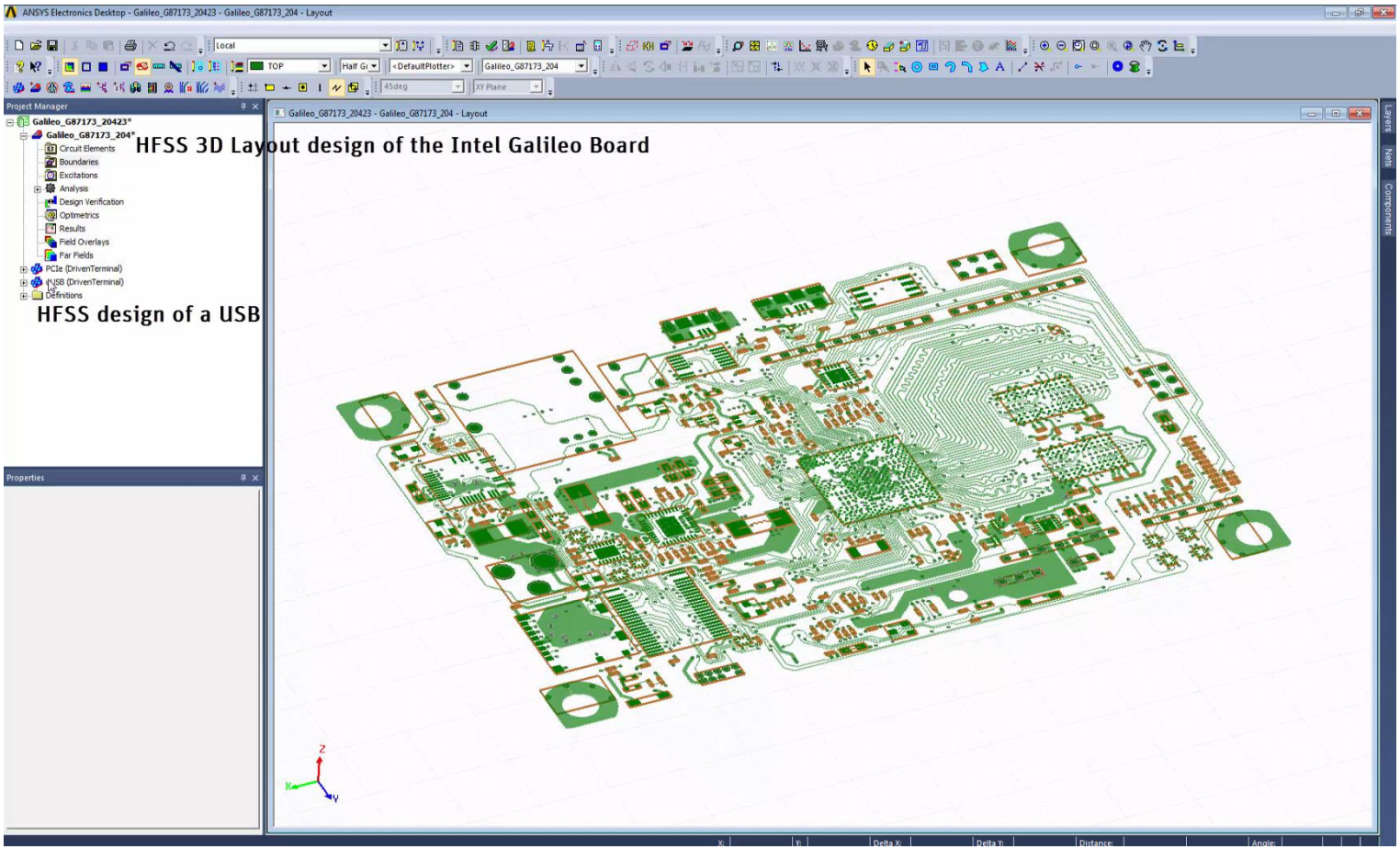
Place and connect components in Layout
Simulate components with 3D accuracy

ECAD and MCAD
HFSS, SIwave, Q3D

Apply automated circuit simulation to capture full system behavior

Ease-of-use drive 3D simulation for design engineers

Layout Driven Assembly



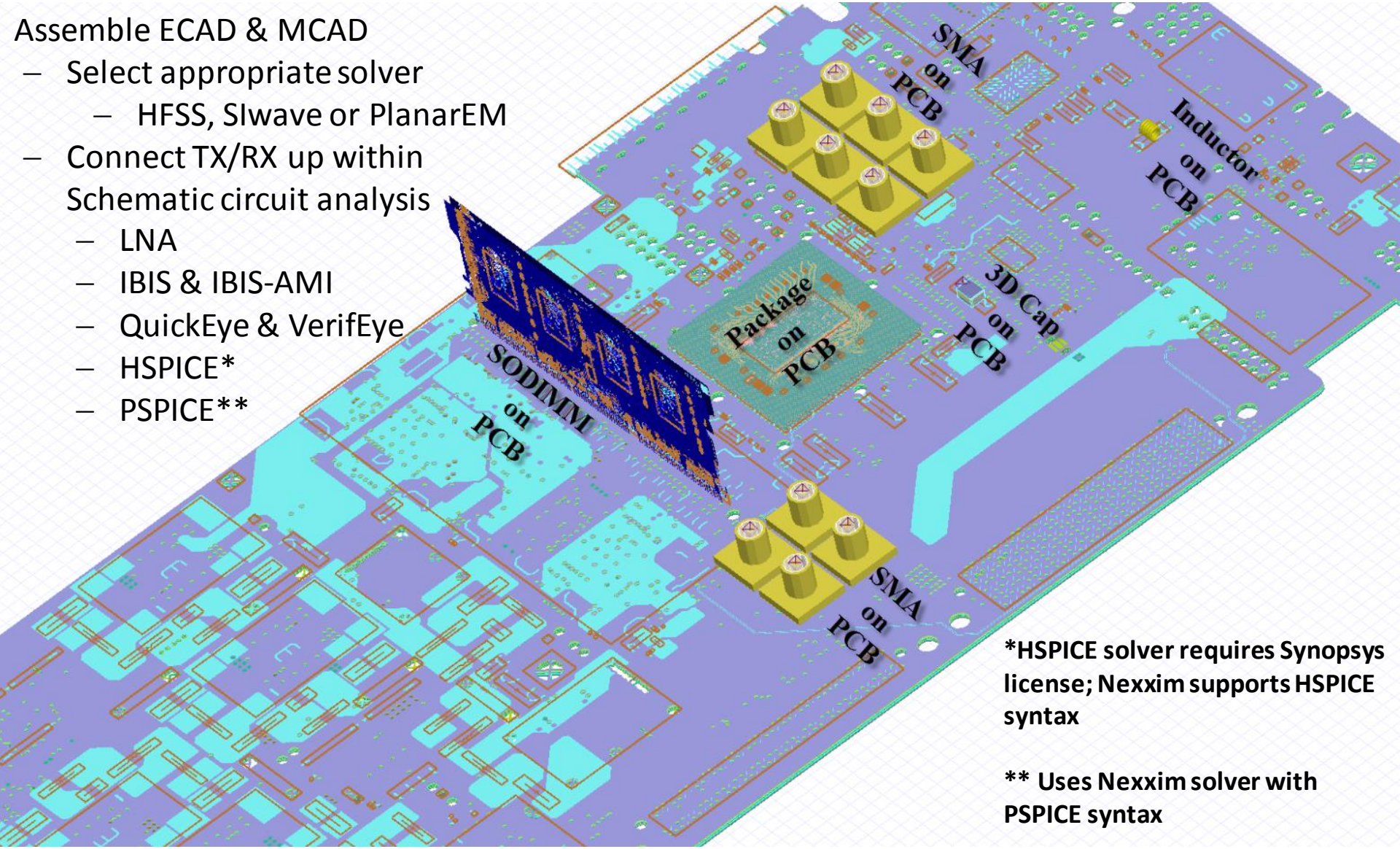
Reducing hands on engineering time

- **Eliminate error prone system wiring**

Virtual System Analysis with HFSS & SIwave

Assemble ECAD & MCAD

- Select appropriate solver
  - HFSS, SIwave or PlanarEM
- Connect TX/RX up within Schematic circuit analysis
  - LNA
  - IBIS & IBIS-AMI
  - QuickEye & VerifEye
  - HSPICE*
  - PSPICE**

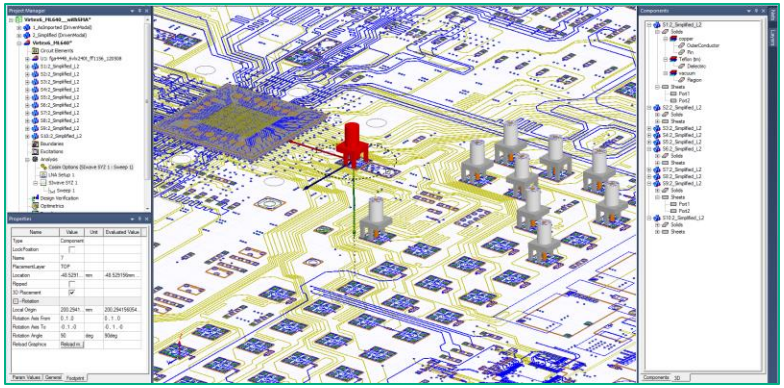


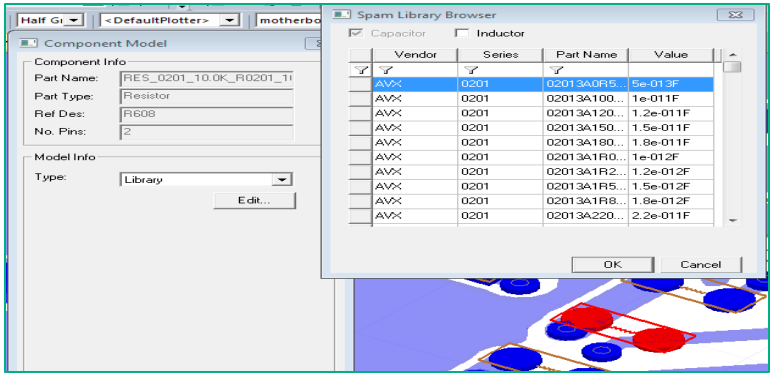
*HSPICE solver requires Synopsys license; Nexxim supports HSPICE syntax

** Uses Nexxim solver with PSPICE syntax

3D Layout: Key Features

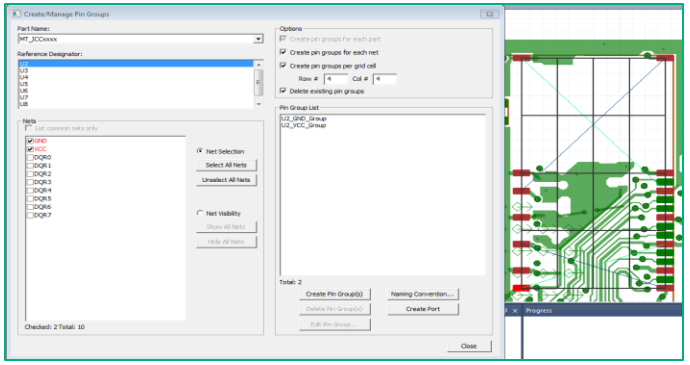
- HFSS 3D Dynamic Link in Layout
- 3D Placement and Positioning
- Improved Capacity and Layout Rendering





Linear Network Analysis for Co-simulation

- LNA Setup and automated Net listing
- Component Models



SIwave technology for large PCBs and packages

- SYZ Solver
- Geometry Checks

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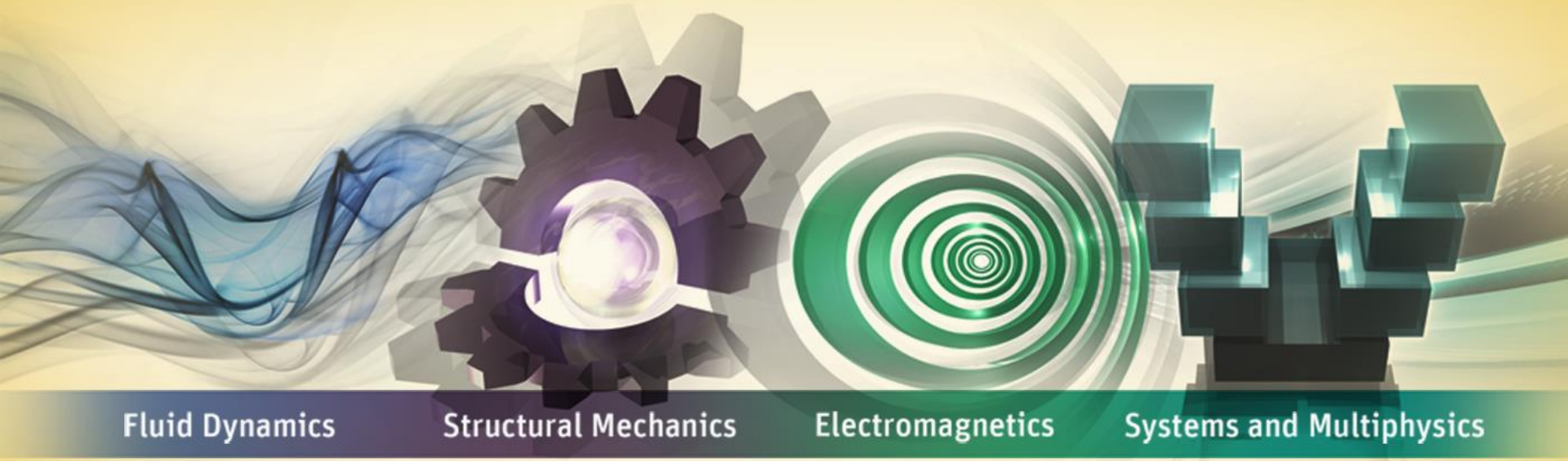
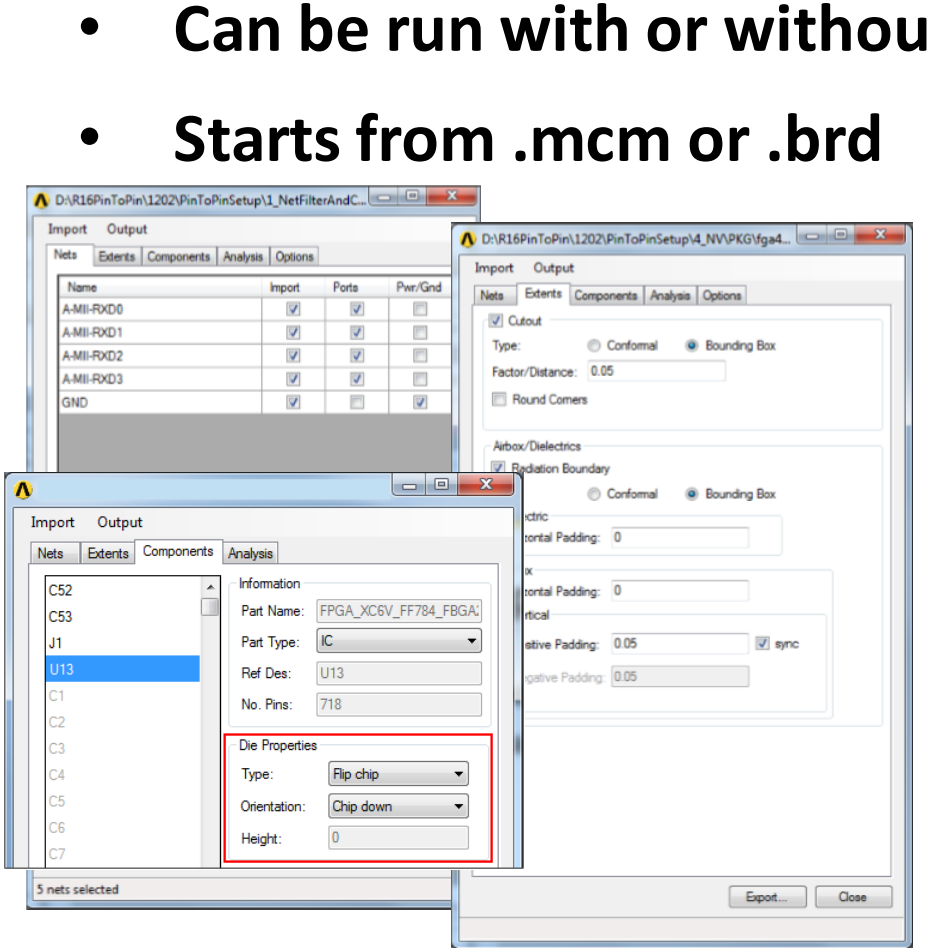
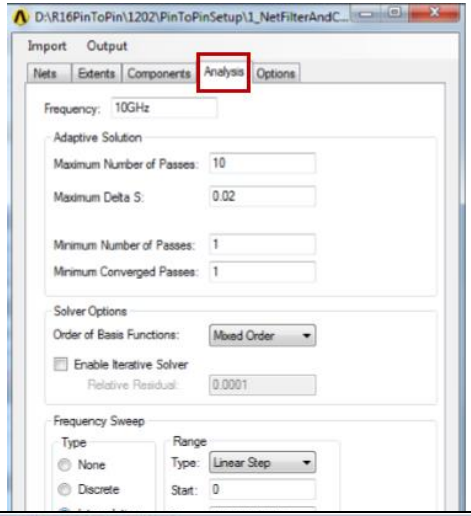
HFSS 3D Workflow Enhancements

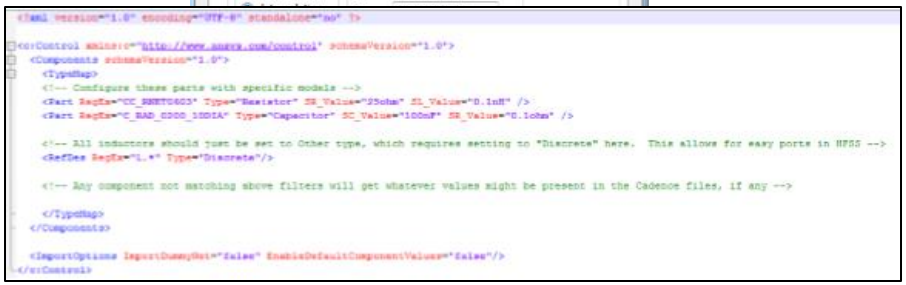


Pin2Pin Utility

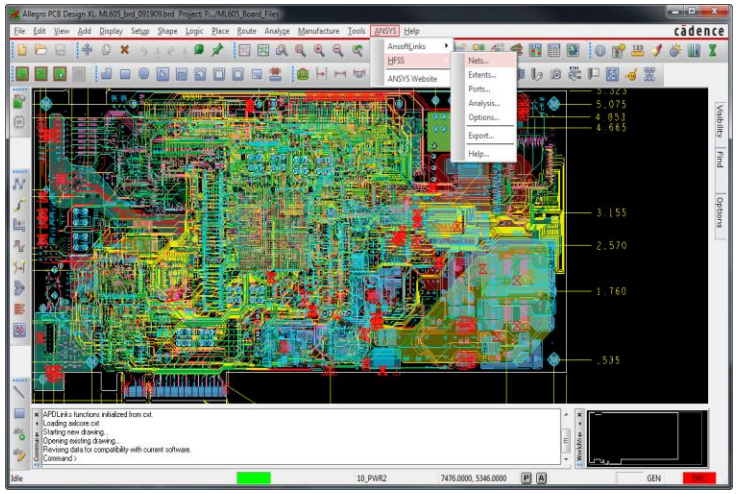
- .Net utility written to highlight layout automation
- Can be run with or without GUI
- Starts from .mcm or .brd



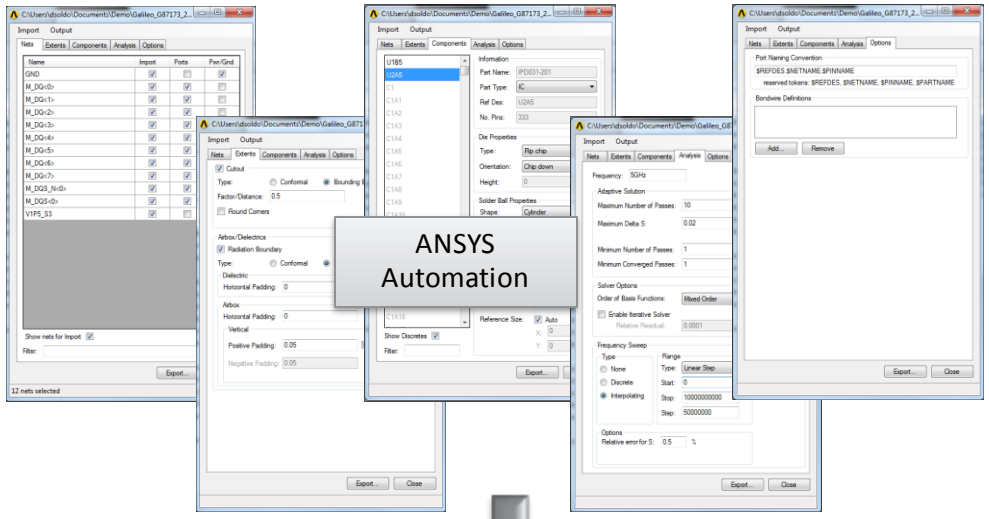




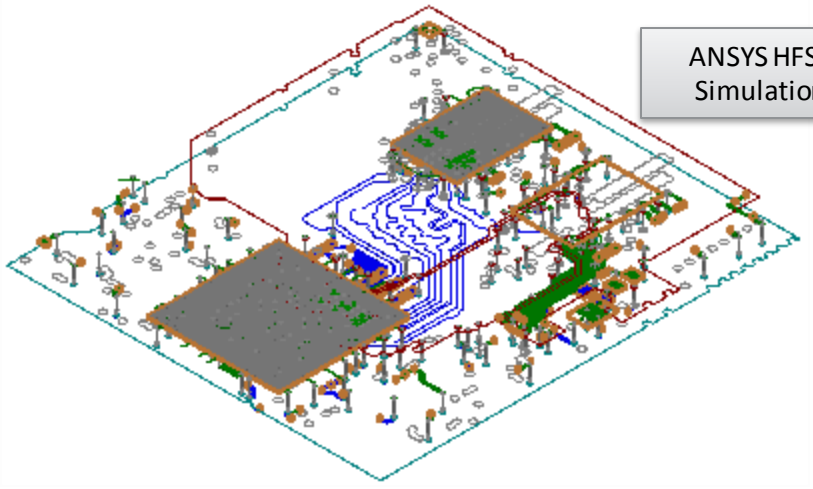
Cadence Automation



Layout



ANSYS Automation



ANSYS HFSS Simulation

Simulation Democratization

- Time is best spent in design exploration and results analysis
- Unfortunately, a lot of time is spent preparing the model for simulation
- Automation of pre-processing would free up more of the engineer's time for design innovation

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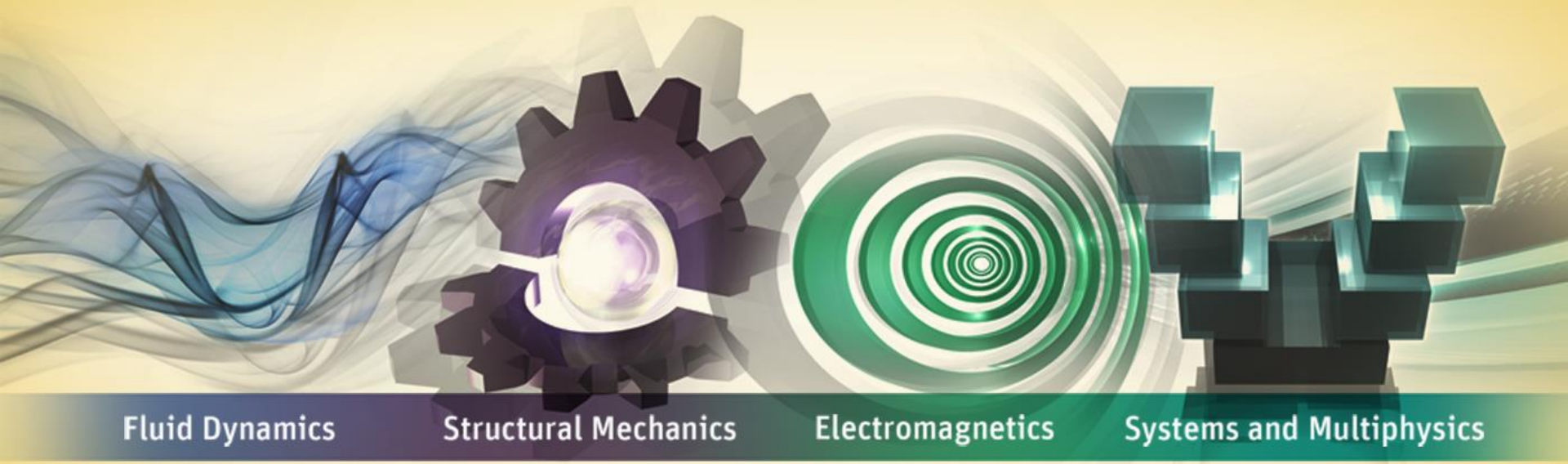
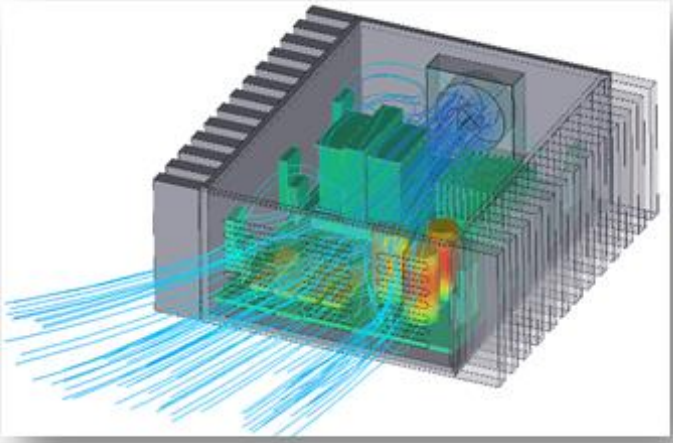
Multiphysics Board Analysis

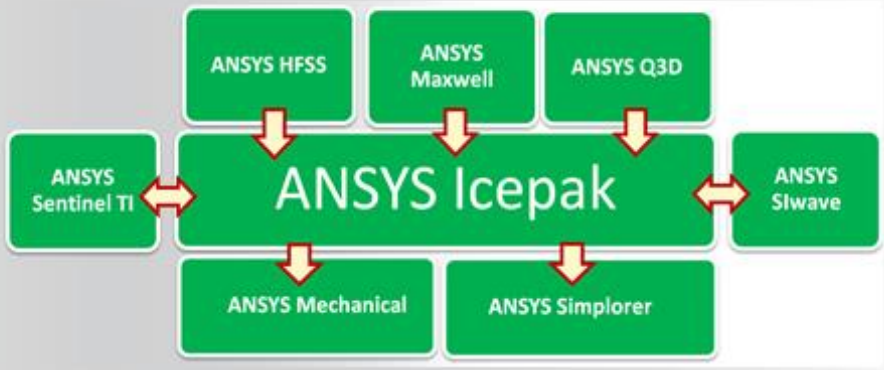


ANSYS Icepak

Solver Validated by Experts

ANSYS Icepak uses ANSYS Fluent as the solver engine, which is recognized as the market leader for both speed and accuracy of CFD



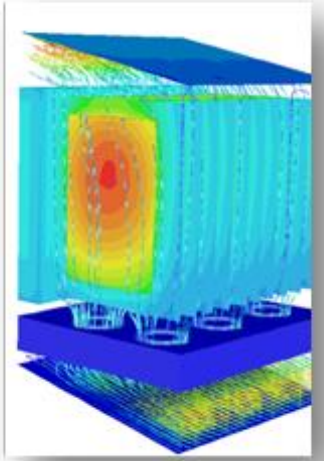


Customized for Thermal Management

ANSYS Icepak contains a streamlined user interface with "smart objects" to rapidly create models of electronics assemblies

Coupling Electromagnetics, Mechanical & Thermal Simulations

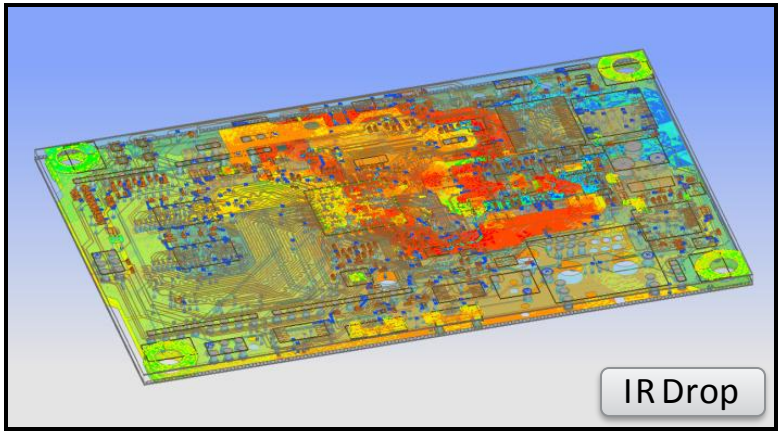
ANSYS Icepak can be connected to ANSYS mechanical or electromagnetic simulation solutions inside the Workbench environments to simulate the complete performance of a product

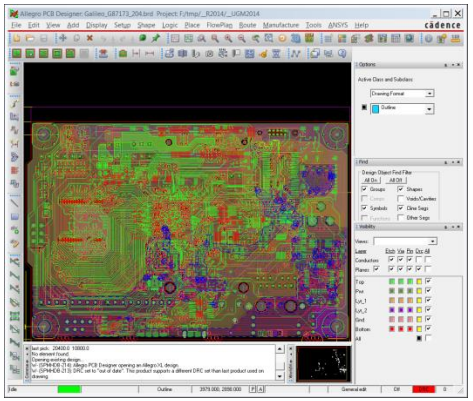


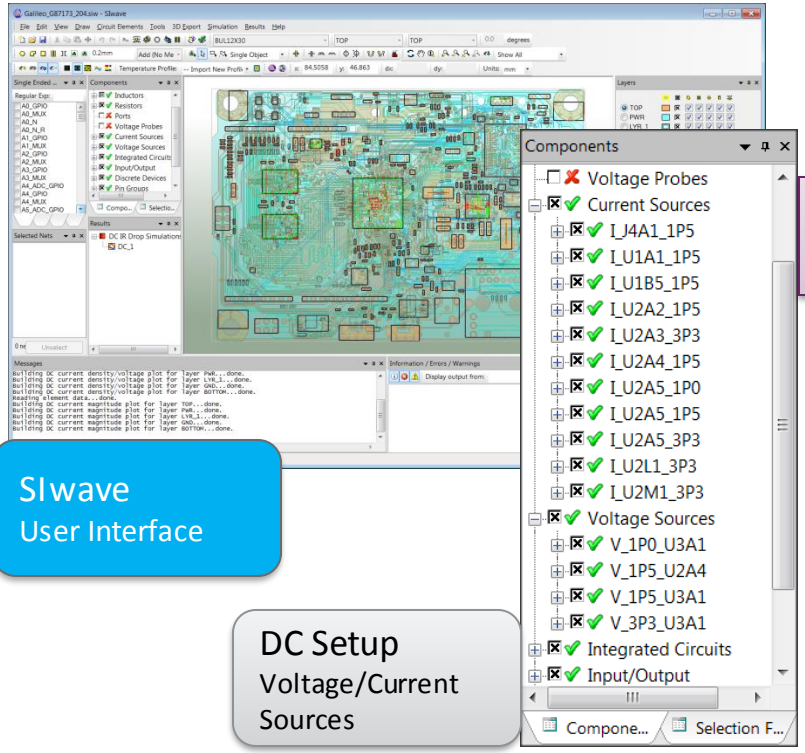
DC Heating

SIwave for DC

ECAD Translators
User Interface
I^2R DC Analysis







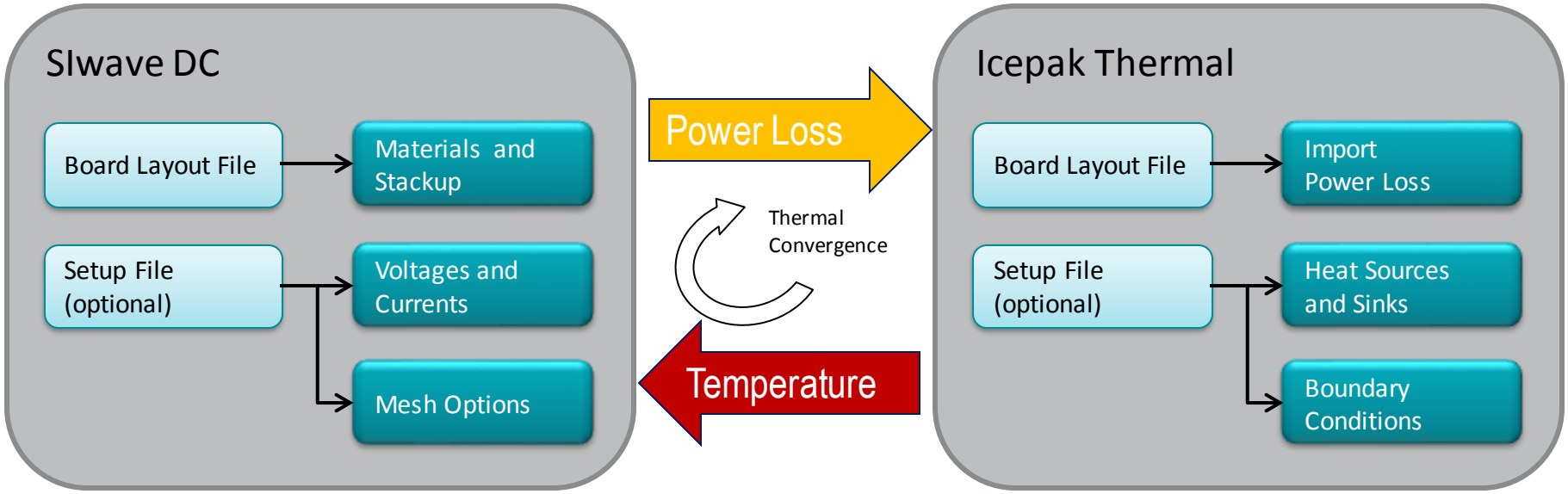
Simulate

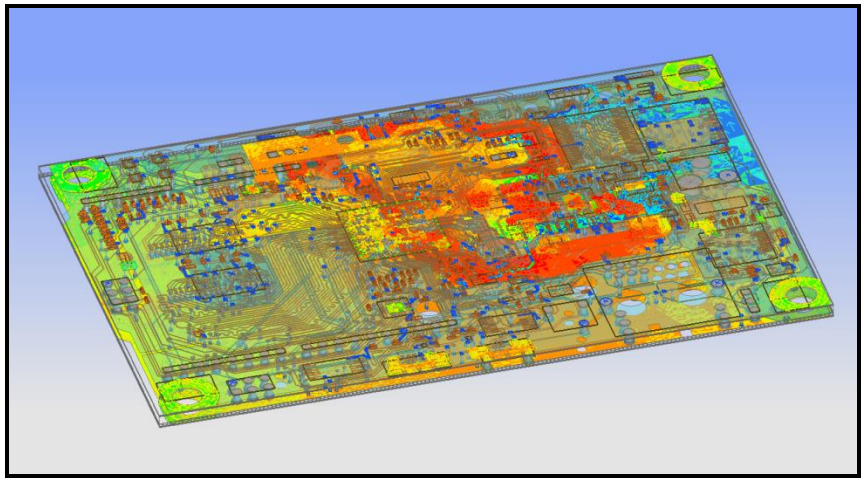
Cadence Allegro
BRD file

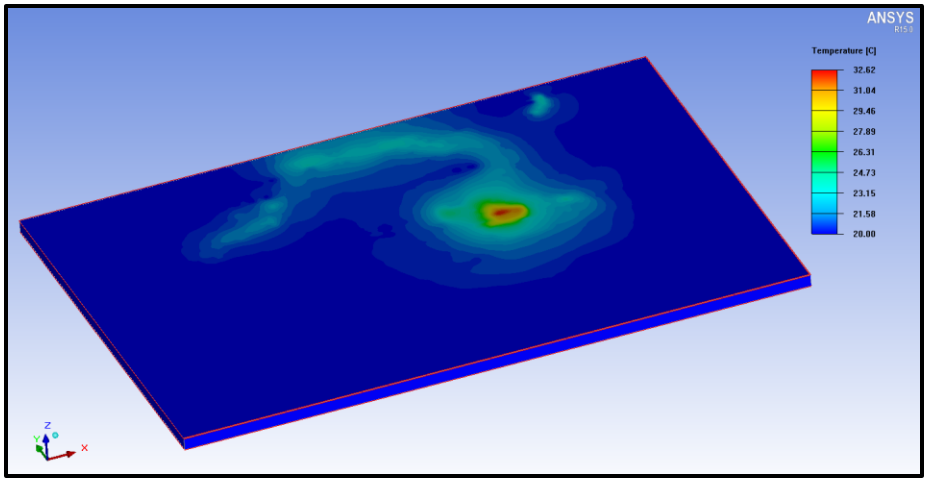
SIwave
User Interface

DC Setup
Voltage/Current
Sources

Two-way coupled Thermal Heating





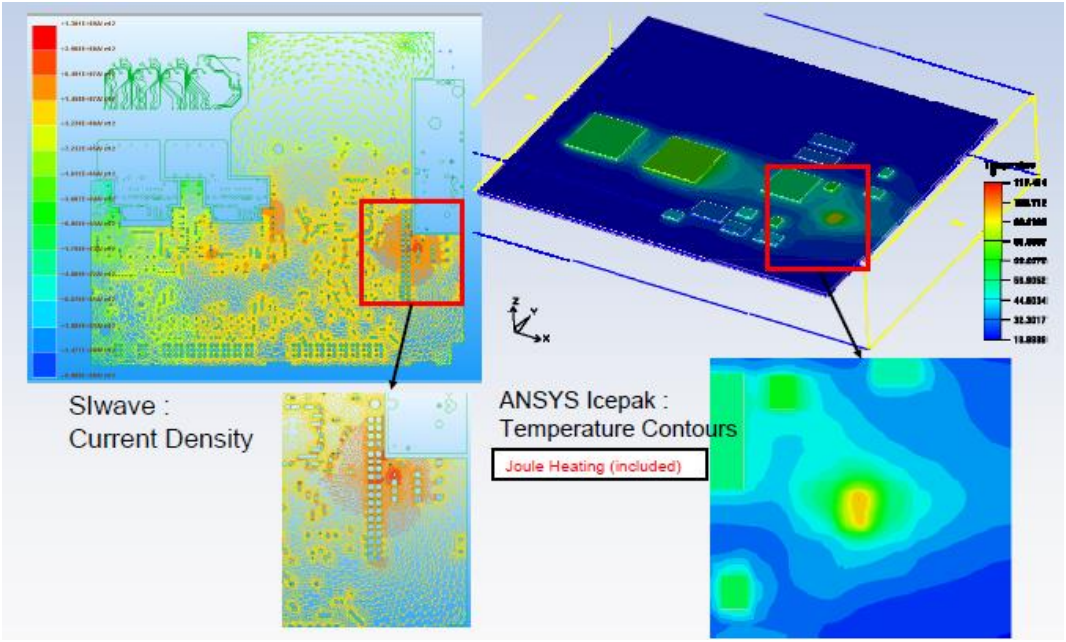


ANSYS Solutions for Pkg/PCB

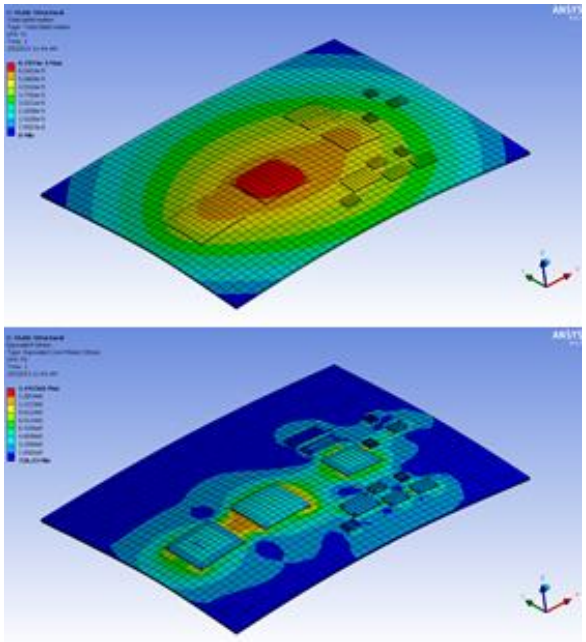
Thermal Management Design Challenges

- Thermal impact to IC
- Electric / Thermal Co-Analysis for PKG/PCB
- Automation of pre-processing would free up more of the engineer's time for design innovation
- Thermal impact for mechanical stress
- Optimization of power, weight, and thermal design requirements

Electrical / Thermal Co-Simulation



Thermal / Mechanical Co-Simulation

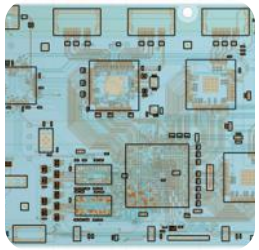


Coupled Thermal/Stress
Electronics assembly reliability

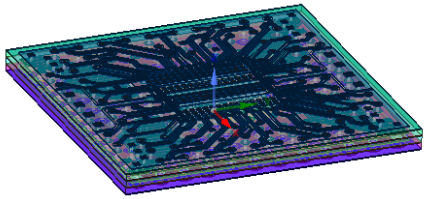
Mechanical Reliability

ANSYS Mechanical can be used to predict stresses and deformation in the package during

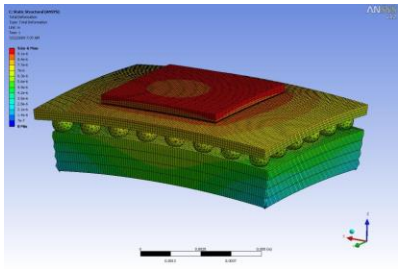
- Flip Chip Attachment
  - Crack Initiation and Crack Growth
- Thermal Cycling
  - Solder Joint Reliability
- Shock Analysis



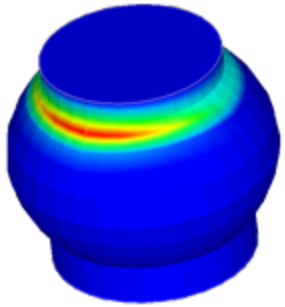
Layout Tool*



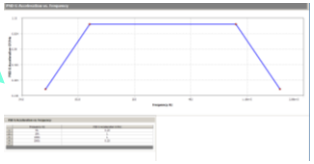
ANSYS Mechanical



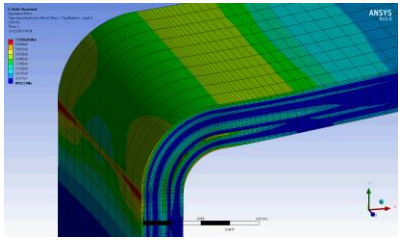
Flip chip Attachment



Solder Joint Reliability

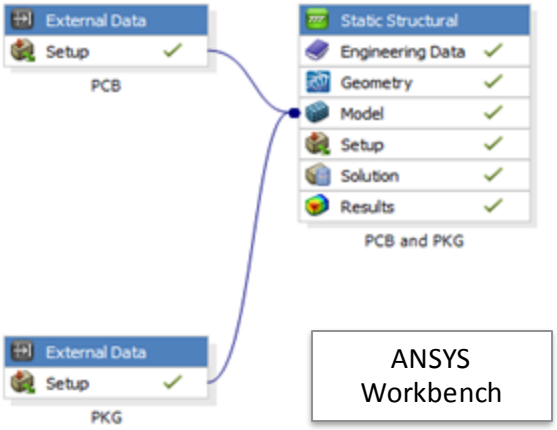


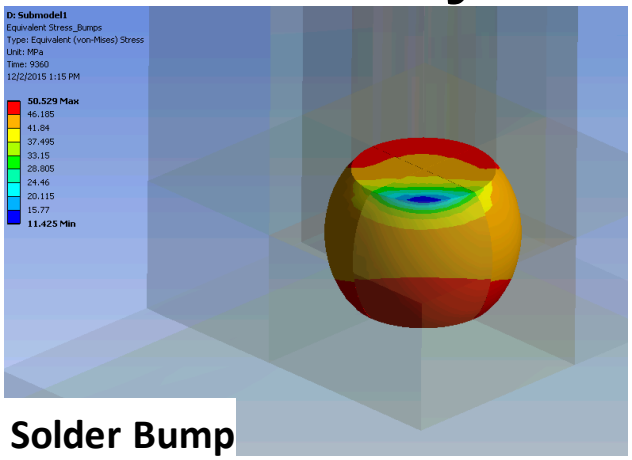
Shock Analysis

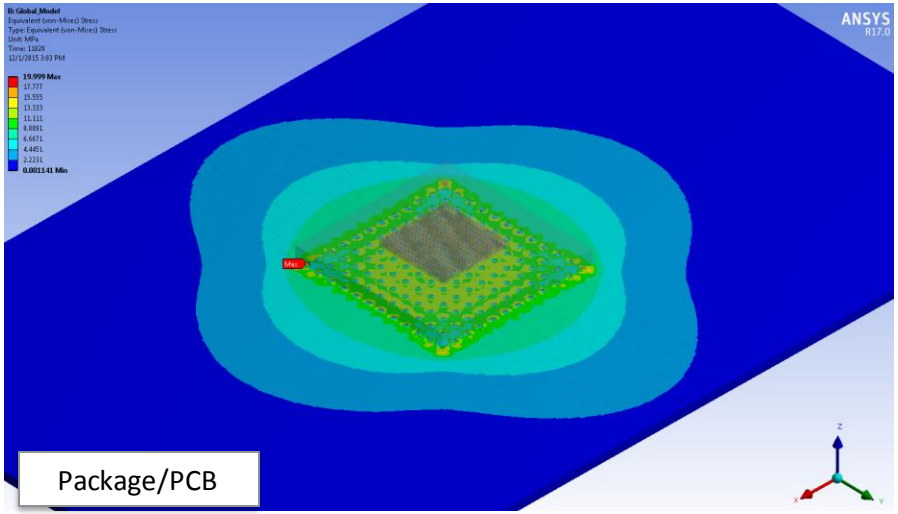


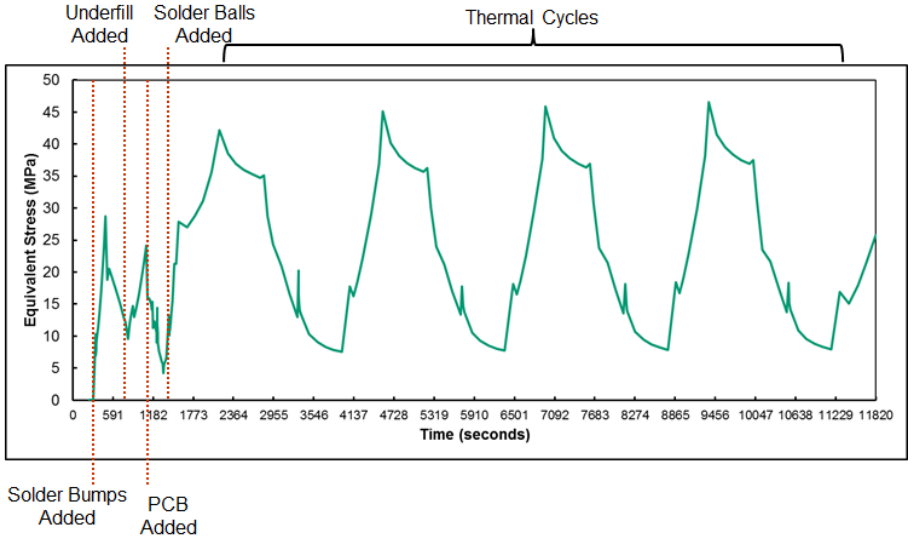
Crack

Mechanical: Electronics Assembly









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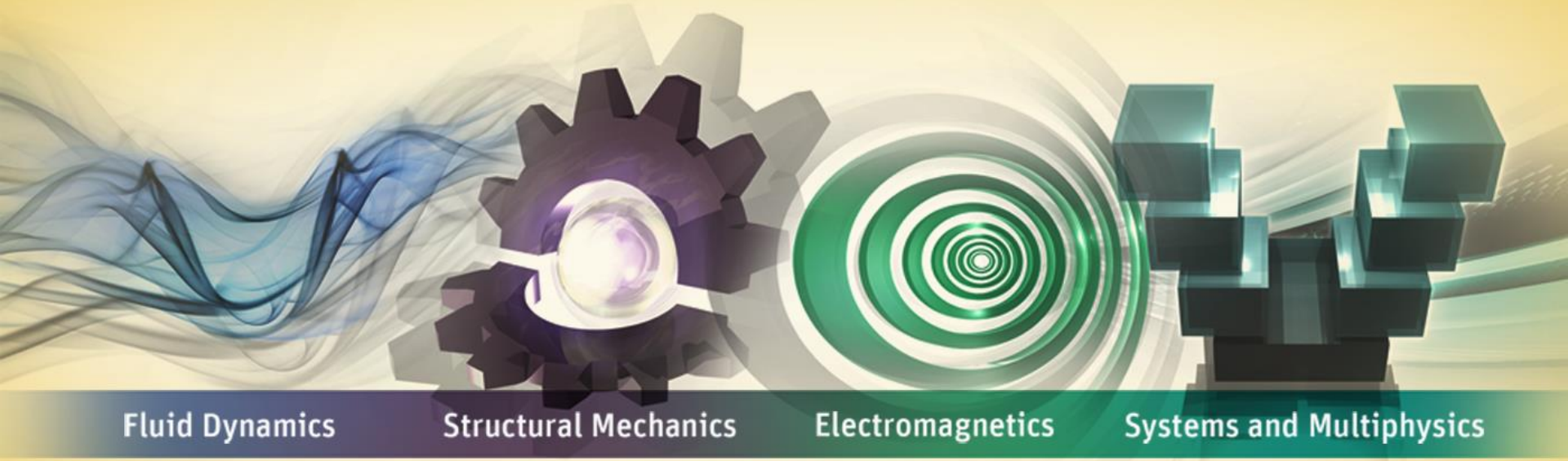
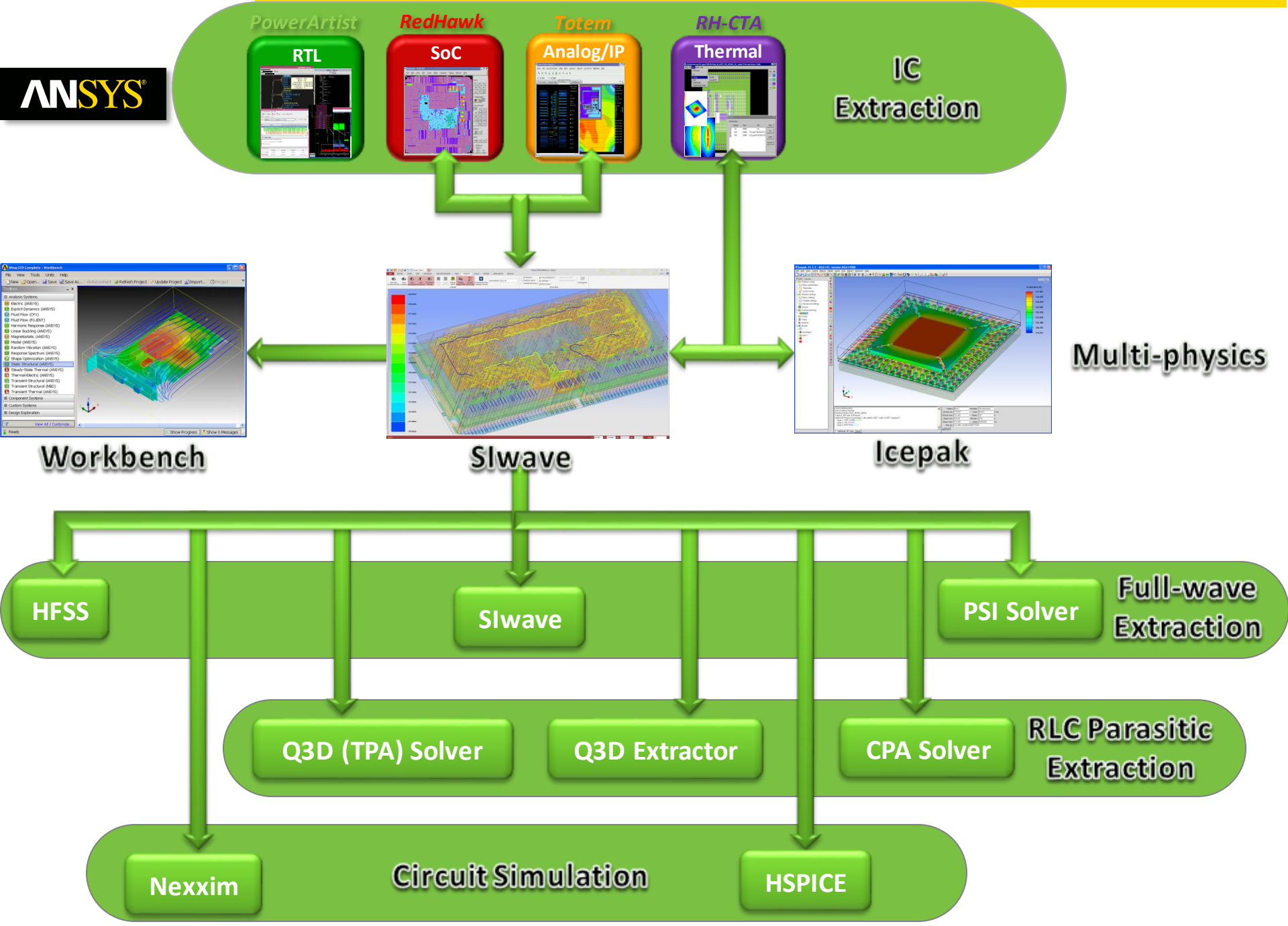
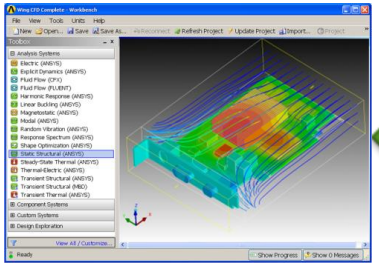
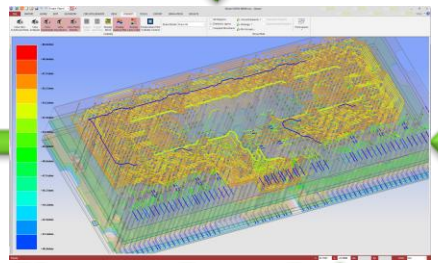
SIwave Workflow Enhancements

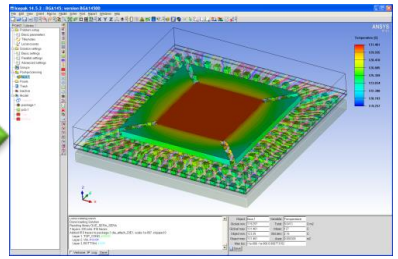




PowerArtist
RTL
RedHawk
SoC
Totem
Analog/IP
RH-CTA
Thermal
IC Extraction


Workbench


SIwave Core Solvers


Icepak

DC
ALinks for EDA: ECAD Translation
AC SYZ
Loop Inductance
Plane Resonance
Frequency Sweep
PI Advisor: Decoupling Optimization
Near/Far Field
Signal Net Analyzer Z_o & X-talk Scans
SI Circuit Analyses: IBIS, IBIS-AMI, Transient

SIwave-DC
SIwave-PI
SIwave

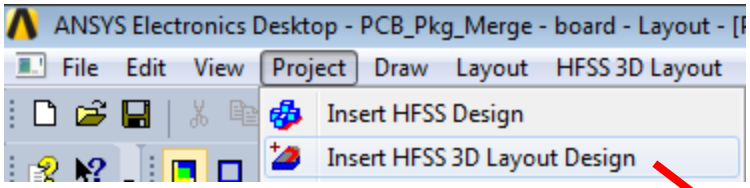
SIwave SYZ Solver Integration into AEDT 3D Layout

SIwave Solution Setups are now part of ANSYS Electronics Desktop 3D Layout

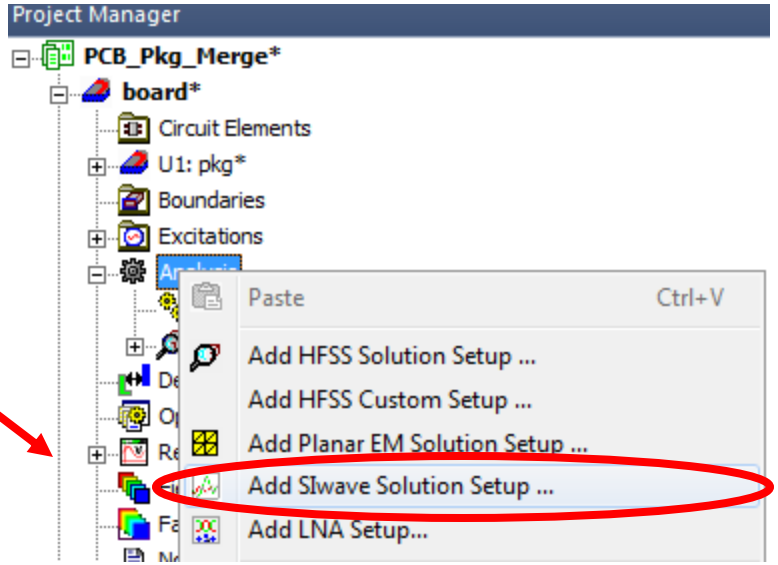
Enables parametric solves

Enables usage of Electromagnetics RSM

Insert HFSS 3D Layout Design



Add SIwave AC SYZ Solution

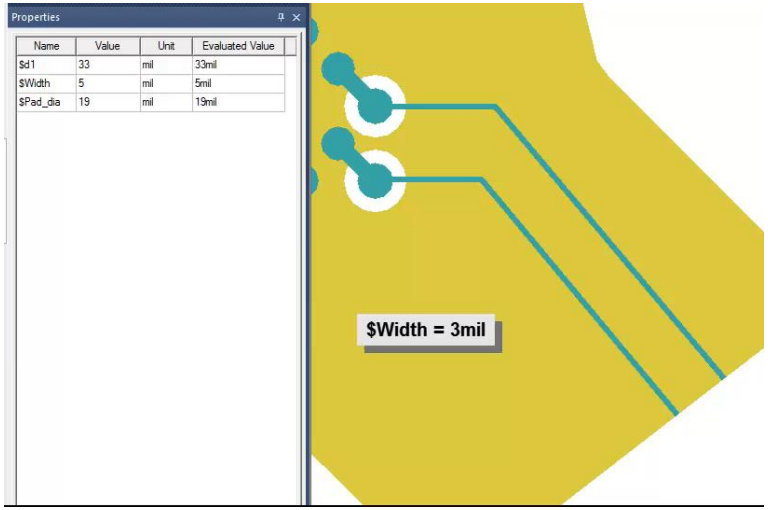


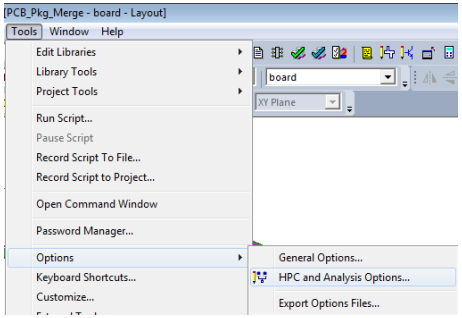
Slwave SYZ Solver Integration into AEDT 3D Layout

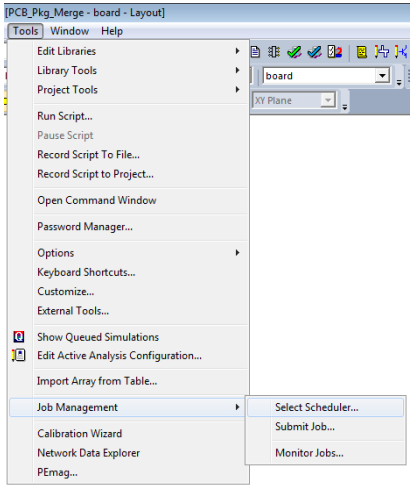
Slwave Solution Setups are now part of ANSYS Electronics Desktop 3D Layout

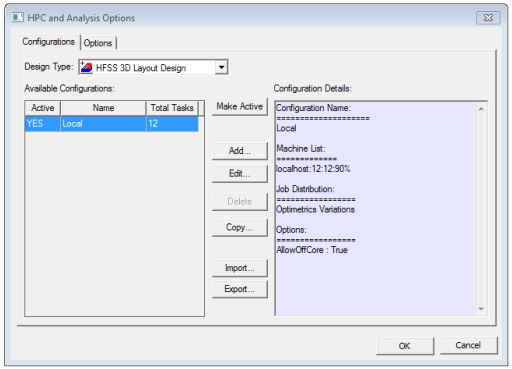
Enables parametric solves

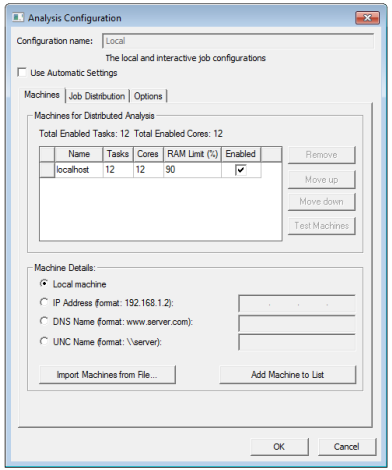
Enables usage of Electromagnetics RSM so that jobs can be submitted to a cluster



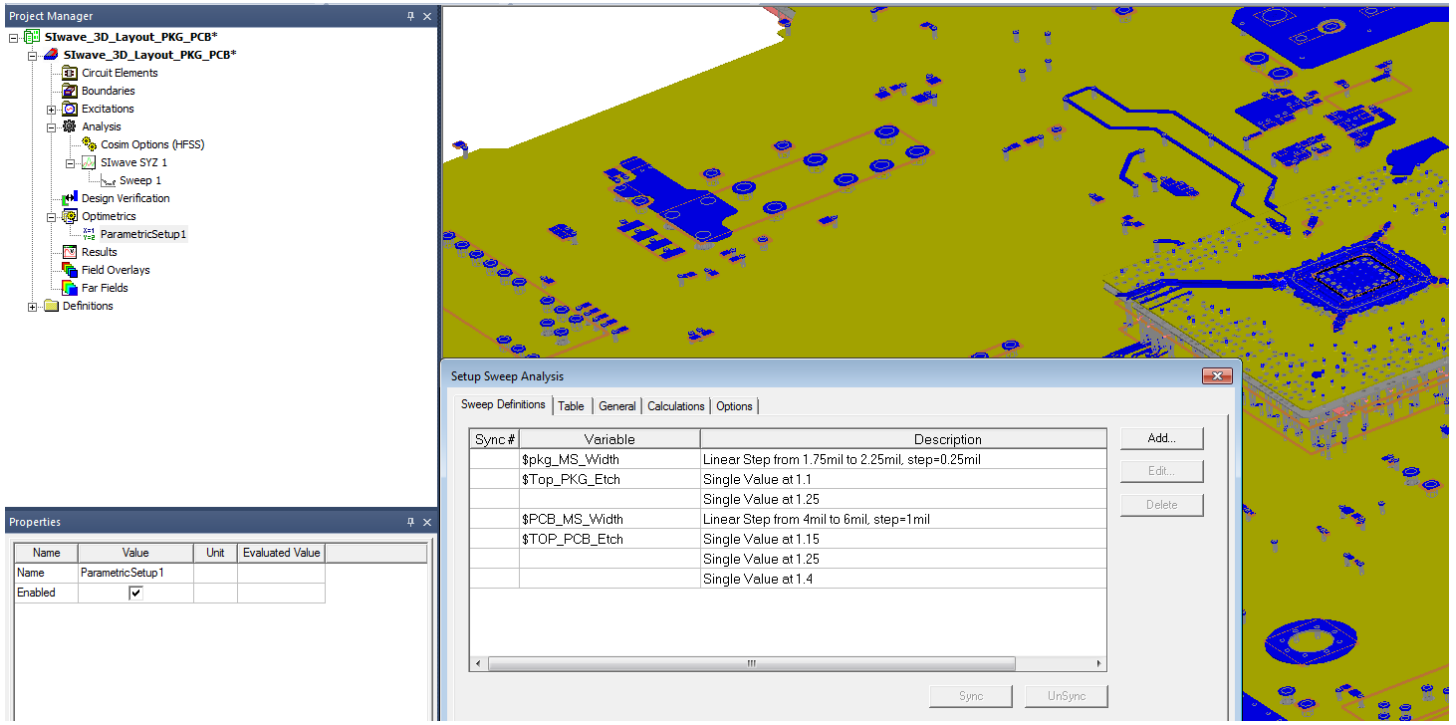


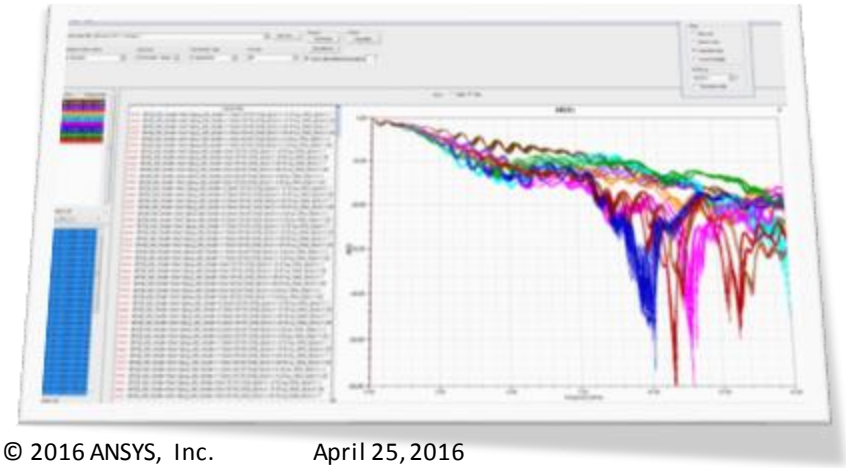


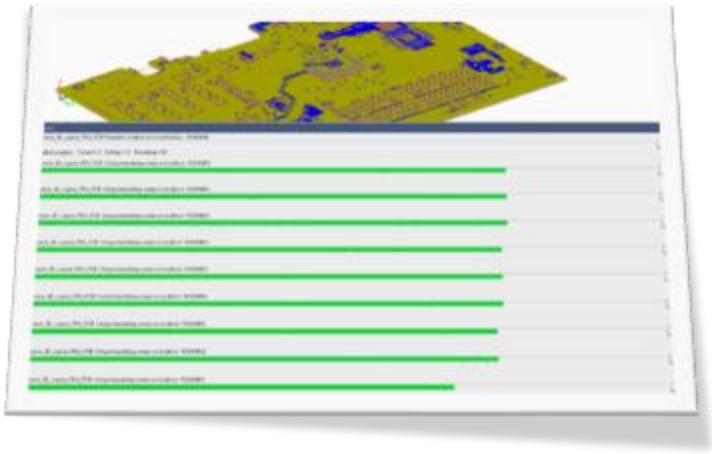




SIwave Parametric Design within AEDT 3D Layout



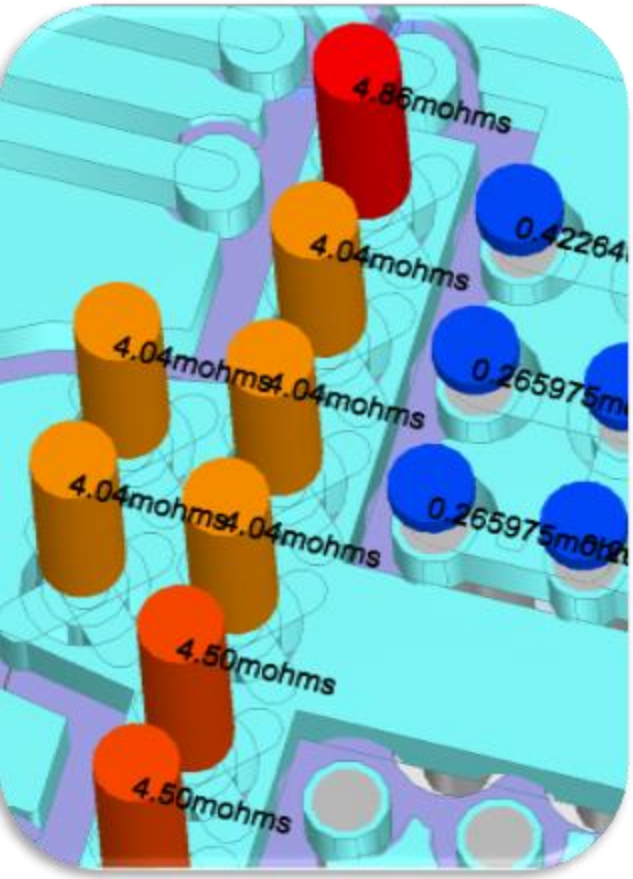


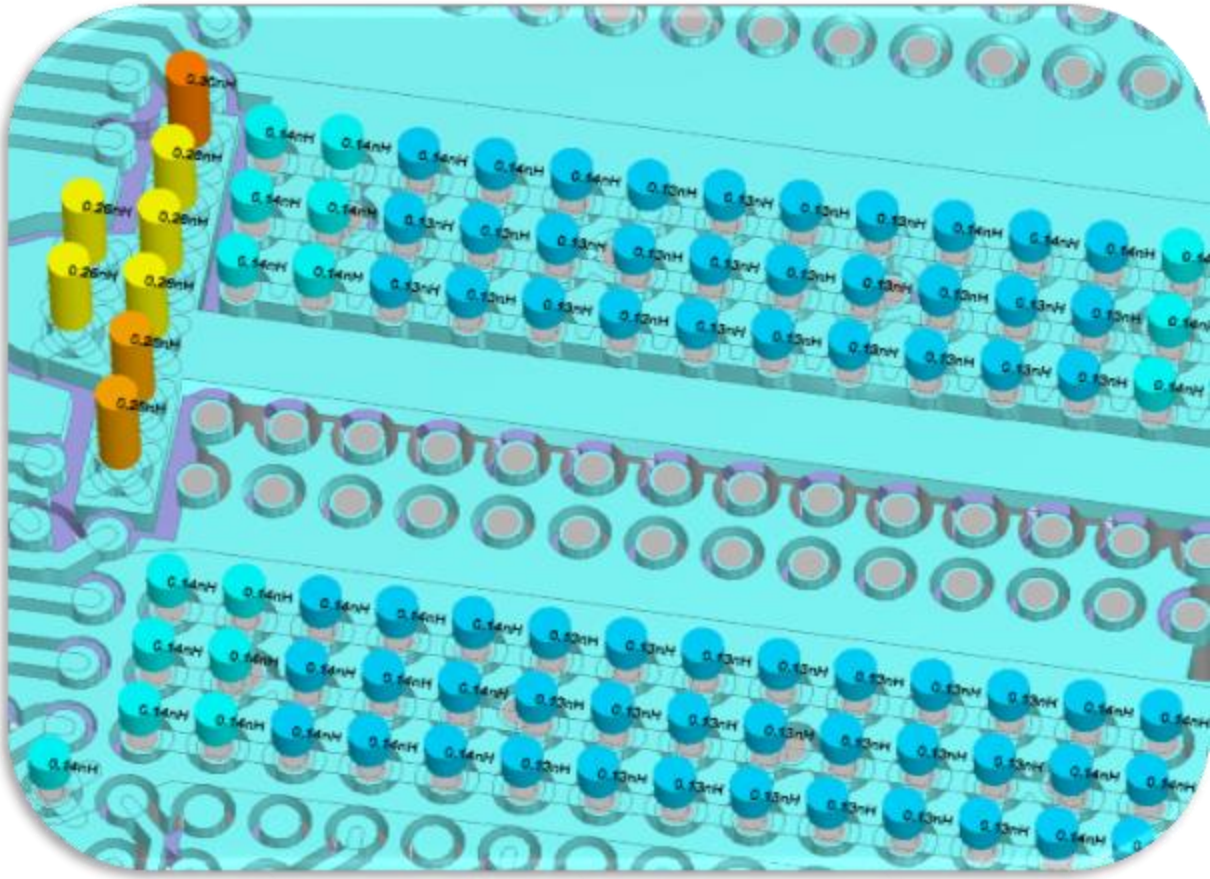


What is SIwave-CPA?

The CPA (Chip-Package-Analysis) solver is a 3D full-wave, FEM based solver for fast and accurate extraction of RLC parasitics.

- It is optimized to analyze power and signal nets on packages





SIwave-CPA

- Automated .html reporting for partial and loop resistance/inductance
- The CPA solver is capable of producing per bump/ball resolution RLC extracted parasitics
- Visual Bar graph plotting is available for solderball/bump and Pin Groups

Flip-Chip PDN System

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (minutes)	Speed Up	RAM (MB)	RAM Reduction
Q3D (TPA)	PDN A	12.3	310.6	24.8	4.51	-	748	-
CPA	PDN A	12.9	312.4	25.8	0.4	**11x**	210	**4x**
Q3D (TPA)	PDN B	9.1	224.8	24.8	4.51	-	748	-
CPA	PDN B	9.2	230.7	25.9	0.4	**11x**	210	**4x**

SIwave-CPA

Wirebond Package PDN System

Solver	Net	R (mΩ)	L (pH)	C (pF)	Solve Time (Hours)	Speed Up	RAM (GB)	RAM Reduction
Q3D (TPA)	PDN C	1.58	79.2	128.4	48	-	71	-
CPA	PDN C	1.61	79.9	129.3	0.1	**480x**	13	**5x**
Q3D (TPA)	PDN D	0.16	12.6	973.4	48	-	71	-
CPA	PDN D	0.16	12.9	979.3	0.1	**480x**	13	**5x**

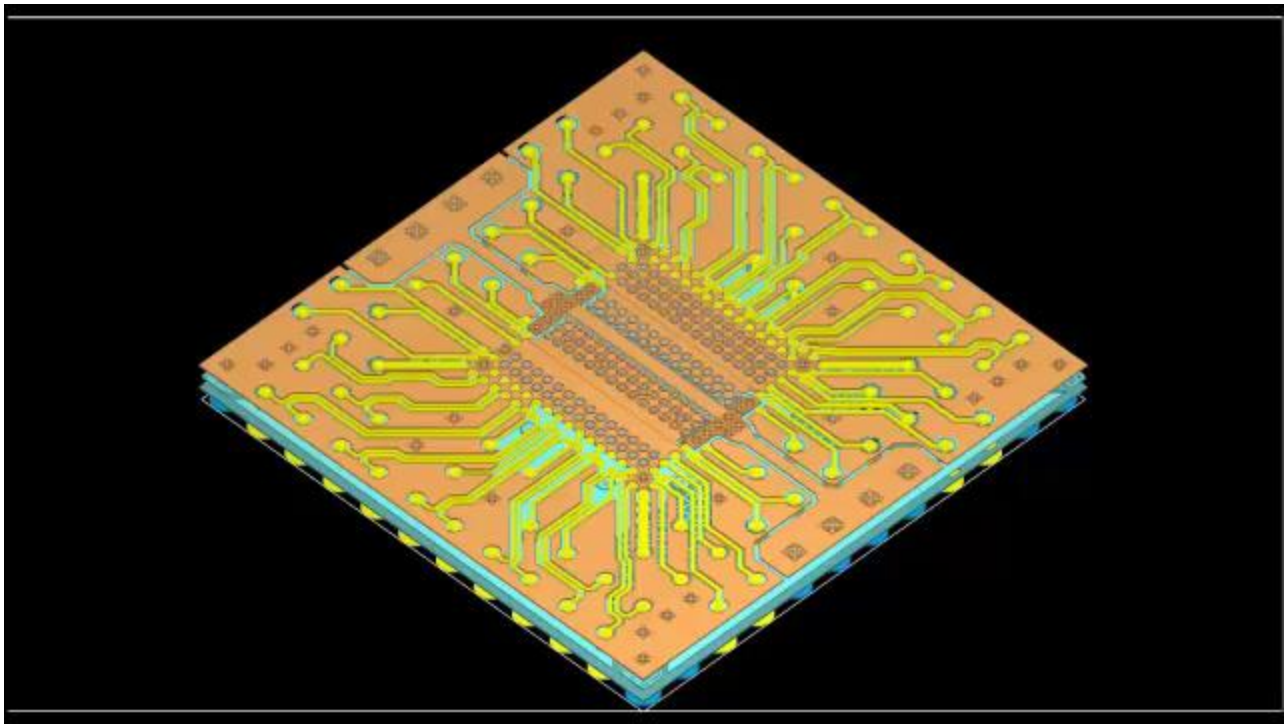
Coupled Microstrip Lines

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (Minutes)	Speed Up	RAM (MB)	RAM Reduction
NPE	Trace A	386	3.42	1.17	3.0	-	450	-
CPA	Trace A	386	3.22	1.17	1.0	**3x**	300	**3x**
NPE	Trace B	386	3.44	1.19	3.0	-	450	-
CPA	Trace B	386	3.30	1.17	1.0	**3x**	300	**3x**

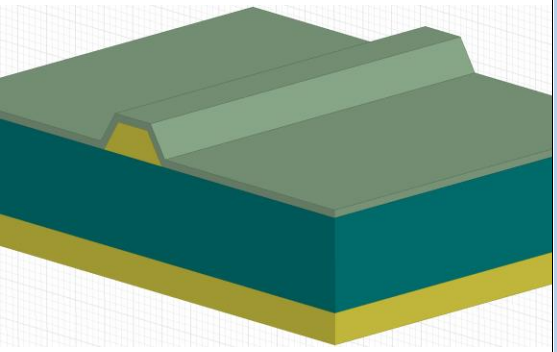
SIwave-Q3D (TPA) Improvements

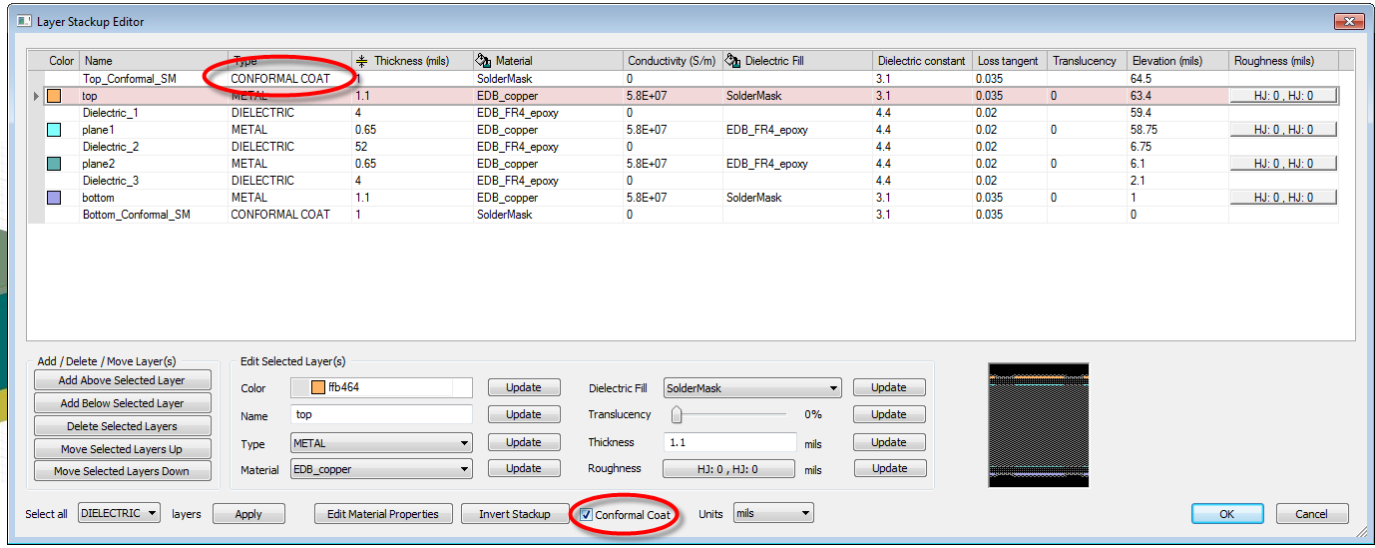
Added DC Adaptive Meshing

Added the ability to use Pin Groups with Q3D (TPA) solver



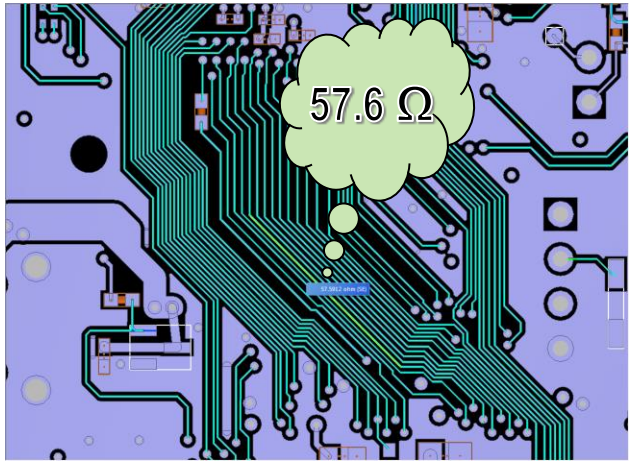
SIwave Conformal Soldermasks



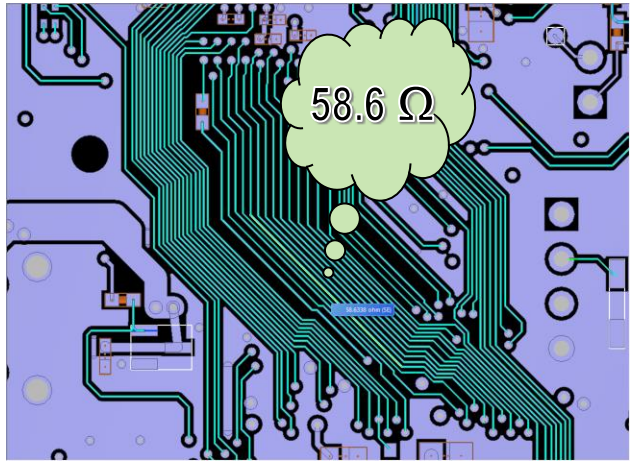


Single Ended Zo
Without Trace-Trace Coupling
Without Conformal Soldermask

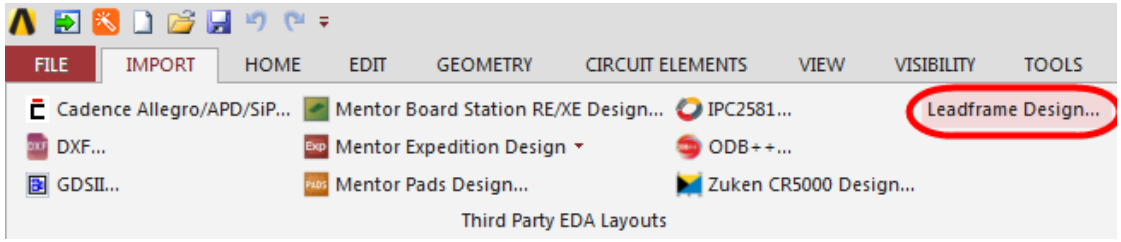
Single Ended Zo
With Trace-Trace Coupling
Without Conformal Soldermask

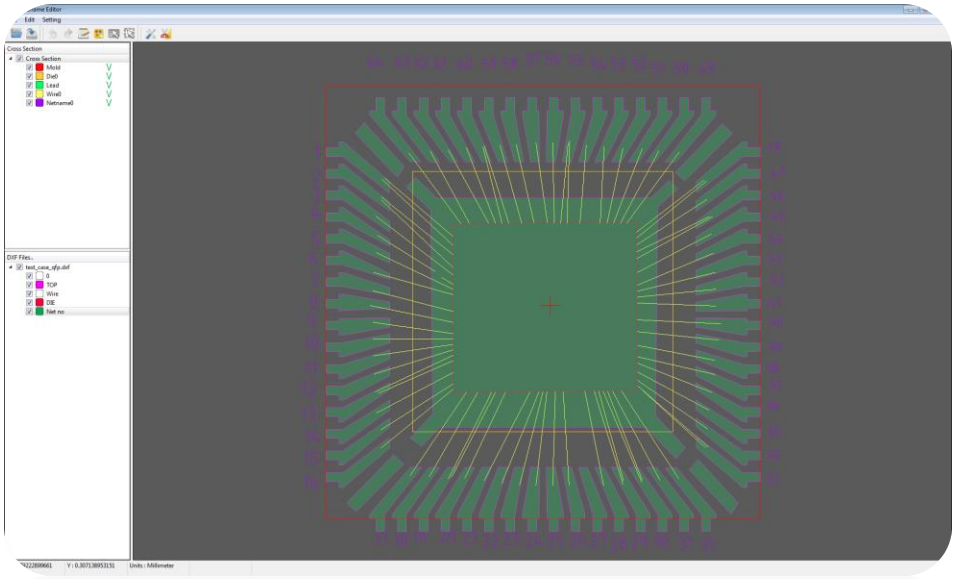


Single Ended Zo
With Trace-Trace Coupling
With Conformal Soldermask



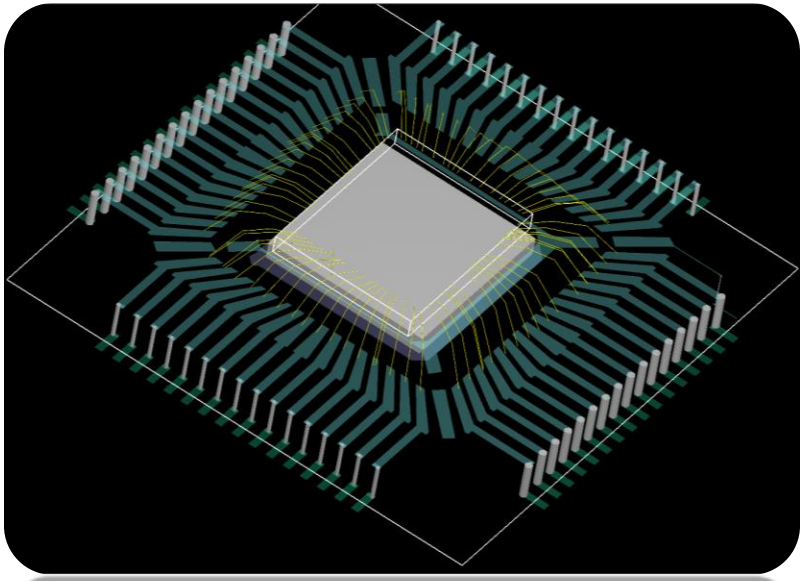
Leadframe Editor





Lead Frame Editor

- **Creates SIwave & 3D Layout .anf Geometries**
- **Creates HFSS & Q3D .sat Geometries**



Lead Frame Editor

- **SIwave QFP Package from Lead Frame Editor**

Thank You