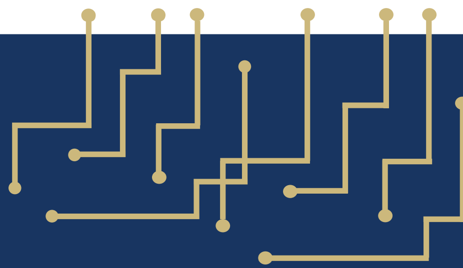

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ALD of Alumina Ceramic Films for Hermetic Protection

A primary issue in electronics reliability for military applications is the ability to ensure long term operability in harsh, extreme environments. This requires more rigid standards, such as the MIL-STD-883 (Department of Defense Test Method Standard for Microcircuits), which commercial grade electronics typically do not satisfy. A solution commonly employed is to package the critical electronic components in hermetically sealed metal or ceramic enclosures which are costly and labor intensive. Not only are the components more expensive, but the assembly process is more difficult to automate, resulting in a substantial cost premium for military grade electronics.

The EMPF is currently investigating a moisture impermeable coating as an alternative to hermetic enclosures. Polymer-based "glob-top" encapsulation and conformal coating techniques are commonly used to improve moisture resistance but they still allow diffusion and can be difficult to rework. Atomic layer deposition (ALD) has recently emerged as a potentially affordable method to coat electronic components with a moisture impermeable ceramic thin film coating.

ALD has been used at the laboratory scale for a few decades but has not achieved widespread commercial use. Recent improvements in manufacturing technologies have increased deposition rates, equipment reliability, and reduced cycle times.

One method to deposit alumina (Al_2O_3) ceramic thin films by ALD uses precursors of trimethyl aluminum ($Al(CH_3)_3$, TMA) and water. The binary self-limiting chemical reactions (A and B) occur

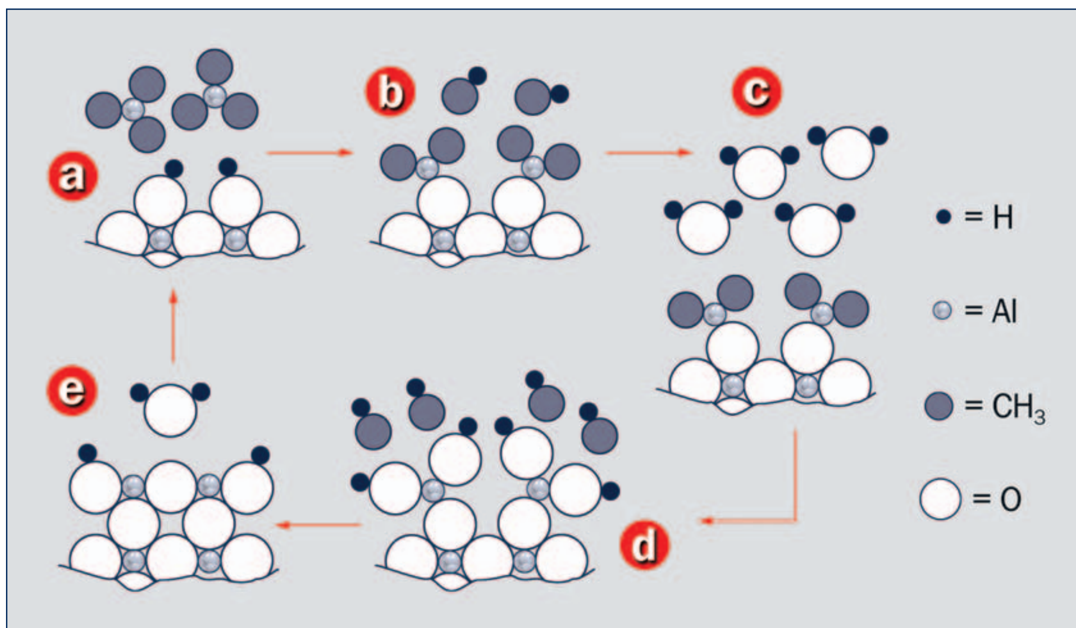

Figure 1-1: Five-step cycle (a through e) to produce one monolayer of alumina ceramic (Al_2O_3). Courtesy of Sundew Technologies, LLC.

continued on page 7

Ask the EMPF Helpline!

Reworking ALD Coatings

A customer recently contacted the EMPF Helpline in regards to reworking ALD coatings on their assemblies.

Atomic layer deposition (ALD) is a process of creating coatings on a molecular layer by layer basis. Using an iterated sequence of self-saturating deposition cycles that are self-terminating, a single layer can be deposited at a time, allowing for highly uniform films with complete conformality. The composition of the film typically used for coating printed wiring boards (PWBs) is a high alumina (Al_2O_3) sequential deposition of alumina and titania capped with a corrosion protective titanium aluminate layer, most notably ALD-Cap from Sundew Technologies, LLC.

Rework is a process of restoring an electronics assembly to full functionality to prolong equipment life and reduce the amount of scrap. The process typically involves:

- identification and removal of a conformal coating
- removing the faulty component through reheating and desoldering
- preparing the lands for resoldering
- repairing any damaged lands, PWB circuits and laminate
- replacement of the conformal coating

These topics are covered in training courses, such as *IPC 7711/7721 - Rework, Repair & Modification of Electronic Assemblies*.

After the component is removed, an ALD pre-coated component is used as the replacement, as shown in Figure 2-1. In cases where RoHS materials are exempt, such as in aerospace and defense applications, tin-lead eutectic soldering of the new component is not likely to grow tin whiskers. The component leads are ALD coated except for the area required to form the solder joints. Tin-lead solder has been shown to wet all the way to the coating, as shown in Figure 2-2 (found on page 7), and lead-free solders should wet in a similar manner. In this type of rework procedure, the solder joints of the reworked component will be left exposed, while the rest of the assembly will be fully protected by the ALD-Cap coating.

More studies need to be performed to evaluate the reliability of solder joints that contain dissolved ALD-Cap coating, as well as more rework of components in and out of active boards to confirm the success of the rework strategy and technique.

The EMPF can assist with all aspects of board and assembly qualifications, inspections, and failure analysis to determine the quality of solder joints, in addition to the root cause of solder joint failures. The EMPF can further assist with surface finish analysis, cleaning processes, and cleanliness testing for ionic and organic residues, and engineering services. Contact the EMPF Helpline at 610.362.1320 or visit us on the web at www.empf.org for more information.

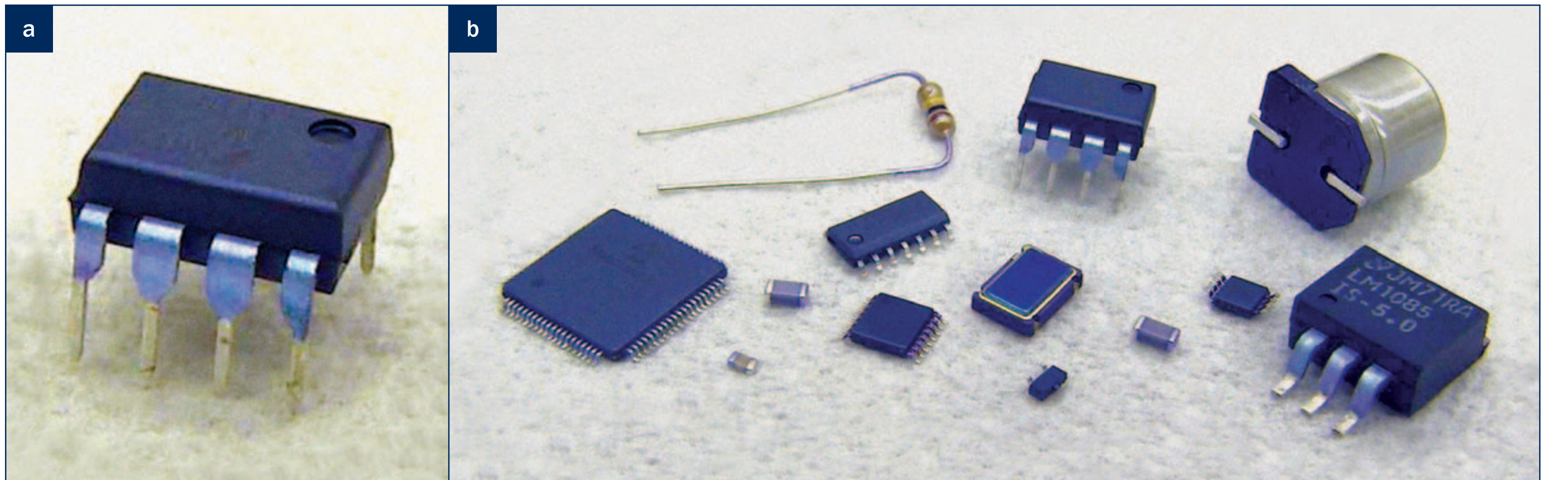

Figure 2-1: Images of ALD coated components with the solderable surface left uncoated. The ALD coating has a matte appearance while the uncoated region appears glossy. Image courtesy of Sundew Technologies, LLC.

Since the ALD-Cap coating is a new conformal coating process, the topic has not yet been incorporated into the IPC training materials. Unlike other traditional conformal coatings, ALD-Cap coatings do not require mechanical or chemical methods to remove prior to rework. The ALD-Cap film is removed by the melted solder once it is heated to reflow temperatures. The amount of ALD-Cap material incorporated in the new solder joint is minimal, but its effects have not yet been studied in detail.

continued on page 7

Implementation of ALD Coating

Conformal coating continues to be a growing need in the microelectronics industry to protect circuitry from environmental extremes. In this article, we will study some of the thin film coating techniques, their advantages, and disadvantages. A brief discussion on equipment specification for ALD process implementation will be discussed.

Thin films are defined as coatings with a thickness of a few angstroms (Å) to a few micrometers (µm). Several materials may be deposited as thin films on passive substrates (glass or ceramic) or on active substrates such as silicon. The deposition process is divided into two broad types, physical or chemical (Figure 3-1).

Physical Deposition Techniques

Several different thin films materials are deposited by evaporation and sputtering deposition techniques. In several applications, sputtering is preferred over evaporation because of the wider choice of materials available, better adhesion to the substrate, and better step coverage. Evaporation is mainly a laboratory technique while sputtering is employed in laboratories and the industrial production of thin films.

Evaporation (PVD)

The physical vapor deposition (PVD) technique deposits thin films by condensing a vaporized material onto a variety of surfaces (e.g., semiconductor wafers). This uses high temperature vacuum evaporation rather than a chemical reaction. PVD is extensively used in the semiconductor industry as well as the tool and die making industry to provide a hard, wear resistant metal coating.

Sputtering

Unlike evaporation, sputtering can deposit conductors or insulators onto a substrate without heating. During sputtering, an atom is knocked out of a target material by a stream of accelerated ions from an excited plasma. These sputtered atoms are deposited onto a substrate as a thin, uniform film.

Chemical Deposition Techniques

Chemical deposition uses a precursor fluid or gas to chemically react with a solid surface, forming a thin solid layer. Deposition occurs on every surface providing a conformal thin film.

Chemical Vapor Deposition (CVD)

CVD thin films are obtained by reacting dilute precursor gases with a heated substrate within a vacuum chamber. The resulting reaction deposits a thin solid coating, usually only a few microns thick. The process is slow and takes a few hours to deposit a few hundred microns of coated film. The coating produced is very pure, void free, and adheres well to the substrate. The CVD process is extensively used in the microelectronics industry to produce coatings of almost any metal or metal alloy, oxide, nitride, or intermetallic compound.

Atomic Layer Deposition (ALD)

The ALD process was developed more than 35 years ago but was not extensively used in the microelectronics industry due to its slower throughput. Atomic layer deposition is a subset of the chemical vapor deposition techniques where reaction precursors are alternately introduced into the reaction chamber, one precursor at a time, separated by a purge with an inert gas. Each precursor exposure deposits a thin monolayer until the entire surface is coated and the chemical reaction stops. Excess reactants are then purged and another reactant gas is introduced to build over the first layer. This process continues until the desired coating thickness is achieved. Since the precursor gases are not mixed (as in the case of the CVD process), the deposition thickness can be tightly controlled, providing a uniform and pin-hole free coating over any irregular surface.

With advancements in the semiconductor industry, designers continue to reduce the die footprint to lower cost, reduce operating power, and improve performance. Traditionally high yielding conformal coating processes like PVD and CVD, are pushing the manufacturing process envelop to yield reliable products. ALD has been the preferred choice for conformally coating dies with a high aspect ratio (ASICs and DRAM), obtaining coating thicknesses of tens of angstroms.

The ALD process is still traditionally used in the semiconductor industry to coat high dielectric constant materials or as an alternative to SiO_2 on a silicon wafer. The microelectronics industry is also investigating the use of ALD thin film coatings for large solar panel glass and for microelectromechanical systems (MEMS)[1].

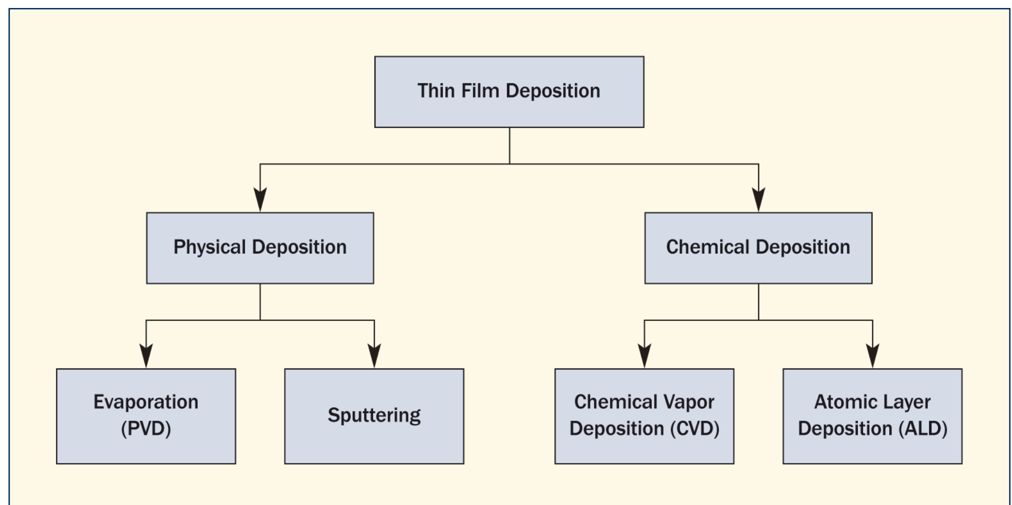

Figure 3-1: Thin film deposition techniques.

continued on page 8

Tech Tips: Masking for Conformal Coatings

Conformal coatings are regularly employed to protect the surface of a soldered printed circuit board assembly (PCBA) from moisture, chemicals in the PCBA's service environment, and foreign objects or debris. Conformal coatings are nonconductive and therefore cannot be placed on any location where electrical contact will be required, such as connector pins, test points, and sockets. Conformal coatings are also not permitted on any mechanical interface location, such as mounting holes or brackets, to assure the proper fit between items in the final assembly. In order to apply conformal coatings to an assembly and comply with the restrictions on keep-out areas, masking is employed to protect those surfaces.

There are two basic strategies for masking of conformal coatings. The first strategy is to use a temporarily installed material that prevents conformal coatings from bonding to locations that forbid coating application. Polyimide tape can be used as a temporary masking agent. The tape must be cut to the proper shape to ensure the tape only covers the area where conformal coatings are not desired. Polyimide tape has a few basic advantages as a masking material. The first advantage is that polyimide tapes are able to withstand a typical oven cure cycle for conformal coatings without damage. Another major advantage is that polyimide tapes have a resistance to tearing that exceeds many other types of adhesive tapes, which allows easy removal after the coating has been cured. Tapes can be cut and formed to cover very precise areas on an assembly. A final advantage is that the assembly is ready for coating immediately after tape is applied.

Another type of temporary masking material is commonly referred to as a "peelable mask" (Figure 4-1). These products are marketed as a means to quickly and easily mask areas to prevent the flow of solder or conformal coatings during assembly. These materials are dispensed to the area where coating is not desired and left to cure. Some peelable masks can cure at room temperature while an oven cure cycle can be used to cure or accelerate cure of some materials. These materials have a very low adhesion to the surface and can be peeled off when required with very little residue remaining on the assembly. A disadvantage of peelable masks is the cure time required after application.

A final type of temporary masking material is plugs or caps. Plugs are used to protect the inner cavity of a connector that cannot be coated and are designed to have a snug fit inside the connector housing, covering all pins or contacts inside the connector. Caps are placed over a connector to prevent any coating from contacting the connector and should fit snugly around the outside surface of a connector housing. The plugs and caps are manufactured from materials that can withstand the temperatures required for the oven cure of conformal coatings. The plugs and caps are removed after the coating has been cured and can be reused on subsequent assemblies. An advantage of plugs and caps is their low cost, especially when considering the many times they may be reused. A significant disadvantage is that plugs and caps can typically only be used on the specific item it is designed to cover, so many different types of plugs or caps may be required if a variety of parts require masking from conformal coatings.

4-1

4-2

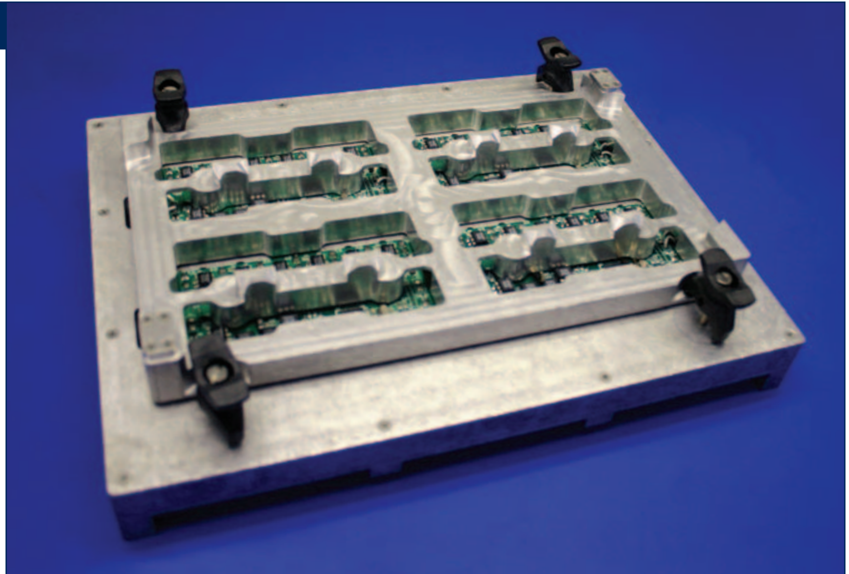

Figure 4-1: Peelable mask products are a temporary means to quickly and easily mask areas to prevent the flow of solder or conformal coatings.
Figure 4-2: Masking fixtures are designed to mask all areas of an assembly that cannot have coating applied and are designed specifically for the assembly in question.

The second basic strategy for masking an assembly is to implement purpose-built masking fixtures (Figure 4-2). These fixtures are designed to mask all areas of an assembly that cannot have coating applied and are designed specifically for the assembly in question. The major advantage for a fixture is the short time required to apply as compared to applying

continued on page 9

Manufacturer's Corner: ScanCAD International

Reverse Engineering Circuit Boards with ScanCAD

Reverse engineering a circuit board is usually a difficult task, but ScanCAD has combined a very high resolution scanner with dedicated application software tools (Figure 5-1) to interpret and translate a scanned image and extract relevant information. Based on the scanned images and component information, the circuit board can be reconstructed layer by layer to develop the board and schematic.

It is worthwhile to determine the level of circuit board re-engineering to be achieved. Is the objective to simply get enough Gerber and drill files to manufacture bare boards? For simple, hand assembled boards, this may be enough. Is the goal to reverse engineer to the point where you can manufacture bare PCBs and have component placement data? To manufacture and assemble circuit boards using surface mount technology and pick and place machines, this may be enough. Or finally, is the goal to have enough data to load into a CAD system and re-create the schematic? If upgrades or modifications are necessary, or there are obsolete parts, this level of effort may be necessary. These three levels will be discussed.

There are several compelling reasons forcing a consideration of reverse engineering. Old artwork is not salvageable, multiple revisions and poor documentation could have confused the integrity of the design, and vendors go out of business. Also, it can simply be less expensive to reverse engineer a circuit board and product than to redesign the board. It is also not uncommon to discover that a product that was thought to have a limited life maintains its popularity.

Using ScanCAD products, the following sequence of steps is used to generate the information necessary to re-engineer a circuit board: Gerber data, drill/route data, and the centroid/BOM information.

1. Scan the loaded PCB with the components attached and get the BOM information.
2. Strip the components.
3. Scan the bare printed circuit board.
4. Delaminate the PCB to the next layer and scan again.
5. Delaminate to the next trace layer and scan again; continue for all layers.
6. Create Gerber/drill/routing data for all layers.

The ScanFAB application software will generate enough information to manufacture the bare circuit boards. If data is required for both assembly and component placement, the additional ScanPLACE application software can generate this necessary information.

With the ScanPLACE software loaded, having completed steps 1 through 6, continue in the following manner.

7. Extract component centroid/BOM data with ScanPLACE.
8. Output all the Gerber, drill, routing and component BOM information using the ScanPLACE software.

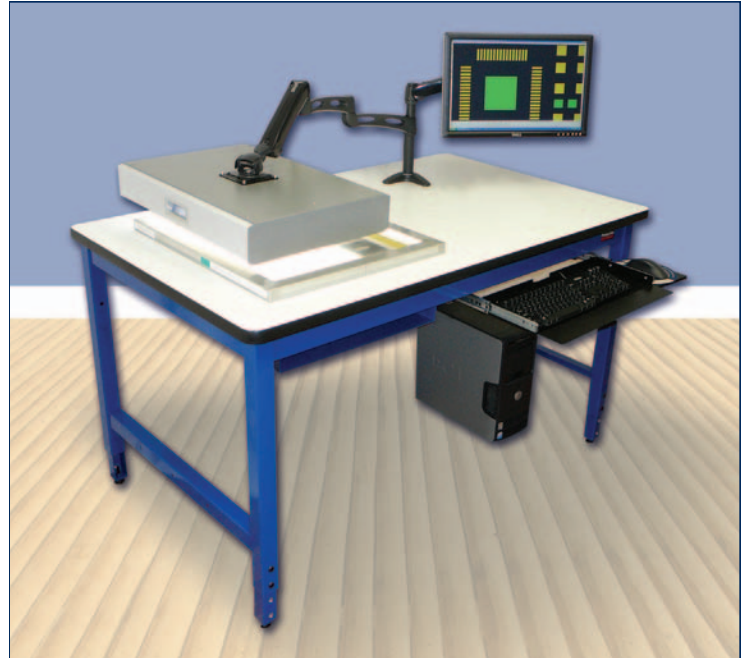

Figure 5-1: ScanCAD has combined a very high resolution scanner with dedicated application software tools.

As seen in step 4, gathering the trace information is destructive for the circuit board. For a multi-layered board, the delamination operation takes some care. The physical removal of each layer to get the trace information can be done by computer numerical controlled (CNC) machine tools, hand sanding, or a combination of both. The fastest way would be to use a CNC machine to mill away the surface a few thousandths of an inch at a time, but care must be taken to keep the board dead flat and supported during the milling process.

As a final step in the re-engineering process, schematics and CAD information can also be developed. ScanCAD ConvertPLUS Automated Reverse Engineering (ARE) and Electronic Design for Windows (EDWinXP) application software can be incorporated to provide schematic generation and CAD upload capabilities.

Using modern equipment and software from ScanCAD International, re-engineering a circuit board is a reasonable alternative to a total redesign. Improvements in the application software is the primary driver for this increased efficiency. The process itself can be measured in days and cost from a few hundred to a few thousand dollars depending on the board. For more information or for a demonstration of this technology, contact Mike Prestoy at the EMPF at 610.362.1200, extension 241.

Mike Prestoy | Senior Applications Engineer

IPC J-STD-001 Revision E

Electronics manufacturing is an ever evolving field of endeavor. In the interest of improving the ease and repeatability of the processes involved in manufacturing, as well as maintaining the quality of the end product, industry standards have been developed for use by the electronics manufacturing community. As new technologies are developed and implemented, the need to keep in step with these changes demands ongoing revisions to the standards utilized in production and quality control. Historically, electronic assembly standards contained more comprehensive and tutorial information relating to principles and techniques; however, the standardization of methods has resulted in conflicts because process methods have changed faster than the standards.

The EMPF now offers training in the IPC J-STD-001E (Requirements for Soldering Electrical and Electronic Assemblies), which is the latest version of this industry standard. Although there is not sufficient space here to address all the changes and additions to the newest revision, it is the purpose of this article to give an overview of what has changed between this and the previous revision.

The most noticeable change to this document is the general layout of the text. The former two column format has been replaced by a simple page format to improve clarity and make the document easier to navigate. Additionally, the previous revision utilized text boxes to specify the condition of materials or processes that did not conform to the standards requirements. Within the latest revision these conditions are stated in brackets directly adjacent to the referenced text to avoid referencing the wrong clause within the text (which sometimes occurred with use of the old text boxes).

In an effort to aid in connecting the J-STD-001 to the associated Space Addendum document, the new revision contains space shuttle shaped icons located adjacent to the clauses that are altered within the "E" revision of the Space Addendum.

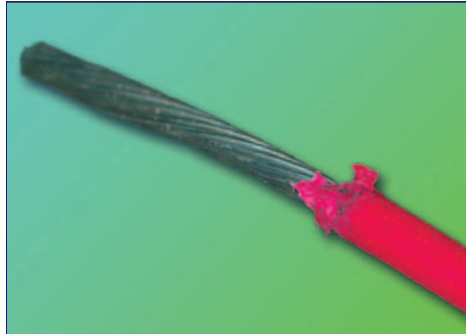

Figure 6-1: Insulation damage.

Figure 6-2: Staking defect condition.

The following are significant technical revisions and additions to the J-STD-001.

- The addition of easy to read tables regarding the mechanical attachment of a wire/lead to a terminal post for the purpose of clarifying the difference between acceptable conditions, process indicators, and defects. Also, new terms have been added to delineate between mechanical attachment variances (e.g., overlap vs. overwrap).
- Expanded criteria for the use of heat shrinkable soldering devices. Expanded criteria for identifying insulation damage of wires attached to terminals (Figure 6-1). These additions bring the J-STD-001 into line with the criteria stated in the IPC/WHMA-A-620 document (Requirements and Acceptance for Cable and Wire Harness Assemblies).
- The addition of criteria for flattened post/nail-head surface mount technology (SMT) terminations (except for Class 3 products) and the expansion of surface mount area arrays into three categories (e.g., collapsible ball, non-collapsible ball, and column arrays).
- The addition of staking criteria specifying coverage limits on a variety of component types and stating magnification limits for visual assessment of adhesive application (Figure 6-2).

The J-STD-001E Applications Specialist (CIS) training provides a modular approach to certification training. The program is a combination of lecture and hands-on soldering skills training. There are five modules, with each module requiring about eight hours to complete. Module One is required, a prerequisite to the other four optional modules of the course. There is no hands-on component to Module One; however, successful completion is dependent upon passing an open and closed book written exam with a minimum score of 70% in each test. This is a change in that the successful completion under the previous revision required only an average of 70% between the two exams.

Instructor Certification (CIT) in the J-STD-001E is not modular. Instructors must demonstrate soldering skills, defect recognition and pass a comprehensive test covering the requirements of all five modules.

If you would like to attend a training session and become certified in the most up to date version of the IPC J-STD-001, call the Registrar at 610.362.1295 or send an email to registrar@empf.org.

Ross Dillman | Technician/Instructor

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ALD of Alumina Ceramic Films for Hermetic Protection

(continued from page 1)

between the gaseous precursor and the solid surface substrate result in a deposition of Al_2O_3.[1]

$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)^*_2 + CH_4, \quad (A)$$

$$AlCH^*_3 + H_2O \rightarrow AlOH^* + CH_4, \quad (B)$$

* represents the surface species

Each AB growth cycle consists of sequentially exposing a substrate to TMA and H_2O. The TMA reacts with all the hydroxyl (-OH) groups on the substrate surface until all the available hydroxyl sites are reacted. All the remaining reactants and by-products are purged from the chamber. Next, H_2O vapor enters the chamber and reacts with the surface methyl (-CH_3) groups until they have all reacted, leaving a fresh surface of available hydroxyl groups. This is followed by another purging step and the next AB cycle[1]. By repeating these AB cycles, the desired film thickness can be achieved one atomic layer at a time. This process, schematically illustrated in Figure 1-1, produces a conformal film that is uniform and free of pinhole defects. The cyclical nature of this process can create highly ordered lamellar nanostructures and incorporate materials with compositions tailored to achieve a variety of performance enhancements.

A monolayer of single crystal alumina is on the order of one nanometer thick (the c-axis lattice constant is 12.991 angstroms). With an atomic scale layer-by-layer approach to deposition, this method results in coherent crystalline thin films with thicknesses in the range of hundreds of nanometers. As a comparison, the average thickness of a human hair is around 100,000 nanometers. Because of its inability to deposit any more or less than one atomic layer of reaction product per cycle, ALD cannot deposit an excess or insufficient film at non-uniformities (corners, edges, or holes) of the object being coated. This is especially important in radio frequency (RF) applications where excess coating can degrade RF electrical performance. The more uniform ALD coating can provide a better electrical performance.

The atomic layer deposition based ALD-Cap process developed by Sundew Technologies delivers hermetic performance that passes MIL-STD-883E environmental endurance testing[2] with a thin conformal coating of high-quality, durable, and flexible ceramic films. It is currently employed as circuit protection on Navy ships. Commercially, ALD has many applications related to the emerging field of nano-technology and commercial success in the area of protective transparent coatings for jewelry[3].

For more information on hermetic ALD coatings, please contact the EMPF at 610.362.1320, via email at helpline@empf.org or visit the website at www.empf.org.

References

[1] Dillon, A. "Surface Chemistry of Al_2O_3 Deposition Using $Al(CH_3)_3$ and H_2O in a Binary Reaction Sequence." *Surface Science* 322.1-3 (1995): 230-42.

[2] Sundew Technologies, LLC. ALD-Cap: Thin Film Encapsulating Coating for Hermetic Environmental Protection. Topic no. N04-058. Navy Success Story. Web. <https://www.navysbirsearch.com/widgets/hyperlinking/successdetails.jsp?url=DocURL&id=90078>.

[3] Jones, Anthony C., and Michael L. Hitchman. "Applications of ALD." *Chemical Vapour Deposition Precursors, Processes and Applications*. Cambridge: RSC, 2009. 197.

Dan Perez | R&D Engineer

Ask the EMPF Helpline!

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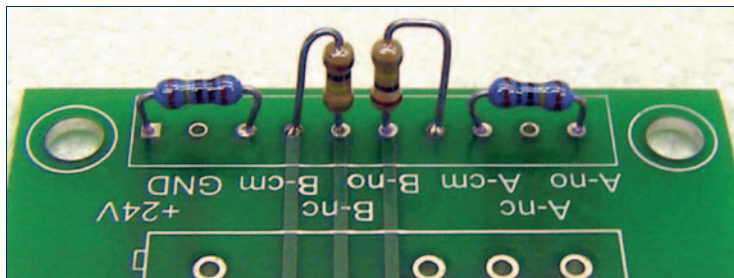


Figure 2-2: Image of ALD coated through hole components soldered to a board with the solder wetting up to the coated area. Image courtesy of Sundew Technologies, LLC.

Sean Clancy, Ph.D. | Research Associate/Chemist

Implementation of ALD Coating

(continued from page 3)

Parylene coatings are often used in the industry to protect the PWB from moisture and mechanical stresses. This is an expensive process and the coating is not truly hermetic. A current project at the EMPF is to evaluate the ALD process as a replacement for Parylene and hermetic packaging in naval applications where electronic components are exposed to extreme environmental conditions. While hermetic packaging is expensive, the presence of moisture and surface ions can cause electric shorting, degradation of circuitry, and eventual device failure. Standard manufacturing practice is to CVD coat the PWB with poly(p-xylylene) polymers (Parylene) or spray coat with a urethane conformal coating. But as shown in Figure 3-2, polymers (silicones, epoxies, fluorocarbons) are more permeable to moisture than glasses, ceramics, and metals, which are typically used for hermetic packaging. The EMPF is currently investigating using an ALD high alumina ceramic coating as an alternative to hermetic enclosures.

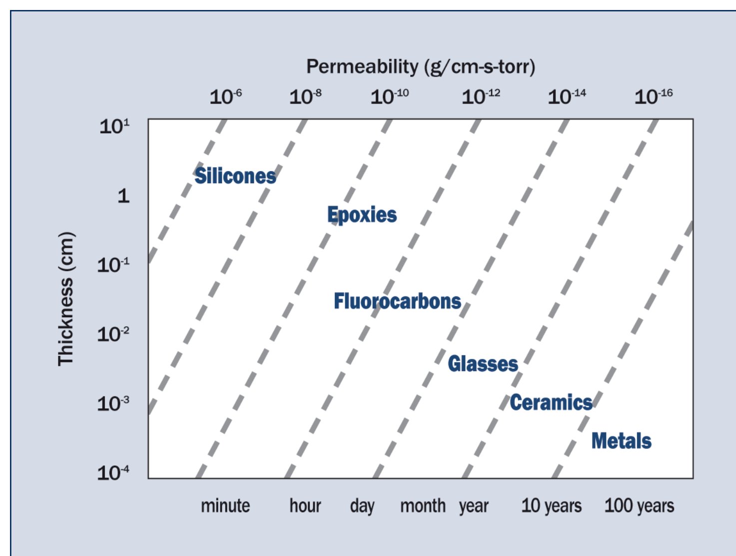


Figure 3-2: Permeability chart for common classes of packaging materials.[2]

ALD Advantages and Limitations

Advantages

Atomic layer deposition provides an easy way to produce uniform, crystalline, high quality thin films over large areas and irregular surfaces. The thickness of the coating can be precisely controlled to a single atomic layer because of the sequential deposition reactions. It is also possible to layer different composition films with this process. Small changes in substrate temperature or precursor pressure does not affect the quality of the film making it easier to reproduce the process.[3]

With the wafer fabrication process advancing from 90 nm to as low as 32 nm thin wafers, the required diffusion barrier thickness has reduced to as low as 5 nm. The conventional CVD process can no longer meet the stringent film thickness requirement making ALD the preferred choice for deposition. The ALD alumina process can uniformly coat a substrate regardless of topography, whether there are deep trenches (Figure 3-3), or high aspect ratio components. Aspect ratio can be defied as the height (depth) to width ratio. While CVD and PVD processing works well when the aspect ratio is < 10:1, ALD processing guarantees pin-hole free, uniform coverage for aspect ratios as large as 60:1.

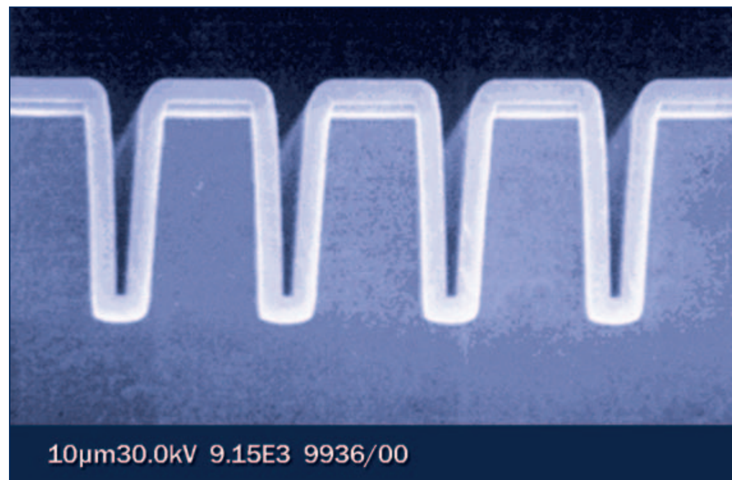


Figure 3-3: Uniform ALD alumina coating inside deep trenches of silicon die.[3]

Limitations

ALD has some limitations keeping it from being more prevalent in production. Growing a film one atomic layer at a time requires a large number of cycles and time to obtain a sufficiently thick film. If the reaction chamber is not sufficiently filled with the reactant gas or purged before saturation occurs, the coating will be non-uniform. If the chamber is not fully desorbed when the new reactant is introduced, the purity of the deposition and well as the deposition thickness will vary.

Equipment Specification for ALD Process Implementation

Equipment design is critical for successful ALD process implementation. This is a clean process requiring equipment installation in a class 1000 clean room or better. While similar to CVD equipment, the ALD process requires the precursor lines be separated all the way from the source to the reaction chamber. This prevents precursor mixing during processing and avoids the possibility of any CVD reactions. A minimum of two separate precursor lines, vacuum line, air, plasma gas lines are required to operate ALD equipment.

Substrate temperature, precursor gas pressures, and reaction time are all critical to the ALD process. The reaction chamber should be large enough for substrates to maintain a uniform temperature, whether they are processed one at a time or as a batch process. Some equipment designs place the reaction chamber inside a vacuum chamber to assure uniform temperatures. Precursor lines should be monitored and regulated to control the pressure and volume entering the reaction chamber. The ability to completely purge excess precursor gas and introduce a second precursor is necessary for ALD to produce a uniform layer.

continued on page 9

Implementation of ALD Coating

(continued from page 8)

With advancements in technology, the need to reduce device footprints, and reduce costs, alternative manufacturing processes like ALD are being considered to hermetically secure the components and protect them from environmental hazards. More work is still needed to characterize thermal stability and RF performance of devices with ALD films.

For any other information regarding using atomic layer deposition as conformal coating on components and PWB, please contact the EMPF Helpline at 610.362.1320.

References

[1] Ritala, Mikko, and Jaakko Niinisto. "Chapter 4: Atomic Layer Deposition." *Chemical Vapour Deposition Precursors, Processes and Applications*. Cambridge: RSC, 2009. 158-206. Print.

[2] Ely, Kevin. "Issues in Hermetic Sealing of Medical Products." *Medical Device & Diagnostic Industry Magazine*. Jan. 2000. Web. <http://www.mddionline.com/article/issues-hermetic-sealing-medical-products>.

[3] Leskelä, Markku. "Industrial Applications of Atomic Layer Deposition (ALD)." 10th MIICS Conference, Mikkeli, Finland. Web. 18 Mar. 2010. <http://www.miics.net/2010/material/Industrial%20Applications%20of%20Atomic%20Layer%20Deposition%20%5bALD%5d.pdf>.

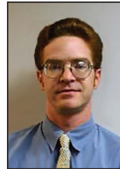
Anand Bhavankar | Senior R&D Engineer

Tech Tips: Masking for Conformal Coatings

(continued from page 4)

tape, peelable mask, or plugs. The major disadvantage of fixtures is that they can require significant upfront investment and may require modification or redesign every time the design of the PCBA is changed.

Masking is a common requirement for processes that apply conformal coatings to PCBAs. A variety of techniques exist for masking a PCBA and the EMPF can assist manufacturers in determining the best technique for each process. For assistance with masking, conformal coatings or any other electronics manufacturing questions, contact the EMPF Helpline at 610.362.1320 or email helpline@empf.org.



Jason Fullerton | Sr. Product and Applications Engineer

Upcoming Courses

IPC Challenge Test

January 21, 2011

Challenge testing is available to both CIS and CIT students. It can be a real time-saver for students with a previous certification or a high level of comprehension of the standard.

IPC A-610

January 24-27, 2011 | CIT Certification

Achieve the highest quality and most cost-effective productivity by knowing how to correctly apply the IPC A-610 acceptability criteria.

IPC 7711/7721

January 24-28, 2011 | CIT Certification

Experience an intense, hands-on printed circuit board rework and repair lab coupled with a review of all the applicable procedures outlined in the IPC 7711/7721A specification.

Contact the Registrar via: *phone* **610.362.1295**
email **registrar@empf.org**
online **www.aciusa.org/courses**

ACI Technologies, Inc.

2011 Class Schedule

National Electronics Manufacturing Technology Center of Excellence

Electronics Manufacturing

Boot Camp A
February 7-11
May 9-13
August 15-19
November 7-11

Boot Camp B
February 14-18
May 16-20
August 22-26
November 14-18

CIS/Operator

IPC J-STD-001
Call for Availability

IPC A-610
Call for Availability

IPC 7711/7721
Call for Availability

IPC/WHMA-A-620A
CIS Certification
March 14-16
June 27-29
September 6-8
December 19-21

IPC CIT Challenge Test

January 21
February 25
March 25
April 29
June 10
July 29
September 9
October 14
November 18
Call for Additional Availabilities

IPC Certifications CIT/Instructor

IPC A-600
CIT Certification
January 19-21
April 18-20
July 25-27
October 24-26

IPC A-610
CIT Certification
January 24-27
March 21-24
April 25-28
June 6-9
July 25-28
September 26-29
October 10-13
November 28 - December 1

IPC A-610
CIT Recertification
January 10-11
February 28 - March 1
April 4-5
May 23-24
June 20-21
July 18-19
August 29-30
October 3-4
December 5-6

IPC J-STD-001
CIT Certification
January 3-7
March 7-11
April 18-22
June 13-17
July 11-15
September 12-16
October 17-21
December 12-16

IPC J-STD-001
CIT Recertification
January 12-13
March 2-3
April 6-7
May 25-26
June 22-23
July 20-21
August 31 - September 1
October 5-6
December 7-8

IPC J-STD-001
Space Addendum
CIT Certification
January 14
March 4
April 8
May 27
June 24
July 22
September 2
October 7
December 9

IPC 7711/7721
CIT Certification
January 24-28
May 2-6
August 8-12
November 28 - December 2

IPC 7711/7721
CIT Recertification
February 7-8
May 9-10
August 15-16
November 7-8

Skills

BGA Manufacturing, Inspection, Rework
January 10-11
April 25-26
August 1-2
November 21-22

Chip Scale Manufacturing
February 28 - March 2
June 13-15
September 19-21
December 5-7

Solder Techniques for Electronic Assemblies
March 17
June 30
September 22

Continuing Professional Advancement

Design for Manufacturability
March 14-15
June 20-21
August 29-30
October 31 - November 1

Failure Analysis and Reliability Testing
March 28-30
June 6-8
September 12-14
December 19-21

Lead Free Manufacturing
February 23-24
June 1-2
September 7-8
December 12-13

For course information and pricing, contact the Registrar at 610.362.1295 or via email at registrar@empf.org

Electronics manufacturing assistance is available on the EMPF Helpline — simply call 610.362.1320 or send an email to helpline@empf.org

ACI is conveniently located next to the Philadelphia International Airport.

All courses and dates subject to change without notice.