Altera Quartus II Tutorial
ECE 552

Quartus II by Altera is a PLD Design Software which is suitable for high-density Field-Programmable Gate Array (FPGA) designs, low-cost FPGA designs, and Complex Programmable Logic Devices CPLD designs. The tutorial is organized as follows. The first section gives pointers to Altera's website from where this software can be downloaded and instructions to install this software. The second section describes a step by step approach to designing a simple 2 to 4 decoder using Quartus II's Schematic Editor. The third section describes the functional simulation process of verifying the logic design of the decoder. Finally, section four describes using buses and hierarchical design. Each section is augmented with figures of each step.

1. Downloading and Installing Quartus II

1.1 Download

The software can be downloaded from Altera's website (www.altera.com) at following URL.
https://www.altera.com/support/software/download/altera_design/quartus_we/dnlquartus_we.jsp

1.2 Installation Instruction

Instructions to install the software can be found at the following URL.
https://www.altera.com/support/software/download/altera_design/quartus_we/inswebdnl_consol.html

1.3 Setting up Licensing

A license is no longer needed for the web version.

2 Creating Design Projects with Quartus II

In this section, we will learn to create a new project using Quartus II. For ease in understanding, I will go through each and every step in designing a simple digital circuit, a 2 to 4 decoder, with accompanying figures illustrating the step. The steps in creating a new project are as follows. After we have successfully installed Quartus II and set up the license, we load the software, go to the file menu and select 'New Project Wizard'. This will open 'New Project Wizard' dialog box. The first screen asks us to provide names of the working directory of the project, name of the project and name of the top level entity in the project. We will have to fill all these fields with the relevant information. Figure 1 illustrates this process.

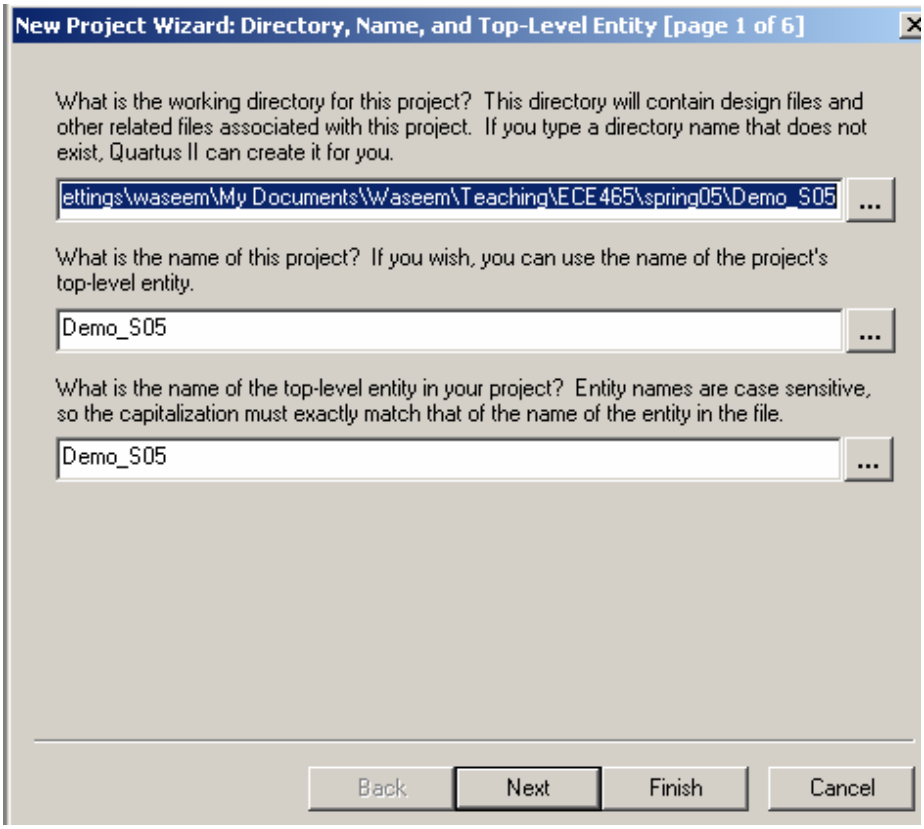

Figure 1. First screen of the 'New Project Wizard' dialog box

The second screen asks us to add files to the project that we may have designed in advance. Since we don't have any such file to add, we will simply click next button to skip this step. Screen 2 is shown in figure 2.

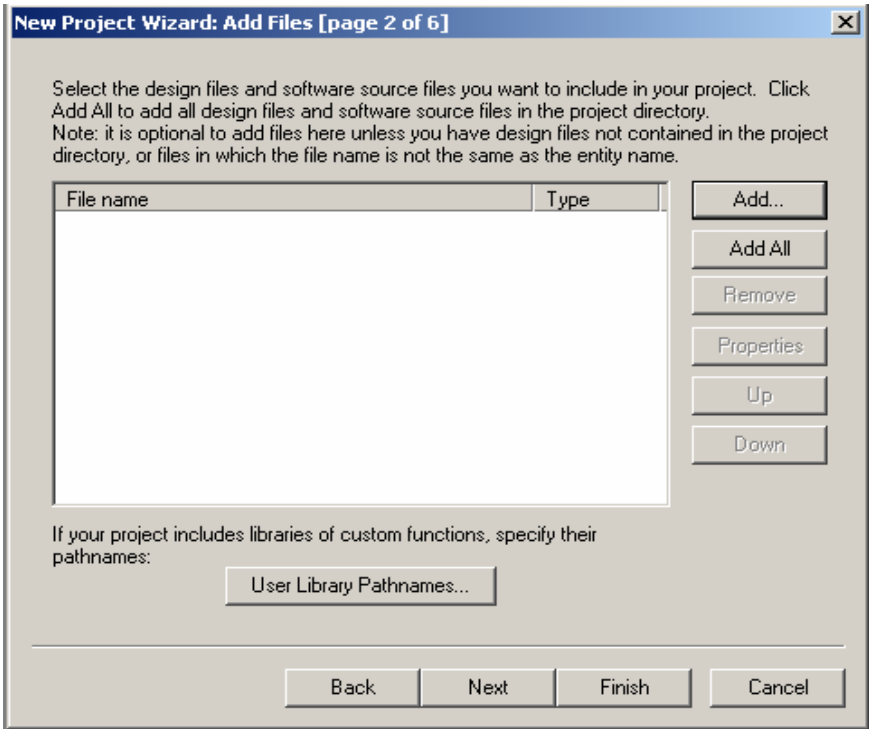

Figure 2. Screen2 of the 'New Project Wizard' Dialog box

Quartus allows users familiar with other PLD tools to integrate their designs from those tools with Quartus II generated projects. Screen3 basically asks if there are other tools apart from Quartus II that we plan to use during the project. Since there are no such tools in our case, we will simply skip this process by clicking 'next'. Screen3 is shown in figure 3.

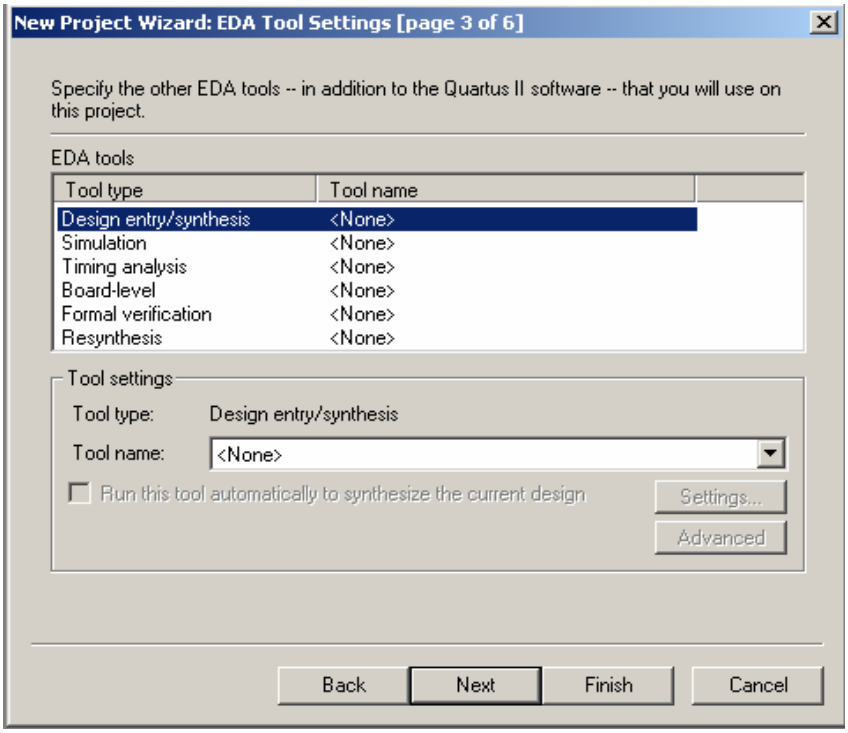

Figure 3. Screen3 of the 'New Project Wizard'

Screen4 of the wizard asks us the target device family for our project. For all projects in ECE552, we will let the compiler select the appropriate device. This step is shown in Figure 4.

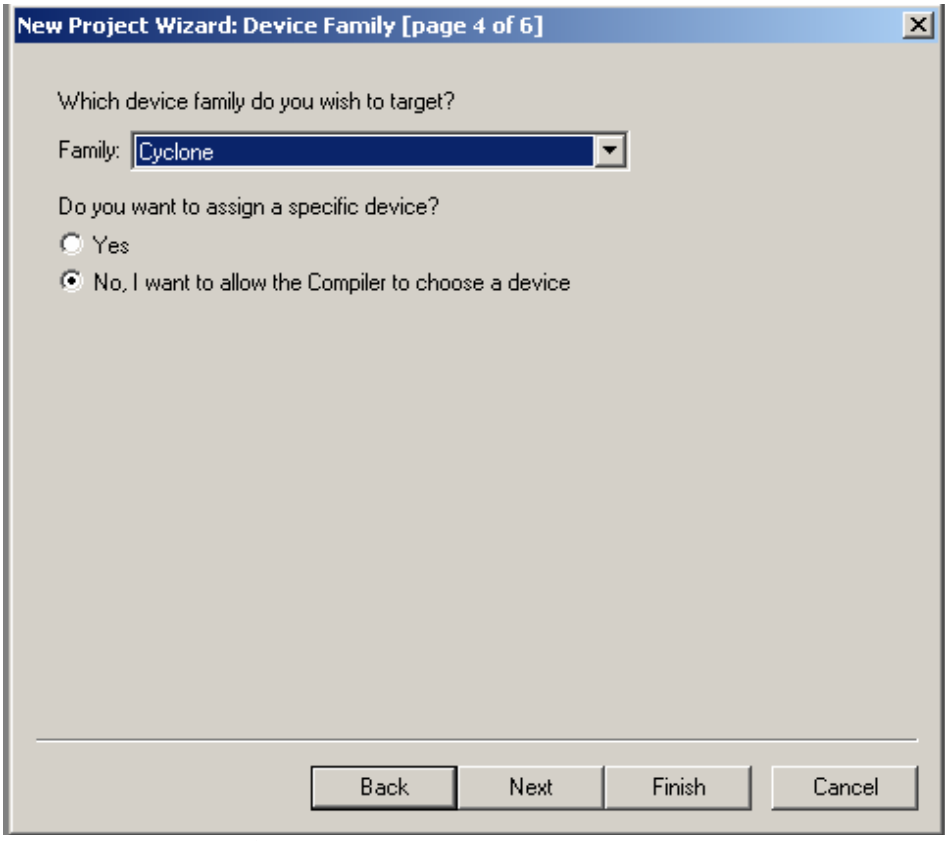

Figure 4. Screen4 of the 'New Project Wizard'

Screen 5 of the 'New Project Wizard' asks us to specify a list of devices so that the compiler can select one of them as the target device. For our case, default list will suffice. Screen5 is shown in Figure 5.

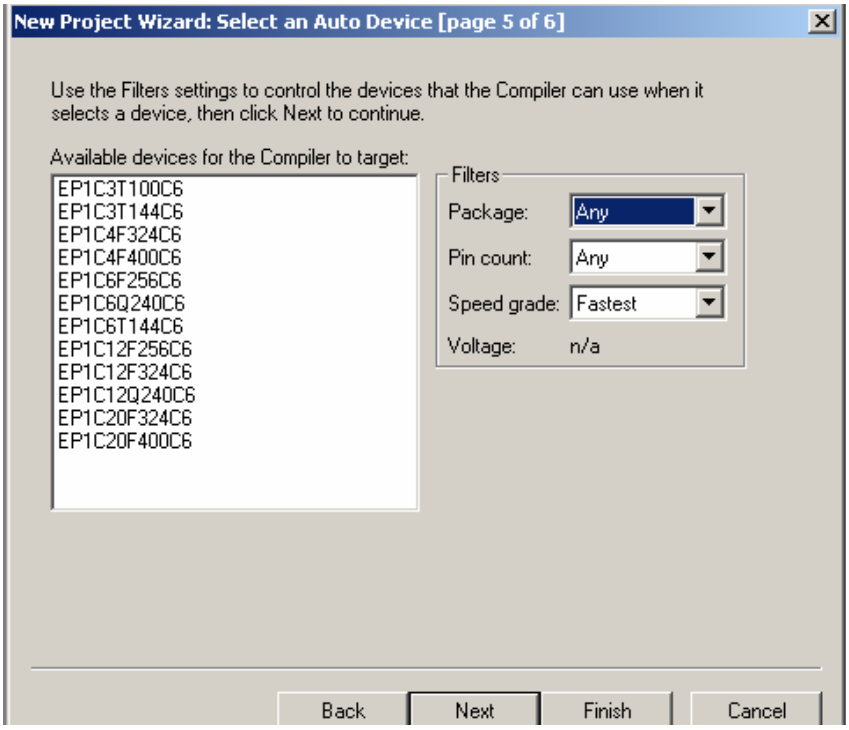

Figure 5. Screen5 of the 'New Project Wizard'

Finally Screen6 tells us that the 'New Project Wizard' is finished and the new project with the shown settings is created. This step is shown in Figure 6.

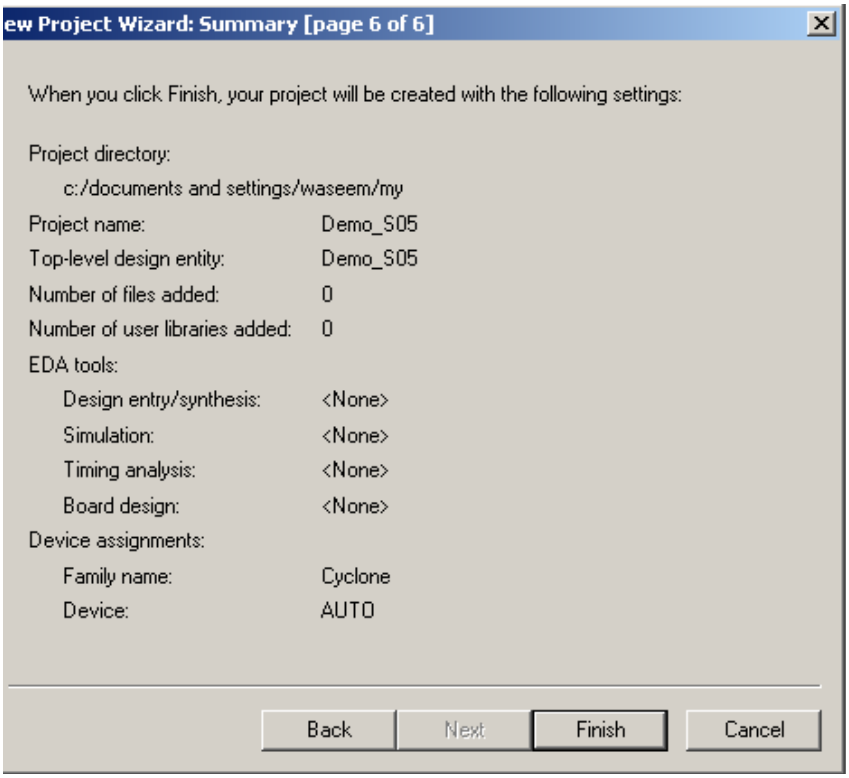

Figure 6. Screen6 of the 'New Project Wizard'

Once we are done creating the project space, we now need to create design files for the project. We will use Block Diagram/Schematic File based design method throughout the course. To create a new design file, we go to file menu and select 'New' which will open the 'New File' Dialog box as shown in Figure 7.

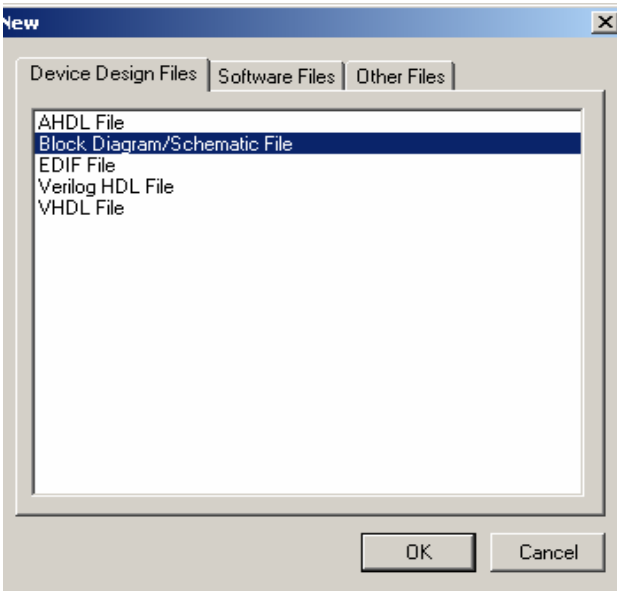

Figure 7. Creating a new schematic based design file

Once we highlight the Block Diagram/Schematic File and press OK. Quartus II will open a schematic editor with an array of tools arranged in sidebar. Figure 8 shows the toolbar holding schematic editor related tools. 'Symbol Tool' which we will use most frequently is highlighted. This tool has the shape of an AND gate.

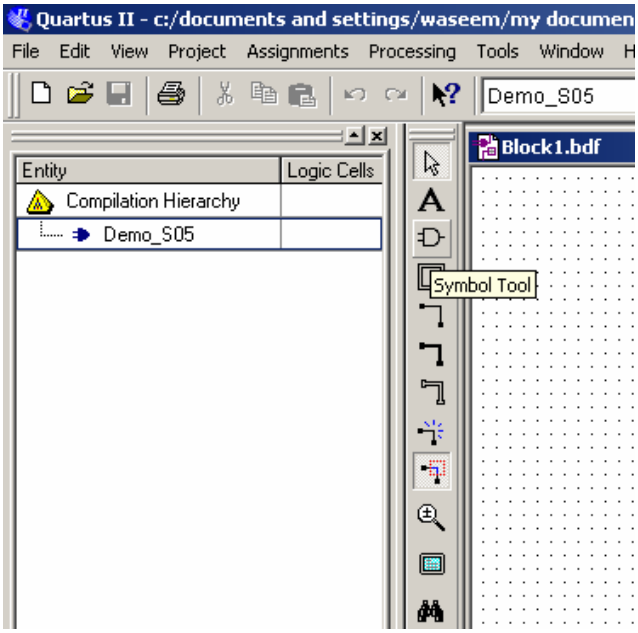

Figure 8. Tools available with Schematic Editor where 'Symbol Tool' with the shape of an 'AND' gate is highlighted

In our example of decoder design, we will use this 'Symbol Tool' to place all the logic elements required for our decoder circuit i.e. four 'AND' gates and two 'NOT' gates as well as input and output pins. The procedure to place any element in the schematic file is very simple, we simply select that element using 'Symbol Tool' and place it on the schematic file by the click of mouse and keep on clicking till we have placed it for the required number of times. When we are done, we just press 'ESC' key and the mouse pointer returns to the normal arrow pointer. Figures 9-13 illustrate this process.

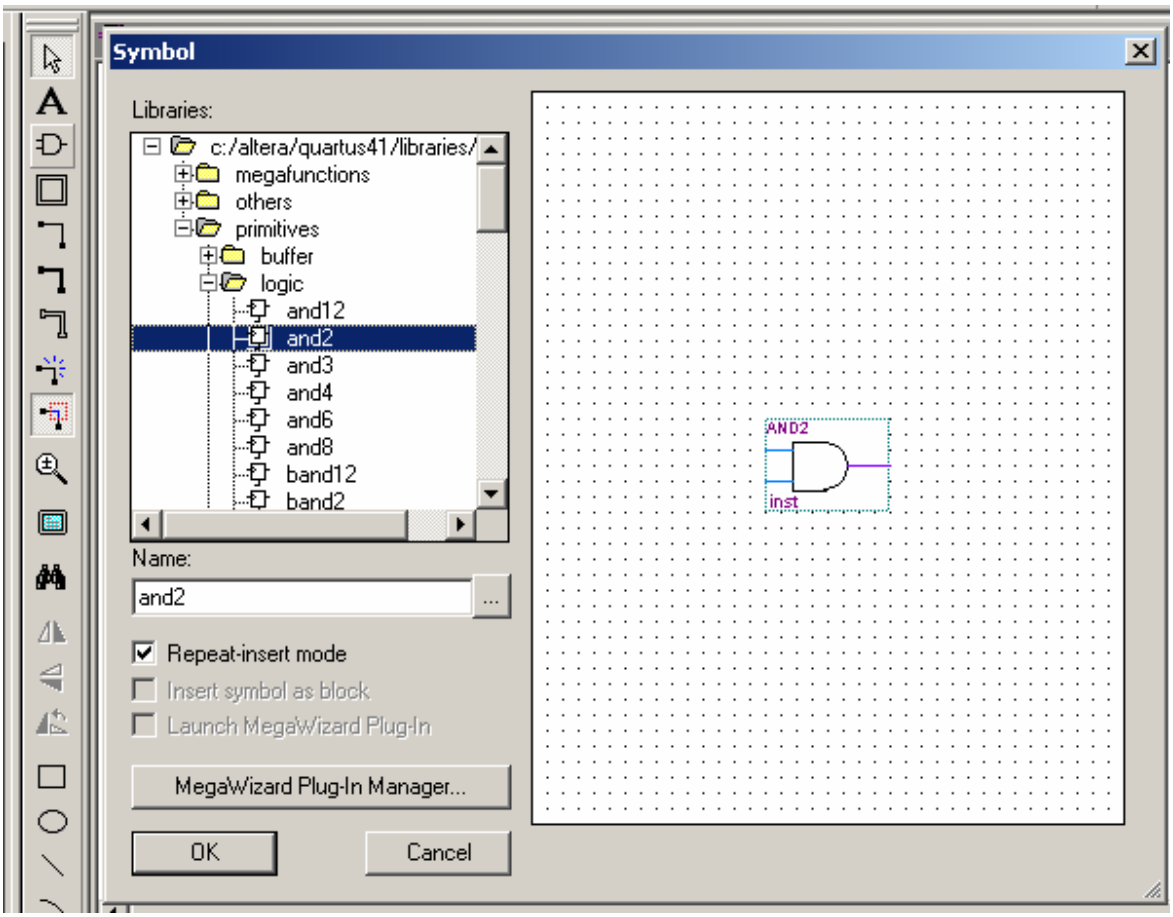

Figure 9. Selecting a 2-input 'AND' gate using 'Symbol Tool'

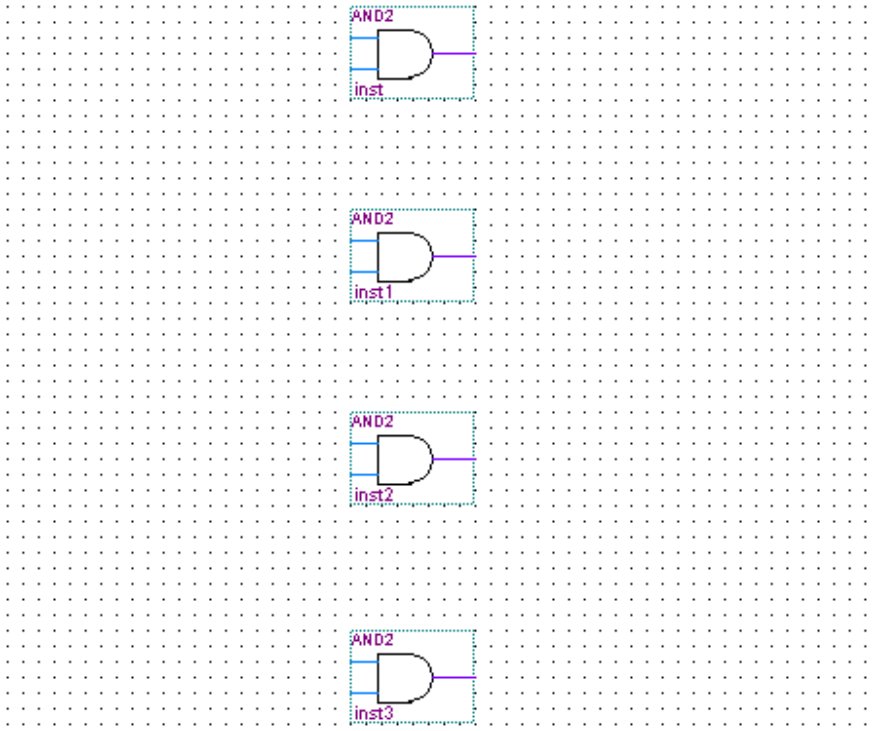

Figure 10. Four AND gates placed on the schematic layout area.

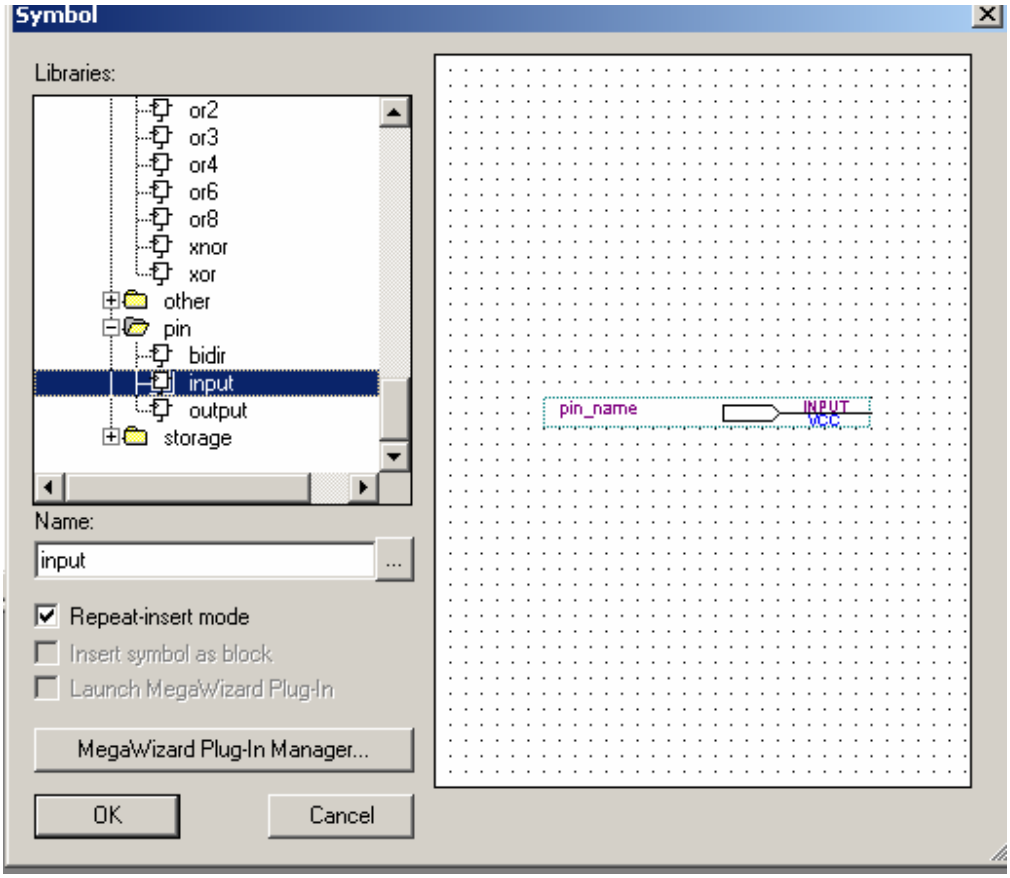

Figure 11. Selecting an 'Input' pin using 'Symbol Tool'

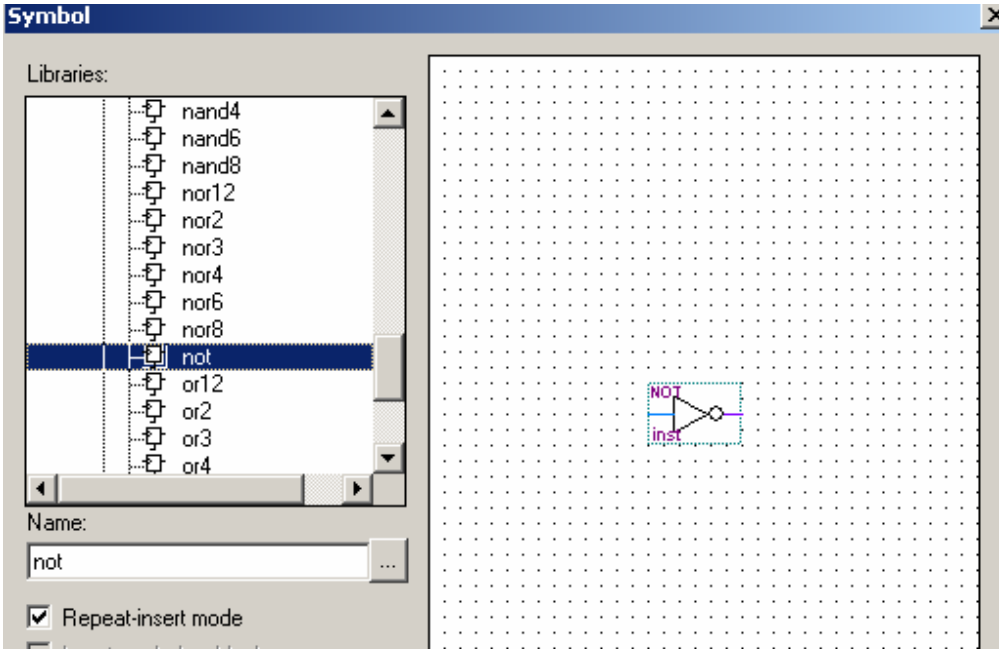

Figure 12. Selecting a 'NOT' gate using 'Symbol Tool'

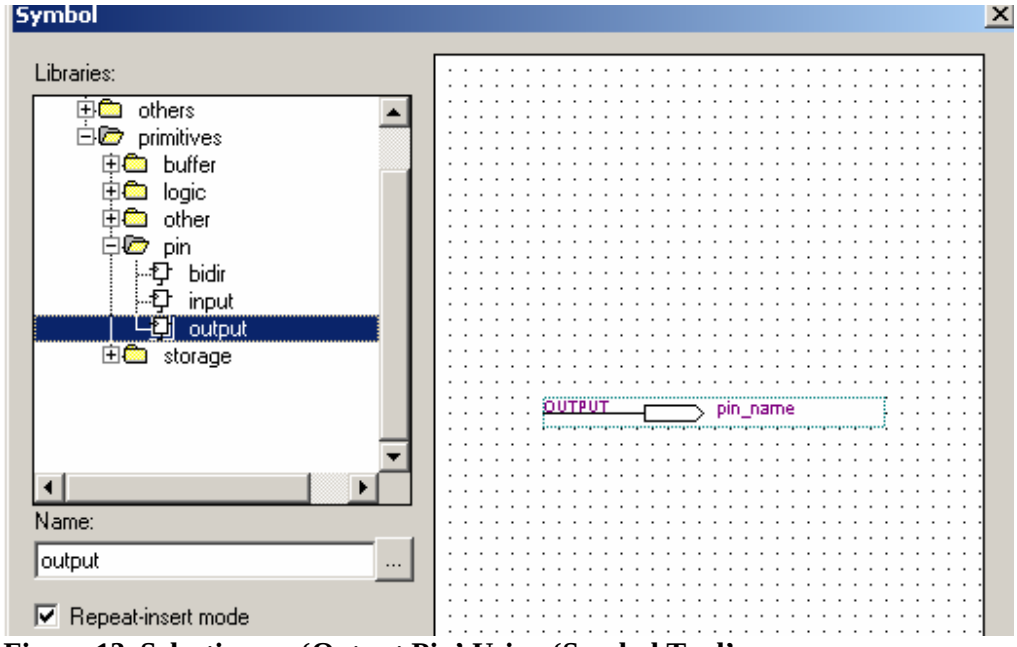

Figure 13. Selecting an 'Output Pin' Using 'Symbol Tool'

Figure 14 shows all the logic elements, without wiring, placed in the schematic file design layout area.

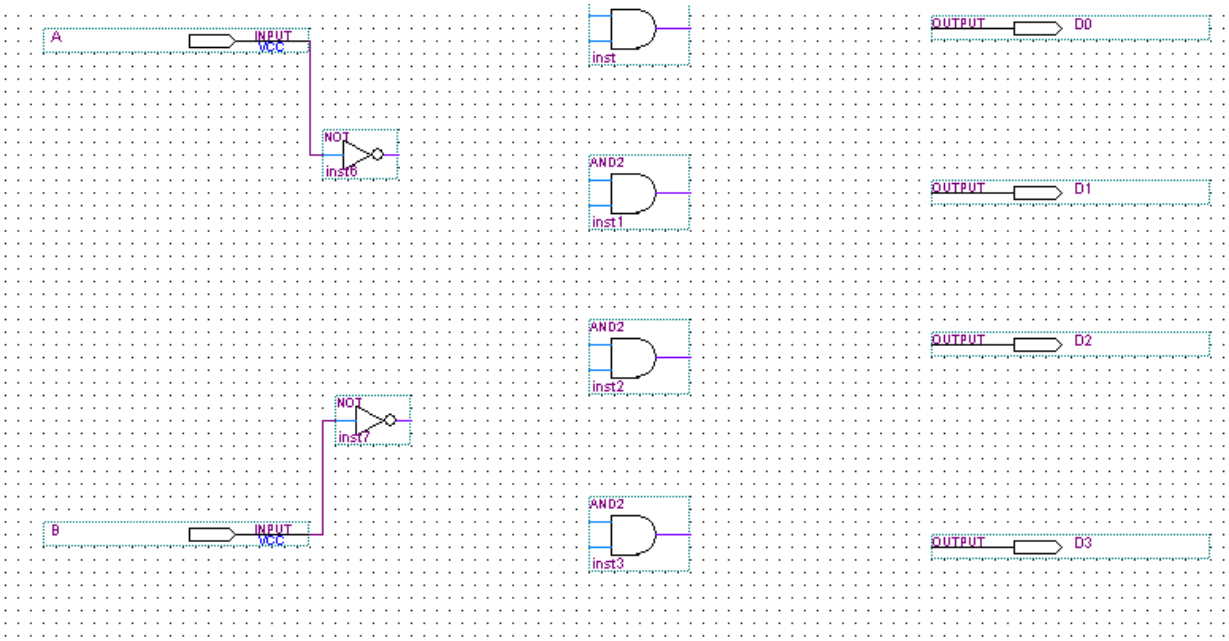

Figure 14. All logic elements required for the 2 to 4 Decoder circuit, shown placed on Schematic design layout area

Figure 15 shows how all these elements are connected to form the eventual decoder circuit.

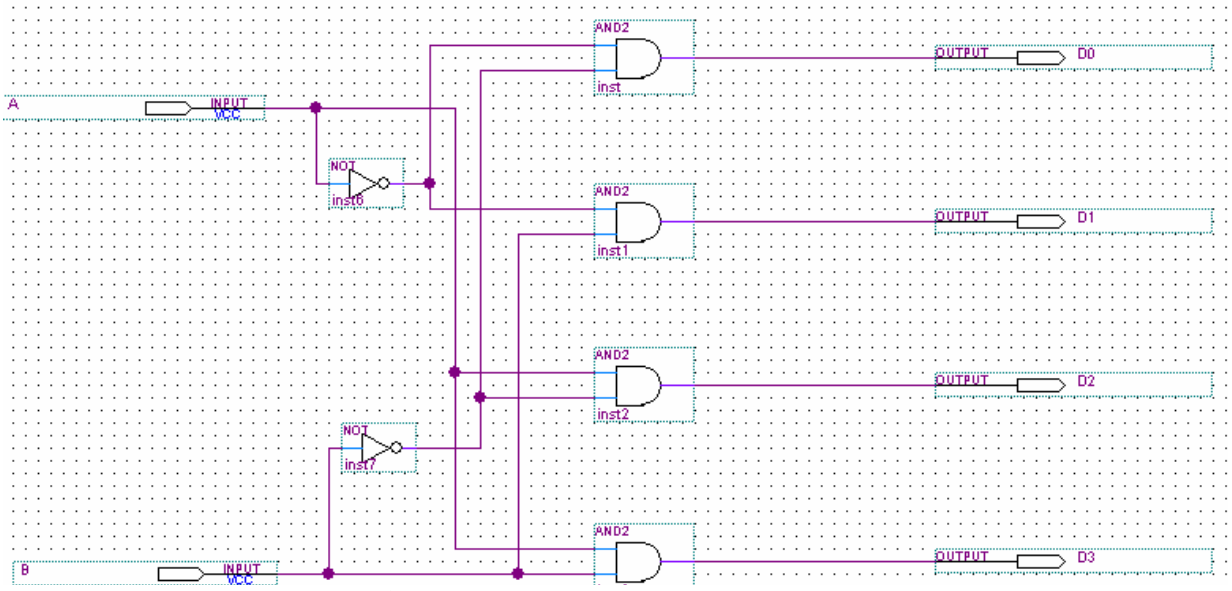

Figure 15. Schematic design of the entire 2 to 4 Decoder circuit

Figure16 shows the step of saving the schematic design file. We must make sure that 'Add file to the Current Project' checkbox is in checked state while saving the file. After saving the file, we compile our project (see figure 17) and if the compilation is successful, move to the next step of simulating the circuit which is explained in the next section.

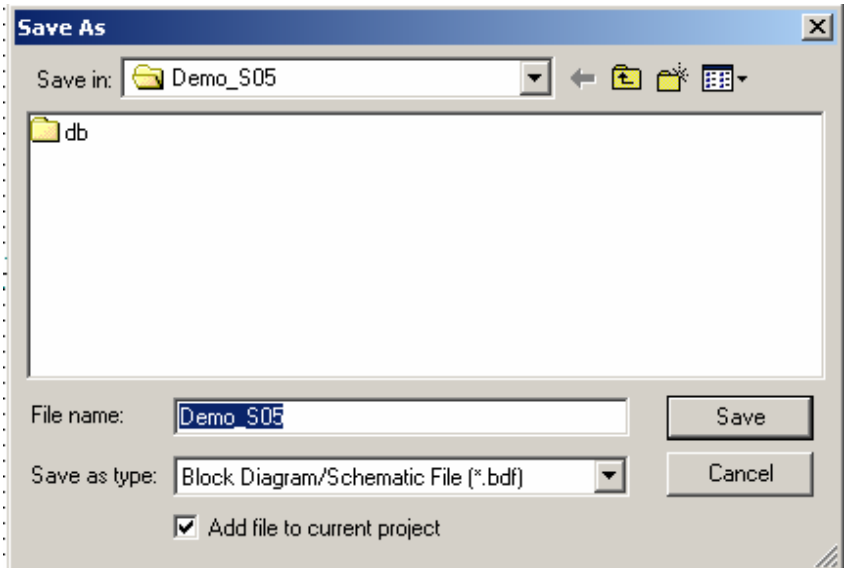

Figure 16. Saving the schematic file, make sure that 'Add File to current project' checkbox is in checked state

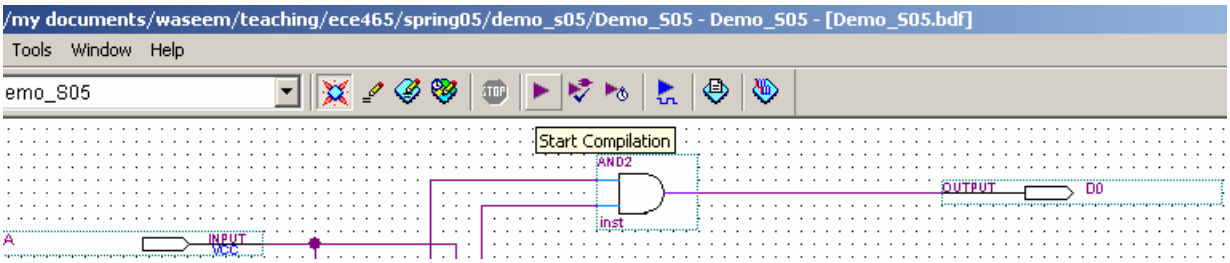

Figure 17. Compiling the schematic design

3 Simulating Designed Circuits Using Quartus

In this section, we will follow the same step by step illustrative approach to go through each step required to perform simulation of the decoder circuit in the previous section. First step is to create a new Simulation Input file. We will use the "Vector Waveform File' format to define simulation inputs. To create a new 'Vector Waveform file' we first go to file menu, select 'New' and then select 'Vector Waveform File' in the 'Other Files' tab on the 'New File' Dialog box. The step is shown in Figure18.

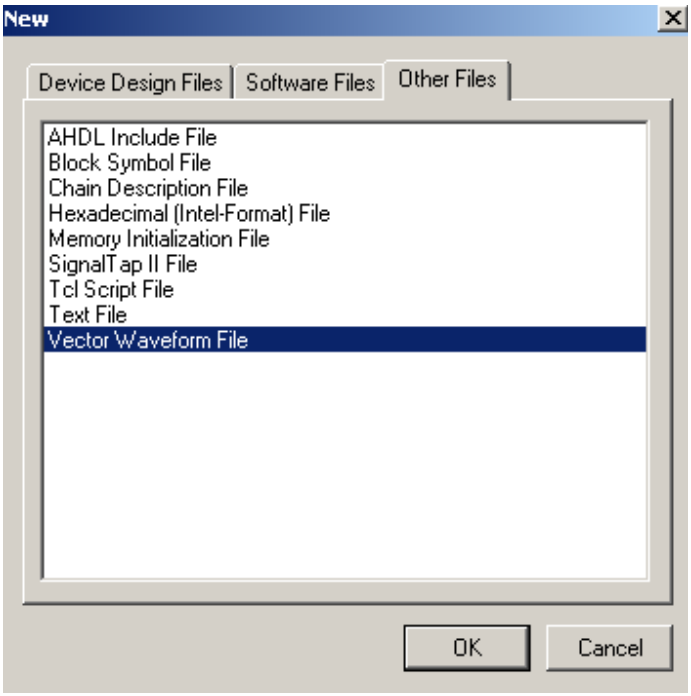

Figure 18. 'New File' Dialog box for creating a new simulation file based upon 'Vector Waveform File' format

After pressing OK on the "New File' Dialog box, we go to the 'View' menu, select 'Utility Windows' and then select 'Node Finder' as shown in Figure19.

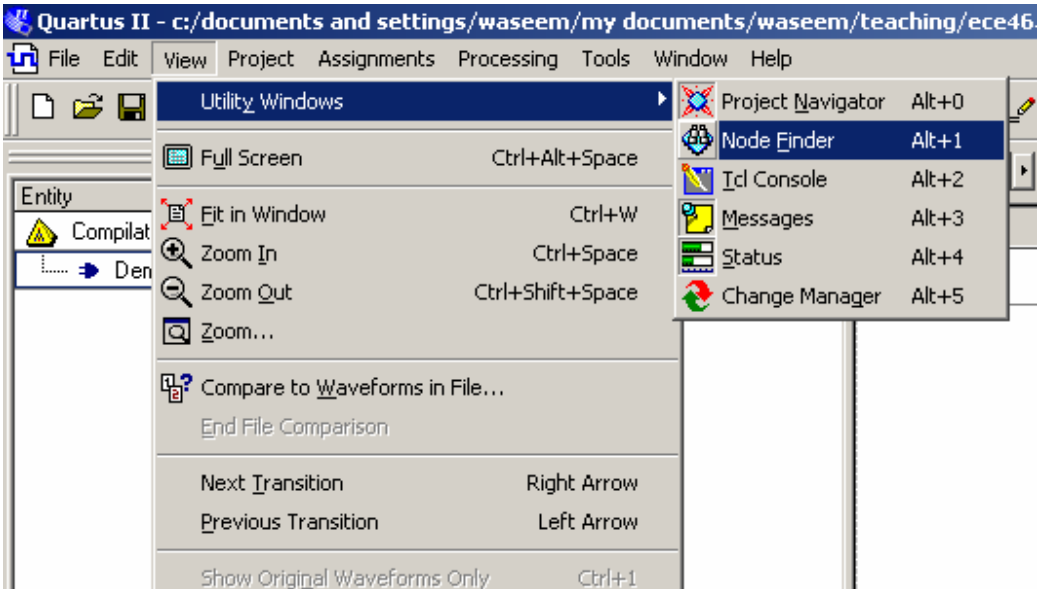

Figure 19. Selecting the 'Node Finder' tool

We will use 'Node Finder' to select input nodes of our newly designed circuit. What I have done here is to simply ask it to list all nodes by using the filter pins: all as illustrated in Figure20.

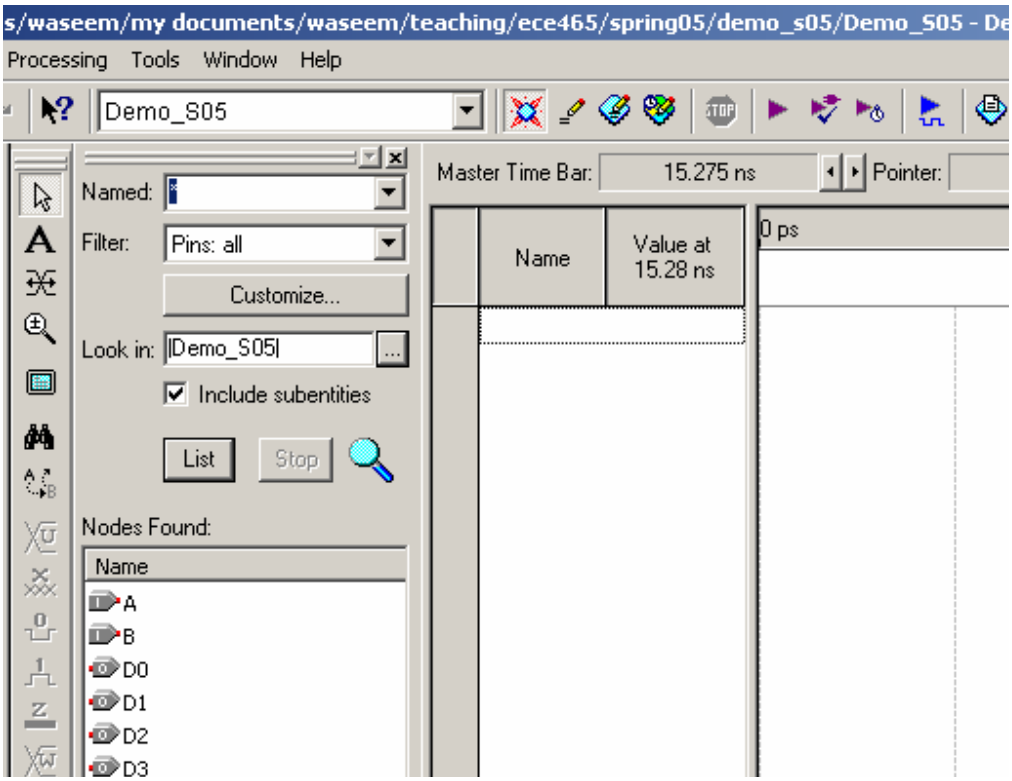

Figure 20. The input and output nodes enumerated by 'Node Finder' tool

Once it shows all the pins I select the input ones (represented by a preceding i on a pin shape) and drag them to the vector waveform file designated area for inputs as shown in Figure21.

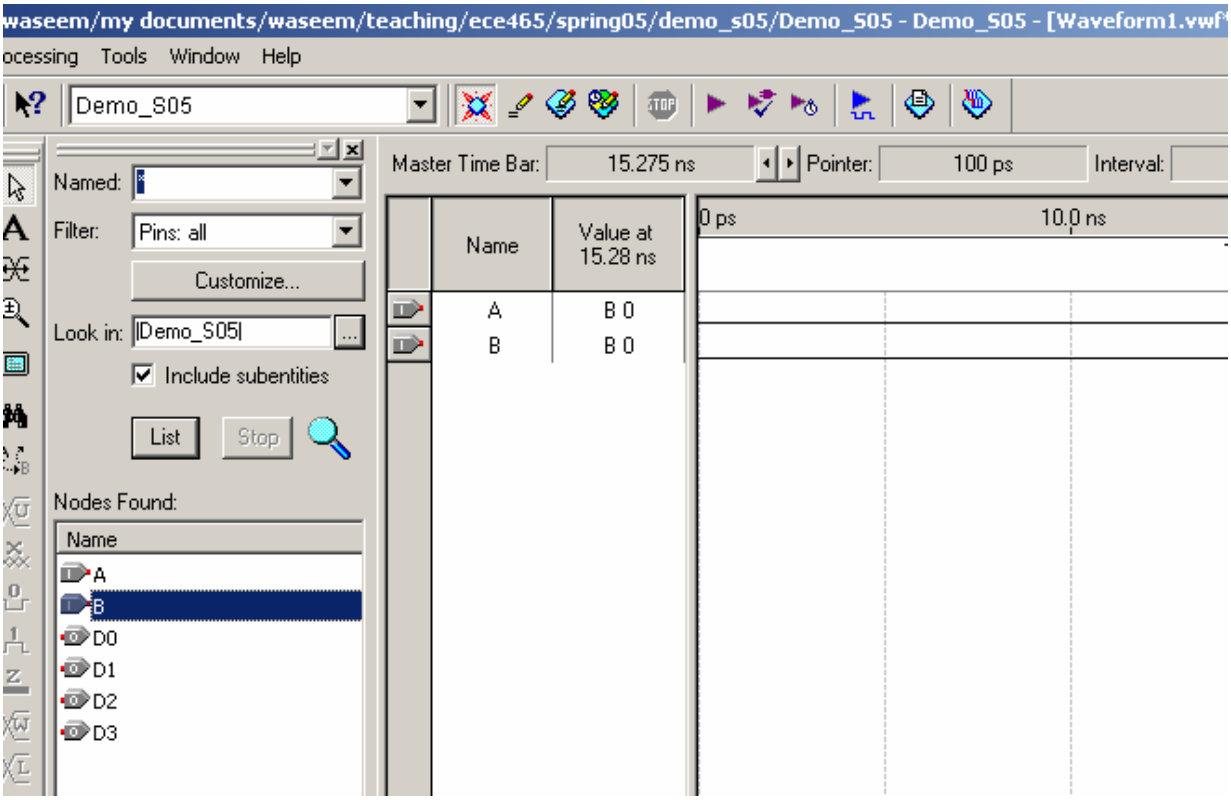

Figure 21. Dragging input nodes onto the simulation input file.

Once we have dragged the input nodes on the Vector Waveform file, we will use the 'Waveform Editing Tool' (shown highlighted!in Figure22) to create simulations waveforms for the inputs. For this, we simply select the 'Waveform Editing Tool' and drag it on the waveform area corresponding to the input for which we want to generate the waveform. Just by dragging mouse pointer, after selecting this tool, on the waveform area we cans switch between logic low and logic high levels as shown in Figure23. Finally once we have generated the waveforms corresponding to all inputs (two in case of decoder) (Figure24) we save the simulation file (Figure25).

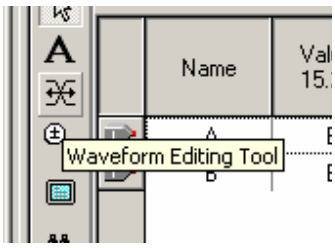

Figure 22. The 'Waveform Editing Tool' highlighted

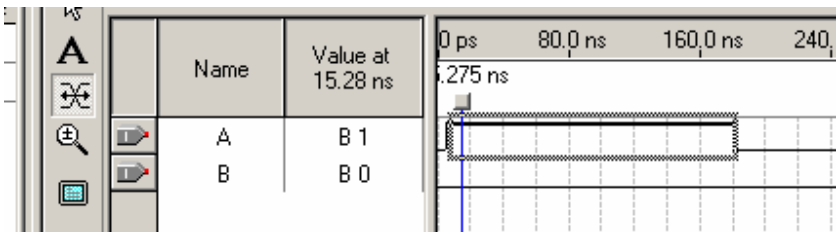

Figure 23. Using 'Waveform Editing Tool' to create waveforms for input nodes A and B

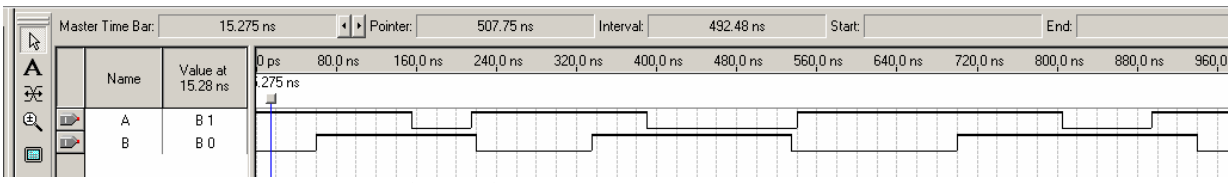

Figure 24. The simulation waveforms for inputs A and B

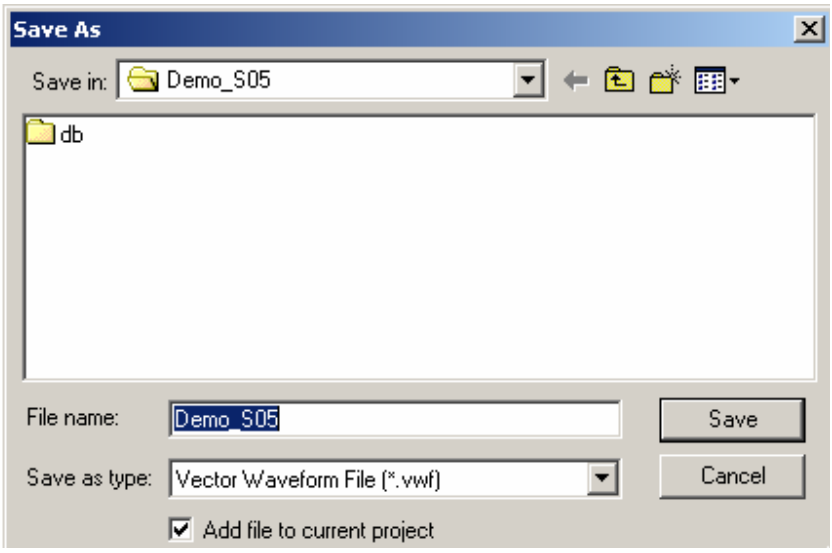

Figure 25. Saving the 'Vector Waveform File' format based simulation input file for decoder circuit.

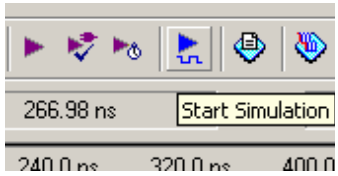

Figure26. "Start Simulation' button highlighted

After saving the simulation input 'Vector Waveform File'. We perform simulation by pressing the 'Start Simulation' button (shown highlighted in Figure26).

Once simulation is done
successfully, we can see output waveforms corsesponding to output pins on the Vector Waveform File as shown in Figure27

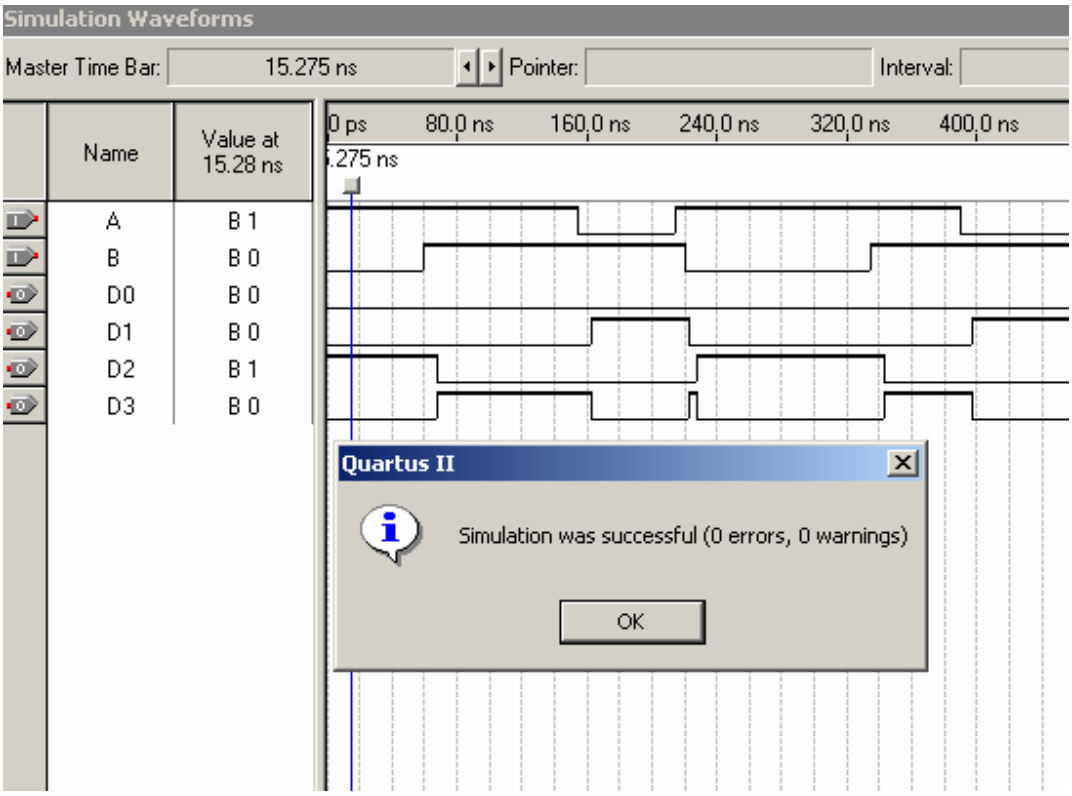

Figure 27. Simulation Results

4 Hierarchical Design and Buses Using Quartus

In this section, we will follow a similar step-by-step illustrative approach to learn how to perform hierarchical design and how to use buses in our design. First, make sure the demo.bdf schematic is open, then we need to save a copy, e.g., *File → saveas → 2to4.bdf.* Then, make sure this file is open in the design window. Delete the nets connecting the inputs and outputs to the rest of the circuitry, and also delete all but one of the inputs and outputs. The results are shown in figure 28.

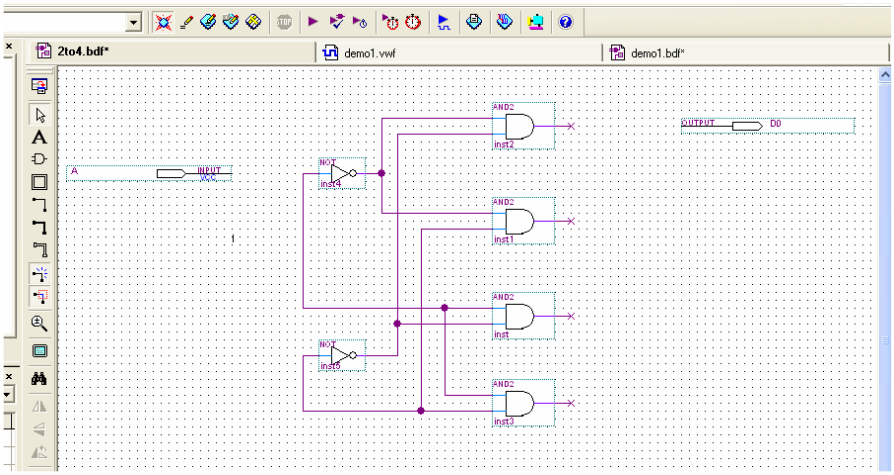

Figure 28.

Rename the input as ‘A[1..0]’ and the output as ‘CS[3..0]’. You can easily do this by putting the mouse over the object, right-clicking, selecting ‘properties’, and changing the name. Add a bus to the input and a bus to the output. Do this by selecting the bus symbol (like the net symbol but with a thicker line) and drawing the bus lines. The results are shown in figure 29.

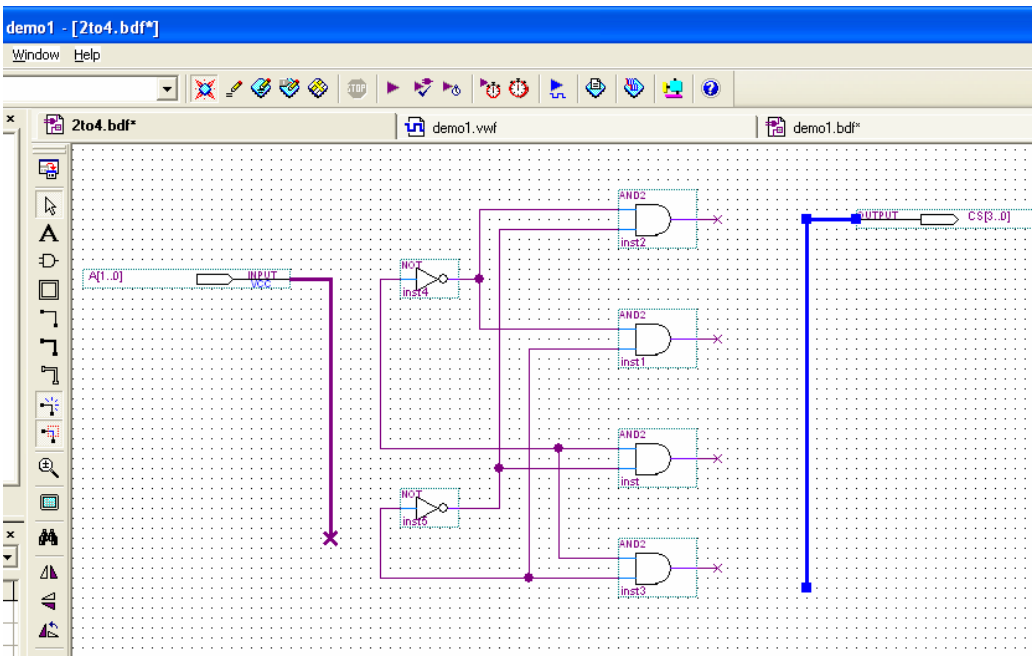

Figure 29.

Now select the net tool and add nets from the NOT gate inputs to the input bus and from the AND gate outputs to the output bus. Name the buses and nets by right-clicking on each in turn, selecting 'properties' and changing the name. See figure 30 for the name assignments.

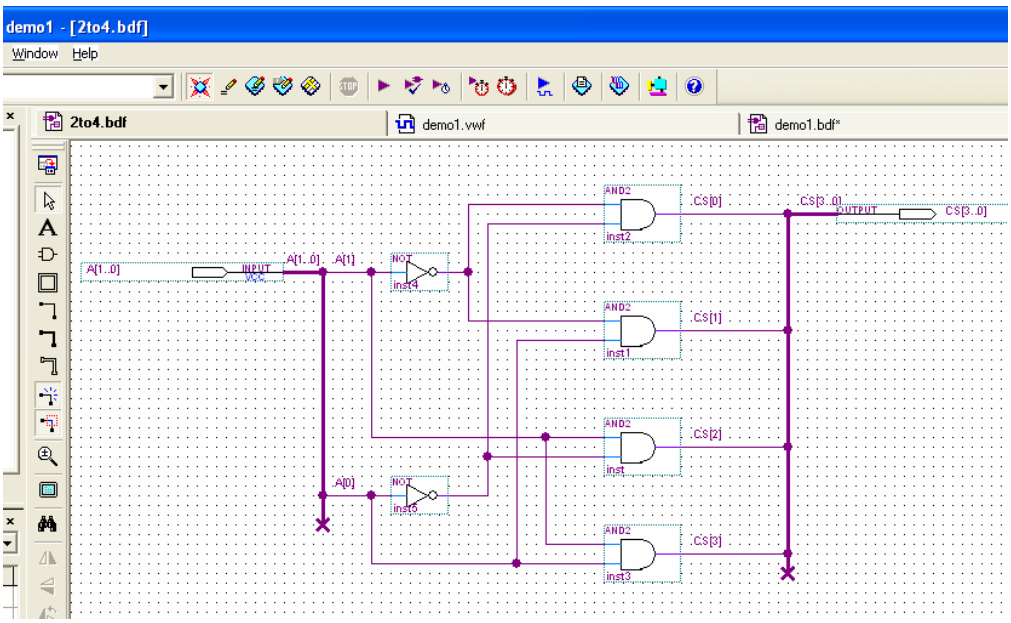

Figure 30.

Save the design file. Now we need to make a symbol file for use in schematics. Do *File → Create/update → Create symbol file* to save 2to4 as a symbol.

Now, open demo.bdf again. Delete the circuit logic symbols and the nets, as well as all inputs and outputs except one of each. Rename the input to A[3..0] by doing a *{right-click} → Properties* and changing the name. Repeat the procedure to change the output to CS[7..0]. Your schematic should look like that of figure 31.

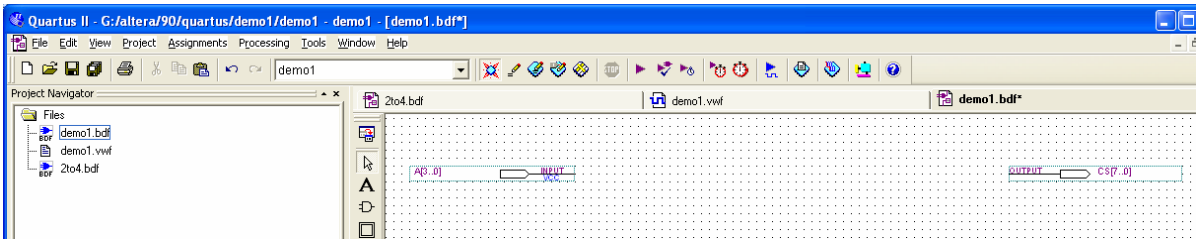

Figure 31.

Now we need to add two 2to4 decoder symbols using the decoder we designed earlier. In the toolbar, select the 'symbol' key and in the dialog box that comes up, select *Project → 2to4* then 'OK'. This dialog is shown in figure 32.

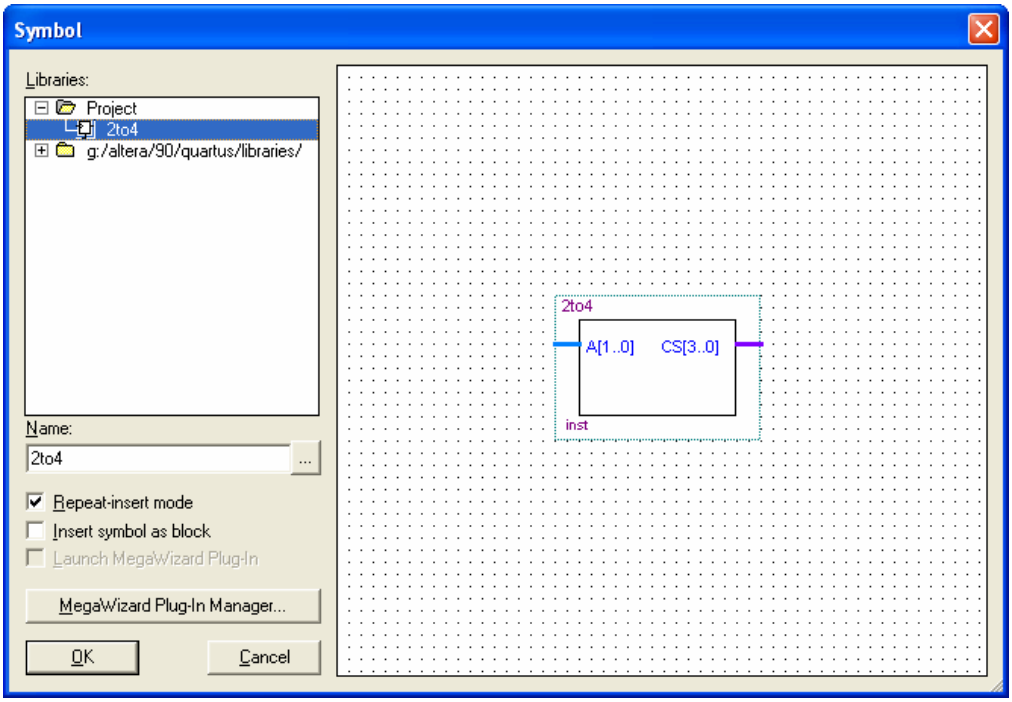

Figure 32.

Place two copies of the 2to4 decoder in the schematic and hit 'Esc'. Your schematic should look like figure 33.

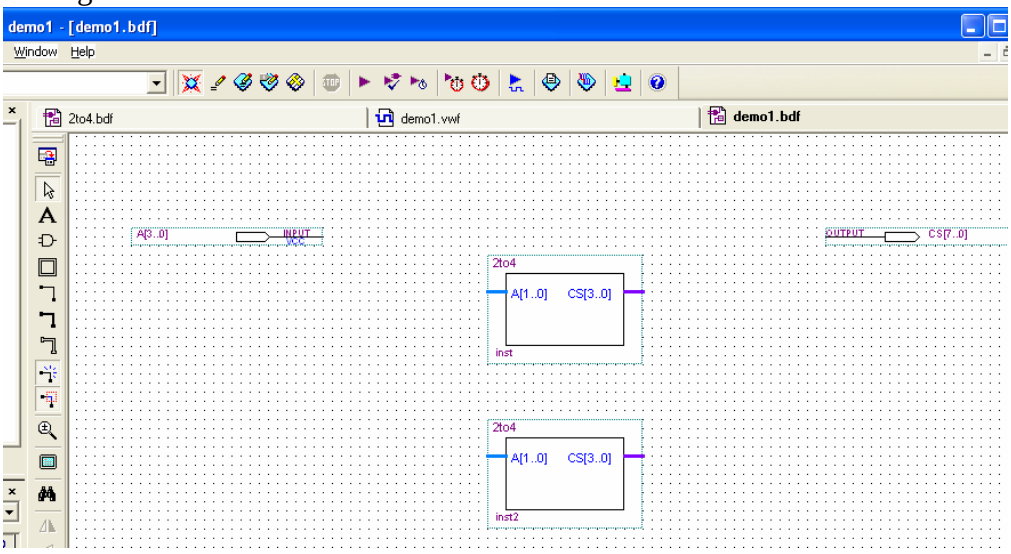

Figure 33.

Add buses to the input and to the output and connect to the decoders with sub-buses. Select each segment of the buses in turn, then *{right-click}* → *Properties* and name them to match figure 34.

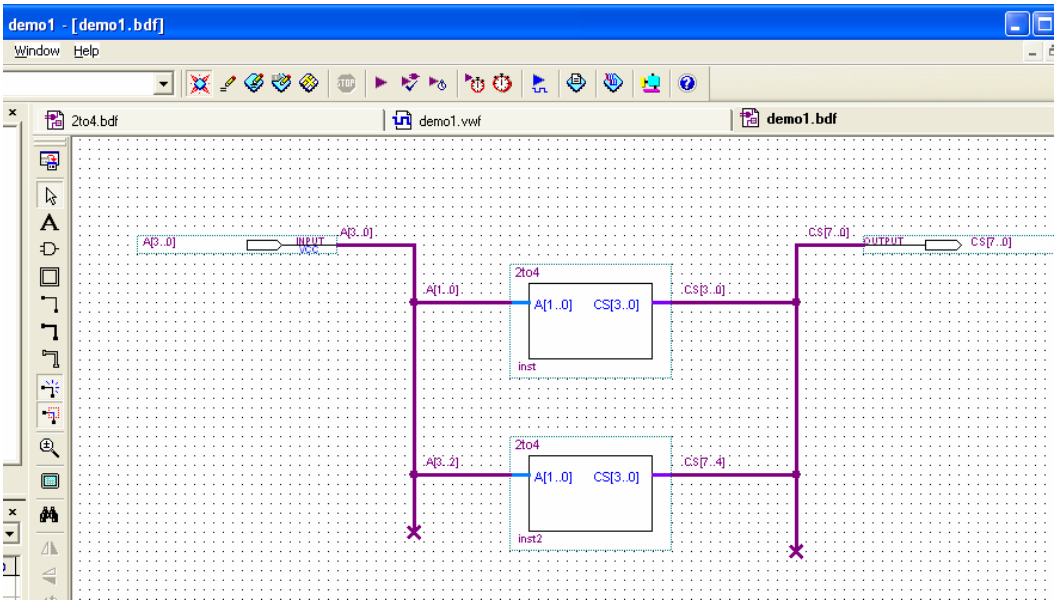

Figure 34.

Save the file. Now we need to set this as the top-level entity. In the 'Project Navigator' area, select demo.bdf and *{right-click}* → *set as top-level entity*.

Congratulations! You are now a Quartus II expert!