Altium

ALTIUMLIVE 2018:
PCB Design Best Practices: Routing Techniques In Altium Designer

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- VP/Founder of *San Diego PCB, Design, LLC*
- 3 PCB Layout Design Service Centers with 20 Fulltime Designers
- 4 Major CAD Platforms: Customers in all Industry Sectors
- Eptac: IPC-CID/CID+ MIT (Master IPC Trainer)
- Primary Contributor of the IPC-CID+ Curriculum
- IPC Designers Counsel – Executive Board Member
- PCB Designer 42 Years: *"I Love PCB Design and I Love Altium"*

Agenda

1. **Layout Designers Perspectives**
2. Routing Challenges of Today and Tomorrow
3. Rules
4. HDI and Via Fanouts – Fine Pitch BGAs
5. Electrical Performance of Advanced Routing
6. Differential Pair Routing

Where Do You Start?

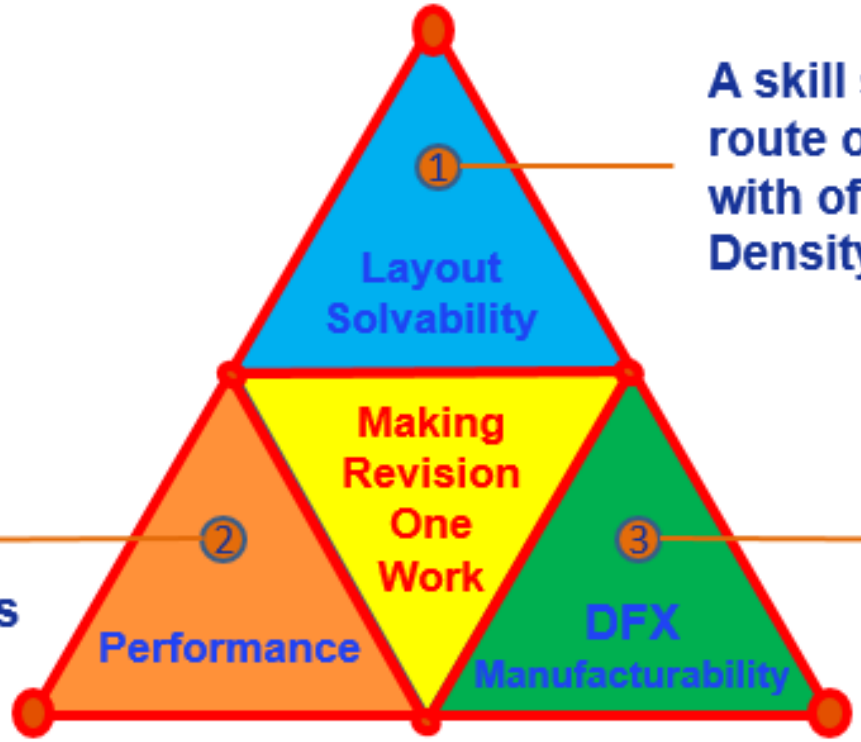
What are the goals or requirements for the "End Usage" ?

- Environment – electrical, mechanical and physical
- Industry segment
- Quantity in production (everything is proto-typed)
- Cost
- Performance
- Schedule and supply chain

Research all requirements at the start of the layout!

MOST IMPORTANT SLIDE

Today's Designer Must Meet 3 Perspectives for Success



A skill set to solve the place and route of all parts and connections with often with complex High Density Interconnect (HDI)

Signal (SI) & Power Integrity (PI) meeting performance requirements on all layers

DFX considerations producing high yield and lower cost

THE RESULT

Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing

PCB Design Layout – Professional Definition

A designer must have knowledge and be competent in:

- **Layout solvability**

  A skill set to solve placement and routing of a complex geometric puzzle that often requires HDI

- **Circuit performance for SI & PI (Signal & Power Integrity, Thermal)**

  "Correct by Construction" is better than "Design, simulate and re-design"

- **DFX Manufacturability: Fabrication, assembly and test**

  Know your supply chain – manufacturer's capabilities (See Julie Ellis's presentation)

…and then know how to implement all this with my CAD software!

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Routing Challenges of Today and Tomorrow

As speed and performance increase, so does the heat…

We all know that heat is not our friend

So heat made us lower our voltages…

As voltage drops, so the size and pin pitch are reduced

So with reduced sizes and increased circuit performance

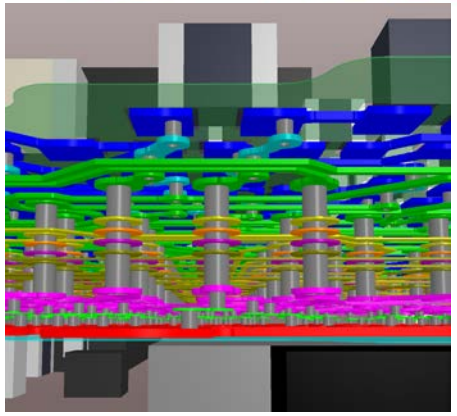
The pin counts often increase

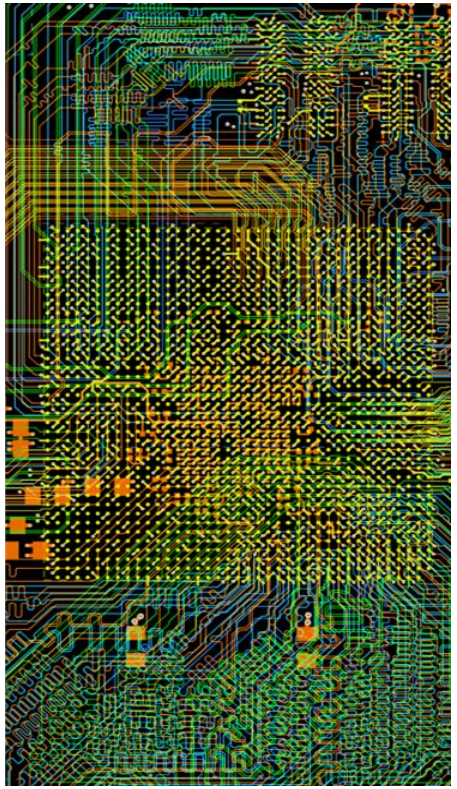
All these challenges lead us to advanced solutions:

- Increased placement density - VIP (Via in Pad) or Embedded Components
- Power delivery challenges - smart stack-ups, BC (Buried Capacitance)
- Increased routing density – HDI (High Density Interconnect)
- Signal integrity with faster switching circuitry EMI concerns
- Meeting all manufacturing concerns

… oh and did I mention,

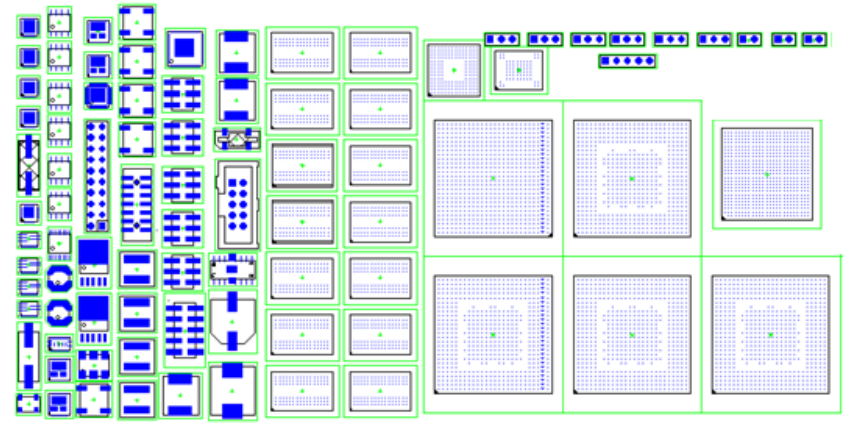
"It must cost less and be completed faster"!





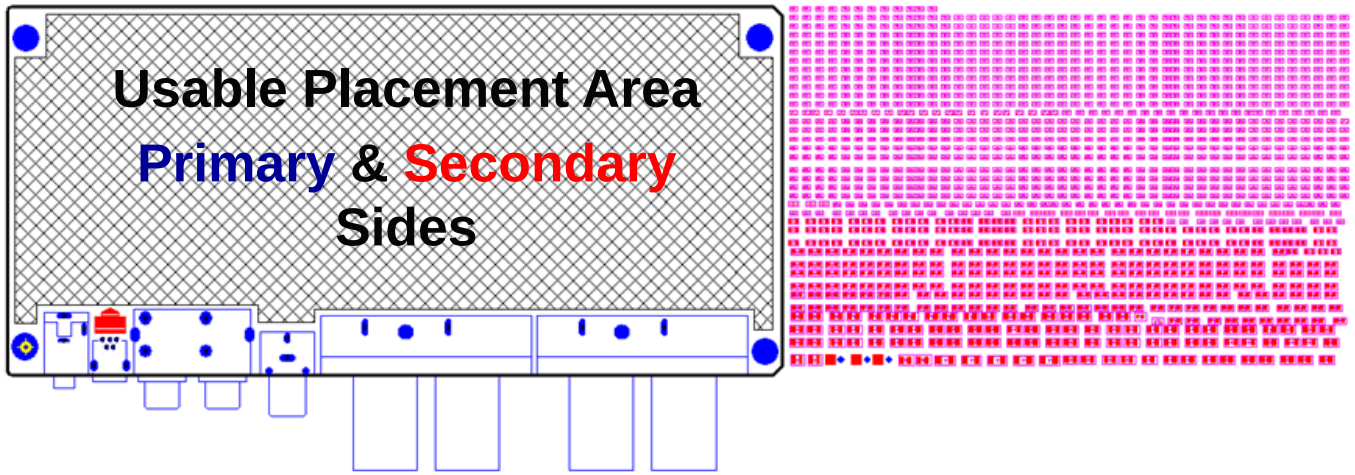
Increased Placement Density (VIP)

Placement Affects Routing



Primary Side: Active Devices Shown in Blue

Secondary Side: Passive Devices Shown in Red



Quick component dispersement shows some feasibility, thus ready for DFM/DFA analysis

Quickly observed, this placement is probably “Not Feasible”

If possible, reduce some parts

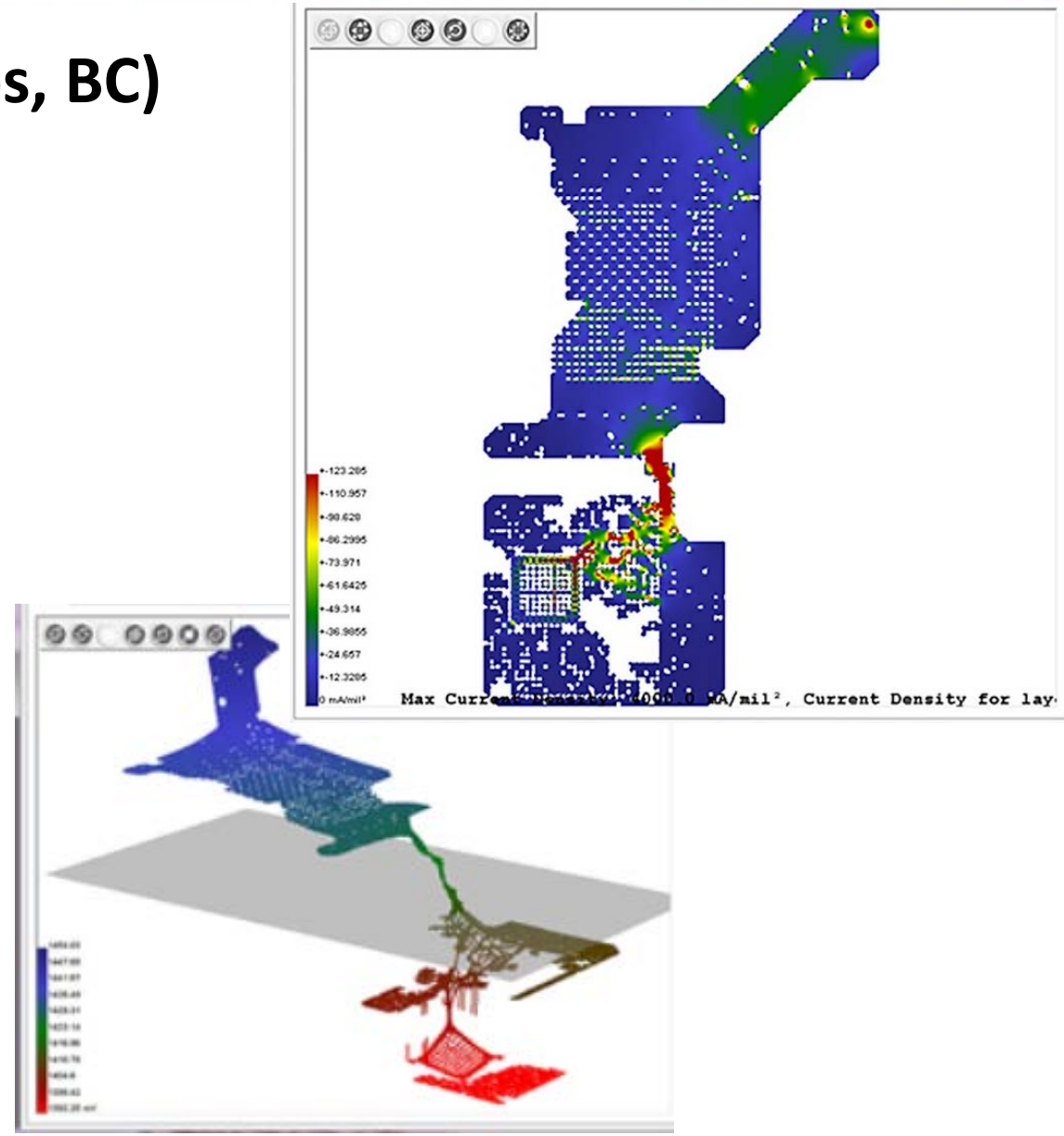
This may also suggest the need for VIP (Via-In-Pad)

- Increased routing density
- Lower EMI signature
- Cost adder
- Perform better because it would have reduced parasitics

Power Delivery Challenges (Smart Stack-ups, BC)

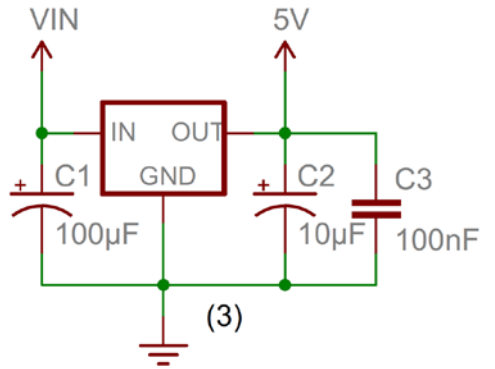
You shouldn’t have a talk about routing if you haven't considered your power delivery FIRST!

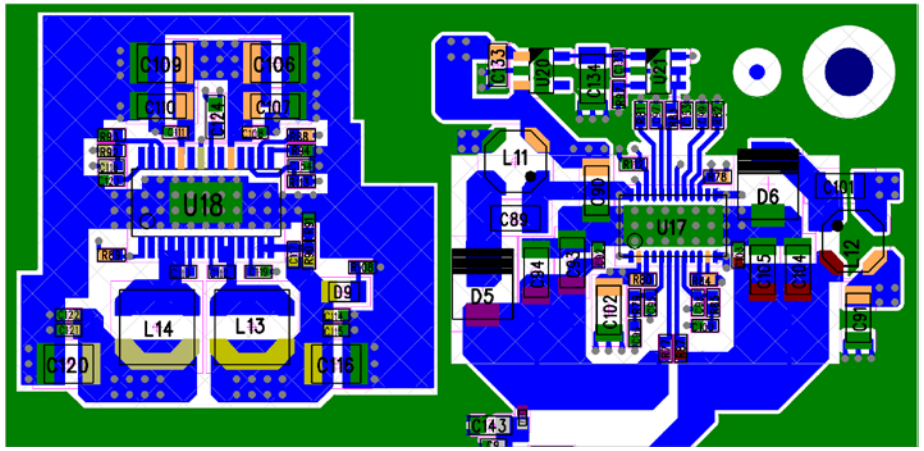
- Wikipedia - PI (Power Integrity) is an analysis to check whether the desired voltage and current are met from source to destination
- We starve the circuit with choke points: 2D & 3D
- Always associate voltage planes with ground planes in a multilayer stack-up for capacitive/inductive coupling

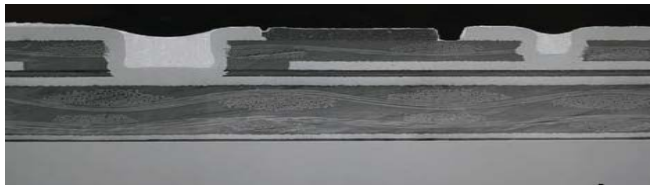


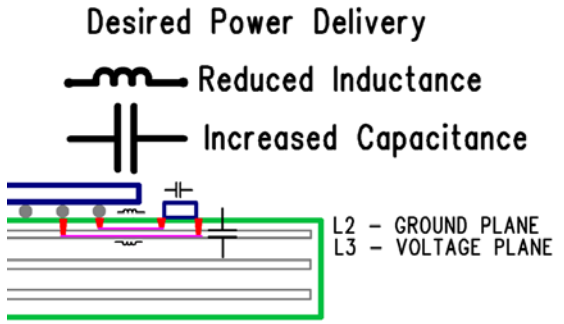
Power Delivery Challenges (Smart Stack-ups, BC)

- The distribution across the board should insure that there is no current loss or voltage drop
- Also, care should be given to not couple to/from other signals and voltages
- The end usage at each device, should insure that the desired power requirements are met with a filtered, high-capacitance and low inductance delivery
- Placing a voltage and ground layer pair higher up in the stack-up, closer to the active devices reduces via inductance and improves power delivery to ICs









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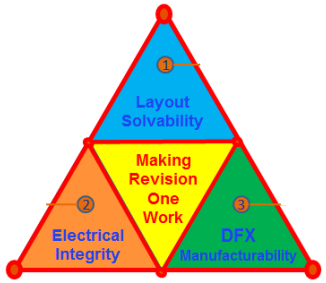
6. Differential Pair Routing

Who defines the Rules?

Signal Constraints Management: Cross-Probed and Tightly Integrated

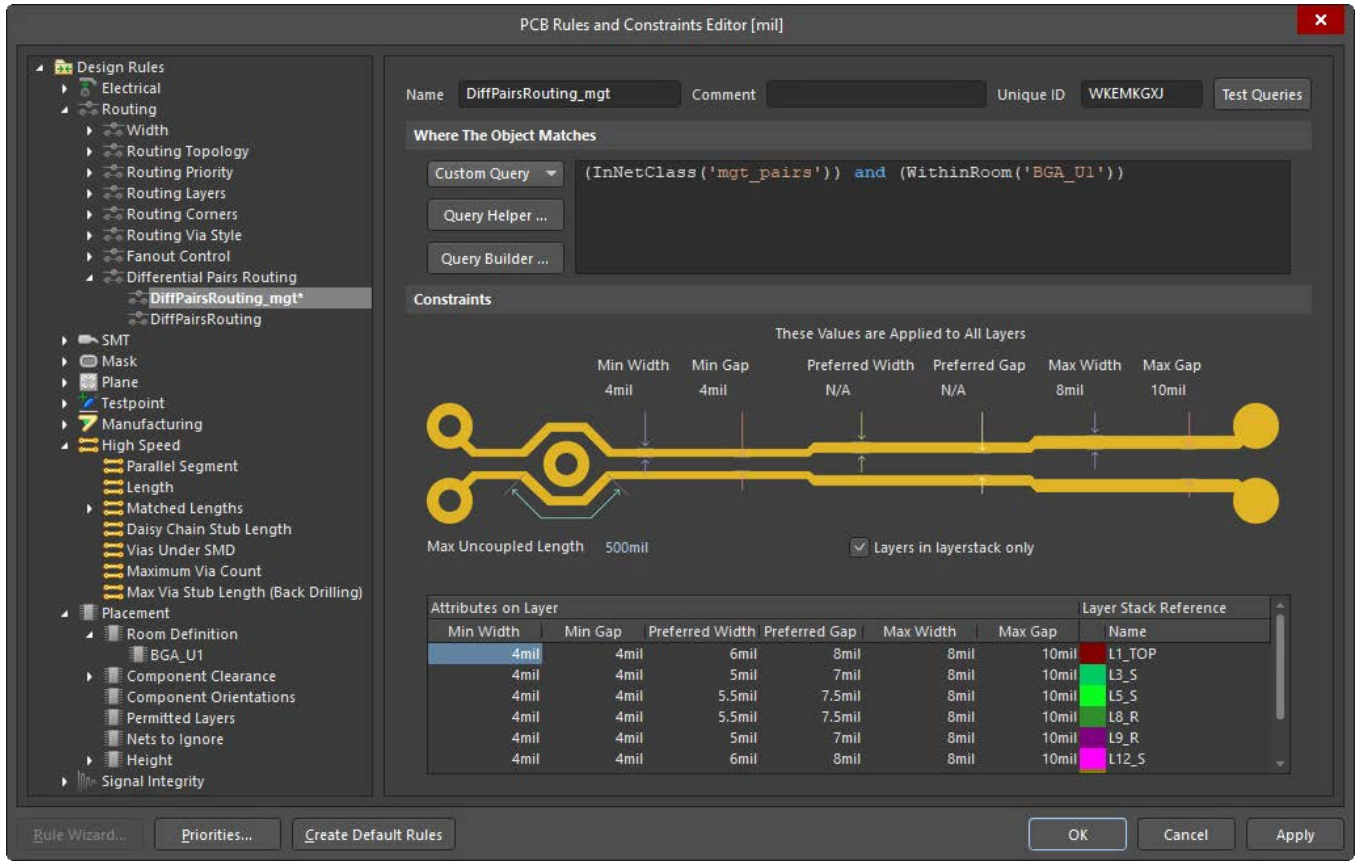


Define the rules from three perspectives:

- **Layout Solvability** for routing, pin-escape, via size, trace and space
- **Electrical performance** – matched delay, cross-talk, impedance, diff-pairs, busses, etc…
- **DFX** – compatible with your manufacturing capabilities

To Ensure Success, Properly Constrain the Routing

- Simplify the rule definitions
- Avoid over-constraining
- Use the rules for DRC and control
- Avoid ignoring rules - Strive for correct-by-construction
- Rules with automation - Can make routing easier and more accurate



Altium has a very robust rule set!

OK, shameless plug...

Avoid Over Constraining Rules

- **Conservative data sheets**
  - Skew budget (length tolerances) often made unnecessarily small Why? Desire to eliminate possibility of potential problems
- **Finding the right balance of compromise**
  - Often not possible to over-constrain everything without sacrificing one or more of these: cost, time, size, performance or reliability
- **Design Software**
  - If the software enables you to easily address the over constrained rules, why not use it?
  - Allows the margin (available skew) to be reserved for other effects

Over constraining a design may result in more layers and higher cost.

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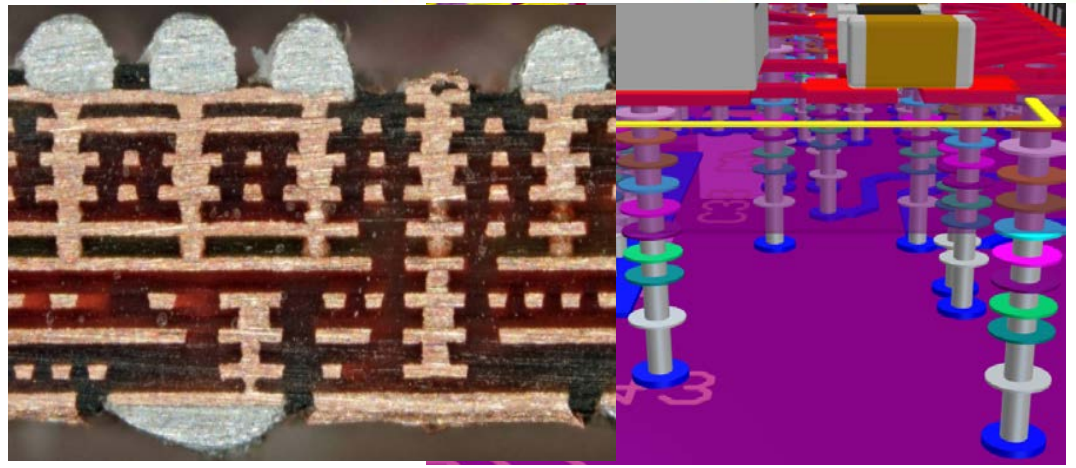
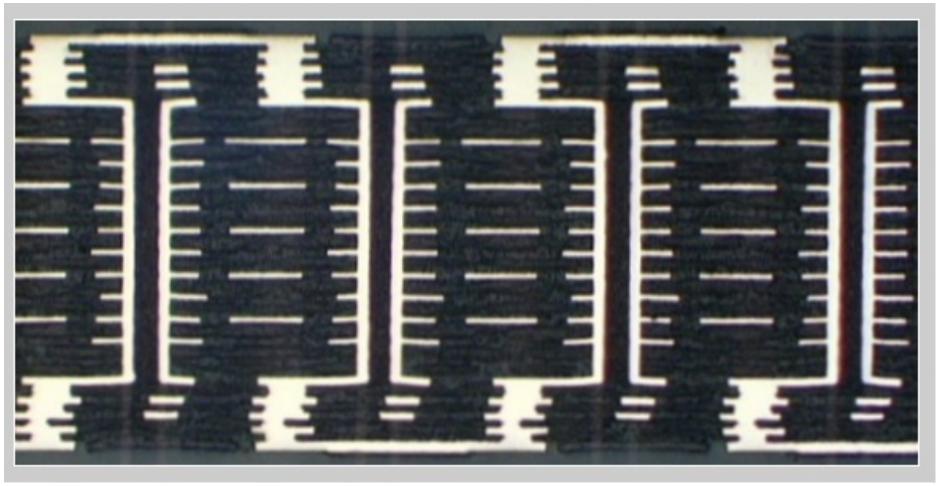
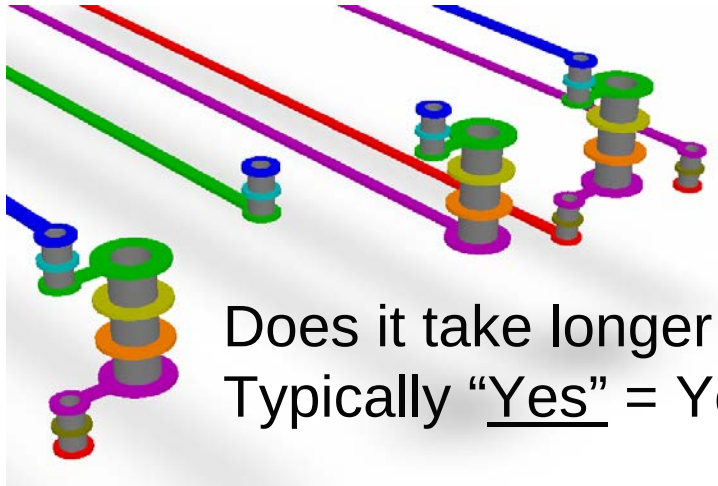
HDI and Via Fanouts – Fine Pitch BGAs

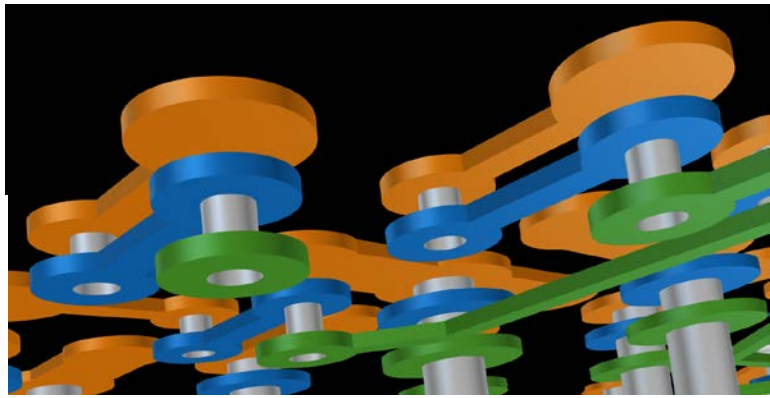
Increased Routing Density (HDI)

- Fine Pitch BGA – <.65mm, .5mm
- Sequential Lamination - multiple stacking options
- Thin Materials - down to 50um [0.002 inch] dielectric
- 3D Routing
- Improved Signal and Power Integrity









Does it take longer to complete an HDI design?
Typically "Yes" = You're routing 3D, Z-Axis

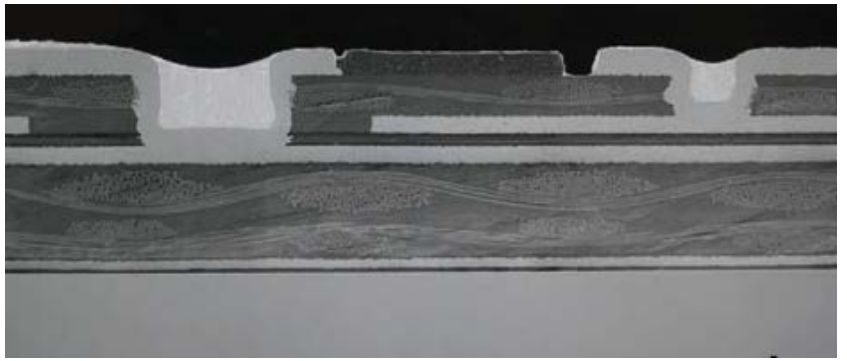
Increased Routing Density (HDI)

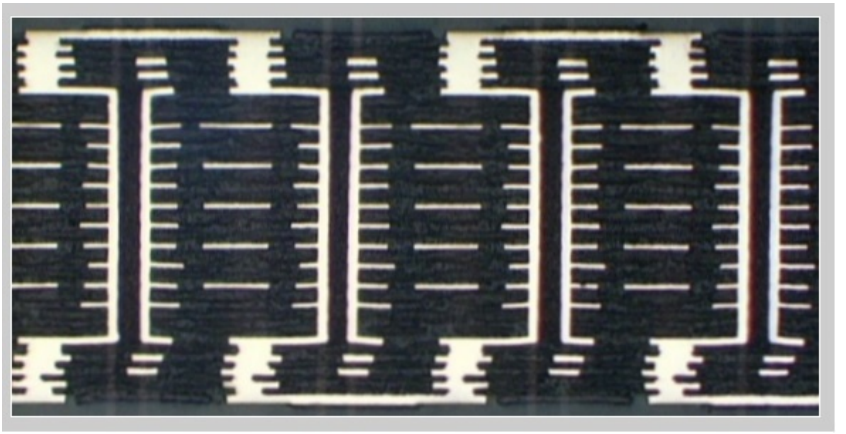
Microvias can be either a buried via or blind via

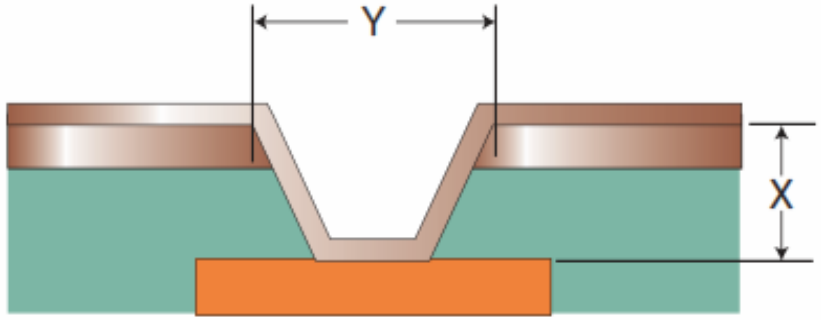
A microvia is defined as a blind structure (as plated) with a maximum aspect ratio of 1:1 terminating on or penetrating a target land, with a total length of no more than 0.25 mm [0.00984 in] measured from the structure's capture land foil to the target land

When utilizing a microvia structure, typically thinner dielectric materials will contribute to higher reliability

Stacking of microvias is ok, but never over a mechanical via due to CTE (Coefficient of Thermal Expansion) mismatch



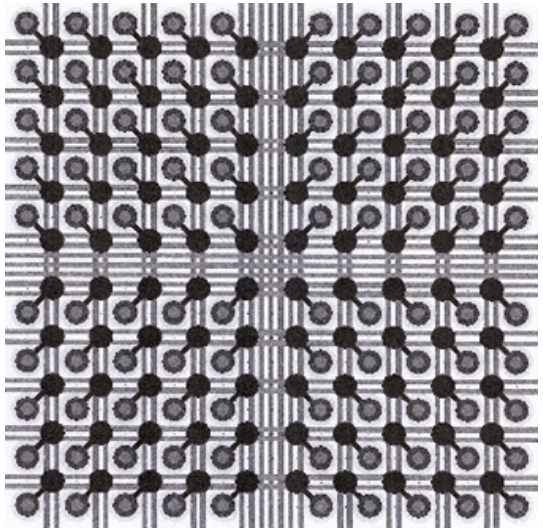


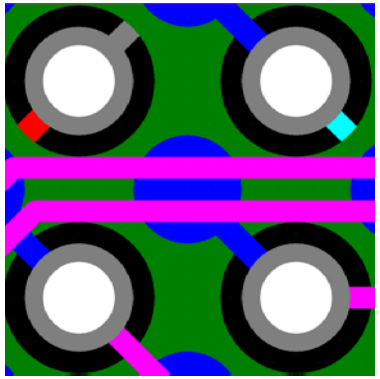


Note: X/Y = Microvia Aspect Ratio, with X=Y 1:1

Via Fanout

- **Copy & Paste**
  - Simplifies fanouts and makes them consistent
  - Use a grid! Factor of pin-pitch, reset origin to pin
- **Pin Swap**
  - Can make routing much more direct, fewer layers
- **Keyboard Shortcuts**
  - Learn the shortcuts, use them
  - Create a list of the ones you use the most





Via Data
Pad: 0.50 (20)
Hole: 0.25 (10)
Anti-Pad: 0.70 (28)
BGA Pad Size: 0.5 (20)

Trace/Space Data
Trace Width: 0.1 (4)
Trace/Trace Space: 0.1
Trace/Via Space: 0.1
Routing Grid: 0.1 (4)
Via Grid: 1 (40)
Part Place Grid: 0.5 (20)

Automated interactive routing tools increase productivity with user control and quality

Via Fanout

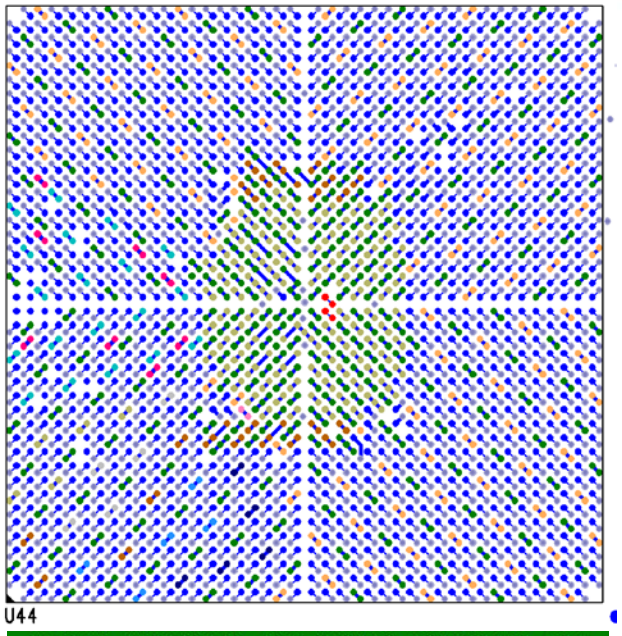
Number of I/O signals on a BGA can determine the layer count

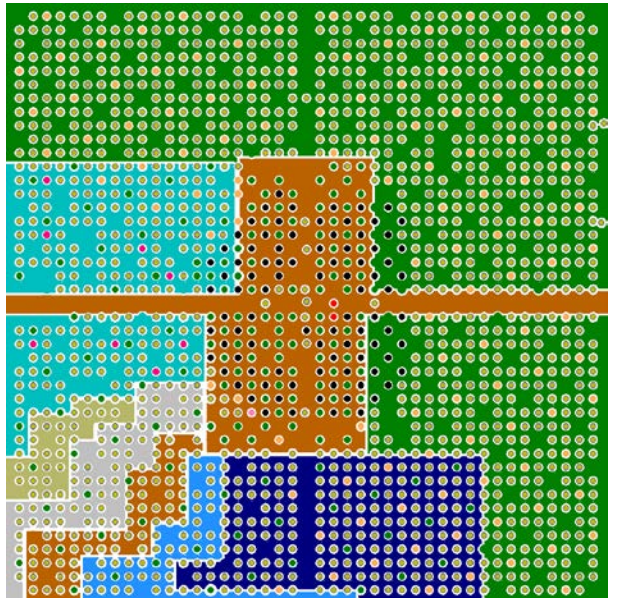
Copy & Paste:

- Simplifies fan outs and makes them consistent
- Use a grid! Factor of pin-pitch, reset origin to pin

Fanout done in a quadrant manner to allow two things:

- Wagon wheel route-away from BGA center - To minimize cross over and layer usage, as shown on top image
- Wagon wheel route-away from BGA center - Allows power rails more robust entry to core power, as shown on bottom image





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Signal Integrity with Faster Switching Circuitry (EM Theory Comprehension)

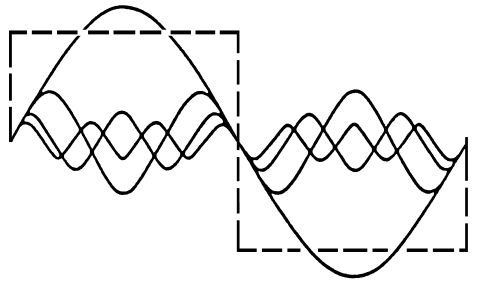
Frequencies and wavelengths are useful for calculations for dielectric constants and loss tangents. It is a measured cycle known as a frequency. This forms switching binary language

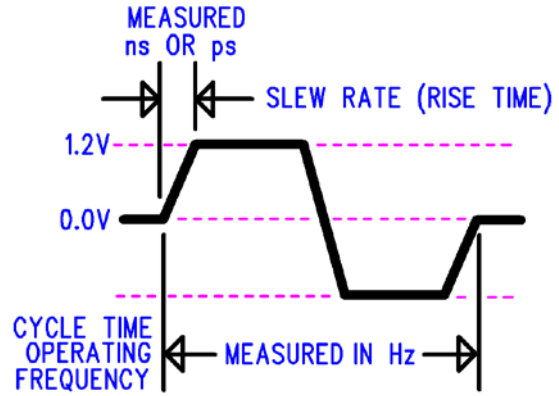
Rise and fall transitions contain many frequencies and their harmonics, within an operating frequency, as shown on the top image. Think of them as squared off

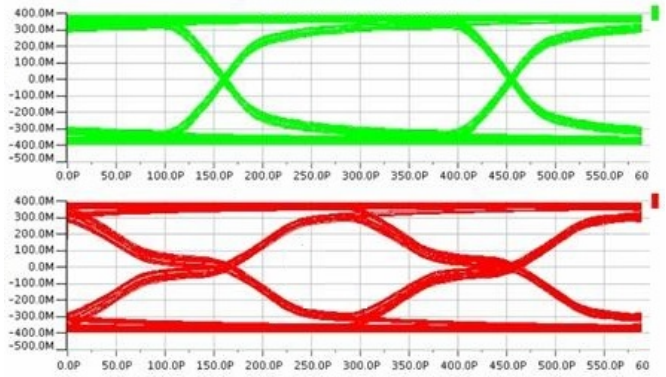
However, the important feature of digital pulses is the slew rate **(rise and fall time),** as measured in ns (nano) or ps (pico) seconds as shown on the middle image

Repeated cycles are measured as an eye-diagram. They should cross in a consistent point or you have a condition known as skew. Red eye diagram shows 155ps of inter-pair skew

Properties of a Sine-Wave

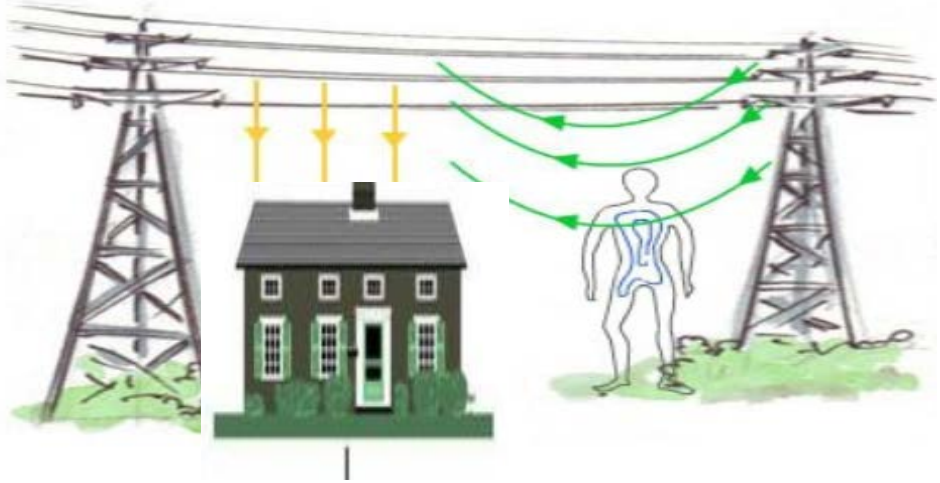






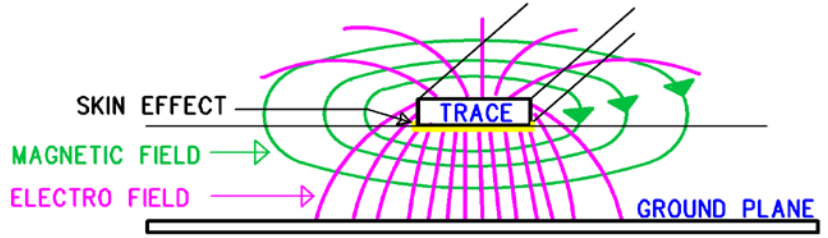
Signal Integrity with Faster Switching Circuitry (EM Theory Comprehension)

In a circuit board, a high capacitance and low inductance environment is ideally created when a forward current is completely surrounded by its return current, totally containing both the electric and magnetic fields, as a coax cable might be



An ideal setting would have a consistent balanced impedance between the forward path and the return path

*Why this is important – you're not just connecting a route, rather you are managing an EM field

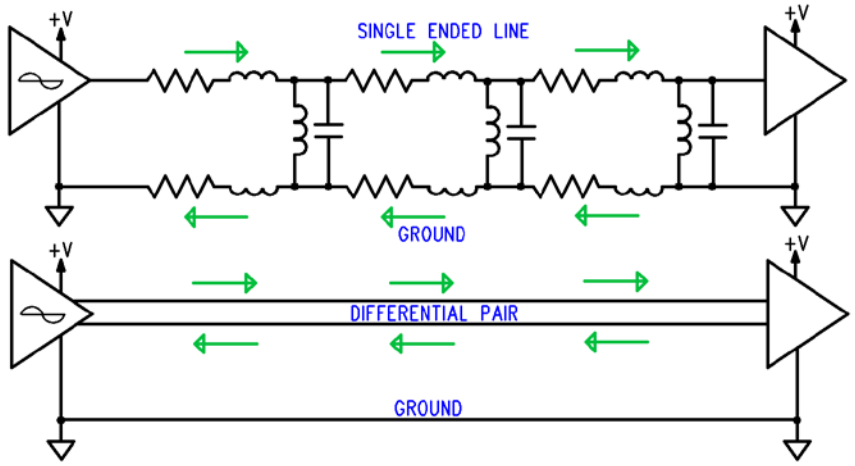


Energy fields exists between the trace and the plane (return path) within the dielectric material

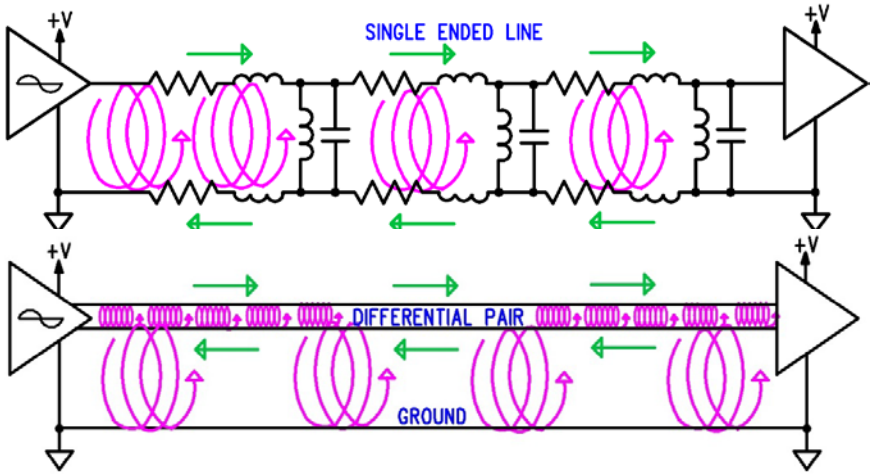
Signal Integrity with Faster Switching Circuitry (EM Theory Comprehension)

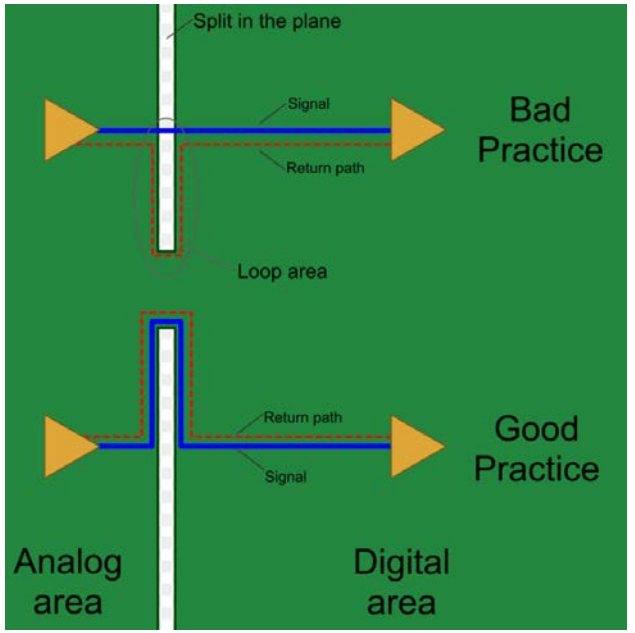
However, it is not really forward and back, rather, the energy field is immediate between the trace and the plane within the dielectric material

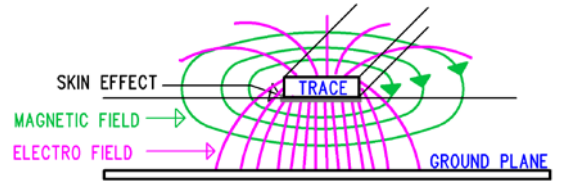
It's not forward and back

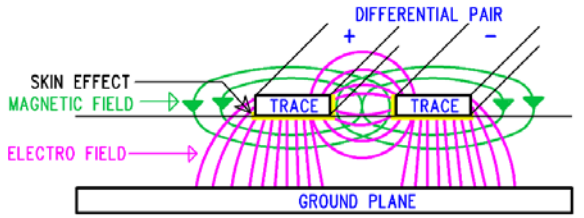


It's in the dielectric material









Stack-Ups that Support Functional EMC

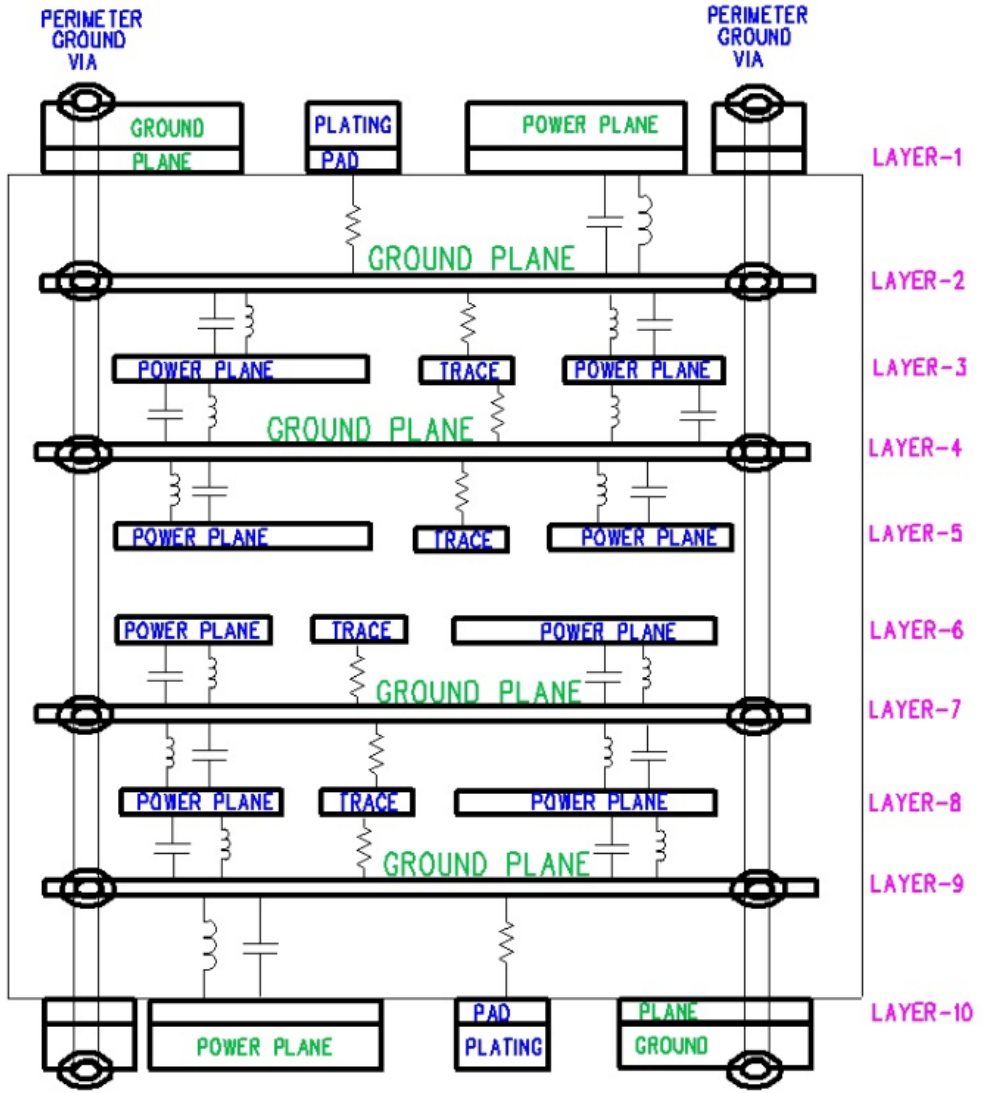
GND (0.0V) is the most important signal in the circuit!

Ground is where you plant tomatoes, but we commonly refer to this signal as GND (0.0V)

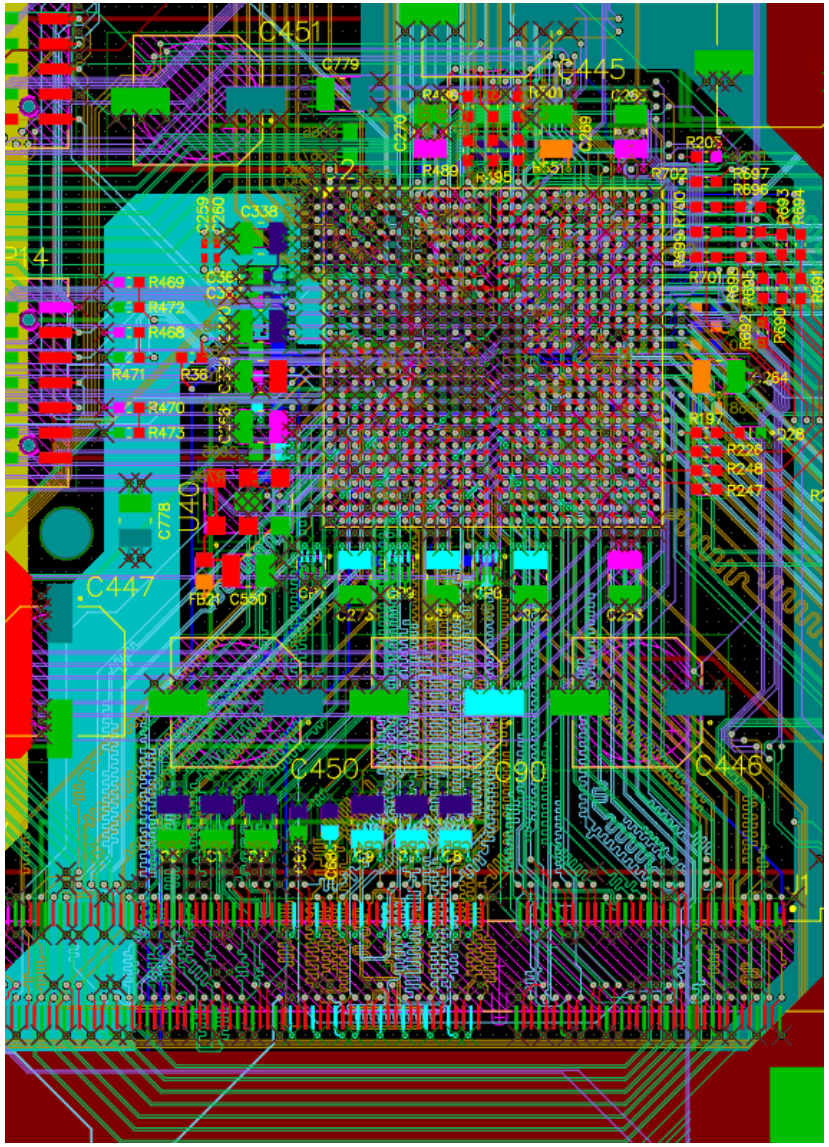
- GND (0.0V) is what is used to reference every signal for a return path. **Never route signals over split GND plane!**
- GND (0.0V) is what is used to reference every PWR net (Voltage rail). **Never place PWR's over split GND plane!**

Get these last two bullets right and you have solved a significant amount of your Signal/PWR Integrity concerns!

10 Layer Stack-up



Perfect 12 layer stackup and route



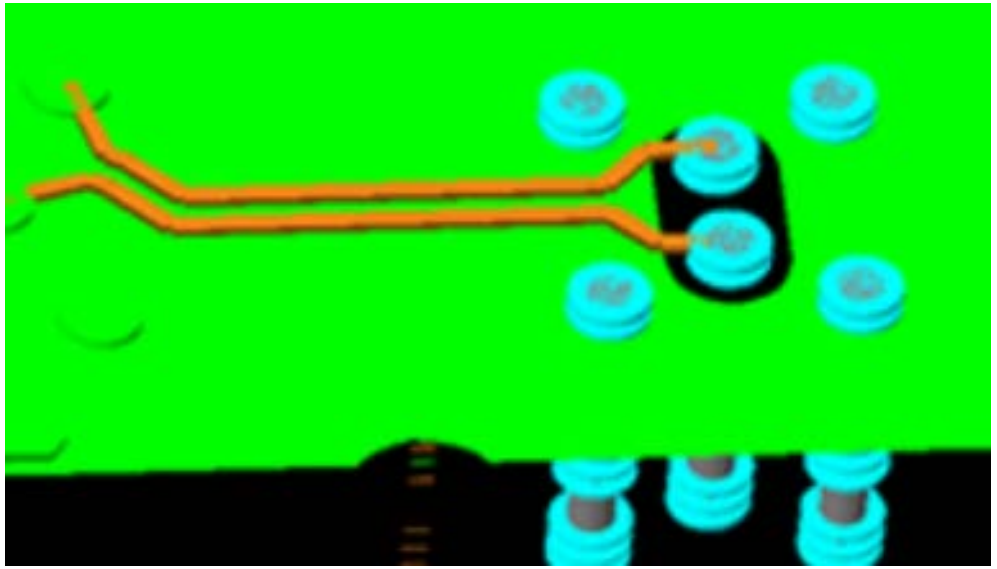
Save... | Load... | Presets | Measurement Unit: Metric | Build

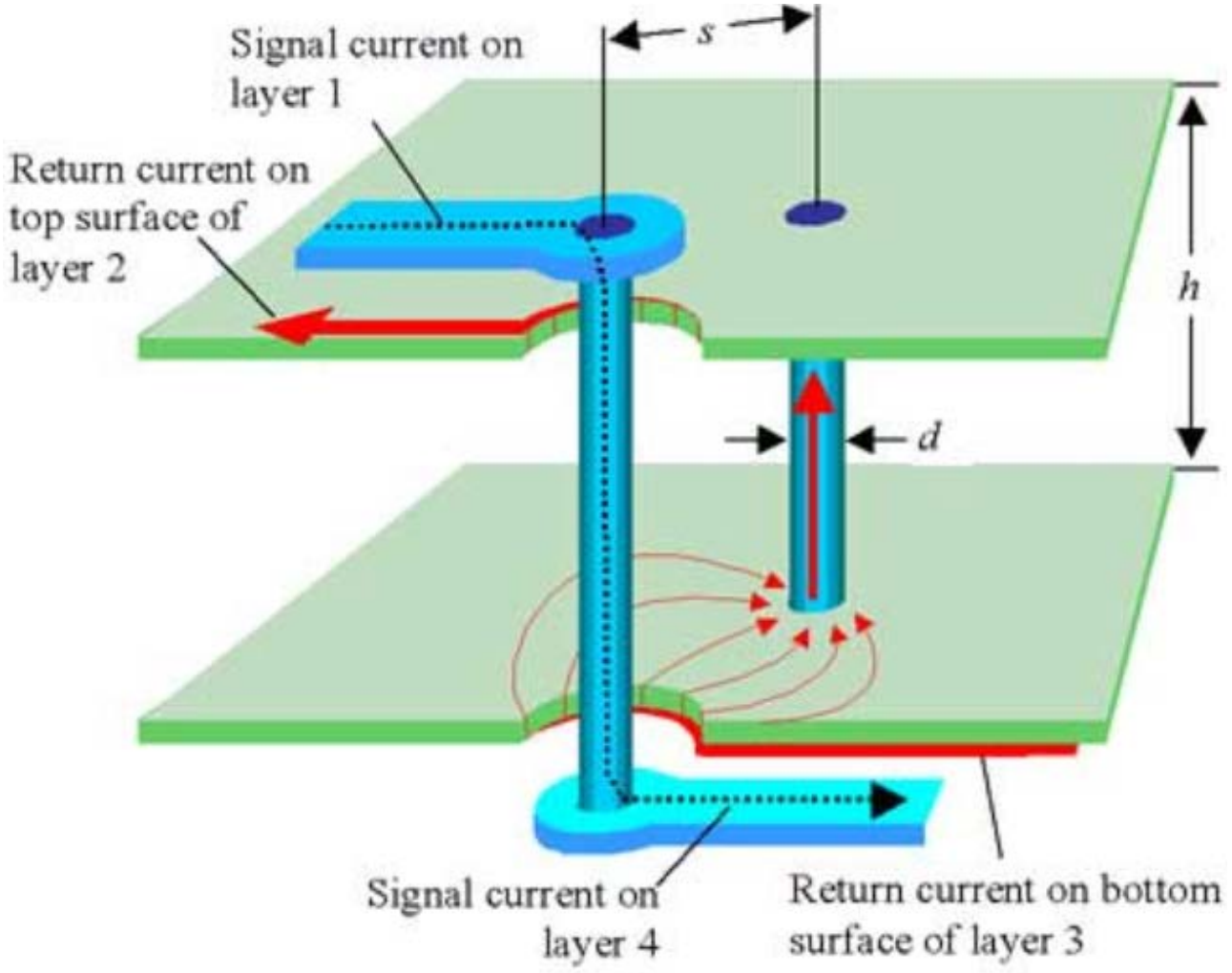
		Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion
	☑	Top Overlay	Overlay							
	☑	Top Solder	Solder Mask/...	Surface Mat...	0.0125	Solder Resist	3.5			0
1	☑	L1-Top	Signal	Copper	0.04826				Top	
	☑	Dielectric1	Dielectric	Prepreg	0.07569	FR-4	3.44			
2	☑	L2-GND	Internal Plane	Copper	0.01524			0.5		
	☑	Dielectric6	Dielectric	Core	0.08458	FR-4	3.75			
3	☑	L3-Signal	Signal	Copper	0.01524				Not Allowed	
	☑	Dielectric5	Dielectric	Prepreg	0.18821	FR-4	3.58			
4	☑	L4-PWR	Internal Plane	Copper	0.01524			1		
	☑	Dielectric10	Dielectric	Core	0.08458	FR-4	3.75			
5	☑	L5-Signal	Signal	Copper	0.01524				Not Allowed	
	☑	Dielectric4	Dielectric	Prepreg	0.18821	FR-4	3.58			
6	☑	L6-GND	Internal Plane	Copper	0.01524			0.5		
	☑	Dielectric8	Dielectric	Core	0.10109	FR-4	3.49			
7	☑	L7-PWR	Internal Plane	Copper	0.01524			1		
	☑	Dielectric11	Dielectric	Prepreg	0.18821	FR-4	3.58			
8	☑	L8-Signal	Signal	Copper	0.01524				Not Allowed	
	☑	Dielectric3	Dielectric	Core	0.08458	FR-4	3.75			
9	☑	L9-GND	Internal Plane	Copper	0.01524			0.5		
	☑	Dielectric9	Dielectric	Prepreg	0.18821	FR-4	3.58			
10	☑	L10-Signal	Signal	Copper	0.01524				Not Allowed	
	☑	Dielectric2	Dielectric	Core	0.08458	FR-4	3.75			
11	☑	L11-GND	Internal Plane	Copper	0.01524			0.5		
	☑	Dielectric7	Dielectric	Prepreg	0.07569	FR-4	3.44			
12	☑	L12-Bottom	Signal	Copper	0.04826				Bottom	
	☑	Bottom Solder	Solder Mask/...	Surface Mat...	0.0125	Solder Resist	3.5			0
	☑	Bottom Over...	Overlay							

Stack-Ups that Support Functional EMC

Return Path Vias for:

- Single-ended signals – shown on right
- Differential Pairs – shown below

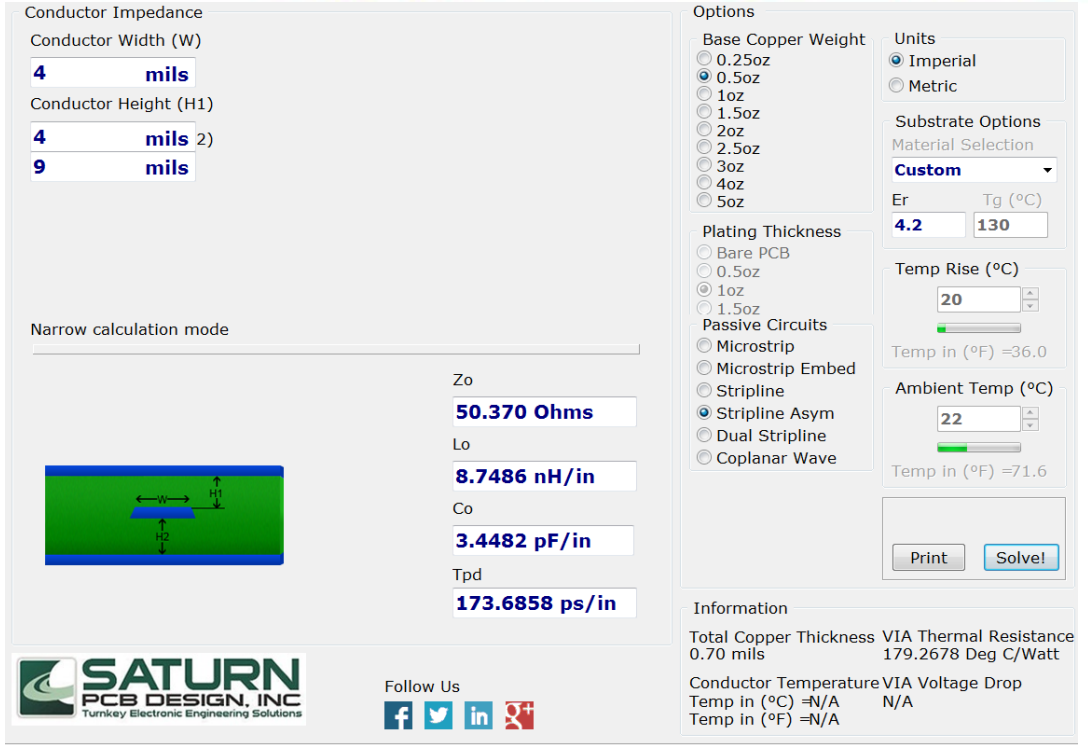


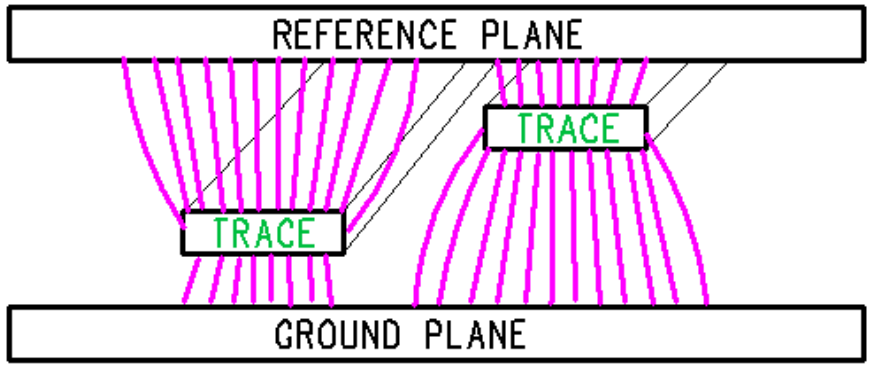


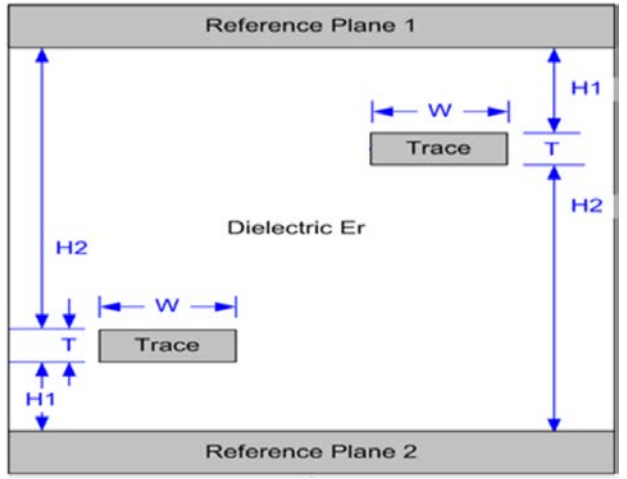
Avoid this stack-up condition
Dual Asymmetrical Stackup

- You conceptualized and setup your stackup
- You secured a stackup from the fabricator
- You make your fabrication drawing reflect this
- You require the fabricator to utilize an impedance coupon based on this stackup
- You require the fabricator to TDR test the coupon
- You setup your rules and simulations to consider these as 2 - 50 ohm SE impedance lines

BUT…

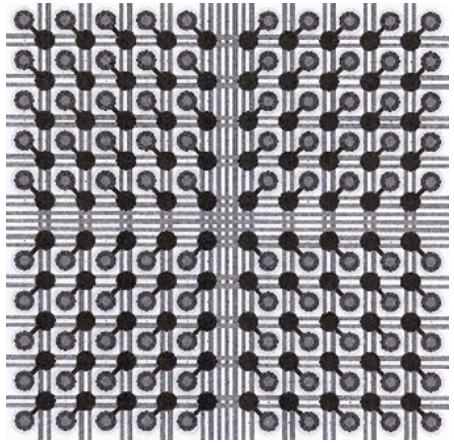


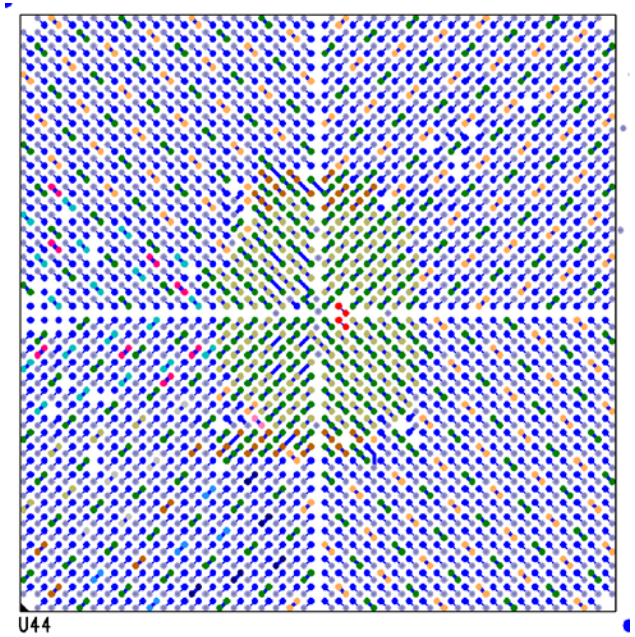




Avoid this stack-up condition
Dual Asymmetrical Stackup

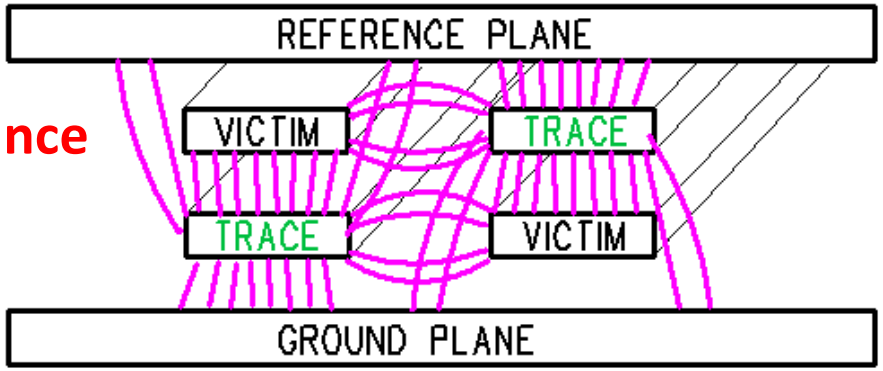
- **BUT…**
- Because the board routing was so dense.
- Because alternating layer perpendicular routing strategy went out with through hole technology
- Because most of the IC's on a dense board are BGA's
- Because BGA's want to route "wagon-wheel" style away from the center of the chip.
- Because the routing channels where available
- Because you did not want to add extra layers
- So you routed like this

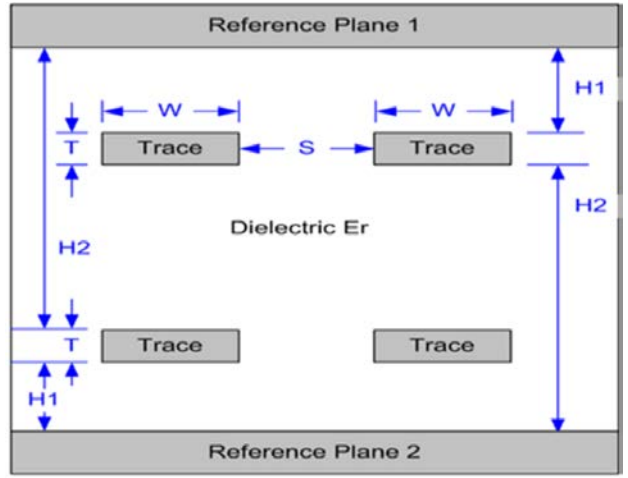




You have changed the actual impedance and made a crosstalk nightmare.

But hey, the coupon is good!





Electrical Performance of Advanced Routing

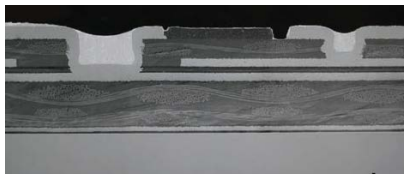
Signal Layer Usage:

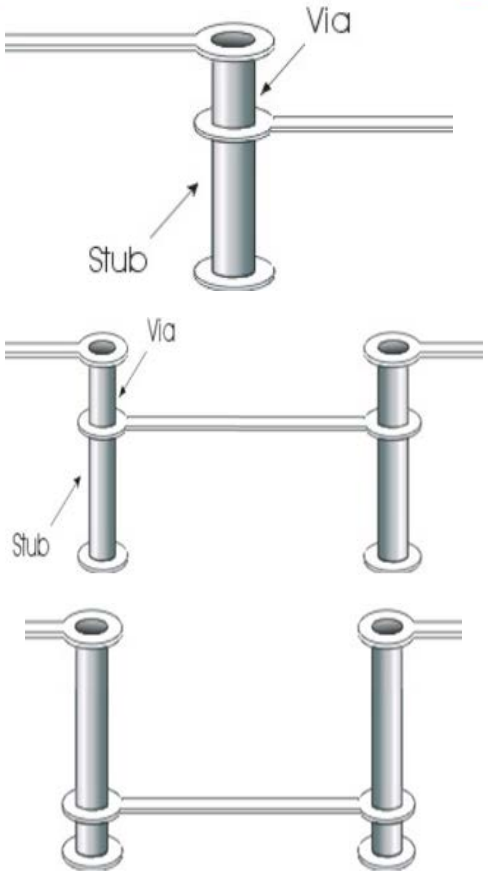
Fabrication allowances should be made for plating, if routed on outer layers

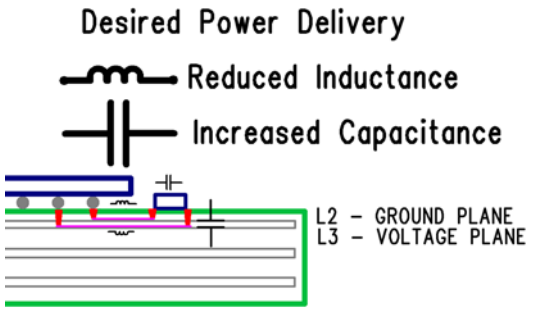
Digital signals when routed stripline (inside of GND planes) will better contain emissions (Route under-GND)

RF circuits often seek to have low noise to their traces and they also seek to reduce parasitics on every feature. As a result, they will often seek to be routed on outer layers with a wide trace (non-lossy) and a matching dielectric to GND. If routed on the surface, no vias would be required as they are considered a parasitic stub

Digital signals perform best when they use the maximum depth of every via, leaving a short stub. Therefore, maximize lower layers first when routing. This will allow for Power Distribution layer-pairs positioned higher in the stack-up and closer to the device of use (Reduced Inductance)

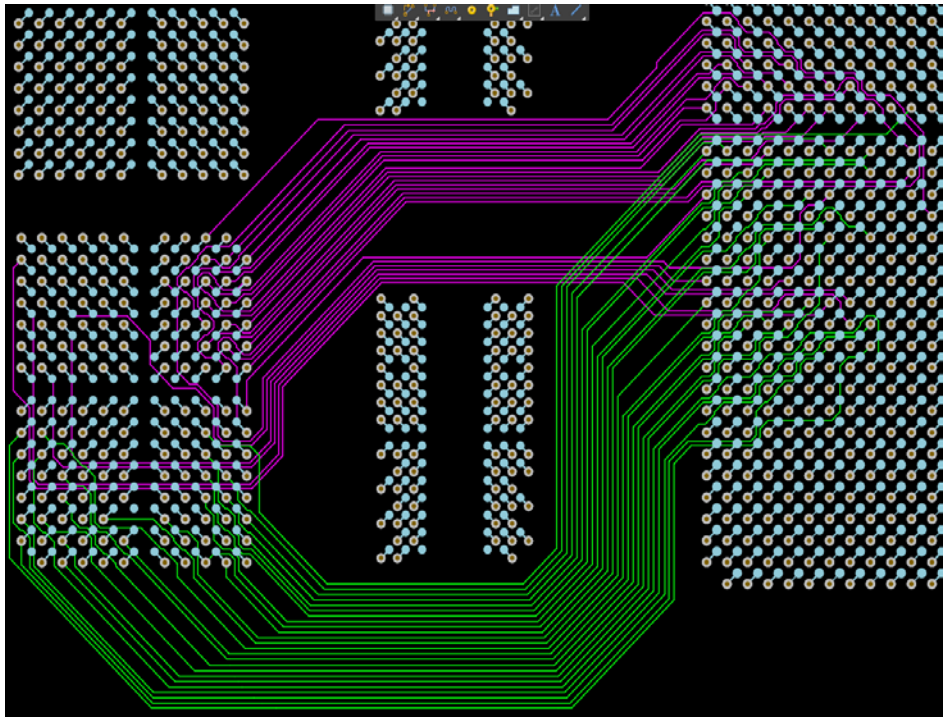






Improved Routing Software Enables Productivity

- **Take advantage of automation**
  - Auto-interactive
  - Does it allow designer control?
  - Does it produce manual quality?
- **After careful via fanout**
  - Quickly solve large amounts of rules-controlled busses
- **Gloss & Retrace**
  - Better diff. pair quality and implemented faster
  - Pad entry, change width gap, etc…



Interactive routing tools continue to increase levels of automation

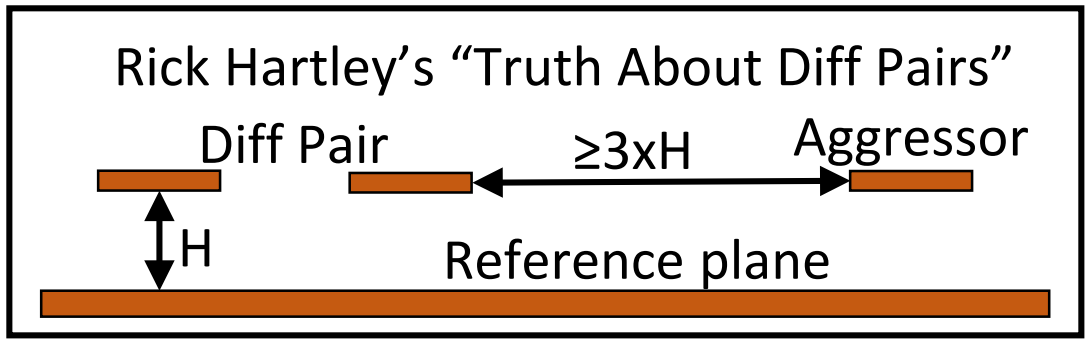
Agenda

1. Layout Designers Perspectives
2. Routing Challenges of Today and Tomorrow
3. HDI and Breakouts – Fine Pitch BGAs
4. Electrical Performance of Advanced Routing
5. Rules
6. **Differential Pair Routing**

Differential Pair Routing

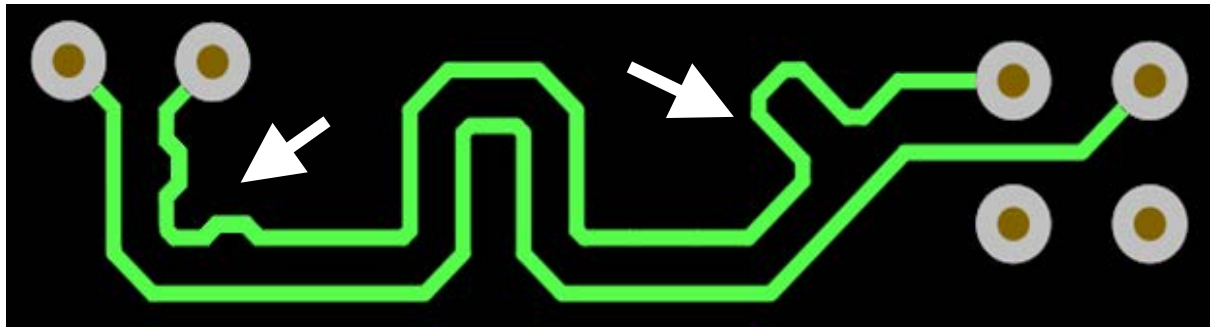
Diff Pair Concerns	Data Rates	Solution	Comments
Intra Pair Differential Skew	All	Pair Length Matching	Within skew budget
Bus/Clock Timing Margin	All	Group Length Matching	Within bus timing margin
Crosstalk - Agressor to Diff Pair	All	Space Aggressors Rule	≥ 3X space to reference plane

- LVDS (Low Voltage Diff Signals) operate at low power and can run at very high speeds
- Maintain - matched length and differential impedance



To prevent crosstalk on diff pair

- In length matching, include vias used and pin-package lengths, avoid common mode rejection
- In differential impedance maintain coupling to avoid skew, avoid events on one trace of the pair



Corner and pad entry skew adjustments

Differential Pair Routing

Quality is About Routing Efficiently and Accurately Meeting Requirements

Layout Solvability –

- Reduce meandering route segments and extra vias
  Makes it easier to edit later

Electrical performance -

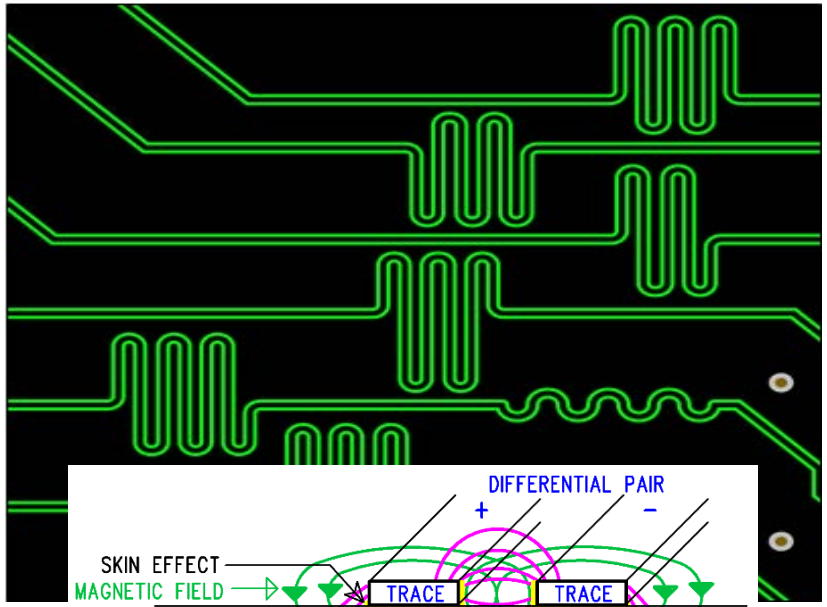
- Symmetry looks nice, but avoid enabling crosstalk

Manufacturability -

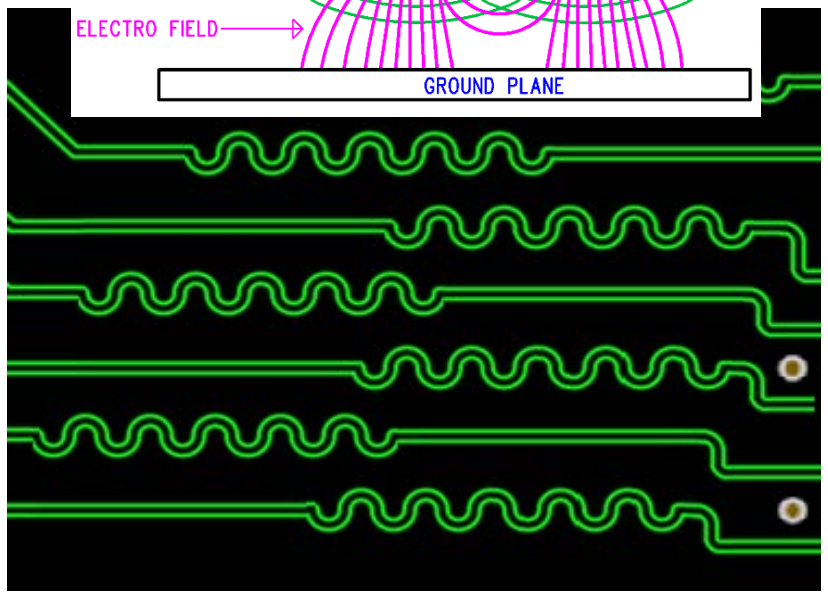
- Fabricators say, "Space is King" increase clearances

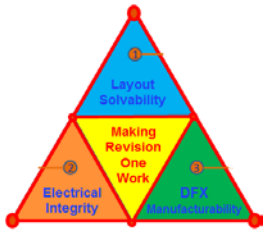
Use automation that improves **solvability, performance and manufacturability,** making revision-1 work is our goal!

Bad →
It's coupled to itself



Good→
It's horiz. biased

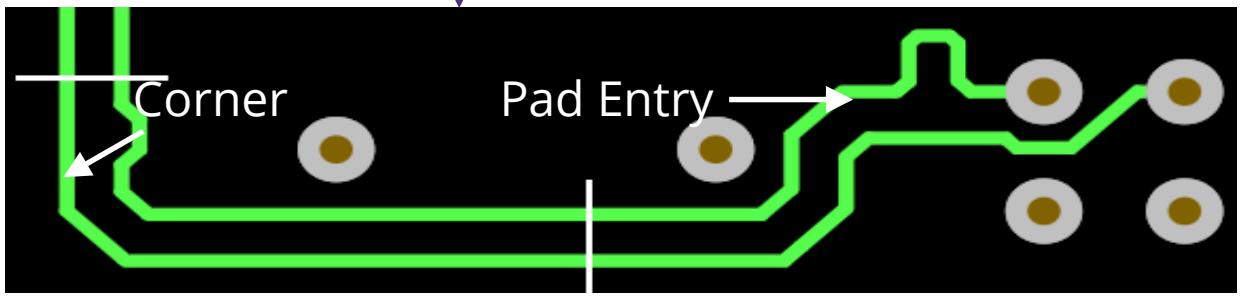




Differential Pair Routing

Diff Pair Concerns	Data Rates	Solution	Comments
Coupling to Reference Plane	≥ 5Gb/s	Use Microstrip, Stitch Vias	Minimize space to ref plane
Phase Matching Compliments	≥ 10Gb/s	Match with Phase Bumps	Tolerance over distance
Skew Mismatch in Materials	≥ 10Gb/s	Fiberweave Routing	Angle offset

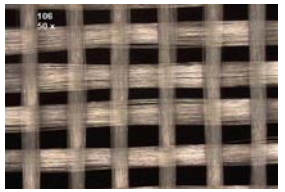
Keep GND return vias equidistant to DP vias



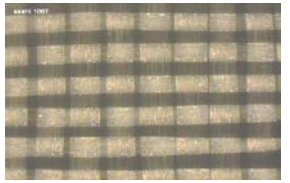
Phase match start at driver, bump at mismatch

Fiber Weave routing vs. Spread Weave

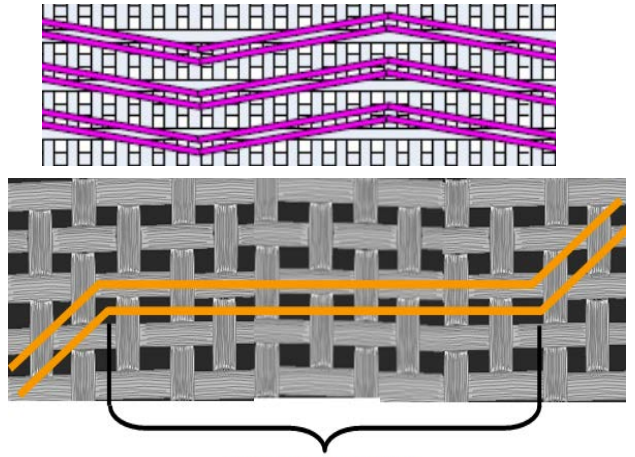
- Loose FR4 weave makes one trace for over glass and the other trace over the resin, results in a mismatched impedance
- Search: “Jeff Loyer fiber weave effect” Best paper on this topic



106 Loose



1067 Spread



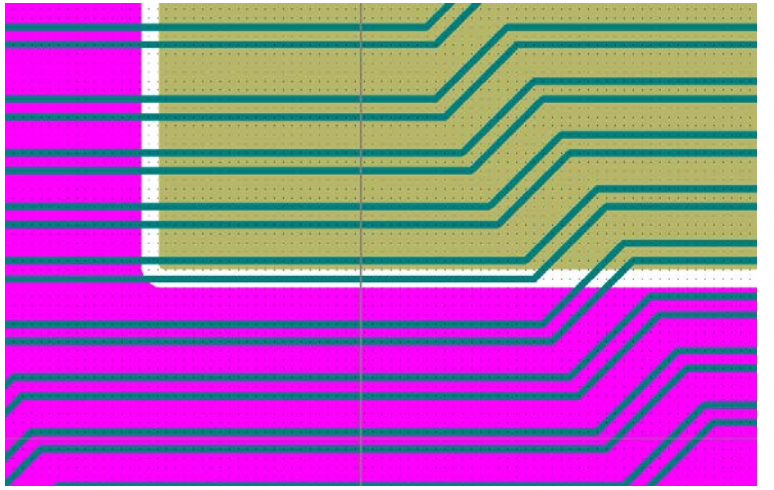
Differential Pair Routing

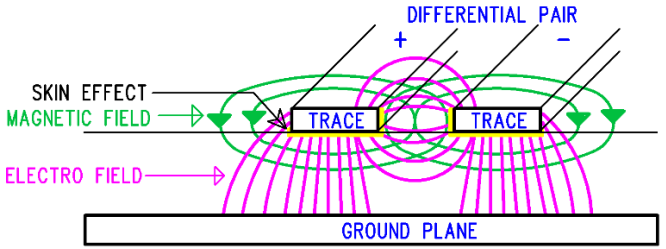
Quality is About Routing Efficiently and Accurately Meeting Requirements

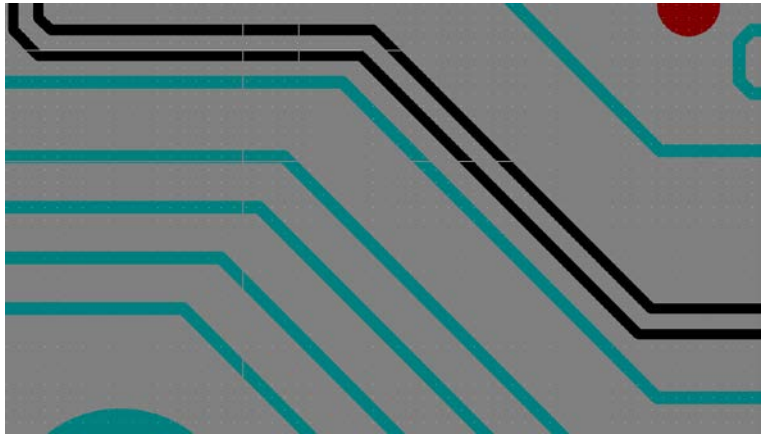
On the top image, one signal of the differential pair is riding along the gap of the adjacent split plane and may have an effect on the impedance, resulting in energy loss. The theoretical constructs were correct but instance was incorrectly routed

On the bottom image, the differential pair is routing per constraint but a third signal has been routed too close and may couple and have an effect on the differential impedance

Use your rules to detect these violations

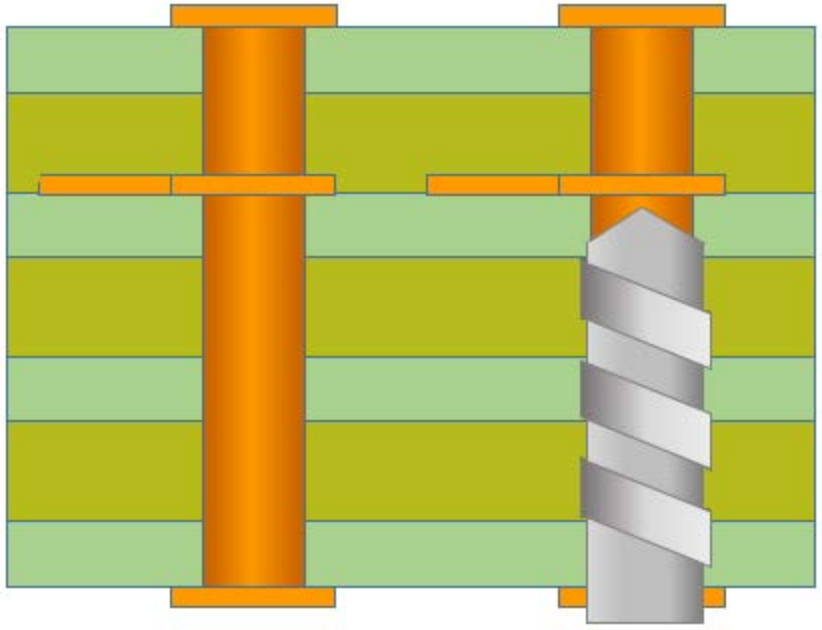




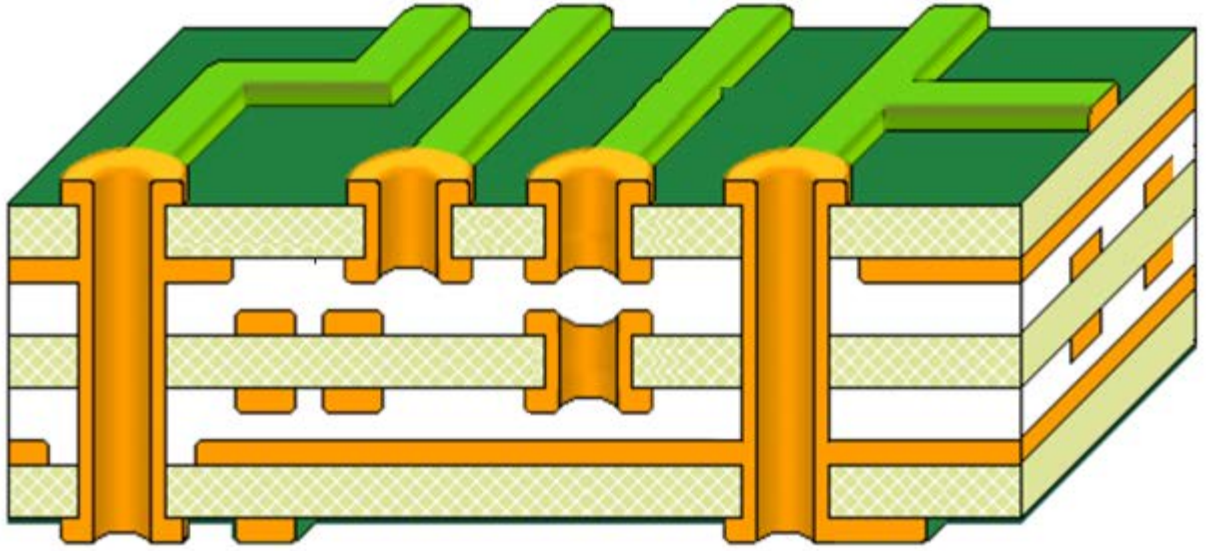


Differential Pair Routing

Diff Pair Concerns		Data Rates	Solution	Comments
Via Effects				
	Stub Discontinuities	≥ 5Gb/s	Backdrill, uVias	Delete non-functional pads
	Losing return path	≥ 5Gb/s	Balanced Stitch Vias	Equal distance to pair vias
	Phase Matching	≥ 10Gb/s	Phase Matched at Via	



Remove stubs with backdrilling



Eliminate stubs with µVias

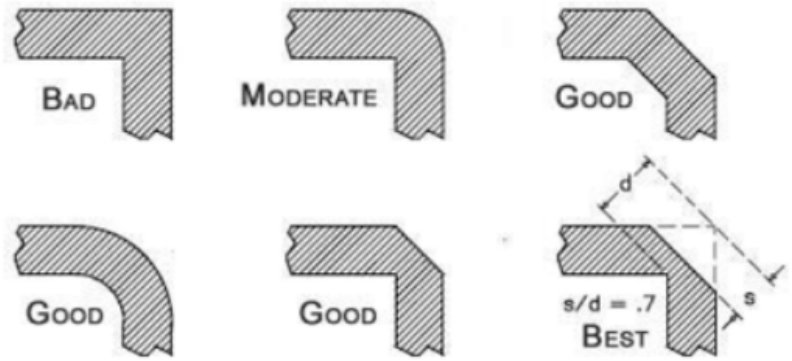
Differential Pair Routing

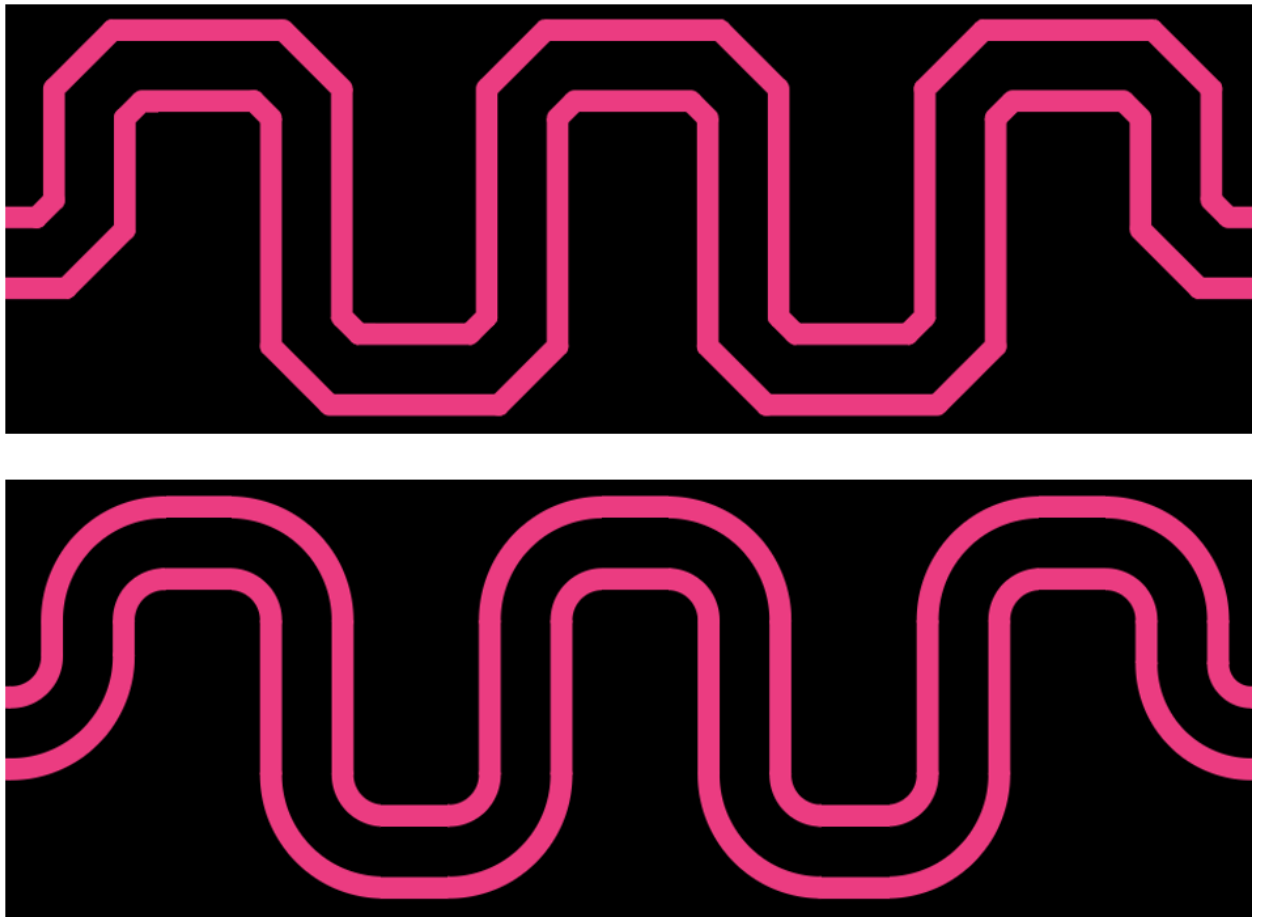
Using Arcs

When does it matter?

- “When the data rate is >16Gb/s everything matters”

- With RF - The chamfering of 90 degree routing corners is a technique used to reduce reflections caused by the corner in a microwave frequency route.



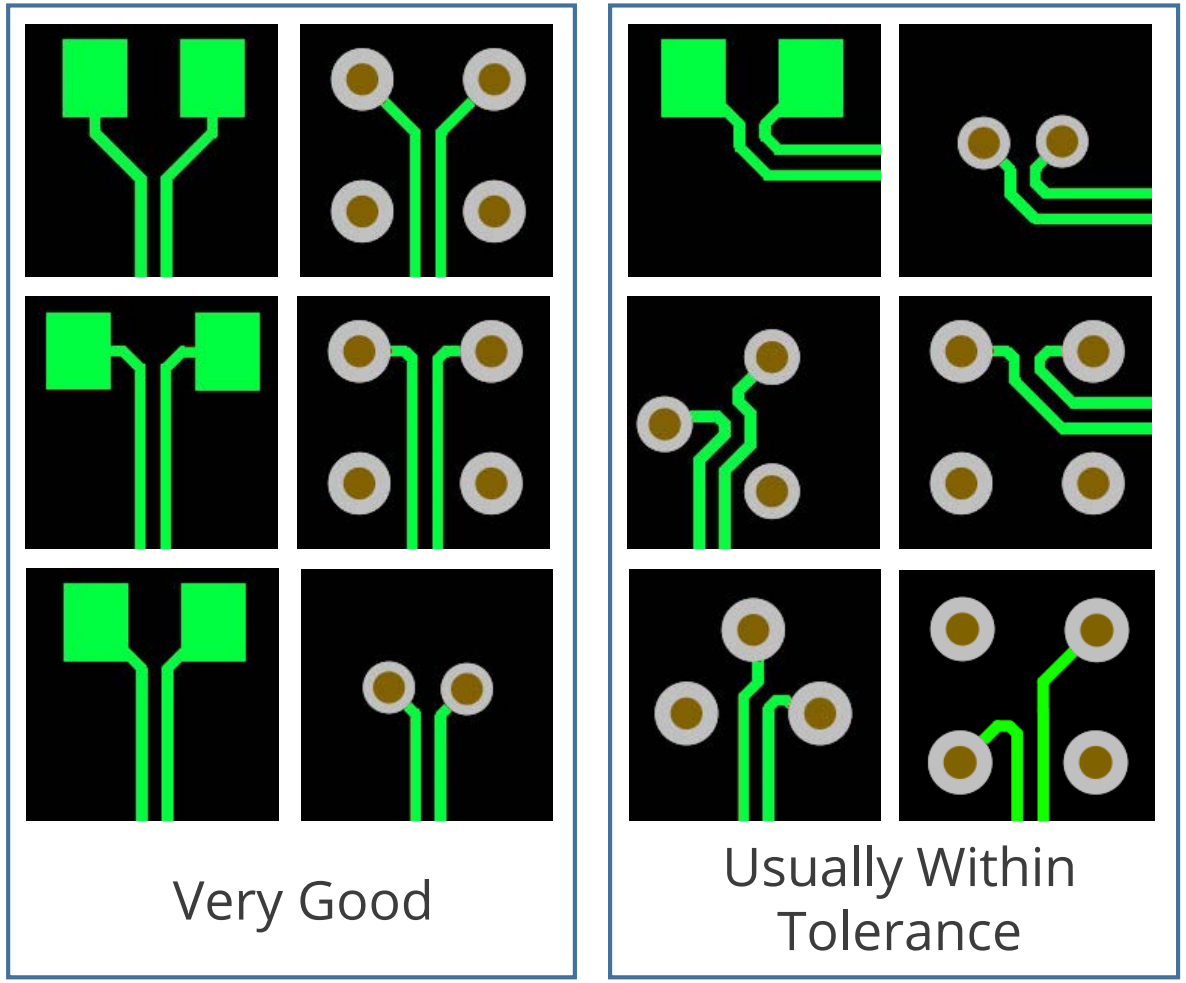


Arcs are beautiful, but usually not necessary

Differential Pair Routing

Pad Entry

- **Converge ASAP with equal length**
  - This will help to eliminate skew at the start and end of the routing
- **Pad entry gloss may work well**
- **Fabrication concerns**
  - Teardrops, etch traps, soldermask
  - Balanced pad entry

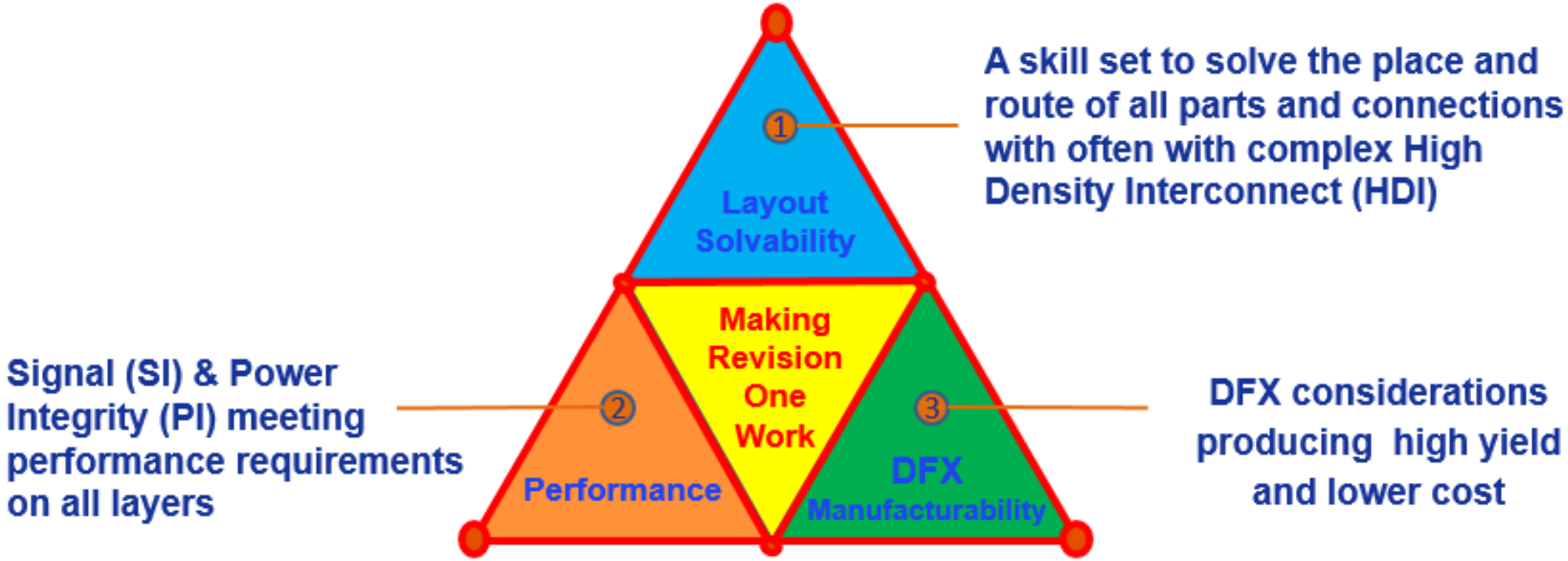


Pad entry is a good example in which automation can make routing a lot easier

Conclusions

<u>As David starts getting ready to show some of the new routing features in Release 19</u>

- Software enhancements and effective automation should increase productivity, accuracy and quality
- You should always seek to improve your knowledge base and competence with technology trends and seek to be a Master of your software tool!



mike.creeden@sdpcb.com

Thank you for your Attention!

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Questions?

Stay tuned for
Software demonstration of
Advanced Routing Methods
By: David Marrakchi