Altium

ALTIUMLIVE
Success Using HDI

Mike Creeden, MIT CID+
VP - San Diego PCB Design, LLC

Andrew Mitchell
Sr. Field Applications Engineer

Munich
Jan 15-17

BIO: Mike Creeden, MIT CID+

- VP/Founder of *San Diego PCB, Design, LLC*
  - 3 PCB Layout Design Centers, 20 Fulltime Designers
  - 4 Major CAD Platforms: Customers in all Industry Sectors
- Eptac: IPC-CID/CID+ MIT (Master IPC Trainer)
- Primary Contributor of the IPC-CID+ Curriculum
- IPC Designers Counsel – Executive Board Member
- PCB Designer 42 Years: "*I Love PCB Design and I Love Altium*"

Agenda

1. What is HDI (High Density Interconnect)
2. 3 Layout Designer Perspectives
3. Layout Solvability: Routing Density with HDI
4. Circuit Performance Using HDI
5. Improved Manufacturing Reliability and Yield with HDI
6. Benefits and Challenges of Using HDI

HDI Definition

High Density Interconnect, or HDI, circuit boards are printed circuit boards with a higher wiring density per unit area than traditional printed circuit boards (PCB). In general, HDI PCBs are defined as PCBs with one or all of the following: micro-traces, VIP (Via In Pad), microvias, blind vias, buried vias or other microvia technique, built-up laminations and high signal performance considerations.

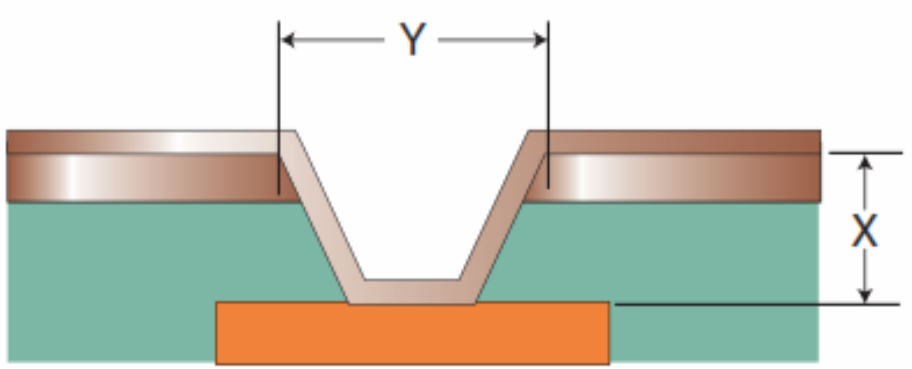
Printed circuit board technology has been evolving with changing technology that calls for smaller and faster products. HDI products are more compact and have smaller vias, pad pitch, and lines and spaces. As a result, HDIs have denser wiring, which means lighter, compact, lower layer count PCBs. In essence, they can perform better and be more reliable.

Microvia IPC-2221 Definition

Microvias can be either a buried via or blind via.

A microvia is defined as a blind structure (as plated) with a max. aspect ratio of 1:1 terminating on or penetrating a target land, with a total length of no more than 0.25 mm [0.00984 in] measured from the structure's capture land foil to the target land.

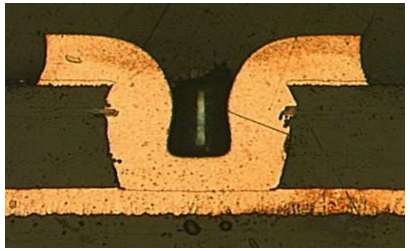
When utilizing a microvia structure, typically thinner dielectric materials will contribute to higher reliability. This is due to the physics of plating copper into the hole.



Note: X/Y = Microvia Aspect Ratio, with X=Y 1:1

Typical aspect ratio is about .8:1 (.004 dielectric with a .005 drill)

Building the uVia Structures in CAD Software

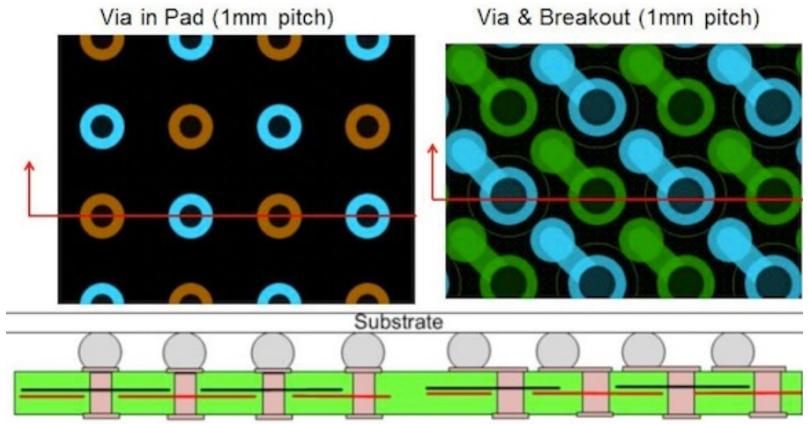


- The microvia built in CAD software will result with a normal pad/hole/pad scenario.
- Landing pad can be slightly larger if possible, but at least the same size.
- Recommended pad diameter is drill + .006” More pad helps prevent breakout.
- Correct uVia layer definition and usage ensures proper utilization that will be in line with manufacturing capabilities. Assign layer pairs.
- Plan the routing requirements, signal performance in conjunction with the manufacturing capabilities, at the start of the layout.

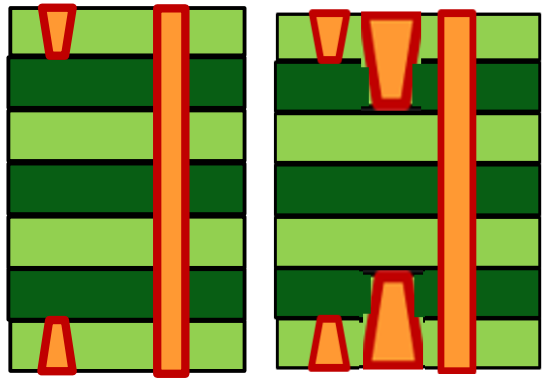
IPC Types of HDI Stack-up (IPC-2226 HDI std.)

VIP, Via In Pad

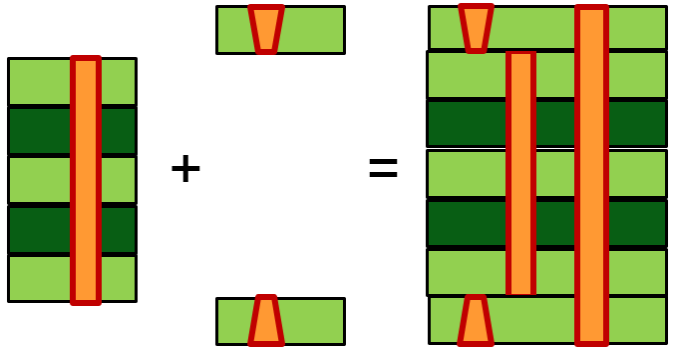
(Plated surface, planar finish)



IPC Type I

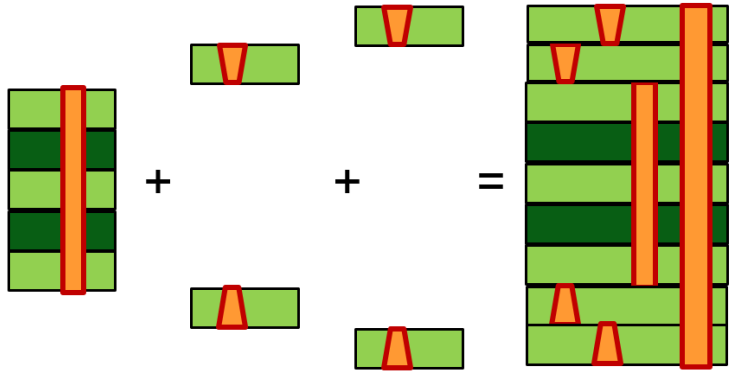


IPC Type II



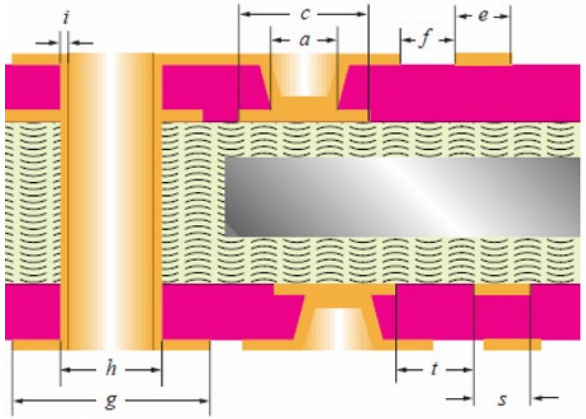
IPC Type III

(2-N-2, etc…)



IPC Type IV

(over core)



IPC Type V-VI

(ALV, any layer via)

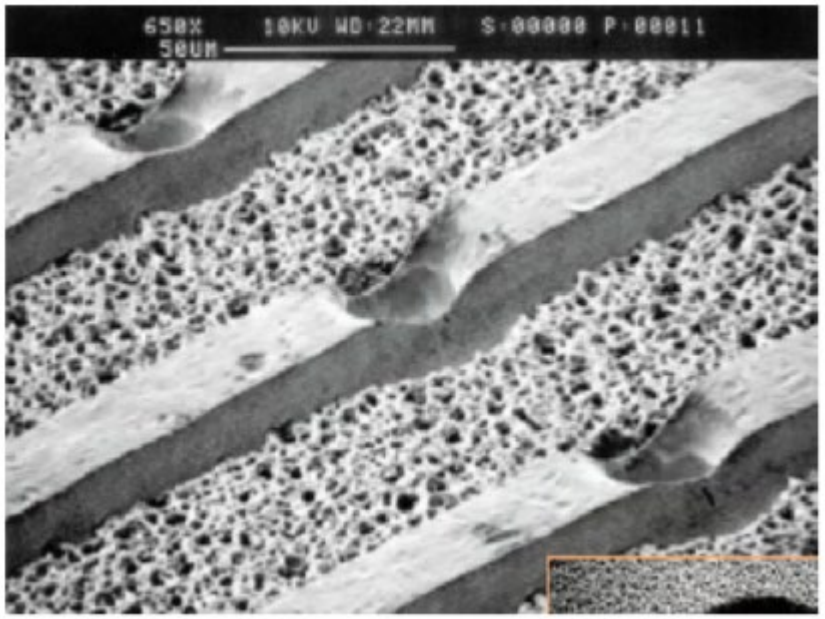
Filled with sintered CU paste

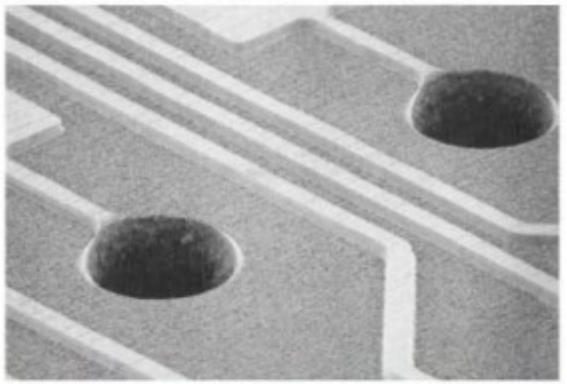
Landless Vias

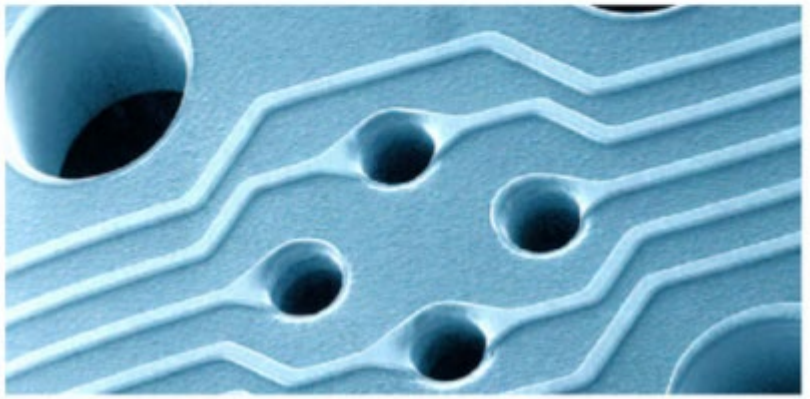
Warning

The best practice is that vias should always have an annular ring to avoid drill breakout and unless your fabricator tells you different, use a sufficient annular ring!

Landless Vias: *From the past and needed for the future…*





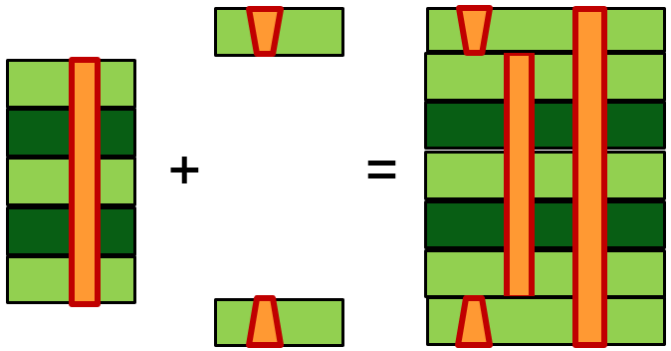


Once done as a proprietary practice and not shared with industry, it has remained lost. Currently, the IPC-6012 standards committee is investigating this technology with multiple test cases, so stay tuned!

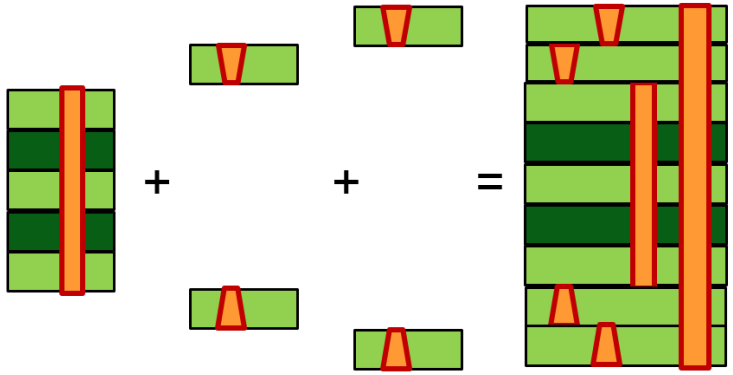
Landless Vias: Once the annular ring from the foil-copper completely disappeared, the ductility of the plated-copper in the hole, makes this work.

IPC Types of HDI Stack-up (IPC-2226 HDI std.)

IPC Type II
(1-N-1, etc…)



IPC Type III
(2-N-2, etc…)



IPC Type III
(3-N-3, etc…)

What is done on the top side of the stack-up will be done to the bottom side to achieve a balanced stack up. You will get the potential for the same type microvias on the bottom, even if you don't use them.

Remember additional microvia plating thickness for each layer!

HDI uTraces - Using mSAP and SAP

Upcoming manufacturing process development will allow circuits to be designed with lines and spaces in the range of 1-2 mil (25-50uM) with strict impedance control.

mSAP – Modified Semi-Additive Process

SAP – Semi-Additive Process

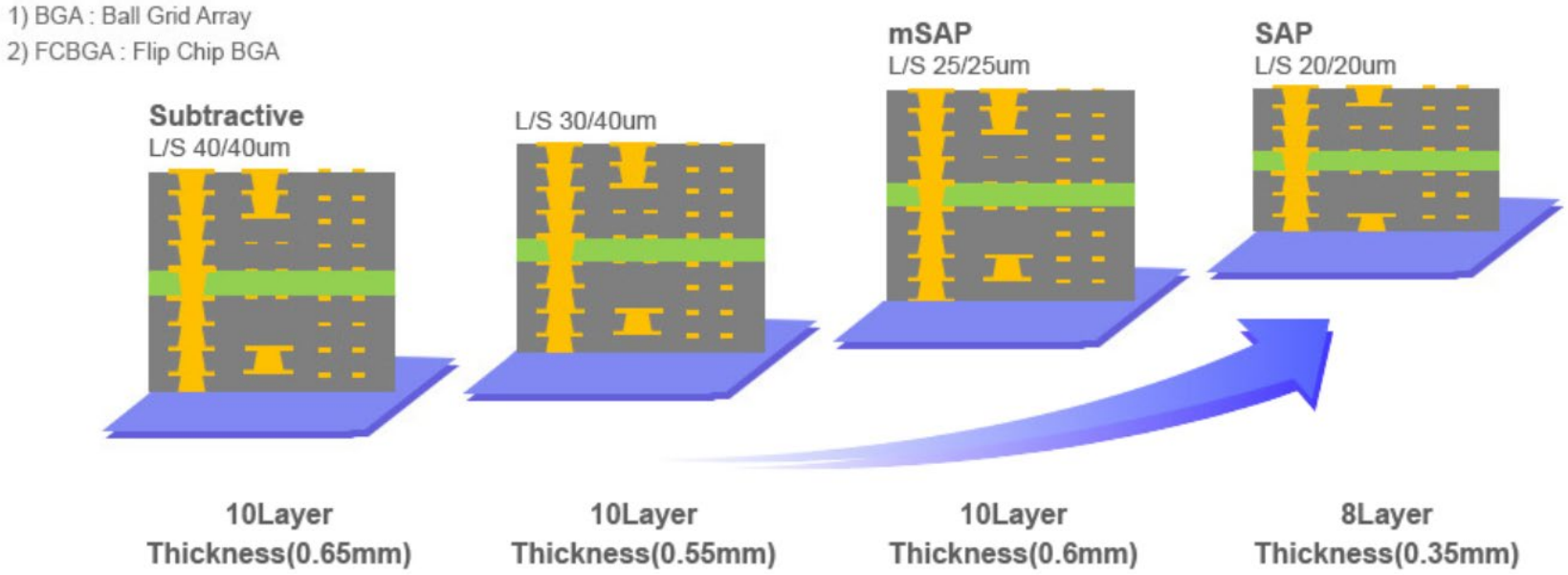
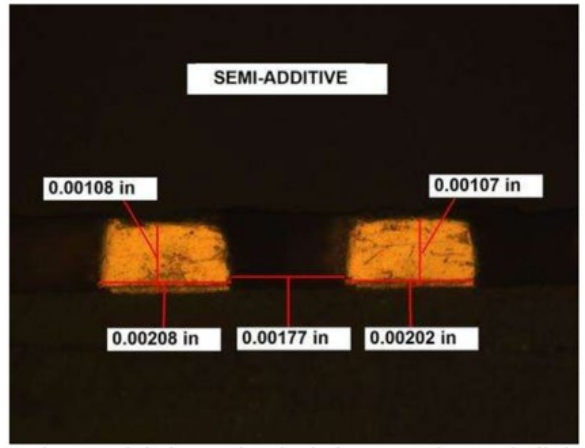
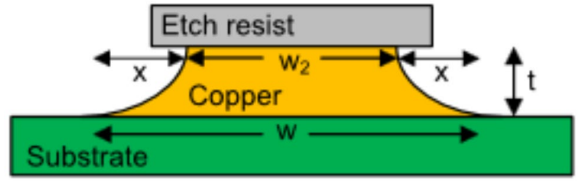


Image cited from SAMSUNG ELECTRO-MECHANICS.



Note: The near vertical trace shapes with the mSAP Process vs. Print and Etch Process as shown below.



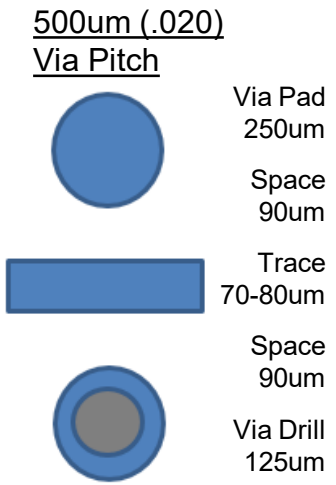
HDI uTraces - Using mSAP and SAP

mSAP – Modified Semi-Additive Process

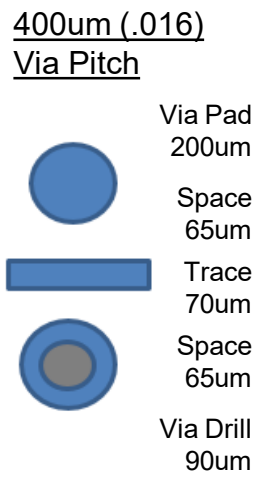
With mSAP, a much thinner copper layer is coated onto the laminate, and plated in the areas where the resist is not applied thus, the “additive” nature of the process. The thin copper remaining in the spaces between conductors is then etched away. Whereas trace geometries are chemically defined during subtractive processes, mSAP allows trace geometries to be defined via photolithography. *You must check with your fabricator to see if this method is available!*

SAP – Semi-Additive Process

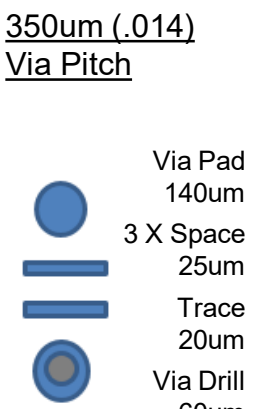
Although the semi-additive process (SAP) used in the IC substrate board can realize more precise circuit fabrication, but there is a problem that the *manufacturing cost is high and the production scale is small*, thus restricted to ICs as of today



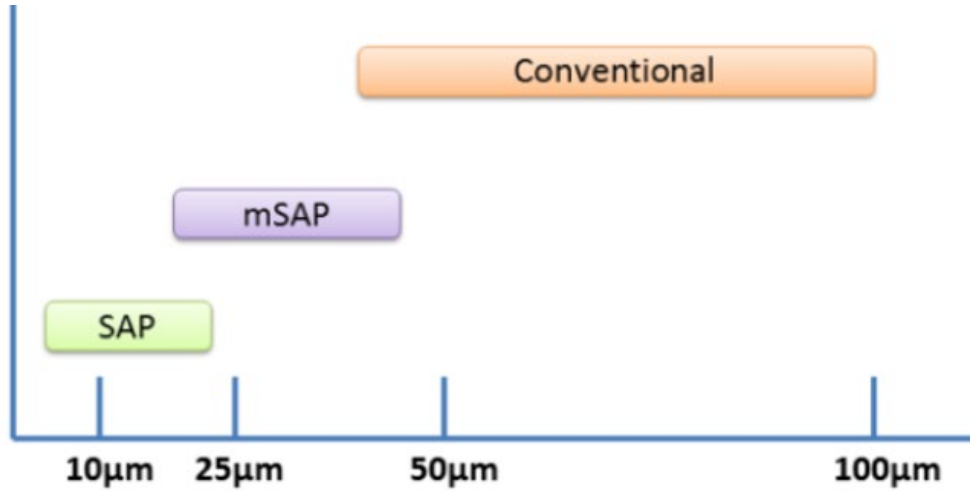
Subtractive
Print & Etch Process



Any-Layer
Via Process



Modified Semi-
Additive Process



PCB Trace Width vs. Process Technology

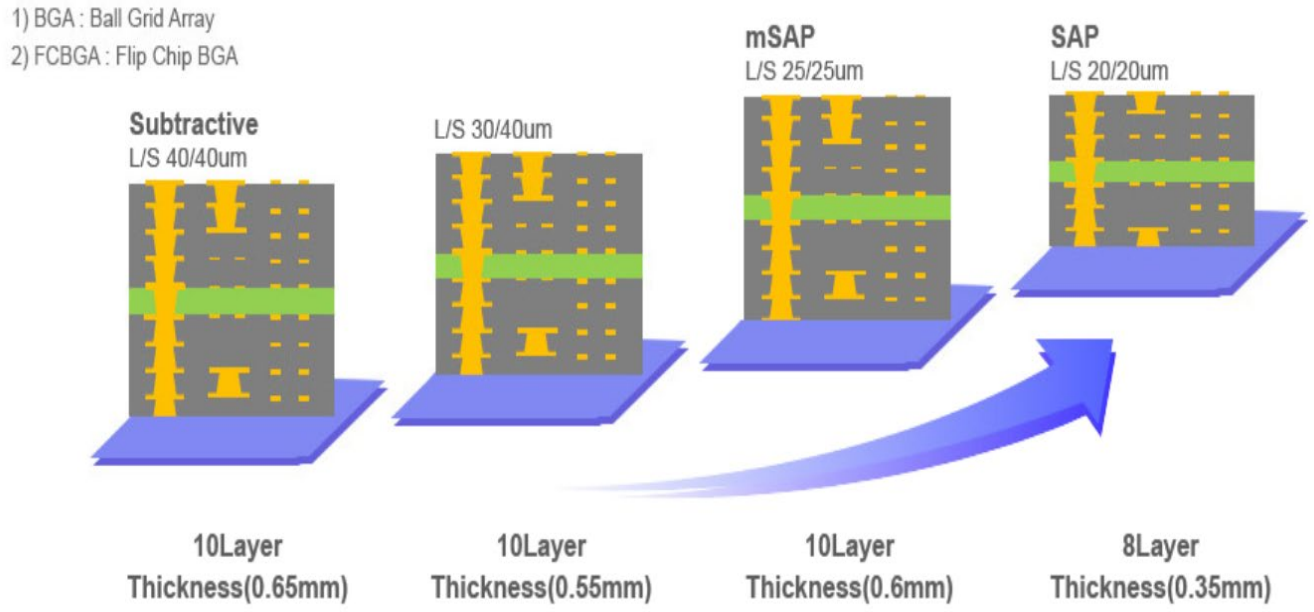
HDI uTraces - Using mSAP and SAP

Trace width typically will closely match the dielectric thickness to achieve a 50 ohm characteristic impedance.

Drill diameter typically will match the dielectric thickness to achieve a 1=1 aspect ratio for plating purposes.

Thus, a thin dielectric thickness allows for thinner traces and smaller holes for microvias.

This in turn pushes the envelope concerning material and process.



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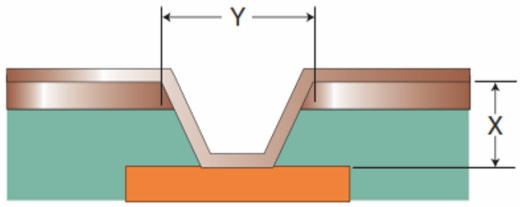
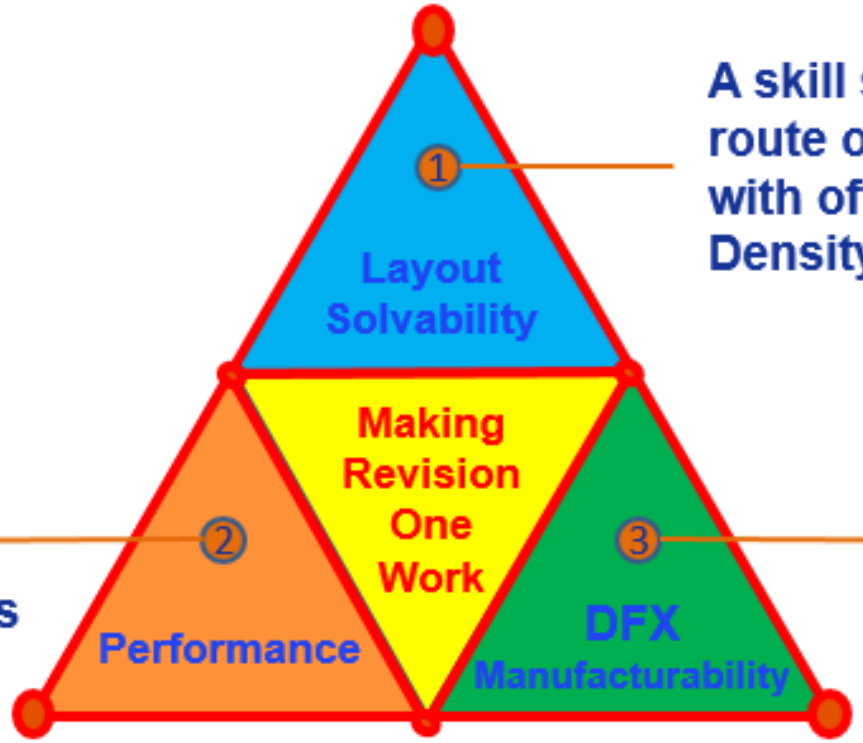


Note: X/Y = Microvia Aspect Ratio, with X=Y 1:1

Layout Designer Perspectives (1)

Today's Designer Must Meet 3 Perspectives for Success



A skill set to solve the place and route of all parts and connections with often with complex High Density Interconnect (HDI)

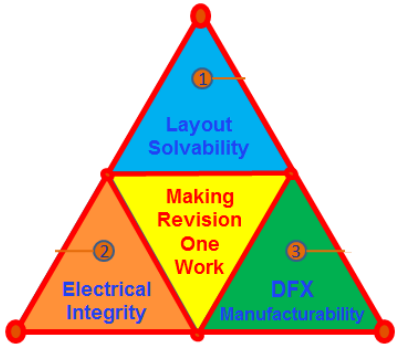
Signal (SI) & Power Integrity (PI) meeting performance requirements on all layers

DFX considerations producing high yield and lower cost

MOST IMPORTANT SLIDE

THE RESULT: Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing. All 3 perspectives must be considered!

Layout Designer Perspectives



As shown on the right the 3 perspectives of the Designer's Triangle will soon exist at the beginning of every sectional of the IPC-2200 series - Design Standard.

IPC-2222B Sectional Design Standard for Rigid Organic Printed Boards

WORKING DRAFT - DECEMBER 2018

Sections identified for editing/updating for this revision are highlighted in yellow text.
Sections identified for transition to the parent IPC-2221 are highlighted in blue text.
Sections identified for removal from this revision are highlighted in ~~red strikeout text.~~
Sections identified in gray-shaded text have been reviewed and approved for this Working Draft beginning April 2018

1 SCOPE

This standard establishes the specific requirements for the design of rigid organic printed boards.

The following overview describes what are the core knowledge and competencies to best serve in the role of *Printed Board Design Layout* as a stand-alone professional, or as the engineer performing this responsibility. Today's printed board designer must address numerous perspectives for success within a given schedule, with the goal of making the first design iteration work as intended, summarized as:

- Layout Solvability - Complex Packaging Skill-Set
- Electrical Integrity - Signal & Power Performance on all Layers
- Manufacturability - DFX Considerations for High Yield and Lower Cost
- Application considerations – Environmental, Performance, Shelf life, etc.

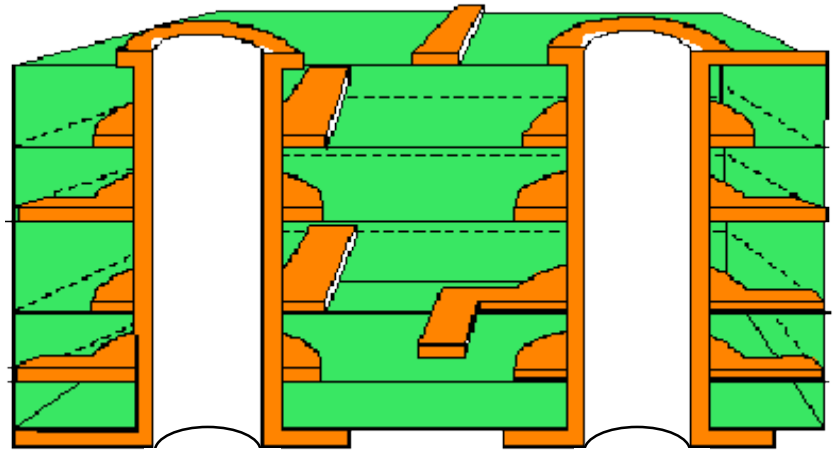
The result provides for maximum component placement and routing density achievable, optimum electrical performance and efficient, high yield, and defect-free manufacturing.

The result provides for optimal component placement, routing density and electrical performance to achieve an efficient design with high yield and defect-free manufacturability. (replaces above sentence)

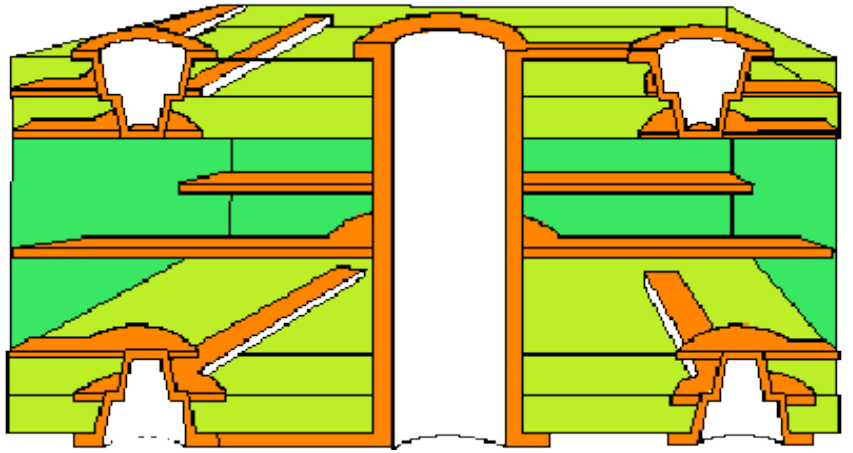
1.1 Purpose The requirements contained herein are intended to establish specific design details that **shall** be used in conjunction with IPC-2221 to produce printed boards that perform as an integral part of functional electronic hardware.

Layout Solvability: Routing Density with HDI

Routing Density



Via Starvation

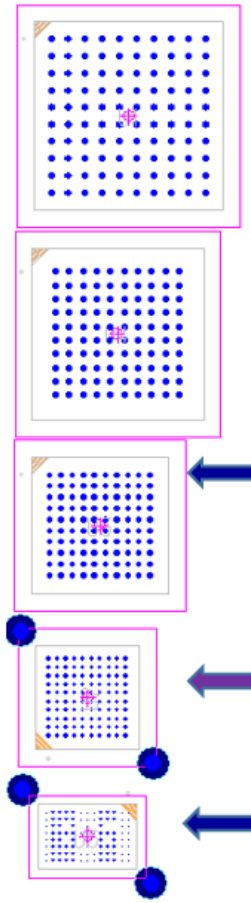


Internal layers are freed up for routing.

Plane layers no longer exhibit the “Swiss Cheese” effect.

Layout Solvability: Routing Density with HDI

100 Pin BGAs with varied Pin Pitch



100 Pin
1.0mm

100 Pin
.80mm

100 Pin
.65mm

100 Pin
.50mm

100 Pin
.40mm

Smaller
.35mm, .30mm

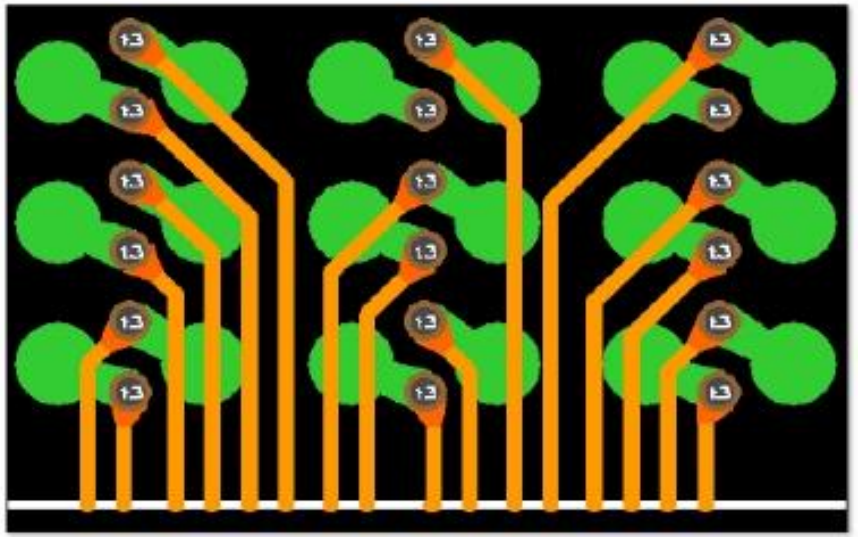
BGAs with a pitch of .65mm and below, require HDI solutions

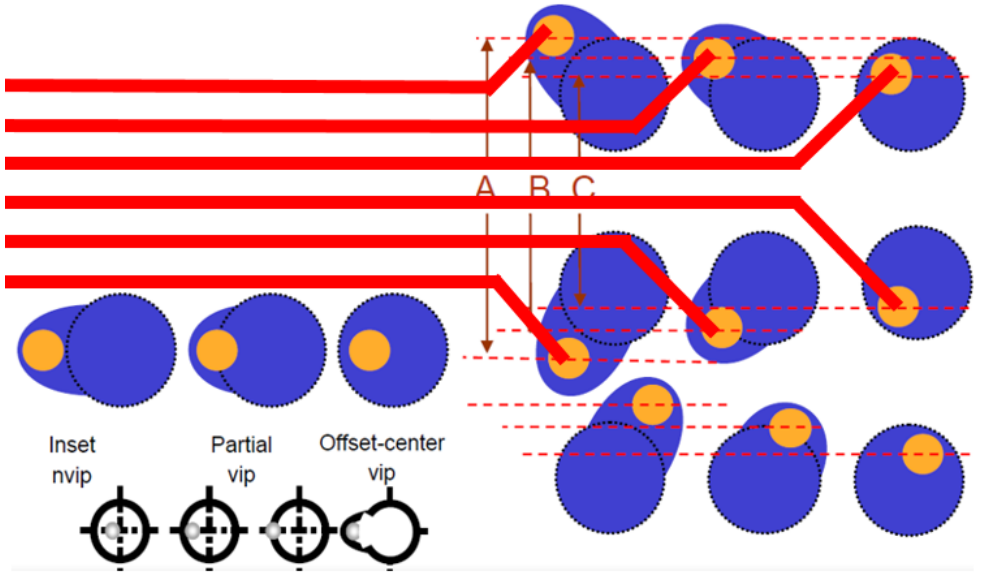
Layout Solvability: Via Fanout

Via fanout on a grid pattern aligned with the BGA pitch is typically beneficial for consistency and optimization.

However, microvias may require varied angled via fanouts from the BGA land to maximize routing channels on the escape layer.

Careful consideration should be observed to avoid solderability issues on BGA land sizes in assembly.





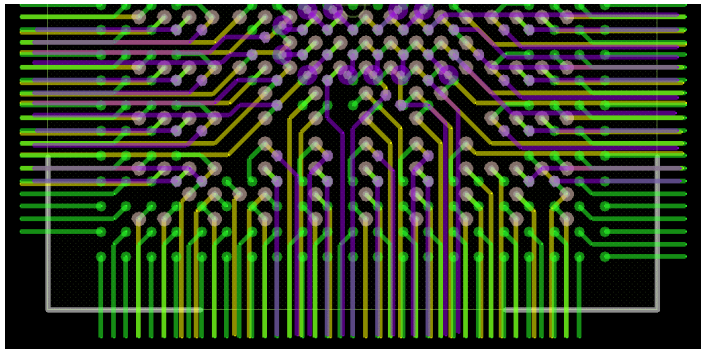
Reprinted with permission from The HDI Handbook, by Happy Holden

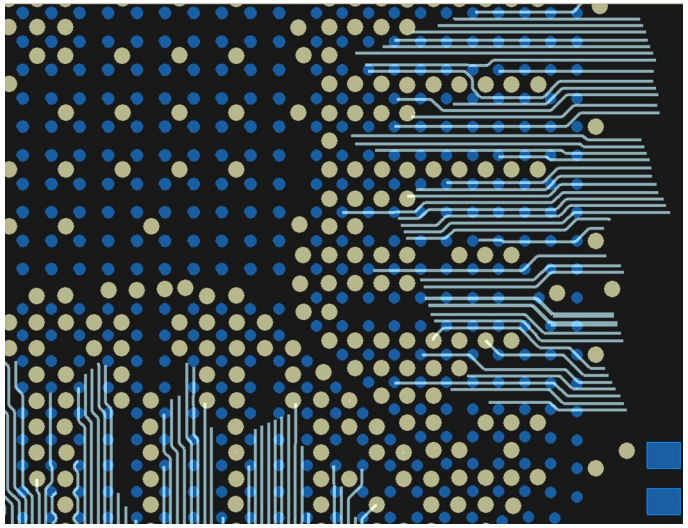
Layout Solvability: Via Fanout

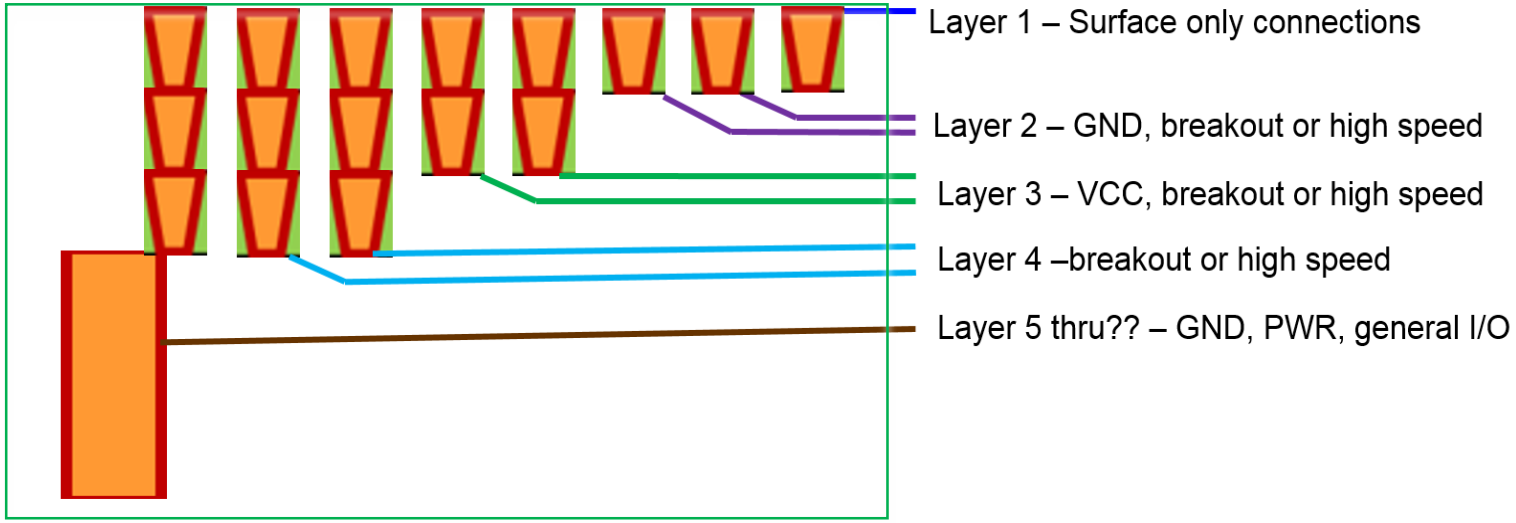
Pin-escape feasibility study:
Use a trial route to see how many traces will fit in an area and what via routing strategy will solve the pin-escape.

This may be required to determine the stack-up and manufacturing requirements. This can be saved as a re-use.

Plan the usage, see it from a cross section perspective.

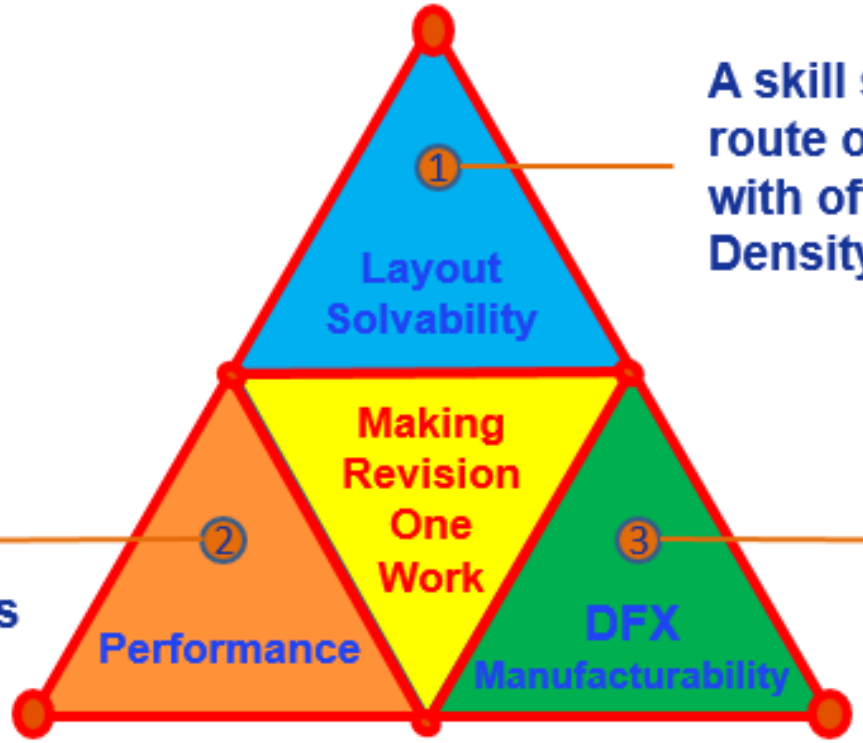






Layout Designer Perspectives (2)

Today's Designer Must Meet 3 Perspectives for Success



A skill set to solve the place and route of all parts and connections with often with complex High Density Interconnect (HDI)

Signal (SI) & Power Integrity (PI) meeting performance requirements on all layers

DFX considerations producing high yield and lower cost

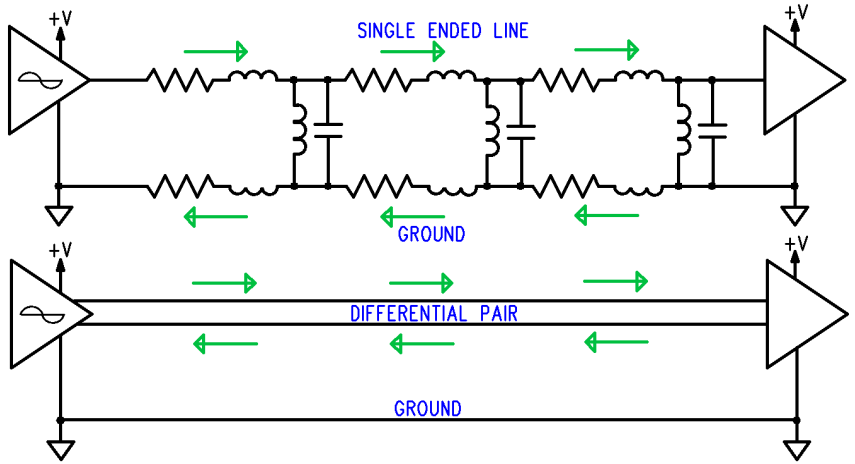
MOST IMPORTANT SLIDE

THE RESULT: Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing. All 3 perspectives must be considered!

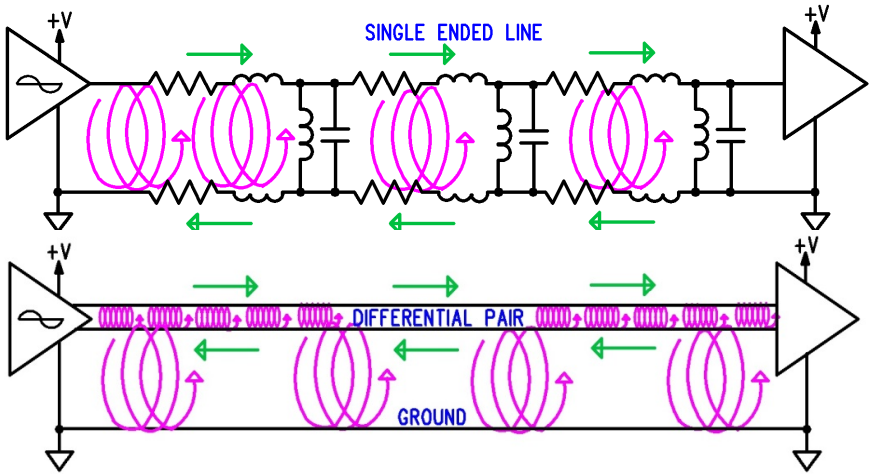
Signal Integrity with Faster Switching Circuitry (EM Theory Comprehension)

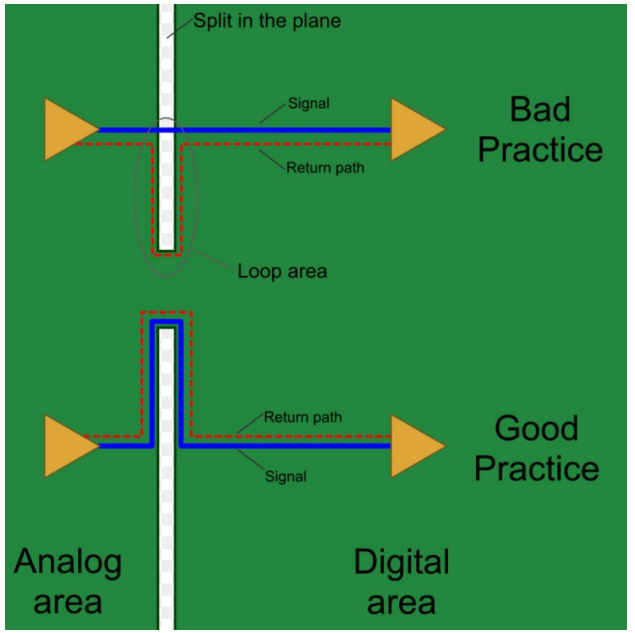
However, it is not really forward and back, rather, the energy field is immediate between the trace and the plane within the dielectric material

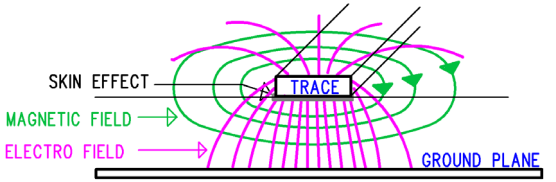
It's not forward and back

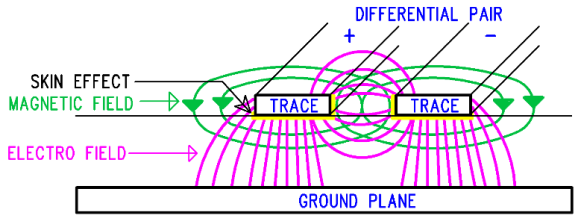


It's in the dielectric material









Circuit Performance Using HDI

Stack-ups that Support Functional EMC

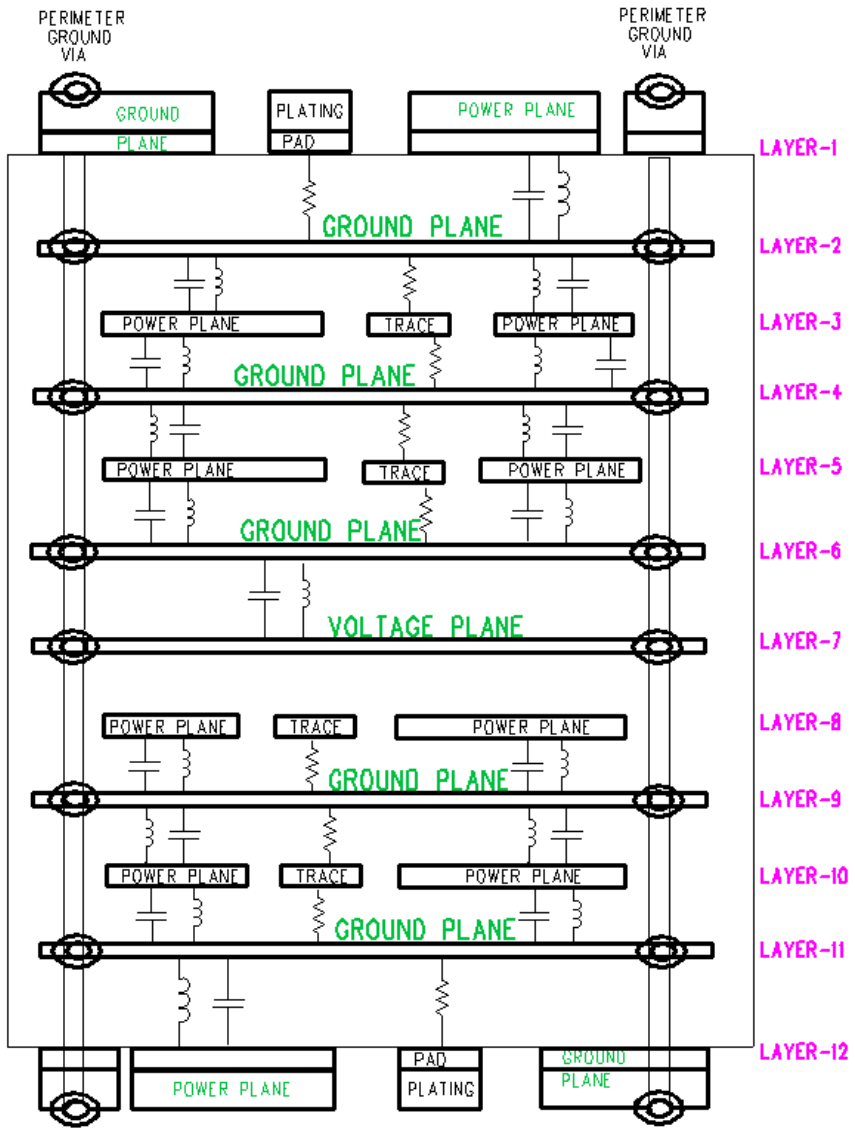
GND (0.0V) is the most important signal in the circuit!

Ground is where you plant tomatoes, but we commonly refer to this signal as GND (0.0V).

- **GND (0.0V) is what is used to reference every signal for a return path. *Never route signals over split GND plane!***
- **GND (0.0V) is what is used to reference every PWR net (Voltage rail). *Never place PWR's over split GND plane!***

Get these last two bullets right and you have solved a significant amount of your Signal/PWR Integrity concerns!

12 Layer Stack-up

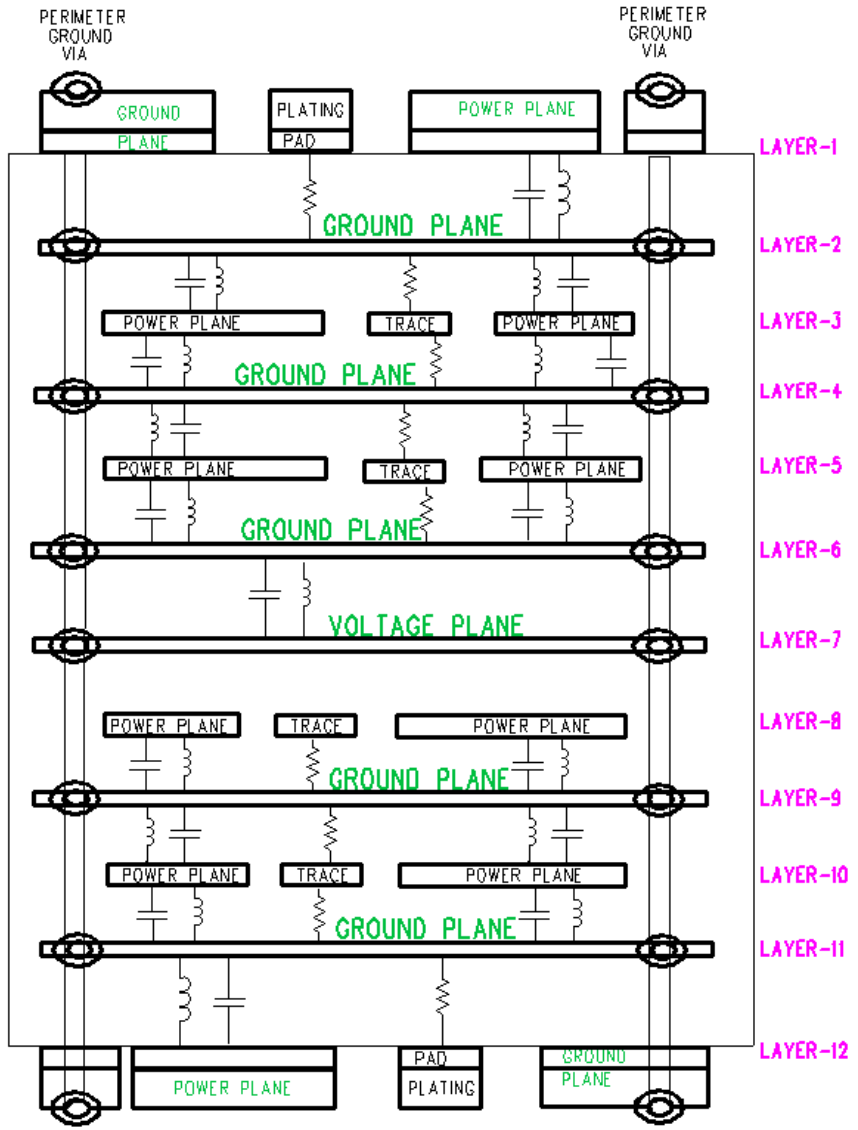


Circuit Performance Using HDI

Moving Signals Through the Stack-up

- A return plane is needed for each routing and power layer.
- Need power/ground connections that join all like plane layers together.
- Stacked and staggered microvias help get signals to move layer to layer, but require multiple laminations.
- Other signals may use TH vias or buried TH vias to get signals to deep internal layers.

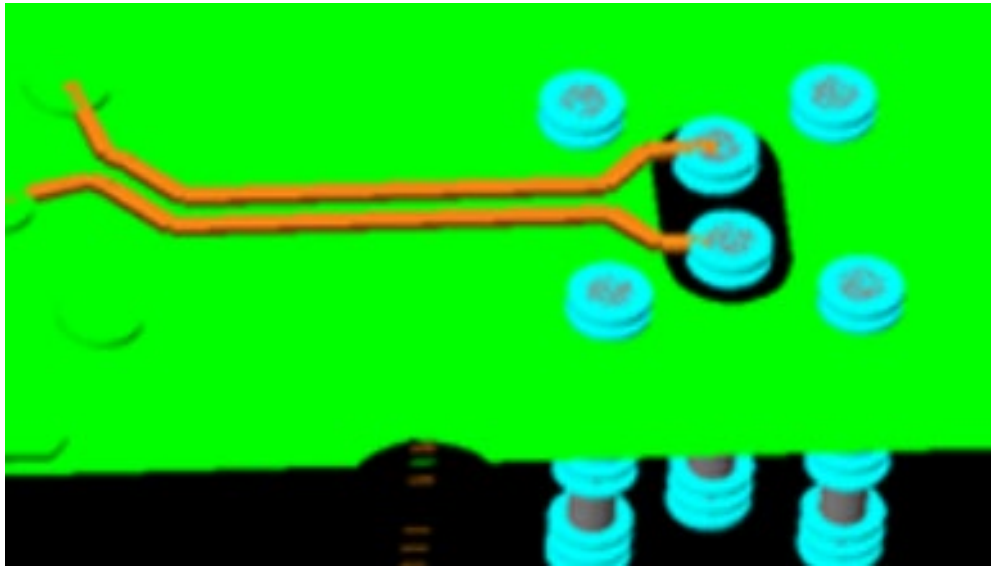
12 Layer Stack-up

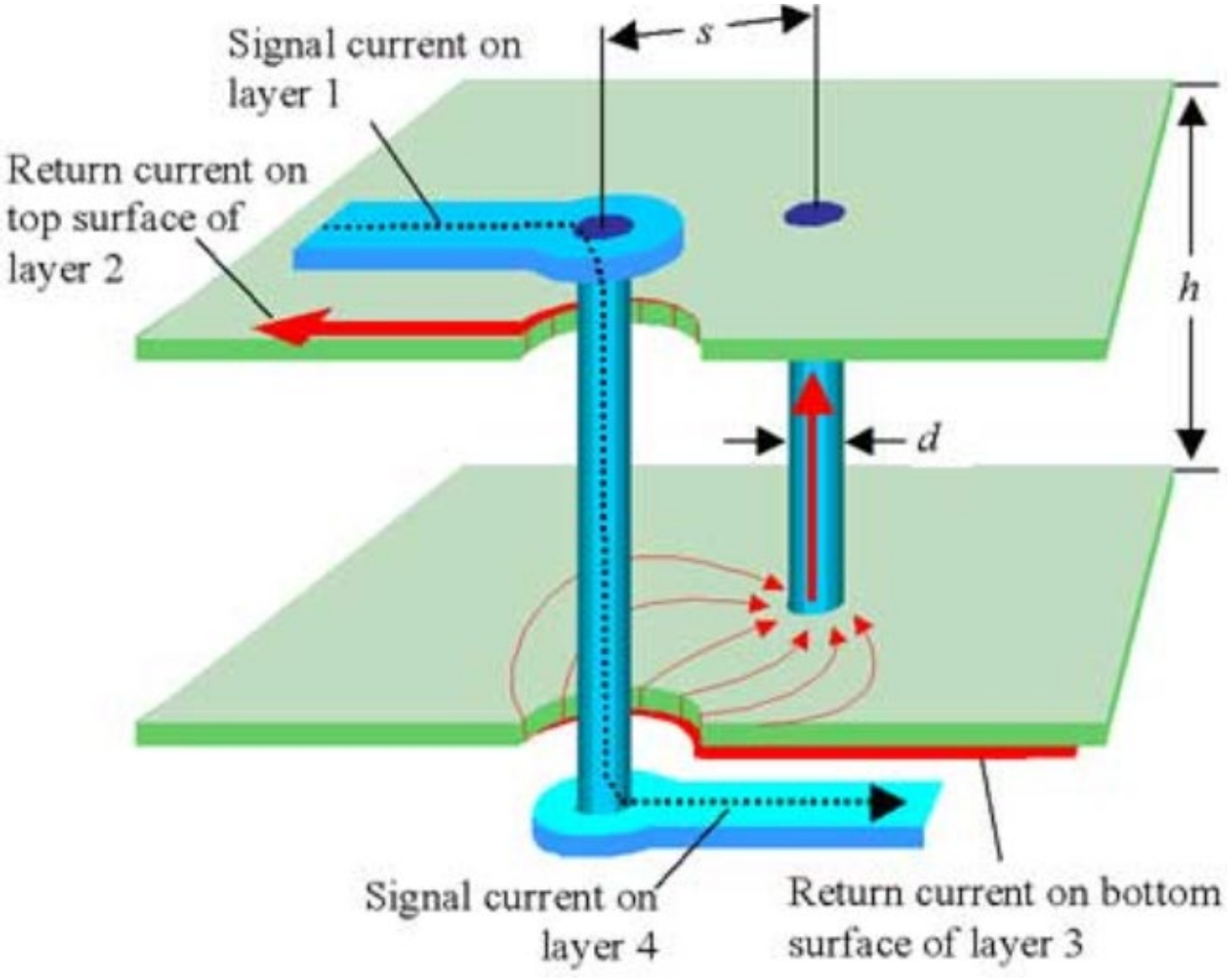


Stack-ups that Support Functional EMC

Return Path Vias for:

- Single-ended signals – shown on right
- Differential Pairs – shown below



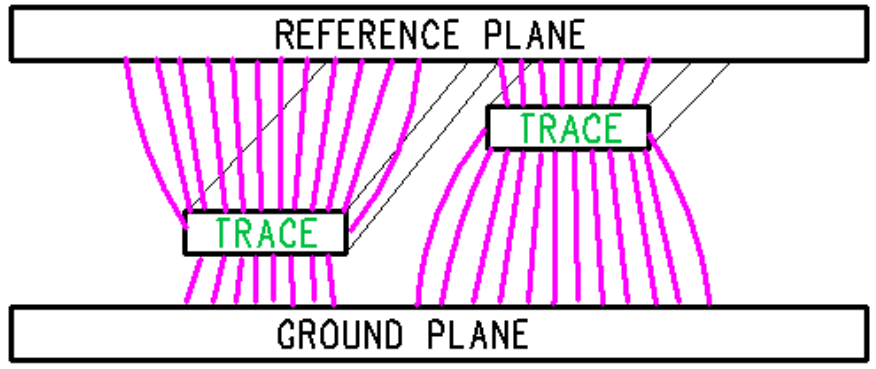


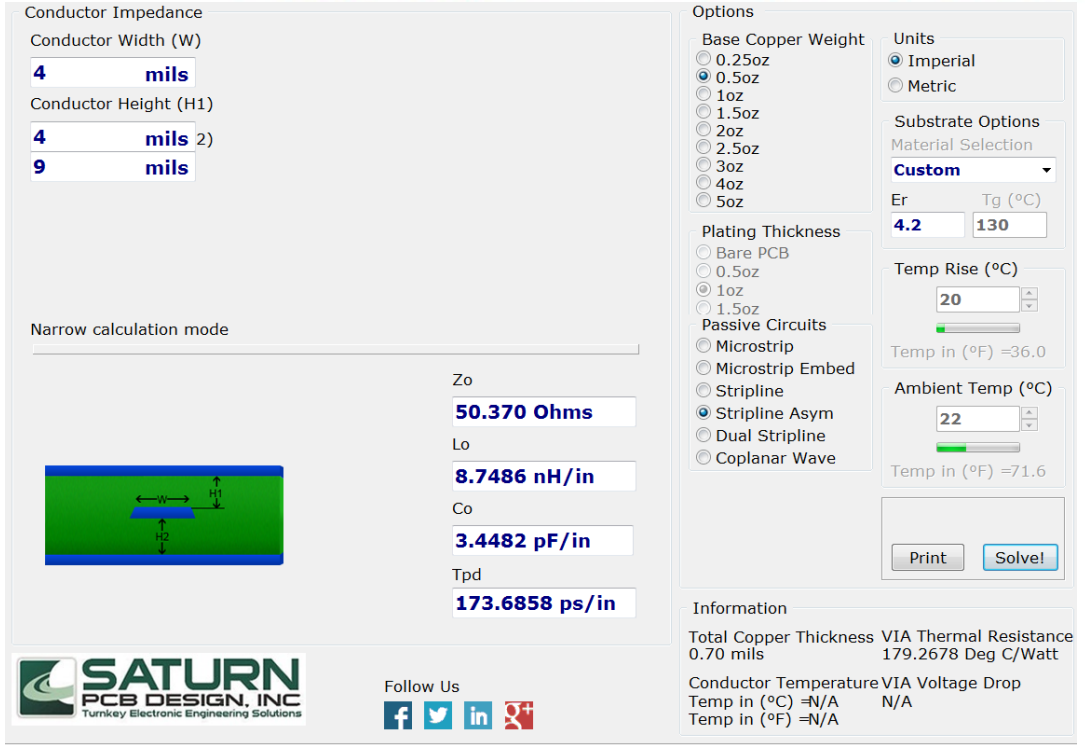
Circuit Performance Using HDI

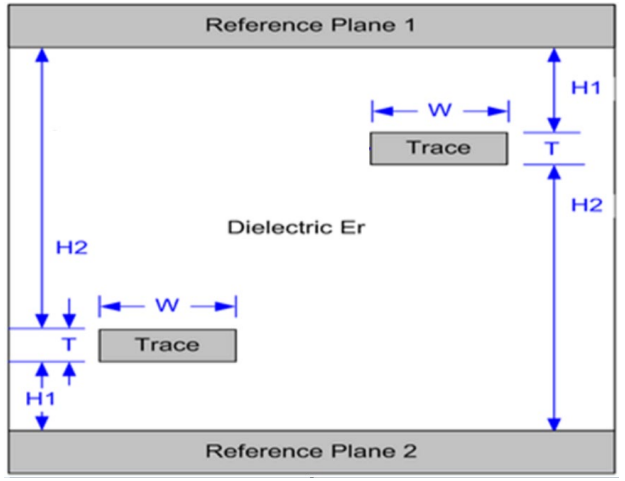
Avoid this Stack-up Condition: Dual Asymmetrical Stack-up

- You conceptualized and setup your stack-up
- You secured a stackup from the fabricator
- You make your fabrication drawing reflect this
- You require the fabricator to utilize an impedance coupon based on this stack-up
- You require the fabricator to TDR test the coupon
- You setup your rules and simulations to consider these as 2 - 50 ohm SE impedance lines

BUT…



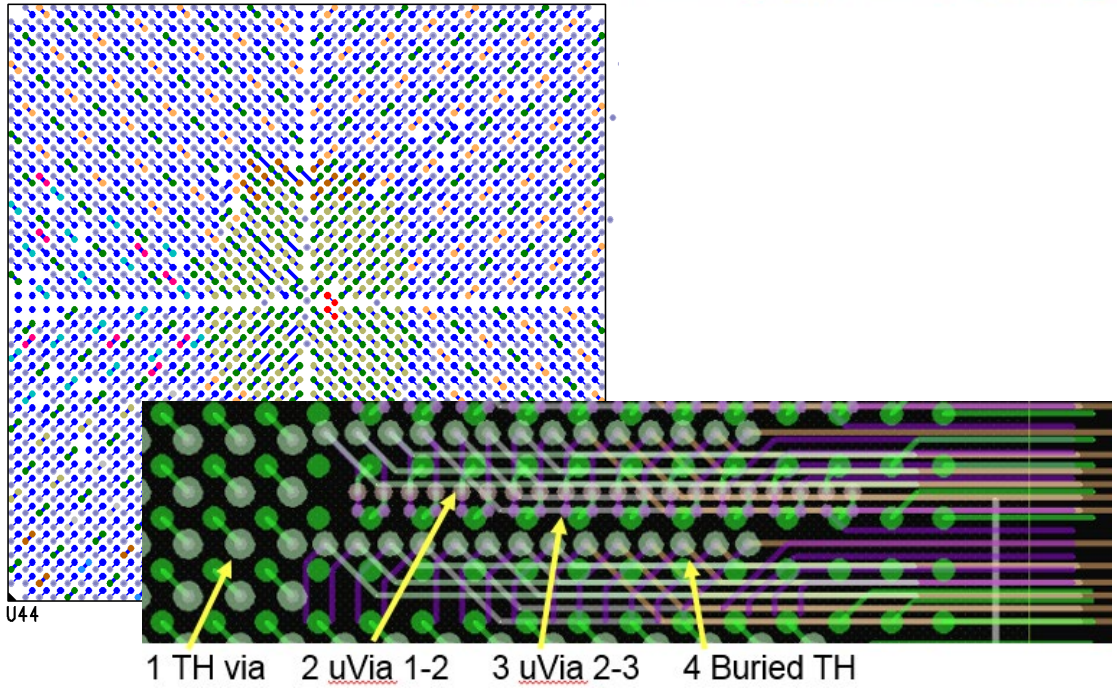




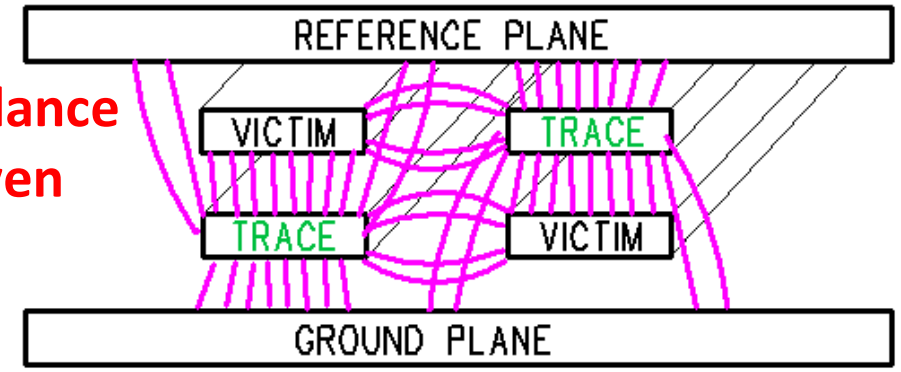
Circuit Performance Using HDI

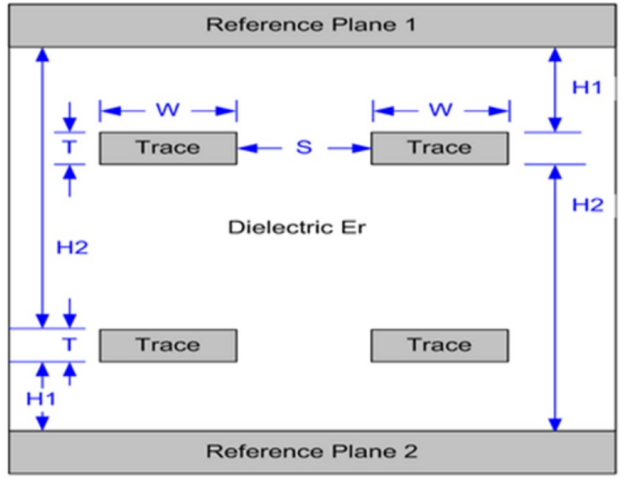
Avoid this Stack-up Condition: Dual Asymmetrical Stack-up

- **BUT…**
- Because the board routing was so dense.
- Because alternating layer perpendicular routing strategy went out with through hole technology.
- Because most of the ICs on a dense board are BGAs.
- Because BGAs want to route “wagon-wheel” style away from the center of the chip.
- Because the routing channels where available.
- Because you did not want to add extra layers.
- So you routed like this.



You have changed the actual impedance and made a crosstalk nightmare, even though the coupon is good.

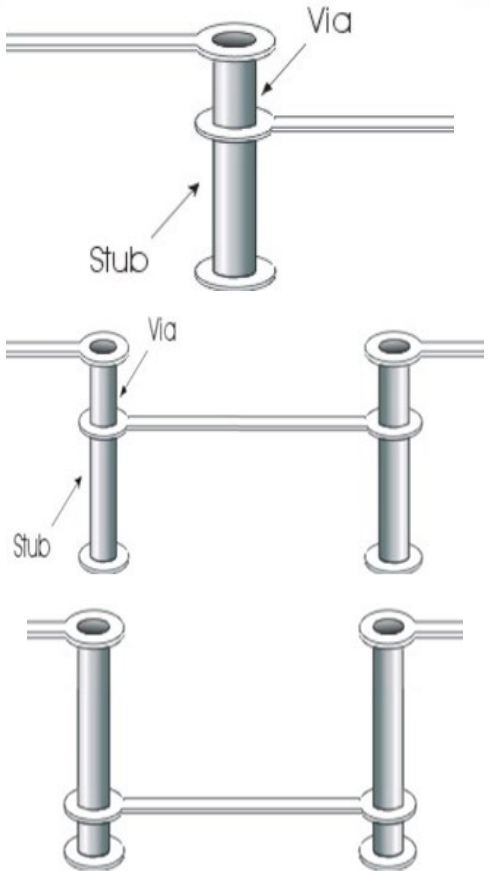


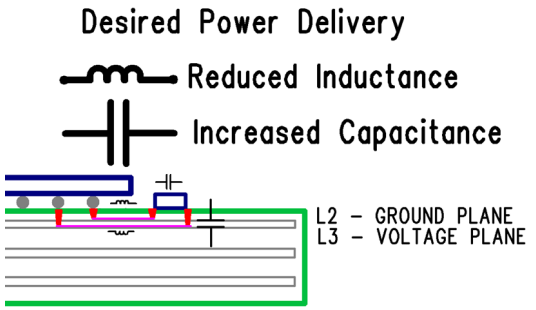


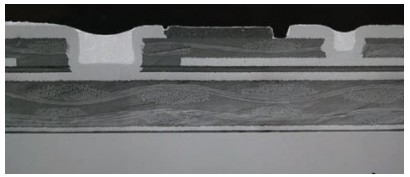
Circuit Performance Using HDI

Signal Layer Usage:

- Fabrication allowances should be made for plating, if routed on outer layers. Digital signals when routed stripline (inside of GND planes) will better contain emissions.
- RF circuits often seek to have low noise to their traces and they also seek to reduce parasitics on every feature. As a result, they will often seek to be routed on outer layers with a wide trace (non-lossy) and a matching dielectric to GND. If routed on the surface, no vias would be required as they are considered a parasitic stub.
- Digital signals perform best when they use the maximum depth of every via, leaving a short stub on the via. Therefore, maximize lower layers first when routing. This will allow for Power Distribution layer-pairs positioned higher in the stack-up and closer to the device of use (Reduced Inductance).

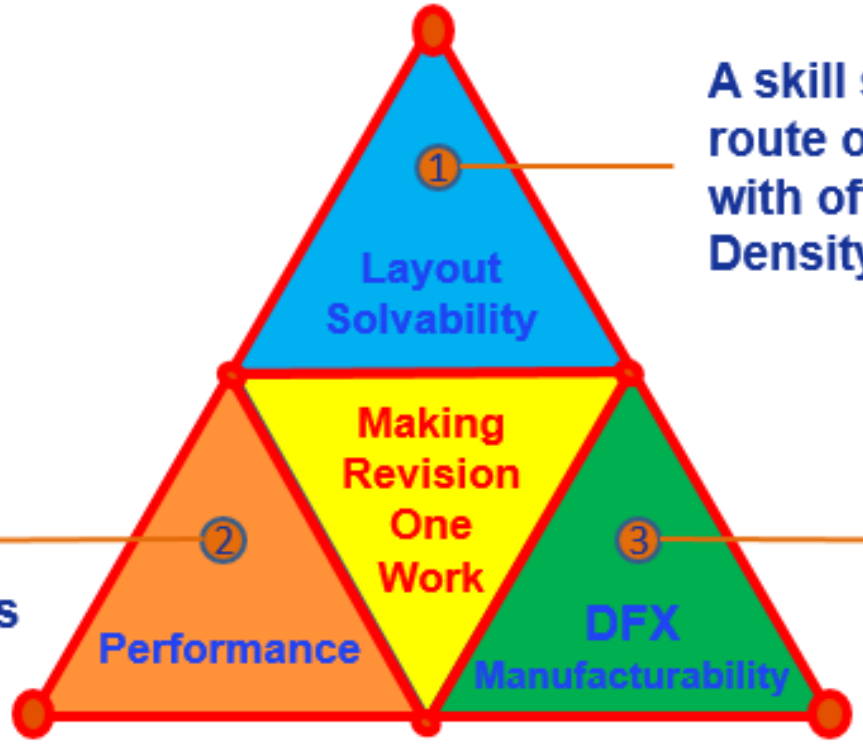






Layout Designer Perspectives (3)

Today's Designer Must Meet 3 Perspectives for Success



A skill set to solve the place and route of all parts and connections with often with complex High Density Interconnect (HDI)

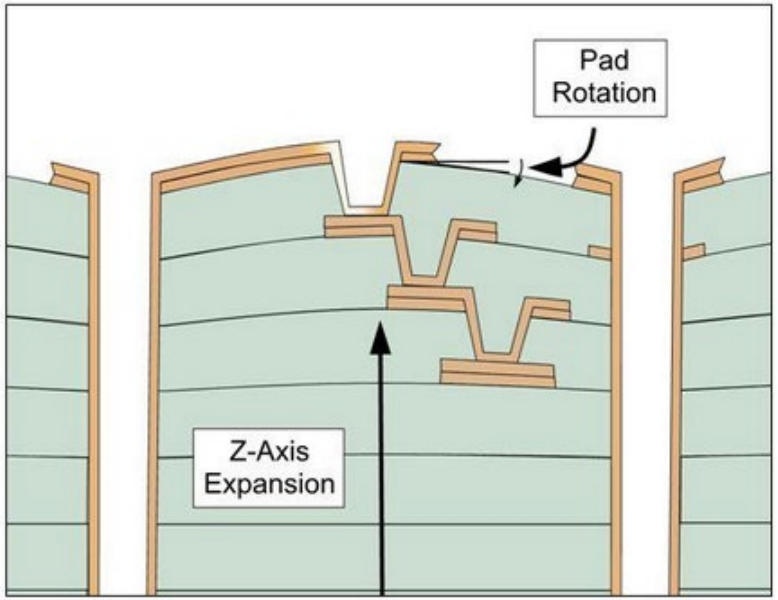
Signal (SI) & Power Integrity (PI) meeting performance requirements on all layers

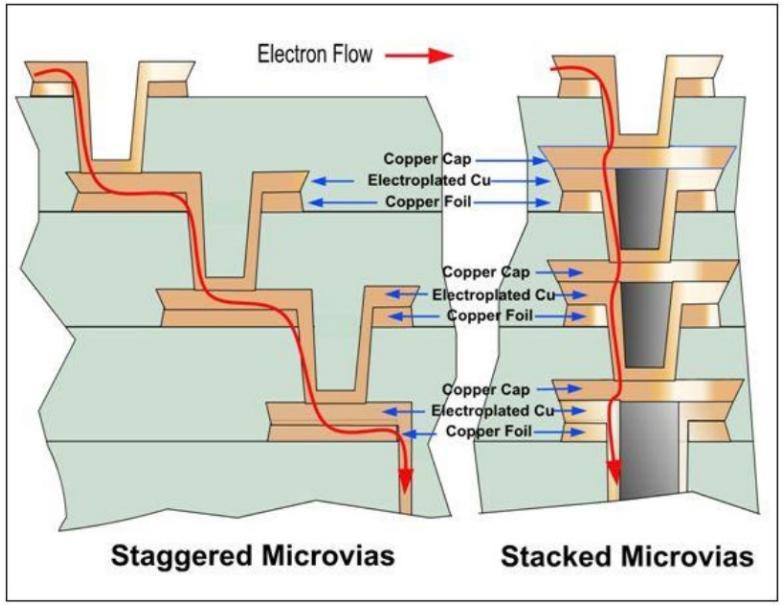
DFX considerations producing high yield and lower cost

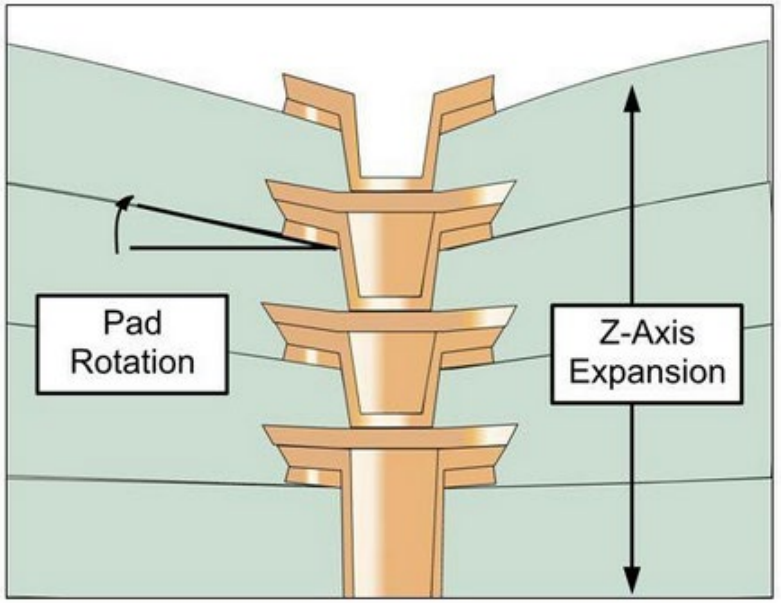
MOST IMPORTANT SLIDE

THE RESULT: Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing. All 3 perspectives must be considered!

Staggered or Stacked Microvias







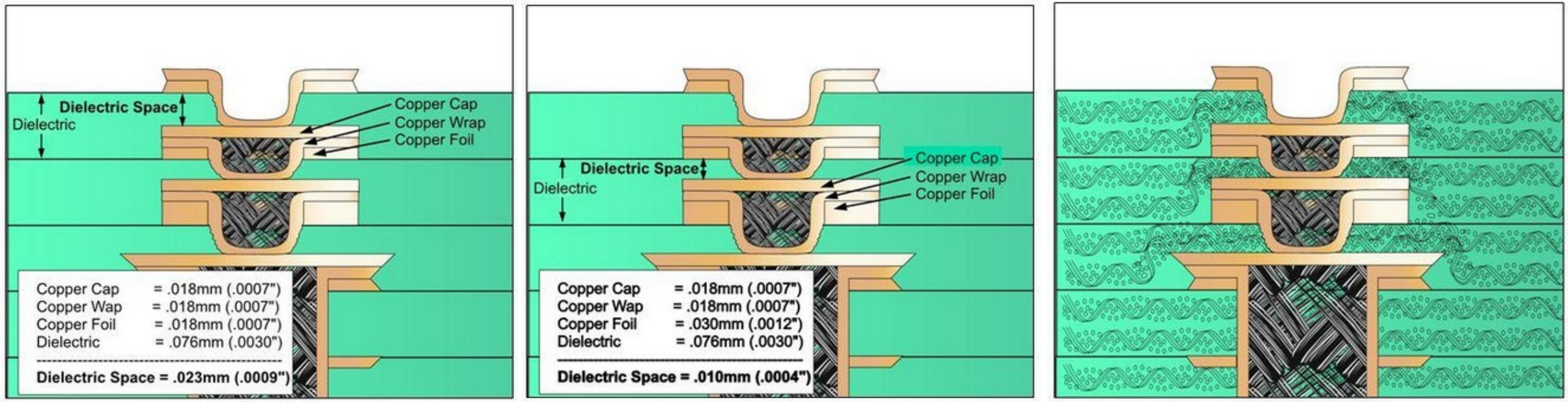
Staggered Microvias don't require plugging and the copper caps.

Stacked Microvias will require plugging and the copper caps.

Note:
Both Staggered and Stacked microvias will require additional plating requirements and thus will add to increased board thickness.

With every additional microvia layer there exists many manufacturing steps (approx. 40) and can be cost considerations.

Stacked Microvias



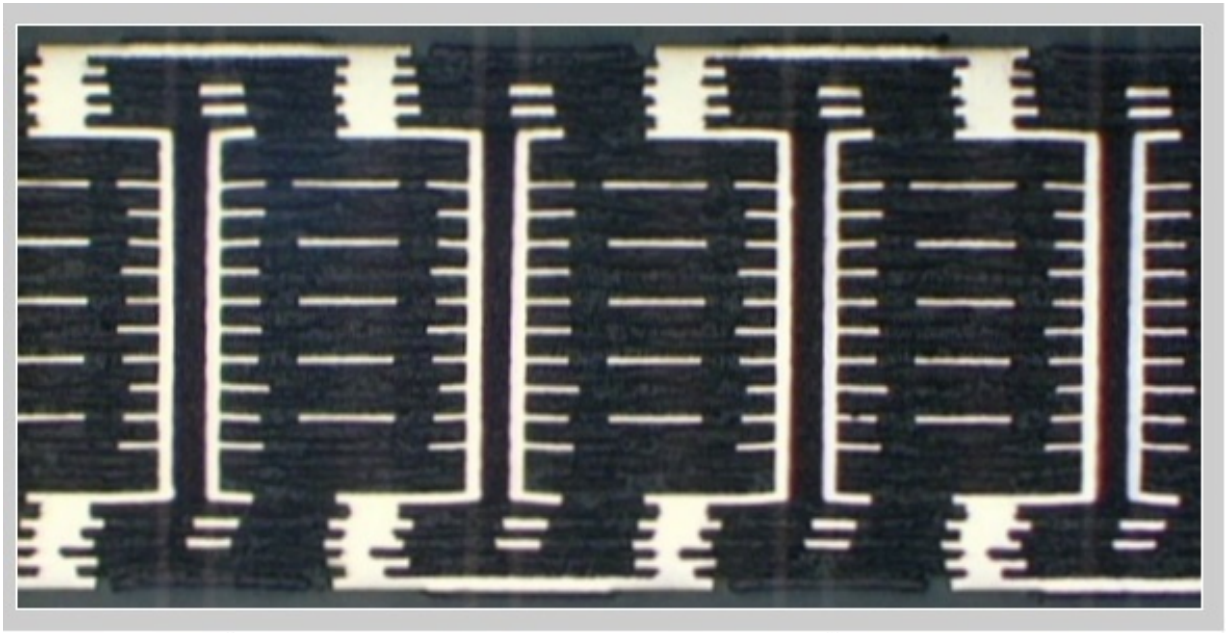
Stacked Vias require metal filling and capping as the glass is squeezed between layers.

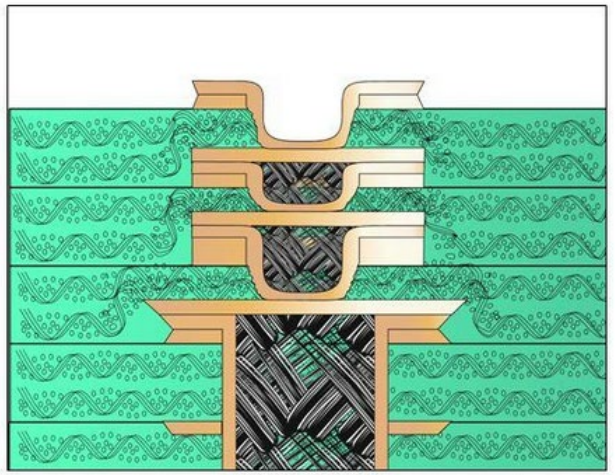
They restrain the Z-Axis expansion because they both expand at a different CTE. Because the dielectric material is so thin that helps this concern.

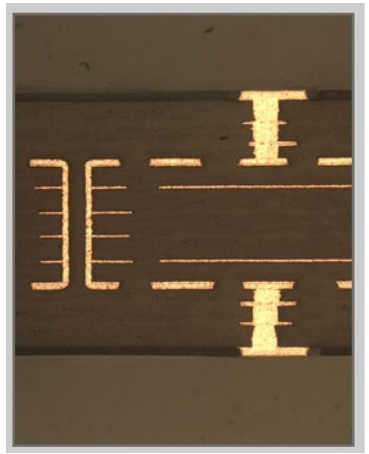
Staggered or Stacked Microvias

The core-via in the center of the board should be plugged with non-conductive epoxy so it will expand in a similar fashion to the surrounding dielectric.

Never stack micro-vias on top of the core-via for dis-similar Z-Axis CTE reasons.



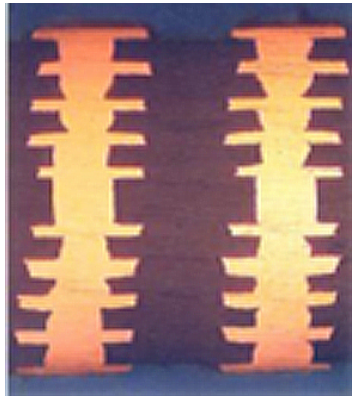




If laser vias are stacked on the core-via, they would require cap plating. This practice has proven to cause reliability problems. *The error condition is shown in these lower left images*.

Benefits and Challenges of Using HDI

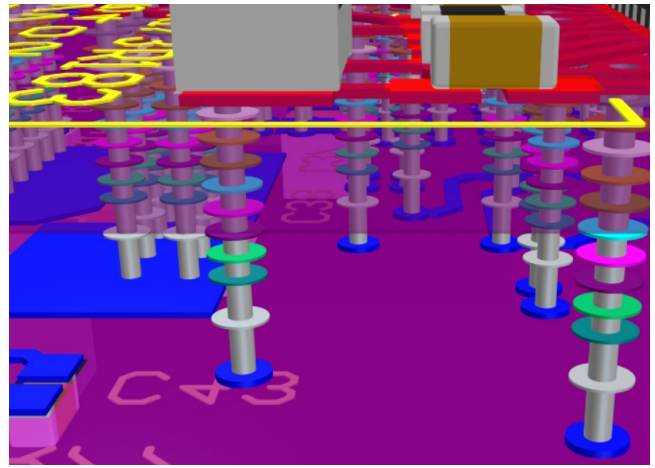
- Smaller - Miniaturization of products, pitch & features.
- More expensive as a general rule, due to more fabrication processes. Might be less expensive if layer reduction is achieved and the cost per connection improves.
- Performance - 1/10th parasitic of PTHs, fewer stubs, improved noise margins.
- Lighter - Lower substrate weight, thickness and volume.
- Reliable – Because of better aspect ratios vias, thinner dielectrics, and improved via metalization.
- Testability - Is significantly challenged due to limited access to all nets.

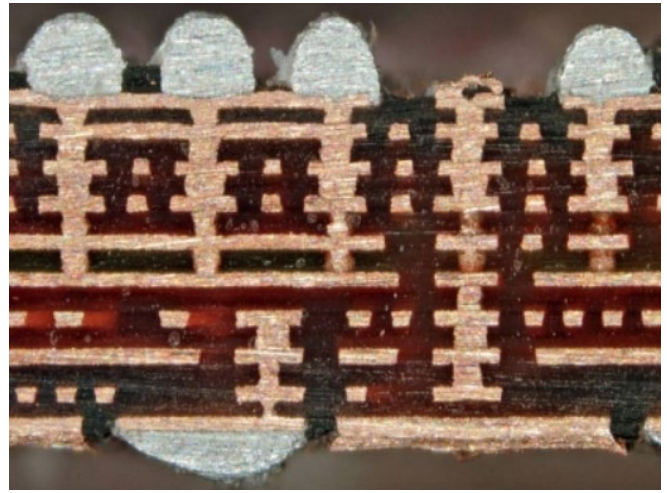


Research all requirements at the start of the layout!

Benefits and Challenges of Using HDI

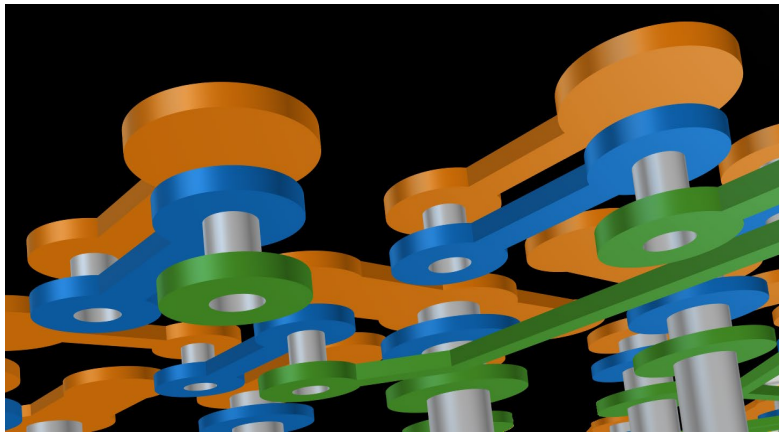
- Placement Feasibility – SMT Parts will not fit with room for pin escapes to PTH vias, so use VIP via in pad.
- Standard PTH vias are too large to pin-escape a uBGA (Typically a .65mm or below pitch device)
- High Speed or RF performance – unwanted parasitics or excess inductance from standard PTH vias
- Requirement for thin PCBs in some market spaces.
- Back to back large active BGA's on both sides of PCB.
- RF on Primary Side / Digital on Secondary side



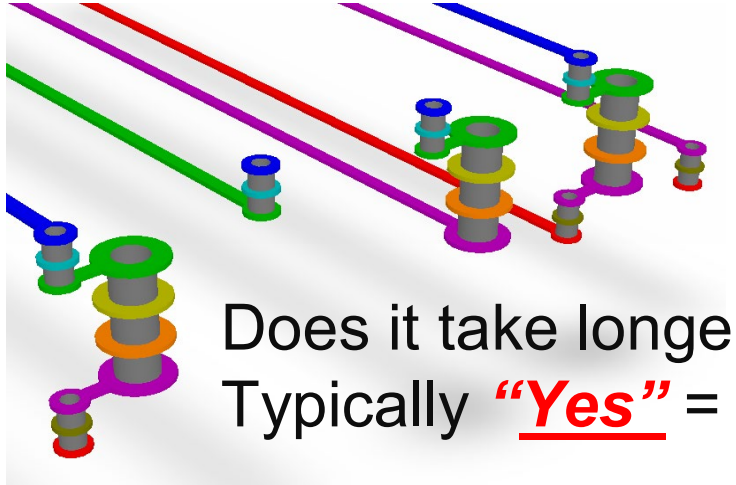


Benefits and Challenges of Using HDI

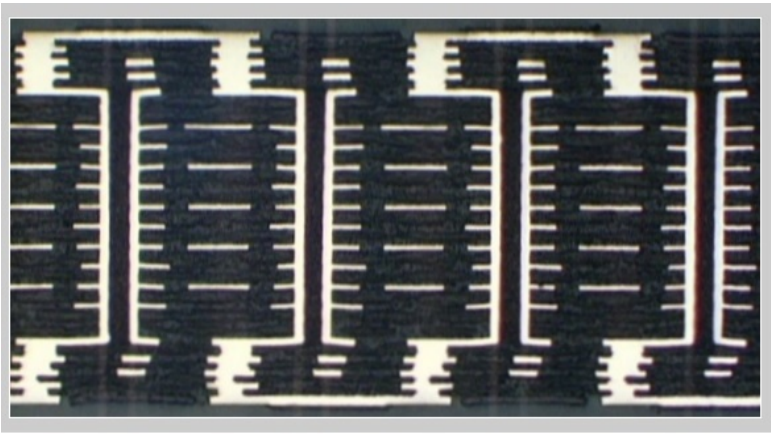
Increased Routing Density (HDI)



- Fine pitch BGA – <.65mm, .5mm (must be used)
- Sequential lamination - multiple stacking options
- Thin materials - down to 50um [0.002 inch] dielectric
- 3D Routing is more challenging from a layout perspective.
- Improved signal and power integrity performance



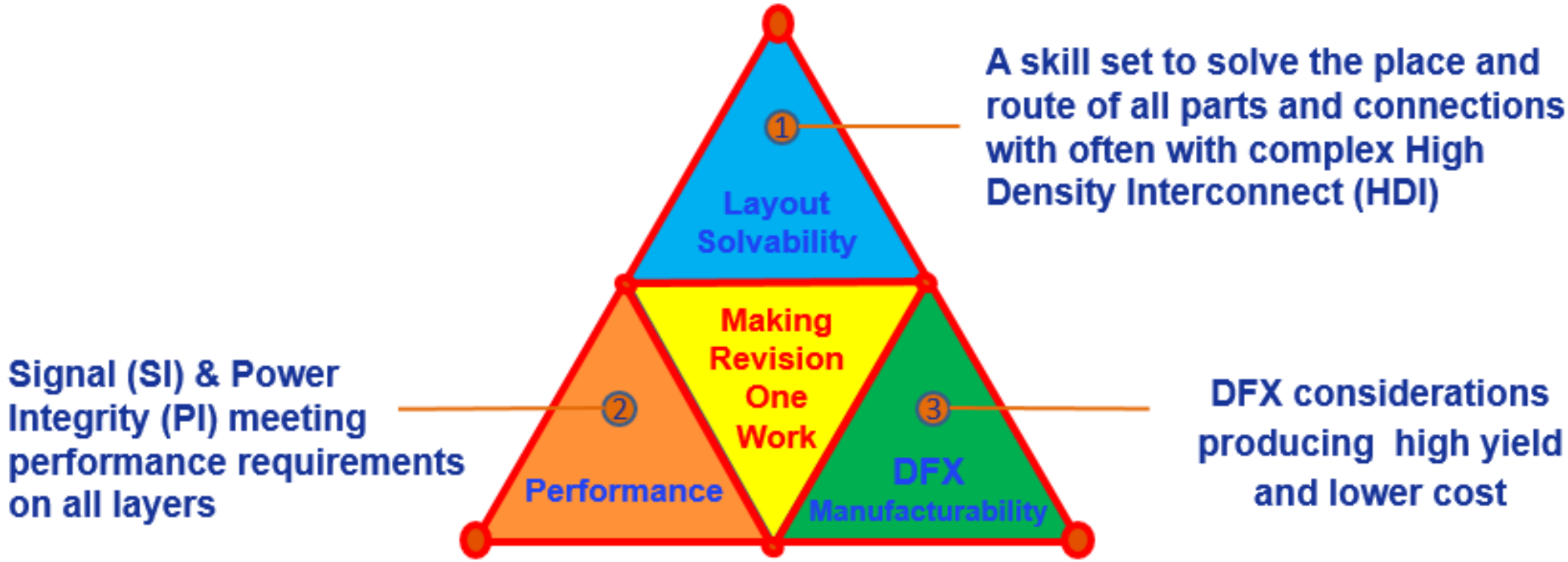
Does it take longer to complete an HDI design?
Typically ***"Yes"*** = You're routing 3D, Z-Axis



Conclusions

As we get ready to show some of the HDI features in Release 19 …

- Software enhancements and industrial automation should increase productivity, accuracy and quality.
- You should always seek to improve your knowledge base and competence with technology trends and seek to be a Master of your software tool!



mike.creeden@sdpcb.com

Thank you for your Attention!

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Questions?

Stay tuned for
Software demonstration
Andrew Mitchell