An AESA Revolution Utilizing the Disruptive Technology of Highly-Integrated Silicon ICs

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Introduction

It is constructive to reflect on the words of Gordon Moore, who said, "The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar." (*Cramming More Components onto Integrated Circuits*, Gordon E. Moore, Life Fellow, IEEE; Proceedings of the IEEE, Vol. 86, No. 1, January 1998)

As will be shown in this paper, silicon is the key to this revolution. In fact, Moore's Law is the reason silicon is so capable at millimeter-wave frequencies today. It brings with it high performance and an impressive array of features—all in highly-integrated IC form.

We will first present an overview of phased-array antenna fundamentals and basic Active Electronically Scanned Array (AESA) principles and challenges, and then we will explain how planar solutions can help with form-factor issues. We will also show how planar solutions at frequencies at or above X-band require increased integration, as well as highlighting some associated challenges.

We will then illustrate how the capabilities of silicon technologies (SiGe BiCMOS, CMOS, SOI) can provide a platform for this integration, while also enabling other performance possibilities. Finally, we will show examples of performance metrics that demonstrate the feasibility of silicon technologies for high-frequency AESAs.

AESAs: Features & Emerging Applications

An AESA is an Active Electronically Scanned Antenna, also known as a phased array antenna. As defined by Robert Mailloux, in his *Phased Array Antenna Handbook*

(Second Edition, 2005 Artech House), "*phased array antennas consist of multiple stationary elements, which are fed coherently and use variable phase or time delay control at each element to scan a beam to given angles in space*." Thus, we have electronically-steered beams with no moving parts.

AESAs are desirable because they are highly reliable, with no moving parts to fail. They have what is referred to as a "soft failure mechanism," meaning that because there are typically many elements in an array, the failure of a few elements typically has little effect on the performance of the AESA as a whole. AESAs can steer beams quite quickly—in microseconds. They can support multiple, simultaneous, independently-steerable beams. With no mechanically gimbaled parts, they are low profile. AESAs are also able to steer nulls, since they have many elements, they have high degrees of freedom to block interferers and jammers. AESAs can also generate precise, radiating aperture patterns.

AESAs are being increasingly used in emerging applications. Traditionally, they have been implemented as brick-style T/R modules, installed orthogonally to the array, typically installed as MMIC/discrete-hybrid assemblies in machined metal housings. These turn out to be expensive, bulky and heavy, and they limit the range of platforms on which they can be deployed.

In contrast, planar solutions have ICs mounted in the same plane, parallel to the array using all surface-mount assembly techniques. This results in a lower-profile antenna, reduced wind drag and detectability, and the reduced size and weight enables tower mounting and smaller platforms, such as UAVs.

The lower cost is also enabling new applications, such as commercial radar, next generation SATCOM and 5G terminals.

Principles and Considerations of AESAs

We will now explore some of the principles and considerations of AESAs.

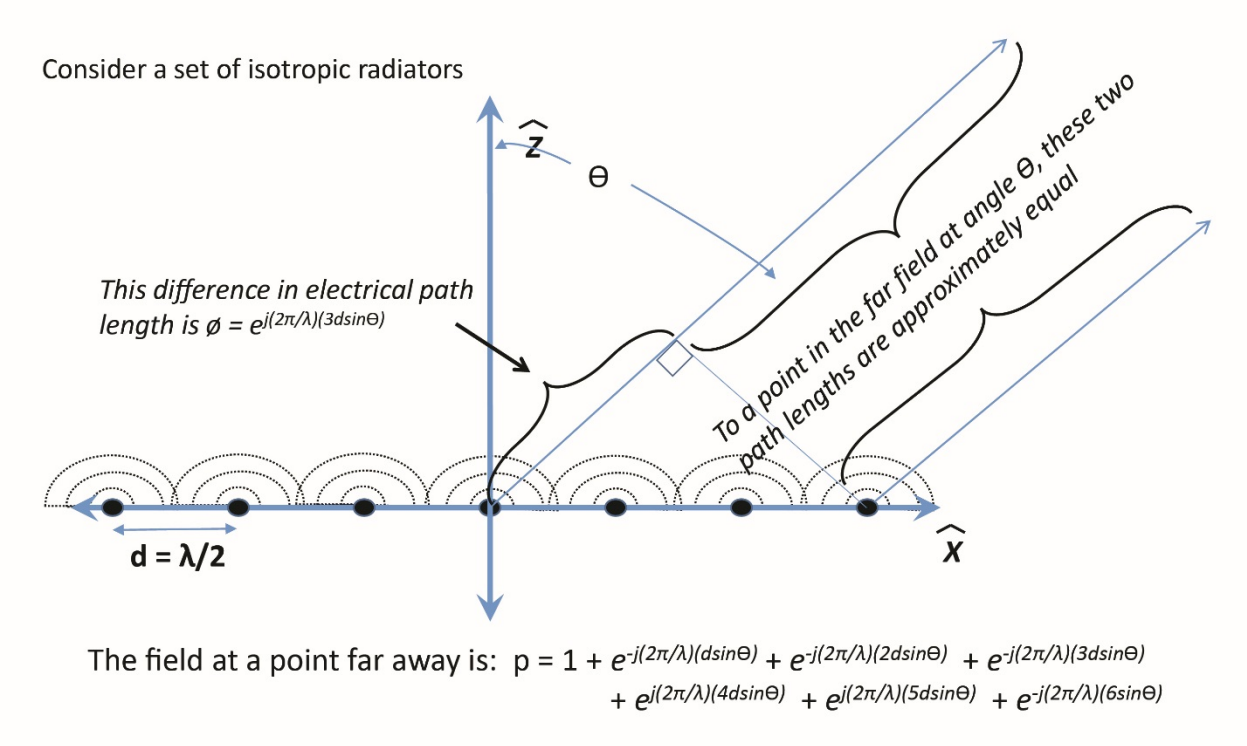


Figure 1: Antenna Pattern Analysis is an Exercise in Complex Arithmetic

The analysis of AESAs is basically an exercise in complex arithmetic. As shown in Figure 1, we have a linear array along the *x*-axis, with the antenna elements spaced by d, which is equal to a free-space wavelength divided by two. If each element is energized by the appropriate phase, then a beam can be formed coherently in the far field at the desired direction.

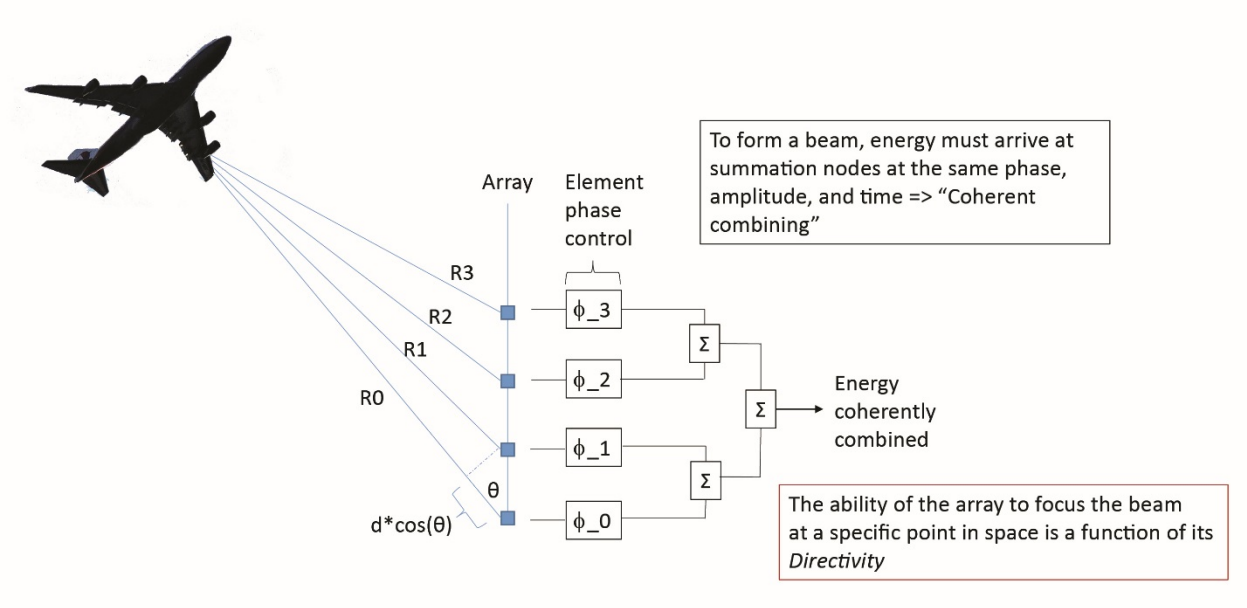


Figure 2: Coherent Summation of Energy – Linear Array

In Figure 2, we take an example of an aircraft target that is not in the boresight direction of the array, such that the range from the aircraft to each element in the array is slightly different. The fact that the elements are spaced at *d* apart, and the angle of arrival of energy from the aircraft is *Θ*, then the incremental path length difference between adjacent elements is *d**cos(*Θ*). To compensate for this difference in path length, we can place phase shifters behind each element. When the appropriate phase shift is applied, we can coherently form a beam in the far field. Remember that to form a beam, energy must arrive at the summation node at the same phase, at the same amplitude, and at the same time. We call this "coherent combining."

Array Directivity and Gain

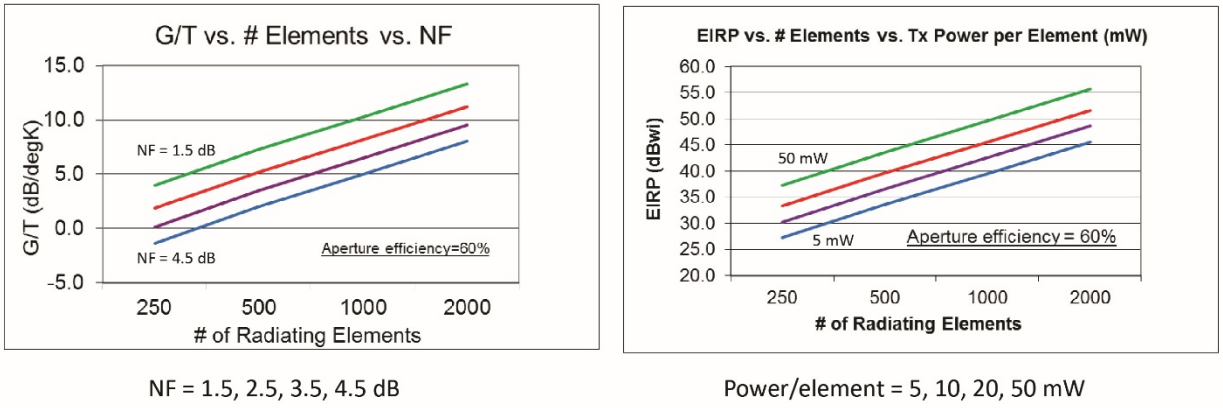
Directivity is the measure of how concentrated the antenna gain is in a given direction relative to an isotropic radiator. It follows a 10*log(N) relationship, where N is the number of elements in the array. Gain, however, takes into account directivity as well as ohmic and scan losses.

So in general, array gain equals 10*log(N) plus the embedded element gain (G_e) minus, the ohmic and scan losses:

$$Array\ gain = 10*log(N) + G_e - L_{OHMIC} - L_{SCAN}$$

G_e is the embedded element gain, which is the gain of a single radiator embedded in the array. Ideally it is hemispheric, but it is typically in the 4–5 dBi range.

Note that for every element added to an array, the G/T of a receiver (Rx) array increases by 10*log(N). You are increasing aperture size, but the noise figure stays constant. In contrast, the EIRP of the transmitter (Tx) array increases by 20*log(N), since for every element you add, you add array gain and transmit power in the far field. It is clear, then, that G/T is much more challenging to achieve with an AESA than EIRP.



NF = 1.5, 2.5, 3.5, 4.5 dB

Power/element = 5, 10, 20, 50 mW

Figure 3: EIRP and G/T Examples

Figure 3 shows two representative curves of how G/T varies with array size and noise figure, as well as how EIRP varies with antenna size and RF power/element. In the graph on the left, we're plotting G/T in units of dB/deg.K vs. the number of radiating elements in the array, and we show a family of system noise figures. Since noise figure is correlated to noise temperature, and temperature is in the denominator of the G/T function, lower noise figure clearly improves G/T of the array.

On the right graph, we have EIRP, measured in units of dBWi vs. the number of radiating elements. The family of curves are different RF powers per element. System engineers typically generate detailed G/T and EIRP budgets that take into

account a wide range of variables, including system noise figure, embedded element gain, frequency of operation, transmit power per element, loss between the element and the T/R functions, scan loss, the effect of polarizers and radomes, and temperature.

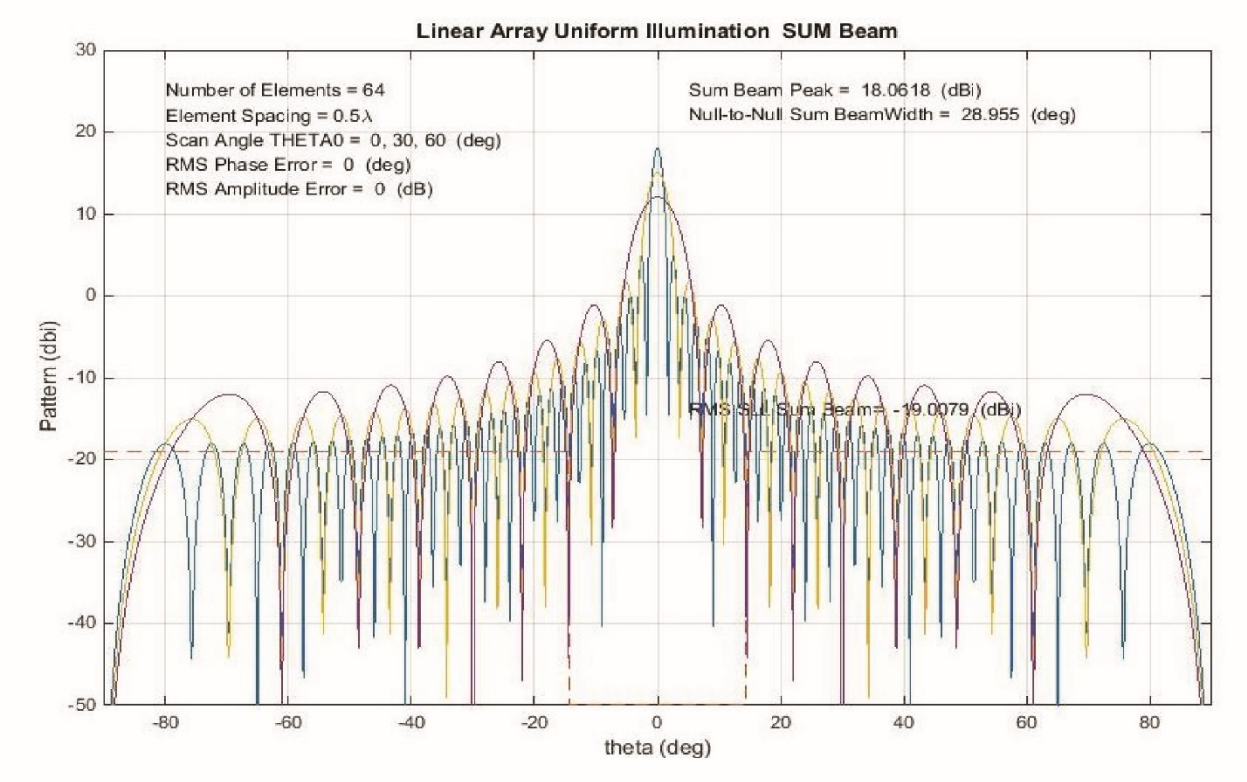


Figure 4: Examples of Uniformly Illuminated Linear Arrays: 64, 32, 16 Elements

Figure 4 shows some examples of linear arrays, specifically 16, 32, and 64 elements. The graph shows main lobes and side lobes. The antenna directivity follows 10*log(N), as we've established previously, where N is the number of elements in the array. Every time we double the size of the antenna, the beam width halves. And every time we double the size of the antenna, the directivity doubles, or increases by 3 dBi.

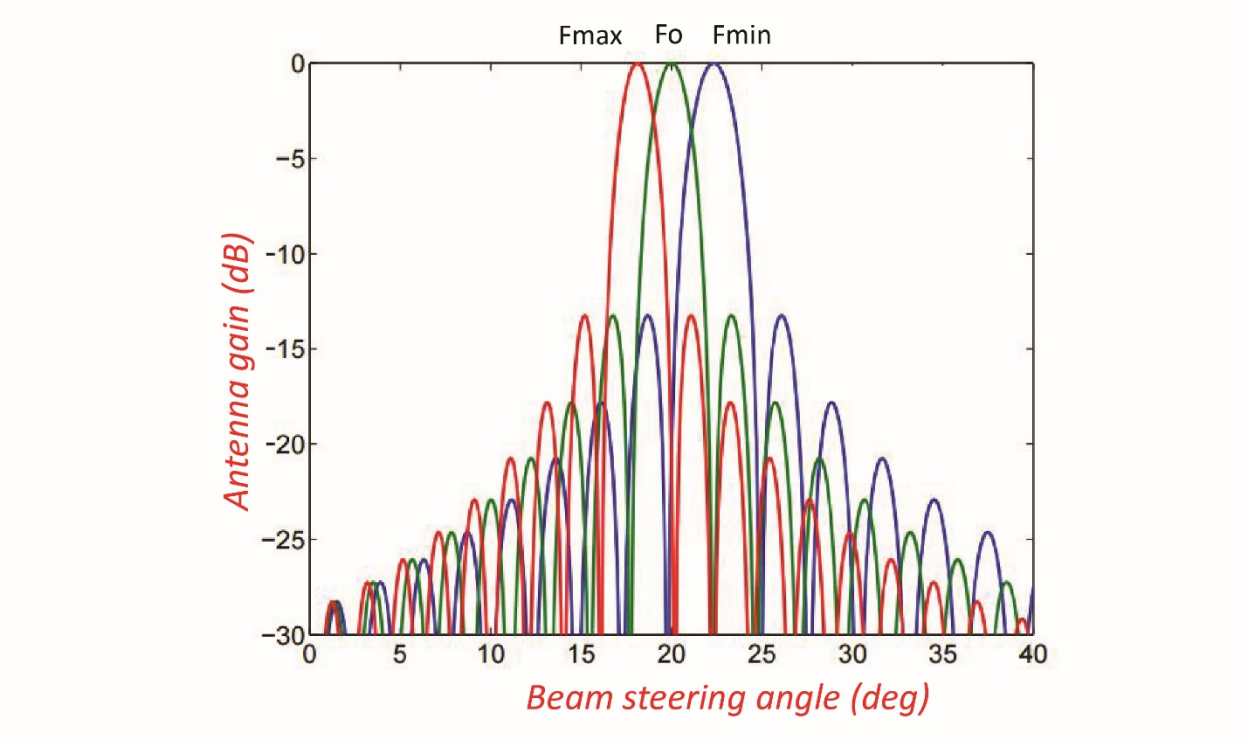


Figure 5: Beam Squint

One of the characteristics of using phase shifters to steer beams of an AESA is called **beam squint**. Phase shifters electrically steer a beam by approximating time delay. The result is that they only steer the beam perfectly at the center frequency; they understeer at the maximum operating frequency, and they oversteer at the minimum operating frequency. Yet phase shifters are preferred over time delay functions, because of the tradeoff between accuracy and circuit size. In fact, phase shifters provide good accuracy for almost all AESA applications, with the exceptions being very wide instantaneous bandwidth applications, such as EW, or for very large arrays.

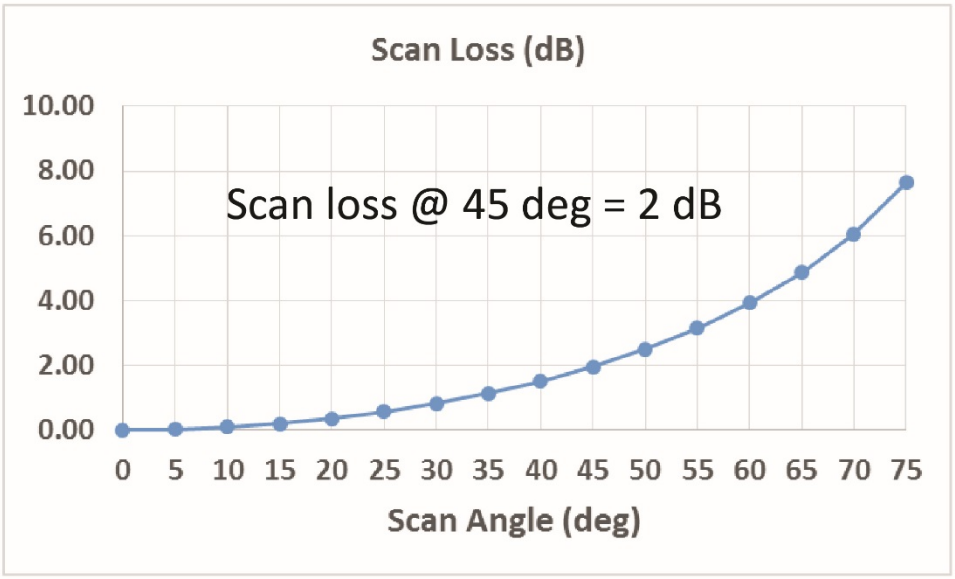


Figure 6: Scan Loss

Another characteristic of all AESAs is called **scan loss**. This is the loss of aperture gain as the beam is steered away from the boresight direction, defined as Θ=0. Scan loss follows $10*\log(\cos^N(\Theta))$ power where Θ is the scan angle and N is a numeric value, typically in the 1.3 range, which accounts for the non-ideal isotropic behavior of embedded element gain.

Figure 6 plots scan loss in dB vs. scan angle, measured in degrees. Note at the origin, where the boresight angle is zero, there is no scan loss. As the scan angle is increased to 45 degrees, there is now 2 dB scan loss. If you increase scan angle to a practical limit of 60 degrees, there is 4 dB scan loss. AESAs must therefore be oversized to provide the required G/T and EIRP under maximum scan conditions. Scan loss is a significant parameter that must be considered in phased array.

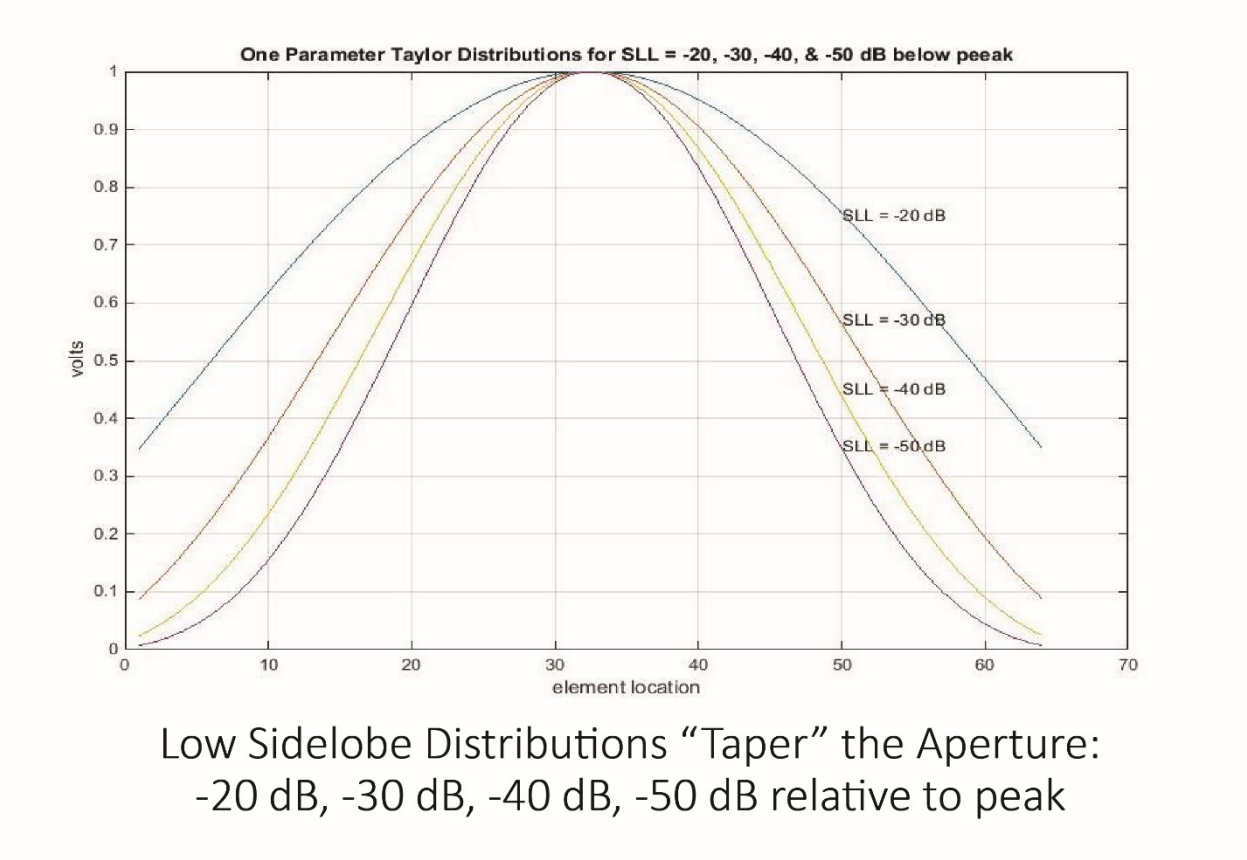


Figure 7: Tapering vs. Side Lobe Level

Tapering is the process of assigning different gains to the various elements within the array, where the center elements are assigned the highest gains, and the outer elements are assigned lower gains. Figure 7 illustrates how various levels of taper can be achieved in an AESA. The example is a 64-element array, so that the maximum gain of each curve occurs at element 32 which is the center of the array. Note that the more quickly that the element gain is reduced as the elements get farther from the center of the array, the greater the suppression of side lobes. The graph shows us the effect of side lobe levels of -20, -30, -40 and -50 dB.

This is why beam forming typically includes amplitude control per element, not just phase control. If all elements are treated with the same gain, it is called "uniform illumination." Uniform illumination results in -13 dBc first side lobe levels, which may be unacceptable for some applications due to regulatory, interference or stealth reasons.

So gain control allows the AESA system engineer to adjust the gain per element to achieve the desired lower side lobe levels.

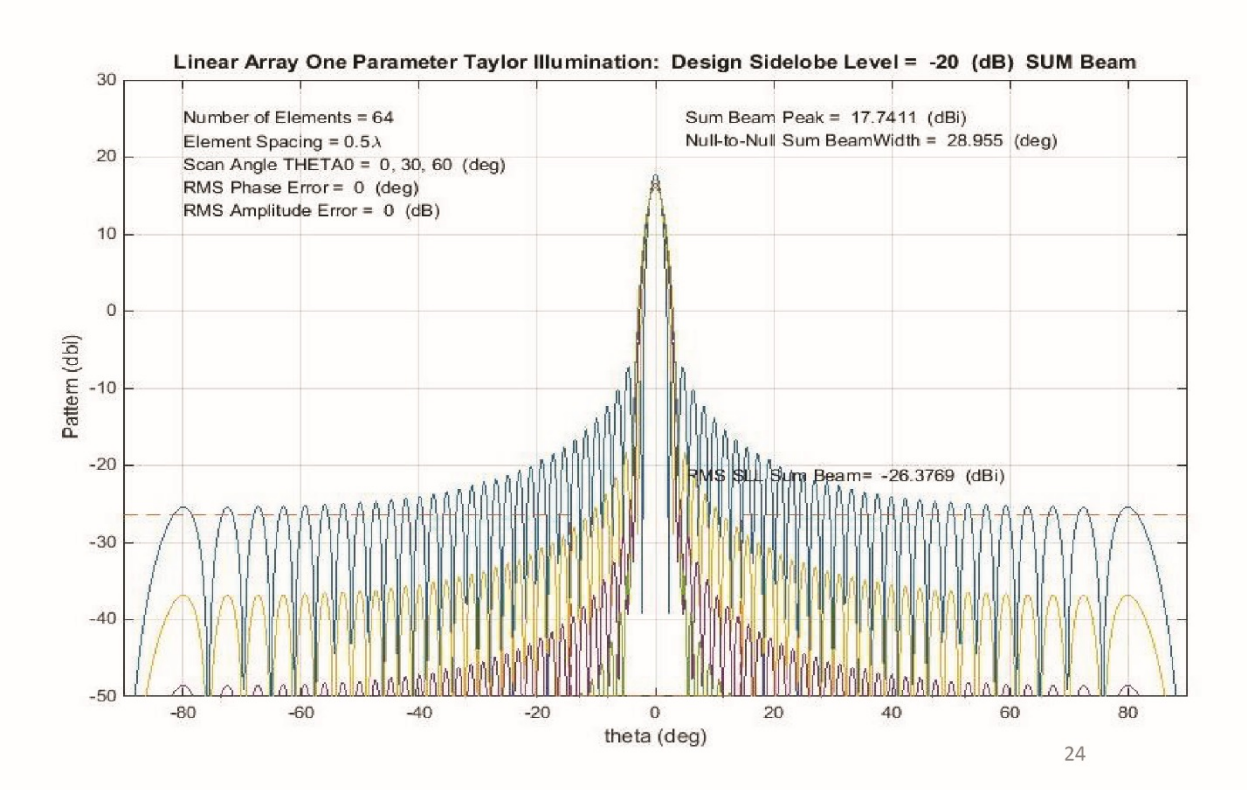


Figure 8: Sample Taylor Distributions: -20 dB, -30 dB, -40 dB, -50 dB Relative to Peak

Figure 8 shows superimposed side lobe levels for various amounts of applied taper, specifically -20, -30, -40 and -50 dB, relative to the peak. Observe the side lobe level suppression, caused by the applied taper. This is a 64-element array with a directivity of 18 dBi.

Although this example shows taper being applied, note that many radar applications prefer uniform illumination on transmit, as it results in maximum power delivered to the far field and maximum range.

At Anokiwave, we typically provide gain controls at the element in the 0–31.5 dB range, in 0.5 dB steps, which is generally sufficient to provide for amplitude taper and other host system control needs. A final note is that taper does not change with scan angle.

Desired SLL dB (wrt peak)	*B*	*D – Directivity (dBi)*	*η – Efficiency (dB)*	$B_{null\text{-}to\text{-}null}$
-13.26	0	18.06	0.0	3.6
-20	.7386	17.74	-.32	4.5
-30	1.2762	17.05	-1.01	5.8
-40	1.7415	16.51	-1.55	7.2
-50	2.1793	16.08	-1.98	8.1

Table 1: Values of B for desired sidelobe levels in One Parameter Taylor Distributions

Taper can be a good thing, but it does come at a price. The directivity is less than uniform illumination for the same size array, and the beam widths are broader. Table 1 shows a range of different tapers applied. The top row is the uniform illumination with -13 dBc side lobes as previously described. Shown below are rows for -20, -30, -40 and -50 dB side lobe levels. Note that their directivity is dropping, and the efficiency is dropping. So if you apply -50 dB taper, you've lost a full 2 dB efficiency on your array.

Another characteristic of AESAs are **grating lobes**, which are primarily affected by lattice spacing—the spacing between elements (variable d). In order to avoid parasitic grating lobes, which are antenna responses in undesired beam directions, the lattice spacing must follow these rules:

$d/\lambda_o < 1/(1+\sin\Theta)$ for a rectangular lattice (Min. spacing = 0.5 λ_o at 90 deg scan)

$d/\lambda_o < 1.15/(1+\sin\Theta)$ for a triangular lattice (Min. spacing = 0.575 λ_o at 90 deg scan)

Where λ_o is the free space wavelength, Θ is the max scan angle, and *d* is the spacing between antenna elements.

Note that a triangular lattice allows element spacing to be 15% greater than a rectangular lattice. This is important because it creates more room for electronics within the lattice spacing. Since we are focused on planar arrays, more real estate is a good thing. It also lowers array cost, since fewer T/R ASICs are required for a given aperture size.

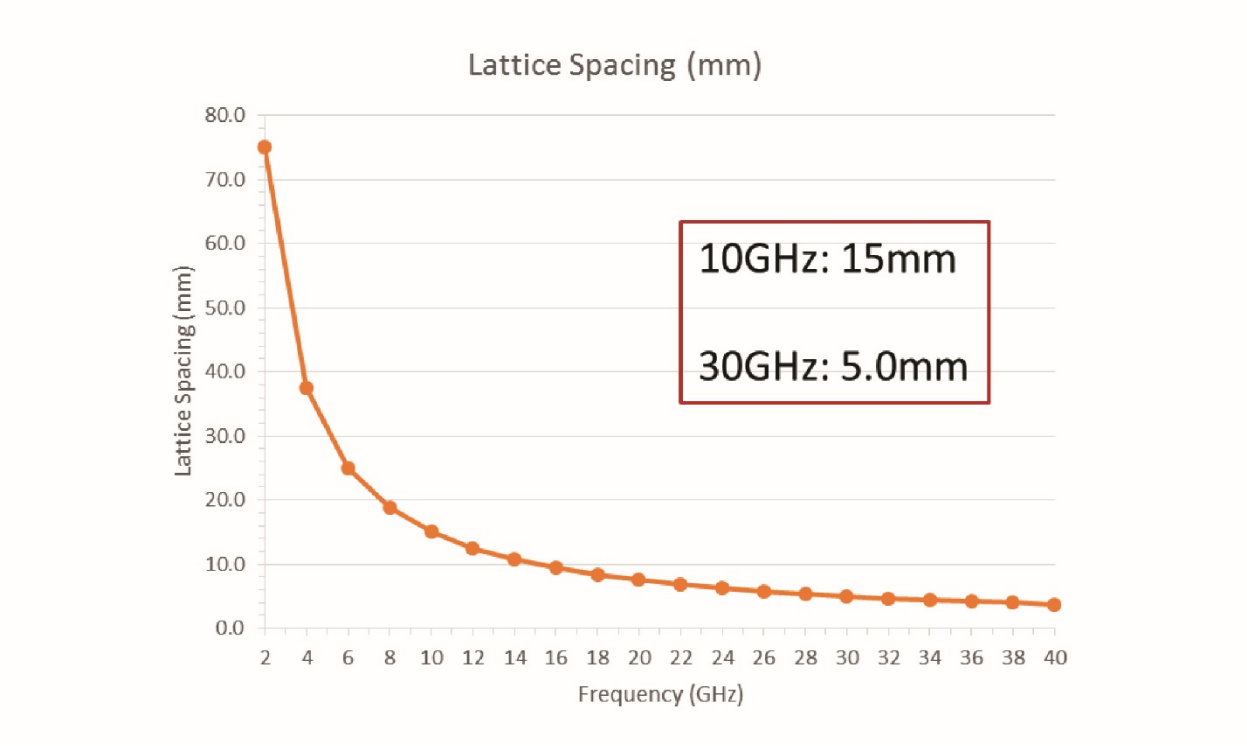


Figure 9: Lattice Spacing Example Calculation

Figure 9 shows that required lattice spacing is a function of frequency. The graph plots lattice spacing in millimeters vs. frequency of operation in GHz. Note that for lower frequencies, large lattice spacing makes planar AESAs not very challenging. But look what happens at X-band (8-12 GHz) and above—the lattice is rapidly contracting, which leaves very little room for the T/R functions and beam forming electronics.

This is where the high level of integration with silicon is critical. The example here shows that at 30 GHz, 5 mm lattice spacing is required, which is very compact and tight. Only silicon can provide this kind of solution.

Silicon and AESAs: Form Factors & Integrated vs. Discrete Implementations

We will now examine in more detail where silicon can be used in AESAs and why it can be described as a disruptive technology.

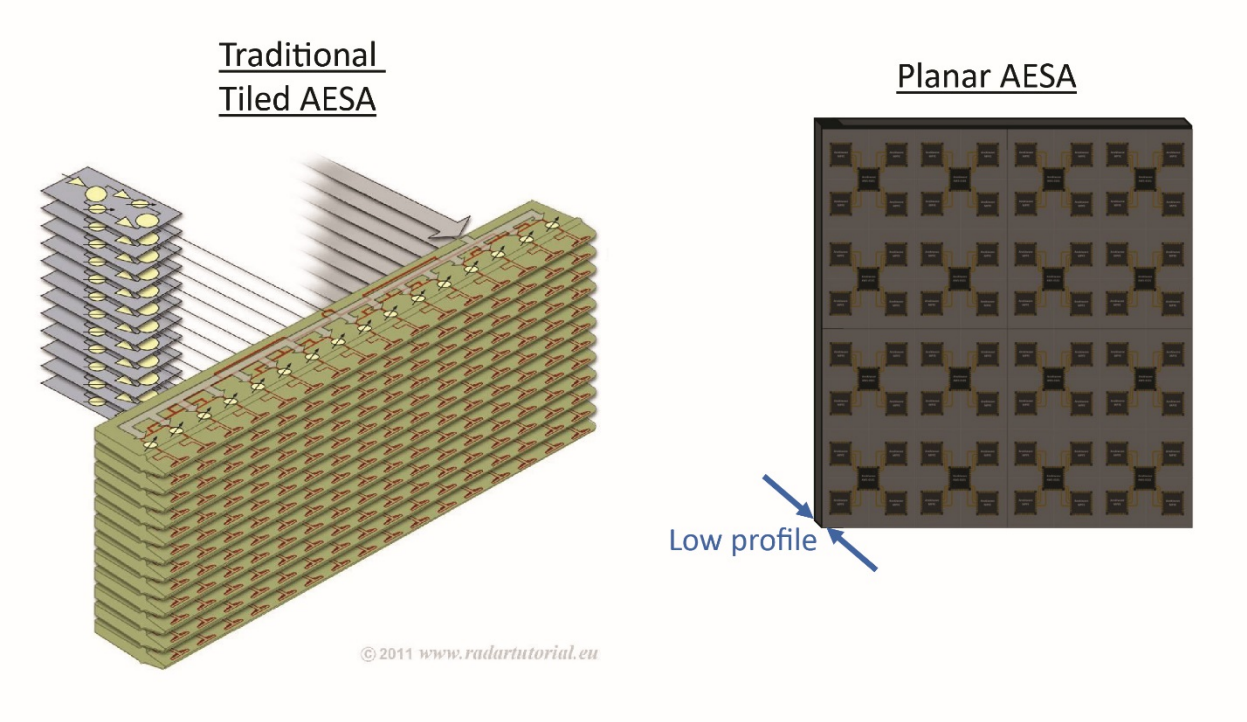


Figure 10: AESA Form Factors

AESAs are not new – they have been built for more than 50 years, but almost exclusively for aerospace and defense applications. The illustration on the left side of Figure 10 shows an example of traditional AESA construction. The antenna consisted of a number of circuit cards installed orthogonally to the antenna array, each of which feeds a row of radiating antenna elements. These are fed in-turn by individual T/R (transmit/receive) modules, mounted in the plane behind the circuit cards. The large size of the T/R modules means it is difficult to easily reduce the size of the AESA.

In contrast, the image on the right side of Figure 10 shows how a planar solution might look. Here, the radiating antenna elements are placed on one side of the circuit board, and all of the beam forming electronics are mounted on the reverse

side of the panel between the antenna elements. This means the aperture will actually be low profile, which makes handling the array much simpler and much more flexible in how and where the antenna can be mounted.

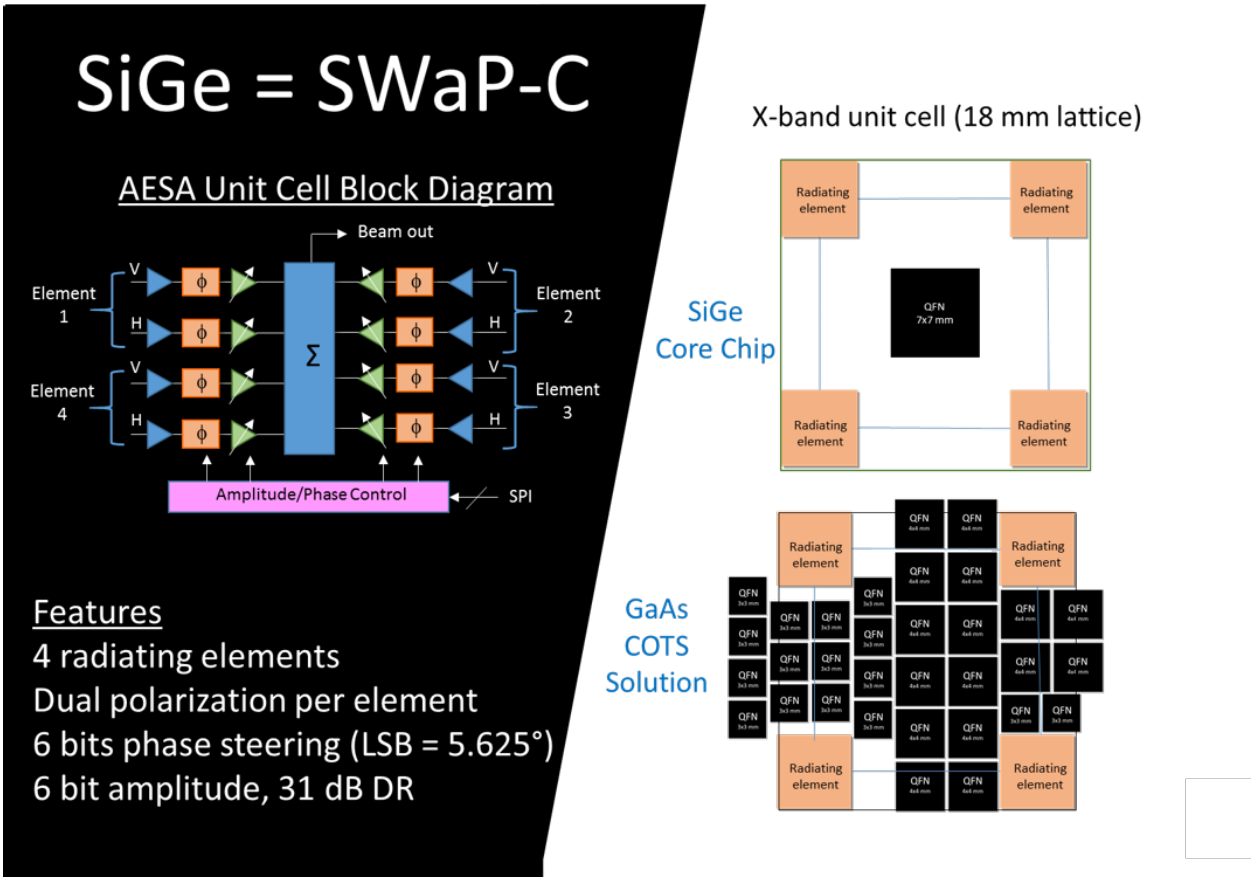


Figure 11: Integrated vs. Discrete AESA

The traditional approach requires a separate T/R module for every radiating element in the array. This means typically that at a minimum, we would require a discrete LNA, a PA or driver amplifier, plus control components for each and every element. If we simply try to design a planar solution using this approach, we end up with the situation shown on the bottom right in Figure 11, where the required components simply do not fit in the allowable space. As you can imagine, as the frequency increases and the spacing between antenna elements gets smaller, the problem just gets worse.

The obvious solution to this problem is to integrate more functions into a single IC, which reduces the number of required parts. The optimal amount of integration is

debatable, but it's clear that if all of the required beam forming circuitry could be included in a single IC, then the floor-planning problems would become significantly easier. This is shown in the upper right of Figure 11, and we will look at additional examples later in this paper.

But if every element needs all of these components, then we're talking about dense integration. And the ability of III-V technologies to do this becomes more challenging. Silicon, though, with its small feature size and multiple metal layers, becomes a more viable candidate as a solution to this problem.

As we are all aware, silicon has been making substantial progress over the last decade in terms of moving higher and higher in frequency. There are many commercial products now in production up to 80 GHz that use silicon ICs for low RF power applications. Which silicon technology you choose, whether it's SiGe BiCMOS, bulk CMOS, or SOI CMOS usually depends on considerations of volume, the price target, and of course, the required performance.

In terms of performance, it's interesting to note how over the last few years, the NF_{min} of many silicon technologies has improved to the point where they are now competitive with GaAs for many applications. For example, there are several commercial technologies available that have typical minimum noise figures of 0.4 dB to 0.5 dB at 10–12 GHz, meaning an LNA noise figure would be within tenths of a dB of a comparable GaAs part.

And this means that for many applications where the required EIRP is relatively low – for example many telecom and SATCOM applications – an all-silicon AESA array can be built.

Silicon Integrated Beamformers

In those applications where high conducted power is needed, then the array can be realized using a common silicon beamforming chip, and a minimal III-V front end, whether that's GaAs or GaN. And the crux of being able to do this, of course, is the ability to integrate all the required beamforming circuitry within a single IC. An example is shown in Figure 12.

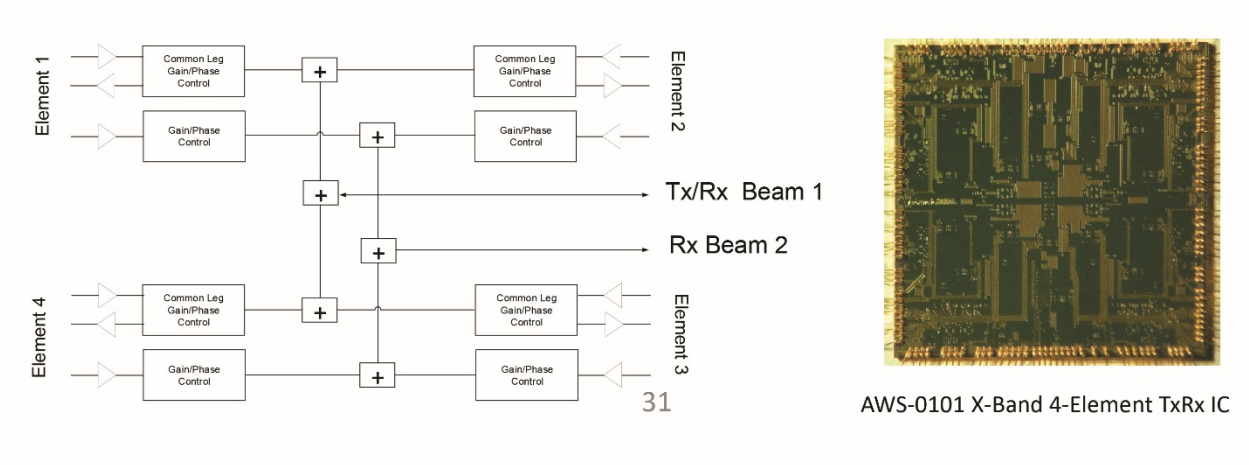


Figure 12:Silicon Integrated Beamformers

Figure 13 presents an example of **an all-silicon array**. On the left is an example of a PCB for a 256 element K-band AESA for SATCOM applications. The antenna element is a fed from a silicon core chip that supports dual polarization for four radiating elements, meaning that the entire array requires only 64 silicon core chips. The eight antenna feeds per IC is shown in the center along with a superimposed patch element to show the relative dimensions. Because the beamformer is polarization-flexible, the array can support either dual linear polarization or right-hand/left-

hand circular polarization by feeding the radiating elements with signals in the correct quadrature relationship. The total aperture size here is approximately 10 cm^2.

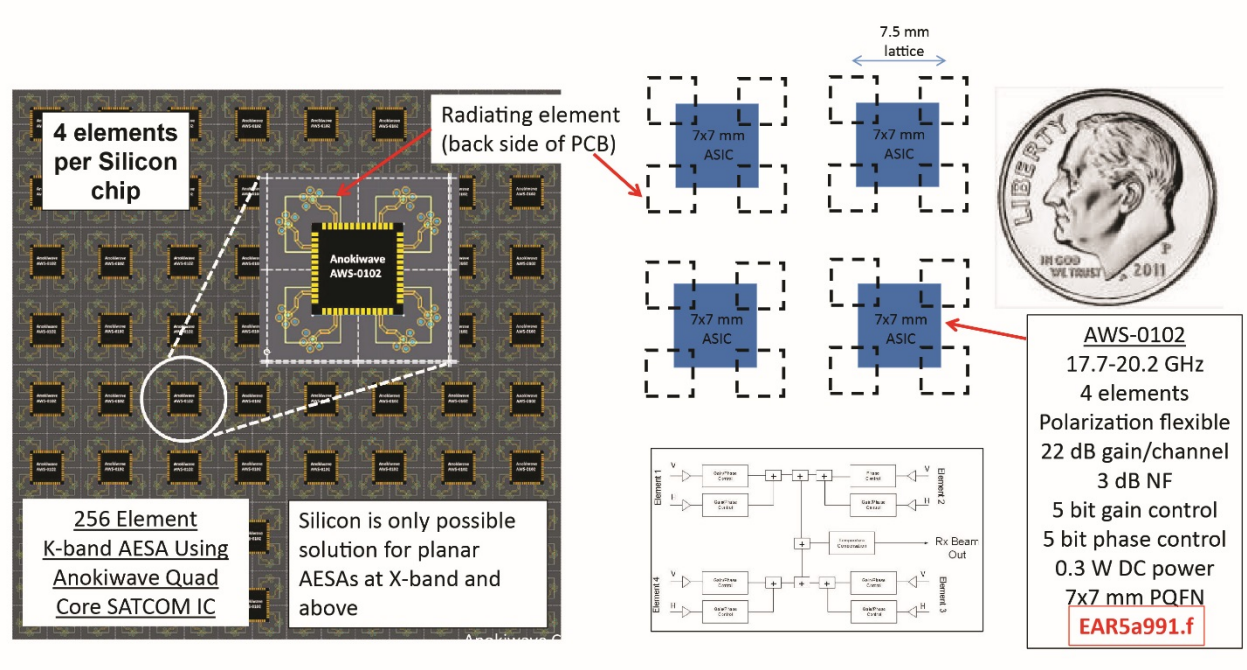


Figure 13: All Silicon Array

Looking at the right side of Figure 13, the challenge of integrating this functionality into such a small area becomes clear. The allocated K-band spectrum for space-to-earth communications is 17.7–20.2 GHz. The lattice spacing between elements at 20 GHz is only 7.5 mm. For comparison, the image of the U.S. dime in the figure is shown to scale.

Fortunately, the required functionality easily fits. The beamformer core IC includes LNAs, independent 5-bit vector-modulators for all eight receive channels, plus coherent combining as well as all signal control. Noise figure for each full receive chain is <3 dB, including the loss of the package. The total power dissipation is about 300 mW from a 1.8V supply. It's difficult to conceive of 8 fully-independent, steerable channels in such a small area using traditional GaAs-based approaches. But as we'll see, even denser functionality is possible.

The other factor to note here is that the package is a standard, commercial surface mount QFN-type plastic package.

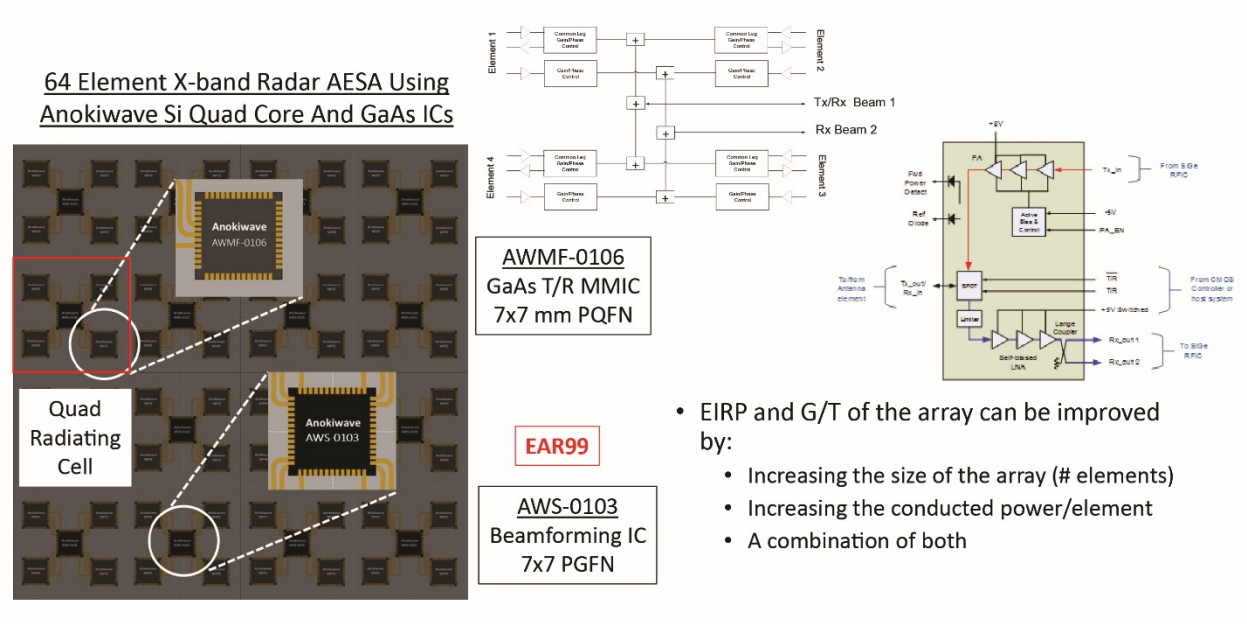


Figure 14: EIRP enhanced array

Figure 14 shows an example with both transmit and receive functionality on the same die. As indicated earlier in the paper, with many radar applications, the EIRP is limited, and therefore the performance is limited by the amount of energy that can be illuminated on the target.

So for some applications, it is necessary to take advantage of the ability of GaAs or GaN to generate higher conducted power at the radiating elements to increase the EIRP per cm^2 at the antenna aperture.

We still have to address spacing requirements between radiating elements at the antenna, due to grating lobe restrictions, meaning that we need to integrate as much of the beam forming electronics into a single chip as possible.

The left side of Figure 14 shows a 64 element X-band planar AESA, again using quad-core chips for all of the beam forming functions, as well as a GaAs T/R MMIC mounted at each radiating element to increase the conducted power to around 4W per element. The entire AESA array is comprised of 16 silicon beamformers and 64 GaAs T/R MMICs, with the total size of the array aperture approximately 10 cm^2.

Note that the beam forming IC here, as well as including 8 independent receive channels, also includes four full transmit chains with driver amplifiers to deliver +15 dBm conducted power to drive the input of the GaAs MMIC.

Despite this additional functionality, plus being lower in frequency, the beamformer IC is still contained within that same 7x7 mm QFN package we saw for the 20 GHz example in Figure 13.

The noise figure of the receive chains is comparable, whether the LNA is realized in silicon or GaAs. So for applications that can work with a lower amount of EIRP per elements, the beam forming IC shown here comes in two versions: one with a low-noise, high-gain LNA included so you can build an all-silicon array, and a second with a lower gain receive path that would utilize the LNA included in the GaAs front-end

Channel Isolation Limitations & Requirements

Of course, the law of unintended consequences tells us that we don't get anything for free. As we move down the path of increased integration and compaction, we must suffer some degradation in performance as a result. The area of greatest concern for the beamformer is the ability to maintain adequate isolation between the independent channels. Unwanted coupling paths between the channels could either be on the board, in the package or package transitions, or through signal paths on the IC itself.

Regardless of the source of the coupling, the effective degradation to the channel-to-channel isolation is the same. A random error vector is introduced and superimposed onto the designed phasor, resulting in a corruption of the desired signal. The net effect of this is to limit the accuracy available from the vector modulator and therefore place an upper limit on the resolution of the number of bits that can be used in the beam steering.

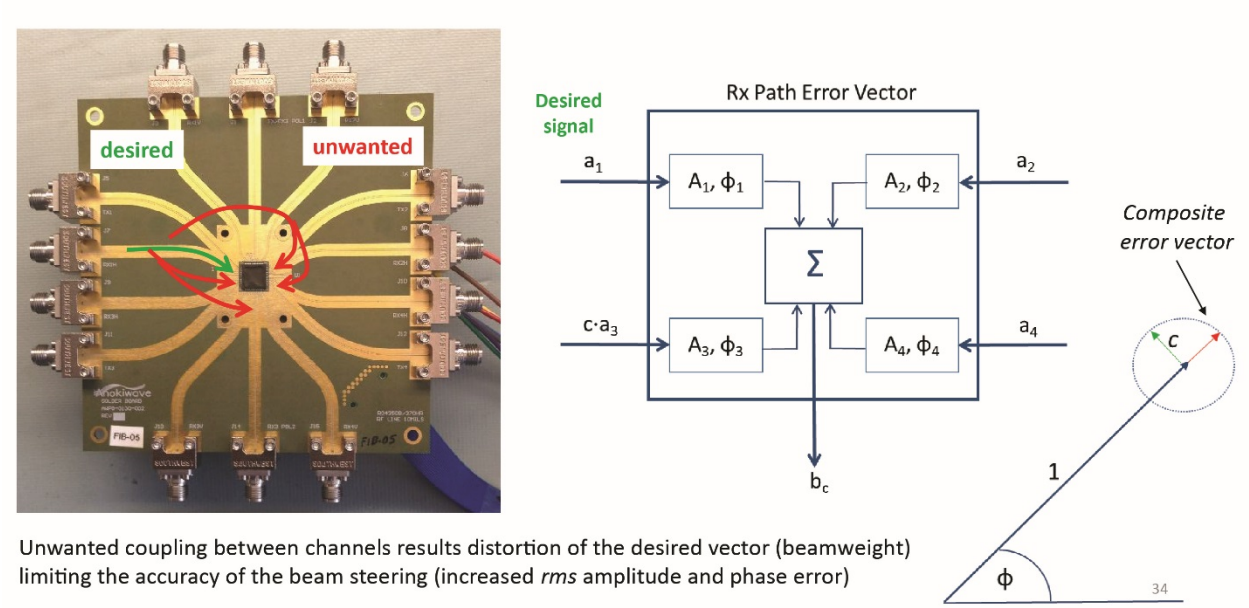


Figure 15: Channel Isolation Limitations

We can consider this effect by considering the simplistic diagram shown in the right of Figure 15. If we consider the desired signal a_1 injected into the beamformer, and we choose a particular magnitude imposed on it by its vector modulator, in an ideal case, if no signal were present from the other boards, then the signal at the output of the combined board would be a representation of the desired phasor.

In reality, there will be some signal leakage through complete paths of all of the input ports, as well as limited isolation between single paths in the IC itself. Each coupling path will have some complex representation, amplitude and phase associated with their transmission characteristic. But for the sake of simplicity, let's assume that they all combine to produce a composite error vector which is added to the desired signal.

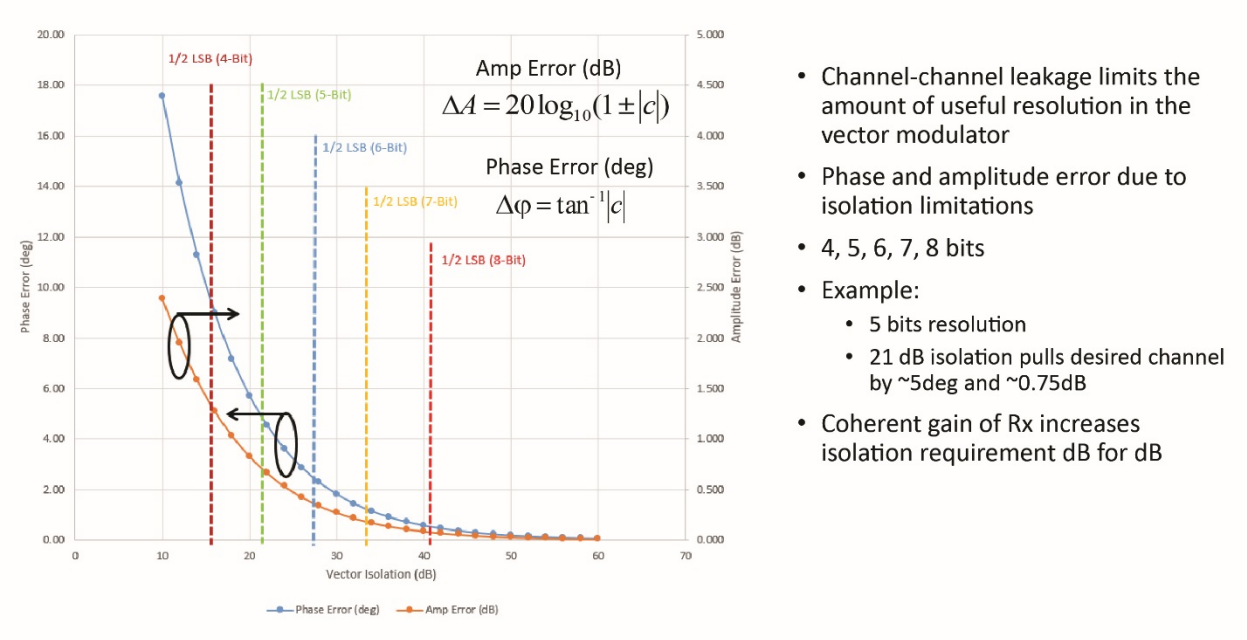


Figure 16: Channel Isolation Requirements

The graph in Figure 16 represents the resulting maximum phase and amplitude error due to that unwanted coupling. If we restrict the maximum allowable error to be less than the least significant bits of the vector modulator, we can determine the level limit for the channel-to-channel isolation requirements. The graphs shows phase error in degrees plotted on the left vertical axis and amplitude error in dBs on the right.

You can see that in order to maintain 5-bit accuracy, for example, we need to maintain a minimum channel-to-channel isolation of around 21 dB. Remember, this is a composite isolation, so the minimum number should really be somewhat higher than this. However the composite error vector assumed in this calculation also assumes worst case coherent combining of all the leakage paths.

The last point to make about this plot is that it does not account for the coherent gain inherent in the receiver. So as the coherent gain of the receiver increases, the minimum isolation requirements will also increase—dB for dB.

Anokiwave X-Band Silicon Quad Core IC (AWS-0103/AWS-0101)

We've seen how increasing the integration level is a pathway to a planar AESA, now we will look in more detail at the X-band quad beamformer.

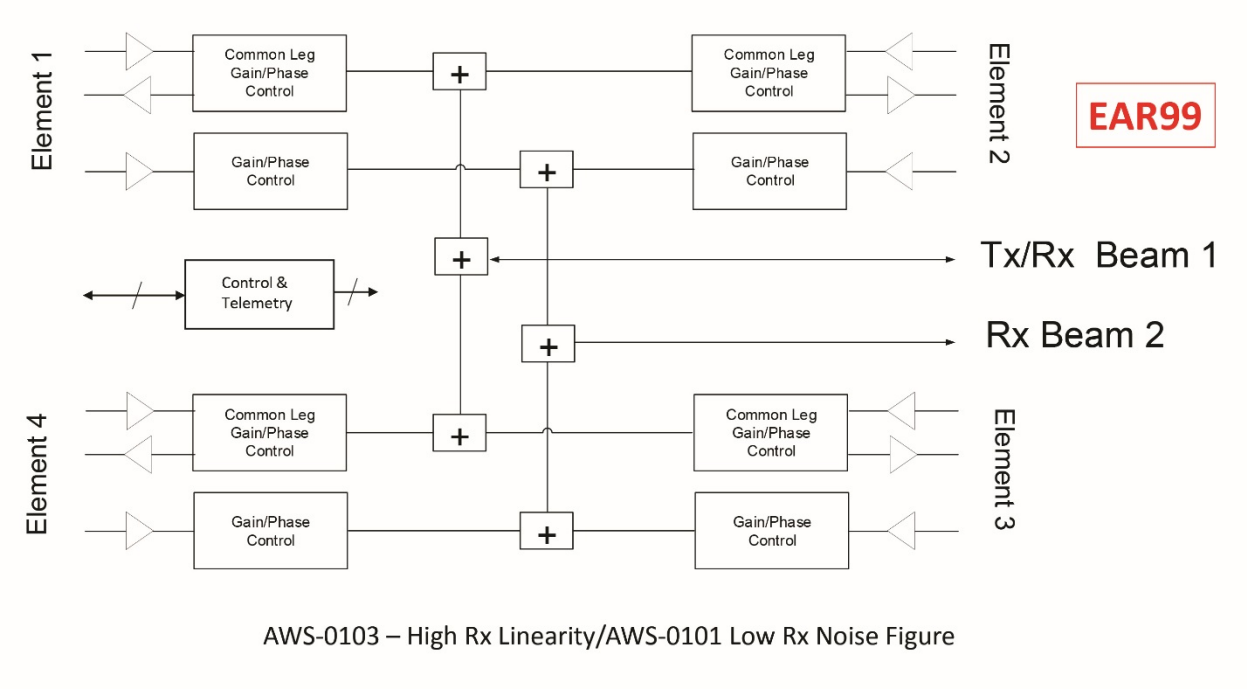


Figure 17: X-band Beam Forming ASIC

Figure 17 shows a top-level block diagram of the X-band quad beam forming ASIC. As mentioned above, this part is available in two versions: a high-receive linearity power feed with a III-V front end, and a high-gain, low noise figure version for use in an all-silicon array. The schematic block diagram of both versions is exactly the same. The quad IC supports four radiating elements, four channels on transmit, eight channels on receive, each of which has independent beam steering. There are two common RF beam forming ports, one of which is shared in time-duplex fashion with a transmitter.

When sending a transmit waveform, the signal is input to the common beam port, split two ways, and then split a second time to give us four transmit signals. After passing through the vector modulators, each path is amplified to a level of about

+15 dBm, which can be used to either drive a high-power III-V stage or used directly at the elements for an all-silicon array.

In receive mode, we have two independent receive paths providing the ability to either do simultaneous processing of orthogonal linear polarizations, or multiple sample processing of the same receive signal. The receive signal paths are coherently combined in two separate combiners and output from the chip to enable the next level of RF signal combining at either the sub-array or the array level.

In addition, there is a control and telemetry block that supports two-way communication over a digital SPI interface, as well as providing and enabling a set of controls for the RF vector modulators. The telemetry block also outputs diagnostic data from on-chip power detectors and temperature sensors. Power detection at all transmit ports as well as local temperature sensing, is sampled, digitized on-chip and then made available to the host system.

A note about vector modulators and the **complex beam weighting** used to steer the Rx and Tx beams. Each vector modulator within the IC used for beam steering can be independently controlled in both amplitude and phase within 6 bits of precision. That means 12 bits per vector modulator: 6 bits amplitude and 6 bits phase and a total of 96 bits for the entire beamformer. Six bits of phase modulation control implies least significant bit of 5.625 degrees. And the six bits of amplitude control uses the least significant bit of 0.5 dB, resulting in almost 32 dB dynamic range of aperture control.

As mentioned previously, amplitude control is useful for an array taper to give added flexibility for control of side lobes for regulator emissions compliance.

Preliminary Measured Data for the X-Band Silicon Quad Core IC: AWS-0103

Polar Constellations. A convenient way of looking at the characteristics of the vector modulator is to plot the output of the normalized polar plots, shown in Figure 18 at a spot frequency of 10 GHz. This plot comprises 4096 states, consisting of every combination of the 32 phase states and the 32 amplitude states. It is

visually more useful than an inspection of the linear plots, because it also captures cross-distortion behavior. The ideal characteristics should look like spokes on a wheel, with the linear radial arms at the outer edge of the circle. If the radial lines are linear, that indicates low AM/PM distortion.

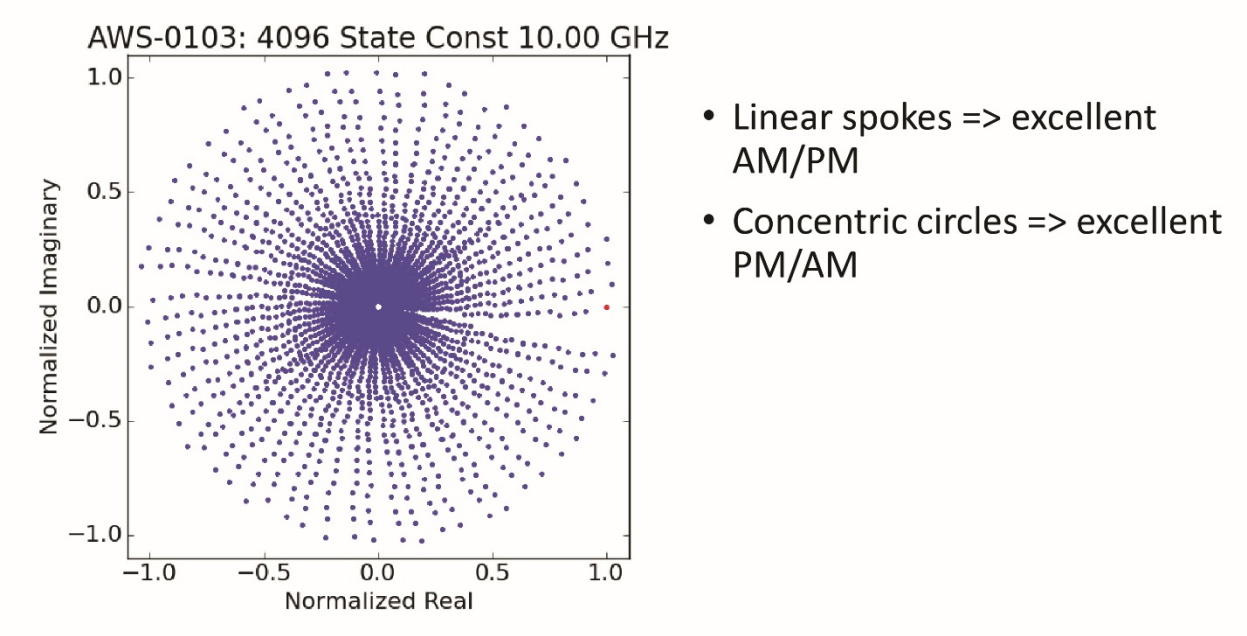


Figure18: Polar Constellations – All Amplitude & Phase States

Likewise if the circles move from the inner edge to the outer and are concentric in their alignment, then the PM/AM distortion is low.

It should be noted that Figure 18 uses raw, uncorrected data that does not include any calibration or correction that would typically be done at the array level. Therefore, we can get a good indication of the accuracy of the vector modulator simply by reviewing the RMS **phase and amplitude error** data, as shown in Figure 19.

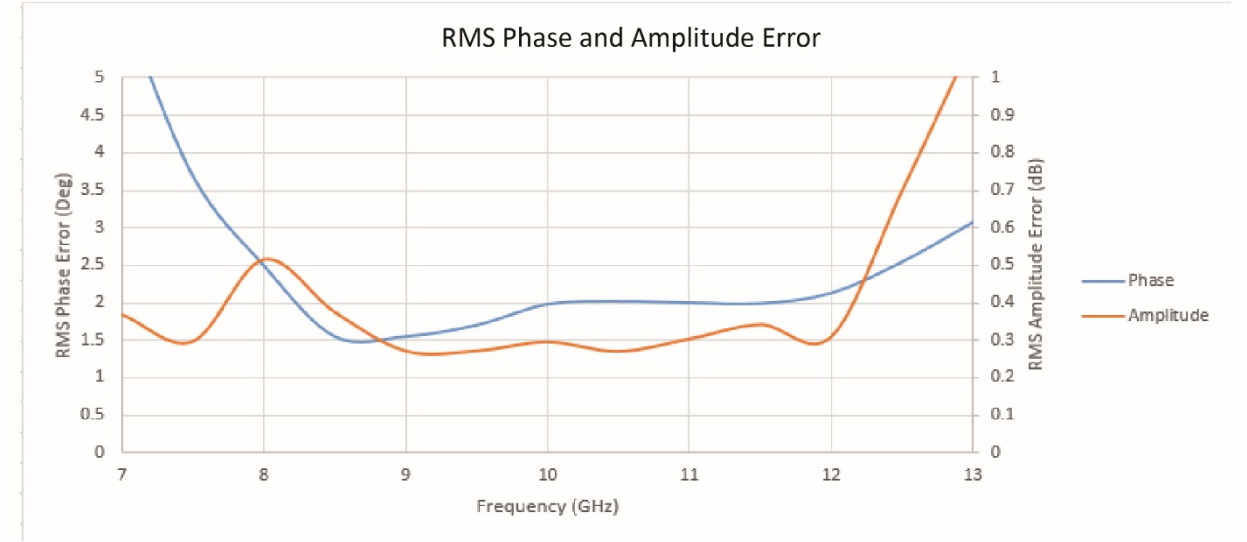


Figure 18: Phase and Amplitude Errors

These results are for a single channel, but as we've seen, the channel consistency across the four quadrants is very good. The X-axis here shows frequency from 7–13 GHz, X-band being 8–12 GHz. RMS phase error is plotted in blue on the left Y-axis, with RMS amplitude error in orange on the right. The RMS phase error is approximately 2 degrees over the 8–12 GHz interval, while the RMS amplitude error is maintained around 0.3 dB across the same bandwidth.

Conclusion

To conclude, we've seen how in order to build and manufacture truly planar AESAs, we need to integrate all of the required beam forming and beam steering electronics, parallel to the antenna and fit between the radiating elements. This becomes increasingly difficult at X-band and above, due to the shrinking dimensions of the lattice, which is a direct function of the wavelength.

One way to achieve this is from a single IC combined with beam forming functions for multiple elements so the AESA can either become an all-silicon array or with the number of external components reduced to a minimum.

We've also seen that the key performance metrics (noise figure, beam steering accuracy, channel-to-channel isolation) are all possible in silicon ICs, even when mounted in low-cost, commercial plastic packages. And this is important, because

emerging applications—especially next generation SATCOM and 5G applications—need AESA technology at commercial and consumer price points in order to be successful.