# An Analysis of the Cost and Performance of Photovoltaic Systems as a Function of Module Area

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**Technical Report**
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April 2017

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# Abstract

We investigate the potential effects of module area on the cost and performance of photovoltaic systems. Applying a bottom-up methodology, we analyzed the costs associated with mc-Si and thin-film modules and systems as a function of module area. We calculate a potential for savings of up to $0.04/W, $0.10/W, and $0.13/W in module manufacturing costs for mc-Si, CdTe, and CIGS respectively, with large area modules. We also find that an additional $0.04/W savings in balance-of-systems costs may be achieved. However, these savings are dependent on the ability to maintain efficiency and manufacturing yield as area scales. Lifetime energy yield must also be maintained to realize reductions in the levelized cost of energy. We explore the possible effects of module size on efficiency and energy production, and find that more research is required to understand these issues for each technology. Sensitivity of the $/W cost savings to module efficiency and manufacturing yield is presented. We also discuss non-cost barriers to adoption of large area modules.

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# 1 Introduction

Area-based economies of scale have been demonstrated in manufacturing of several different technologies, including flat panel displays, coated glass for architectural applications, and wafer-based semiconductor processes. With solar photovoltaic (PV) technology, the vast majority of modules remain relatively small, within the range of 1 to 2 $m^2$; however, several companies have attempted to leverage area-based economies of scale to reduce PV costs. Perhaps the most-well known and extreme example of such attempts was development of an amorphous silicon (a-Si) SunFab module by Applied Materials. Applied Materials claimed that these modules, which had an area of 5.7 $m^2$, reduced installed cost of a PV system by more than 20% [1], but then shut down the SunFab line several years later.

It was unclear whether the struggles SunFab faced were related to the a-Si technology or the large-area module format, and whether these challenges were related to fundamental technology or market conditions. Despite the fact that very large-area modules have not yet succeeded in the marketplace, interest in the concept has not faded. First Solar, the leading manufacturer of cadmium telluride (CdTe) modules, recently announced plans to move toward much larger area panels, claiming this would reduce capital equipment expenditures (CAPEX) by nearly 40% [2]. REEL Solar Inc. (RSI) has developed a process for electroplating on large-areas to help enable manufacture of large CdTe modules. Siva Power, a start-up in copper indium gallium diselenide (CIGS) module manufacturing, is also developing large area products (2 $m^2$, which is similar to 72-cell mc-Si modules but larger than other leading thin-film products) [3]. For PV, there are also potential area-based economies of scale for system costs that scale with module count (e.g., installation labor costs). Indeed, this has been observed in comparing labor, electrical, and racking cost per watt for installing 60-cell modules and larger, 72-cell modules [4].

However, the effect of module area on module and system-level costs for larger sizes has not been quantified in the literature. In this paper, we provide an analysis of these costs for the three leading commercial PV technologies: multicrystalline silicon (mc-Si), CdTe, and CIGS. We focus on the case where rigid glass-glass module architectures are used. Because $/W costs and the levelized cost of energy (LCOE) are strongly influenced by the performance of modules, we also examine the potential affect of module size on efficiency and energy yield.

# 2 The Effect of Module Area on Module Manufacturing Cost per Watt

Module manufacturing costs and minimum sustainable pricing (MSP) were analyzed using NREL's bottom-up methodology, which is described in detail in [5–7]. This approach accounts for labor, material, utilities, maintenance, and depreciation (equipment and building) associated with each step in the manufacturing process flow. Input data are collected from material suppliers, equipment vendors, and PV manufacturers via interviews. MSP is calculating using a standard discounted cash flow tool, and is defined as the price at which the net present value is zero with the internal rate of return equal to the weighted average cost of capital (WACC). In addition to the manufacturing costs, the discounted cash flow accounts for sales, general, and administrative (SG&A) costs, research and development (R&D) costs, and the cost of taxes. Thus, the MSP represents the minimum price that would have to be charged to cover all expenses and repay investors at their expected rates. Note that prices, which are set by the market, can be and have been lower than the MSP, and PV manufacturers can operate in the short-term with margins that fall below those achieved under MSP conditions. The MSP also depends on the WACC, which varies depending on the company and technology. A detailed discussion on the meaning of MSP is provided in [8].

In this work, we build on prior cost models developed for mc-Si [5], CdTe [6], and CIGS [7] modules of standard size. All models used to generate the results shown here were last updated in either in late 2015 (mc-Si, CdTe) or early 2016 (CIGS). In the case of mc-Si, the cell prices were additionally updated in March 2017 (see Section II.A). It is important to note that the goal of this paper is to understand how sensitive module and system costs might be to module area for different technologies. Care must be taken than the differences in cost and MSP across technologies is not based on technology characteristics alone, but also on market and firm-specific factors; for example, our modeled MSP values will be affected by the typical firm structure and overhead costs (R&D and SG&A) for companies producing each technology, as well as the production volumes achieved for each technology. Additionally, more data is available on c-Si costs due to the larger number of c-Si companies, and some of our cost models have been more recently updated than others.

For all technologies, we assume the large area modules are manufactured at a new manufacturing plant with new equipment, where no subsidies or tax incentives are provided. Large modules can experience increased loading compared to smaller modules, which may cause increased stress; large mc-Si modules, for example, may be more prone to cell cracking. Stress experienced by the cells and module can be controlled through a combination of laminate design, frame design (or frame removal), and mounting. Because very large area modules have not yet been implemented, there is uncertainty around which designs will provide the best performance. For purposes of this analysis, we assume a frameless, glass-glass architecture with the cells located in the neutral axis, which is one possible solution for managing this stress. Assumptions about the thickness, type, and reference case area of the glass for each module type were aggregated from the data sheets of current leading manufacturers [9–12]. These are shown in Table 1. Manufacturing locations reflect where the majority of the manufacturing for each

technology currently occurs. Glass pricing for the CdTe case is removed in order to protect business sensitive information. Note that glass pricing can vary significantly by region, glass type, supplier, and negotiating power of the purchaser. All else being equal, 2.5mm thick glass is currently more expensive than 3.2mm glass, due to lower production volumes and yields. However, a large, tier 1 mc-Si manufacturer in China may get a lower price for 2.5mm glass than a U.S. or Japanese thin-film manufacturer gets for 3.2mm glass, because of regional glass pricing, tariffs, lower order volumes, and differences in the quality of the glass. Pricing of 2.5mm glass is also expected to decrease below that of 3.2mm glass as production scales and yields improve. Sensitivity of the results to glass costs over a wide range was performed, and the fundamental conclusions about the effect of module area on cost held under different scenarios. We were able to receive only somewhat limited data from glass manufacturers on how glass prices (per square meter) may scale with area. However, it appears that the per square meter pricing will likely not change until the glass size is the same as that coming off a particular float line, in which case, some savings in packing materials for shipping and in the cost of cutting the glass to size could be realized. Our (limited) interviews suggest this would likely affect glass pricing by < 12%.

**Table 1. Assumptions on Module Glass and Reference Case Area by Technology**

| | **mc-Si (72-cell)** | **CIGS** | **CdTe** |
|---|---|---|---|
| Front glass thickness (mm) | 2.5 | 3.2 | 3.2 |
| Front glass type | Low Fe, tempered with anti-reflective coating | Low Fe, tempered with anti-reflective coating | Low Fe, heat-strengthened with anti-reflective coating |
| Front glass price ($/m$^2$) | $5.10 (China) | $7.00 (United States, Japan) | |
| Back glass thickness (mm) | 2.5 | 2 | 3.2 |
| Back glass type | Soda lime, heat-strengthened | Soda lime, annealed | Soda lime, tempered |
| Back glass price ($/m$^2$) | $3.10 | $2.40 | |
| Reference case module dimensions (mm x mm) | 1,978 x 992 | 1,257 x 977 | 1,200 x 600 |
| Manufacturing location | China | Japan | Malaysia |

Large area glass dimensions were selected based on standard sizes used in the flat panel display industry. In the mid-80s, at the birth of this industry, the typical substrate size was only 300mm x 400mm. This size is referred to as generation 1 or Gen 1 glass. Subsequent generations of flat panel display glass have scaled up significantly. Fabrication facilities (fabs) based on Gen 6, Gen 7, and Gen 8 glass, which measure 1,500 mm x 1,800 mm, 1,870mm x 2200mm, and 2,160 mm x 2,460 mm, respectively, are now used to produce a significant fraction of liquid crystal displays (LCDs). Gen 10 (2,900 mm x 3,100 mm) and, more recently, Gen 10.5 (2,940 mm x 3,370 mm) fabs are also starting to be built. TCL has even announced construction of a Gen 11 fab in Shenzhen, China.

This glass is truly massive compared to current PV glass, with the area of Gen 10.5 glass being roughly 5X that of glass used for typical 72-cell mc-Si modules and 1.74X that used in the SunFab module. While the display industry has consistently realized manufacturing cost reductions per unit area with increased substrate sizes, driven largely by reduced equipment costs per area [13], substrate sizes of Gen 10 and larger have posed shipping and logistics challenges. A striking example, cited by SEMI [14], is that Gen 10 glass is too large to fit through the sliding doors of a Boeing 747 Jumbo freighter. Manufacturing equipment for Gen 10 and above has also proven challenging for the display industry, with AKT citing difficulties in obtaining required materials, finding machine shops with the ability to manufacture the parts, and shipping. Because fewer tools are required for larger glass sizes, and equipment is increasingly difficult to manufacture, there may be some reduction in the economies of scale that can be achieved in equipment pricing. It is also increasingly difficult to ship equipment that is assembled far from the customer. Very large tools, while providing a lower manufacturing cost per area, also require a larger minimum production scale and higher total investment. This could pose a challenge in the current PV market, where manufacturing overcapacity, slim margins, and fierce competition can limit capital expenditures (CAPEX) and encourage more incremental, short-term investments. The use of very large tools also reduces the redundancy in the manufacturing process, resulting in an increased revenue loss associated with downtime and yield loss on each system.

In the following sections, we examine the potential effect of scaling mc-Si and CIGS modules to Gen 6, Gen 8, Gen 10, and Gen 10.5 sizes on module manufacturing costs. Given the limited amount of available data, we look only at the reference and Gen 6 (which we estimate to be similar to the size of First Solar's S6 product) cases for CdTe, and do not include shipping costs for the modules. However, the potential for higher shipping costs with sizes equal to or above Gen 10, discussed above, should be considered.

## 2.1 Analysis of mc-Si Modules

### *2.1.1 Methods and Assumptions*

The mc-Si analysis assumes that standard multicrystalline silicon solar cells with an area of 243 $cm^2$ are used in the module. We assume a cell price of \$0.20/$W_{DC}$ and module efficiency of 17% for all module sizes. The same price per cell as that of current 60-cell and 72-cell modules is used, and thus, any savings with larger area modules shown here are realized entirely in the module manufacturing steps. Industry experience with large area mc-Si modules is extremely limited, and most industry members we interviewed could provide only educated guesses as to what the potential effect on cost may be as module size increases. We combined the feedback from our interviews with our own understanding of the module manufacturing process and equipment to develop a set of assumptions for our cost model with large modules:

- We assume the rated module efficiency is the same for all module sizes; this assumption is discussed in Section IV.
- We assume more factory floor space will be required for bus bar assembly, glass washing and handling, module layup, final assembly (which includes adding the

junction box), and testing. These steps require equipment whose footprint could scale with module area, although this depends on the characteristics of the factory, and in some factories, it may be possible to utilize existing equipment for some or all of these steps.

- We assume floor space requirements scale proportionally with module area.
- We assume a modified flash tester is needed in order to maintain light uniformity over large areas and obtain accurate test measurements. This could just involve replacing the source, which we estimate would cost between $8,000 and $15,000, depending on the module area, or a complete re-design of the tester. While increases in the tester costs are not likely to be a major issue for overall manufacturing costs, each unit would likely be a high-cost, specialty product for early adopters.
- Increased glass size may increase the cost for handling, inter-factory transport, and automation. Modifications may involve only minor adjustments to the end effectors of automation equipment (which are typically low-cost) or more significant upgrades such as replacement of some equipment and reconfiguring of facilities. Based on the experience of the display industry, we expect that these costs may increase more significantly for Gen 10 and Gen 10.5 glass. We assume 5%, 10%, 20%, and 20% relative increases in the auxiliary equipment costs for the bus bar assembly, glass washing and handling, module layup, final assembly (which includes adding the junction box), and testing steps for the Gen 6, Gen 8, Gen 10, and Gen 10.5 sizes respectively. We stress that these are assumptions, and that costs will depend on the existing factory layout and automation equipment, as well as the approach manufacturers take in upgrading to larger modules.
- We assume that more expensive junction boxes (j-box) are required with larger modules. This is because more bypass diodes will be required as the cell count per module increases, leading to higher total cost of the diodes and likely an increase in the footprint of the junction box that houses them. Appendix A includes our calculations and the assumptions of j-box costs for each module size.
- We assume that module packaging costs are proportional to the module area.
- We assume that the percent yield loss for each manufacturing step is constant as module area scales. However, because the amount of material used per module increases proportional to area, yield losses at the end of the manufacturing process, after the cells are assembled into a module, result in increased material waste for larger modules.

### 2.1.2 Results

Results showing module cost versus area for the mc-Si case are presented in Figure 1. We estimate that increasing module size from the current standard 72-cell case to Gen 10.5 glass size could decrease module manufacturing costs and module MSP by $0.035/W and $0.040/W respectively. 74% of this reduction is due to reduced material costs. This decrease is driven mostly by per watt reductions in the material cost of j-box, potting agent, and busbars. While the cost of these materials per module increases with module area, the rate of this increase is lower than the rate of increase in the module power rating; since cost per watt is equal to the cost per module divided by the watts per module, this results in a lower materials cost per watt for larger modules. The impact of yield on materials costs is small, since our model assumes a cumulative manufacturing yield loss of approximately 2%, with very little yield loss occurring in the final steps of the manufacturing process.

Lower per watt equipment and facilities costs account for approximately 6% of the total cost reduction. Total equipment costs are related to the cost per tool and the number of tools required to meet the factory throughput requirement (1 GW/year in this case), which is driven by the cycle time for each process. For many operations, little to no increase in cycle time occurs as module area increases. For example, attaching the j-box takes a fixed amount of time, regardless of module size. Lamination time is also largely fixed, and the time to complete a few additional solder joints on a busbar is small. The per tool cost of certain equipment, described above, increases with module area, but not linearly; the increase in per tool cost for module assembly equipment is expected to be relatively small. The lower tool count also drives down labor costs, since a certain number of line workers are typically required per tool. However, the effect of labor on overall cost savings is small, since we assume a highly automated process and because relatively unskilled, low-cost labor can be used for module assembly. The electricity usage per module for the flash tester, busbar assembly, laminator, and automation equipment increases with module area but, again, not linearly; a doubling of module area does not results in a doubling of electricity usage, and thus an electricity cost savings (in $/W) is also achieved. Electricity cost savings with Urban China electricity prices constitute 16% of the overall manufacturing cost reduction with the Gen 10.5 module compared to the reference case.

66% of the $0.035/W manufacturing cost savings is realized with Gen 8 glass. While additional savings could be achieved by using Gen 10 and Gen 10.5 glass, as shown in Figure 1, there are decreasing returns to scale. There are two reasons for this: first, for sizes above Gen 8, the $/W costs that scale with module area (e.g. the j-box) are significantly reduced, and other costs that do not scale with area become more dominant; second, the increase in auxiliary costs, j-box prices, and very large cell count per module (399 for the Gen 10.5 case) blunt the cost savings. The potential logistics and shipping challenges associated with Gen 10 and Gen 10.5 products, discussed above, could also affect the overall cost competitiveness of these very large modules (although the display industry may be able to find solutions to some of these issues).

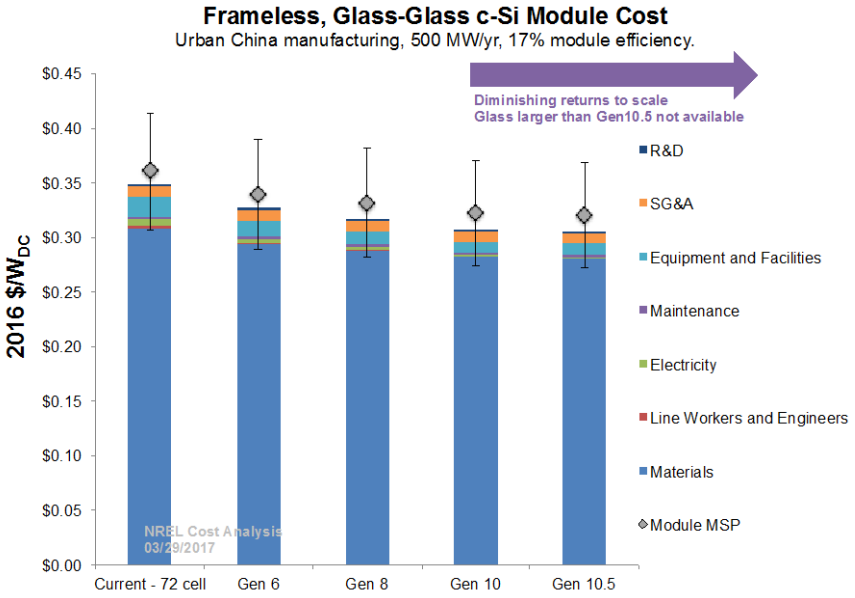


**Figure 1. Effect of module size on mc-Si module manufacturing cost and module MSP.**

The cell prices used are not cell MSPs, but current cell prices, and thus do not necessarily reflect cell prices at margins acceptable in the long-term. Shipping and logistics costs are not included. The black line connecting the module area data points is only meant as a guide for the eye.

Because of the uncertainty surrounding many of our input assumptions, we analyzed the sensitivity of our results to ± 20% changes in key input parameters, shown in Figure 2. The yield loss multiplier is applied equally across all manufacturing steps. As shown in the Figure, the impact of ± 20% changes in auxiliary and testing equipment costs compared to the reference case is very small, < $0.0002/W. Large modules provided at least some manufacturing cost savings over a wide range of possible input values.

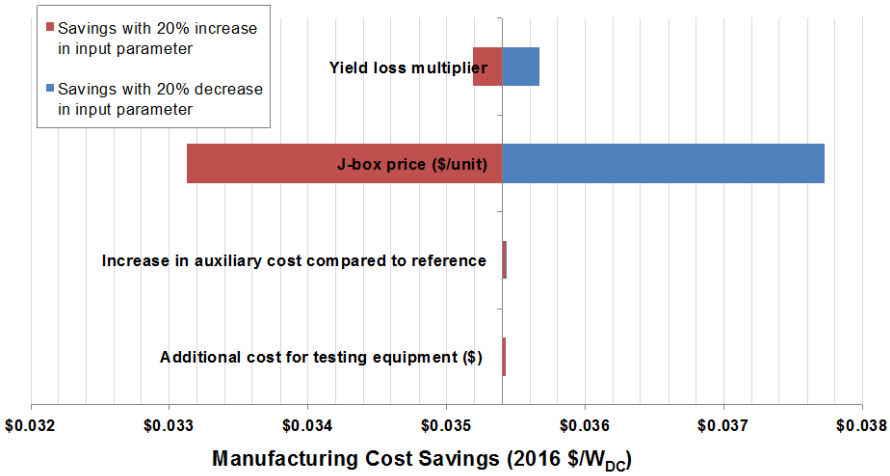


**Figure 2. Sensitivity of mc-Si modules manufacturing cost savings with Gen 10.5 modules (Gen 10.5 cost minus reference case cost) to ±20% changes in key input assumptions.**

The reference j-junction box price assumed for the Gen 10.5 case was $17.20/unit. See Appendix A for details.

## 2.2 Analysis of CdTe Modules

### 2.2.1 Methods and Assumptions

First Solar is the only high volume manufacturer of CdTe modules, and sufficient data for a bottom-up cost analysis of Gen 8, Gen 10, and Gen 10.5 sizes were not available. We were able to estimate potential effect on cost for the Gen 6 case using publicly available information on the S6 product from First Solar's Analyst Day presentation [2] (note that First Solar did not confirm the size of their S6 module; size was estimated by NREL based on information in [2]). Assumptions made in this analysis are shown in Table 2. The manufacturing equipment CAPEX and production volume values—we assume full plant utilization, so that listed plant capacities equal production volume—are used in NREL's CdTe cost model (published in [6] but updated as recently as the end of 2015); we assume these CAPEX numbers include the cost for both the equipment and facilities.

**Table 2. Assumptions for CdTe Analysis**

| Parameter | Reference Case Value | Gen 6 Value |
|---|---|---|
| Production volume | 450 MW/year | 2,000 MW/year |
| Total CAPEX | $300M | $800M |
| Total building square footage | 500,000 sq. ft. | 1,000,000 sq. ft. |
| Electricity consumption scaling | 1 | (Gen 6 area/reference case area)$^{0.8}$ |
| Module dimensions | 1,200mm x 600mm | 1,500mm x 1,800mm |

As with mc-Si, we assumed the same efficiency for both sizes. However, with monolithic, thin-film modules, it may be difficult to maintain uniformity as area scales, potentially affecting module efficiencies. In the display industry, achieving good uniformity with increased glass area has required re-engineering of the process and equipment. Currently, there is insufficient data to assess how challenging it may obtain high efficiency CdTe modules on large area substrates; this is discussed further Section IV.

Material costs per unit, including the junction box cost, are assumed to be the same for both module sizes. Typically, thin-film modules with a monolithic architecture use only one bypass diode per module (or no bypass diodes), and the junction box design does not appear to vary significantly. We assume manufacturing yields are the same for the reference case and large area module case, although it is unclear whether thin-film modules can be manufactured on large area substrates with high yields, as this has not yet been publicly demonstrated.

### 2.2.2 Results

Results are shown in Figure 3. Error bars are estimates of uncertainty, as we have no detailed information regarding the certainty of First Solar's CAPEX values. If the reported CAPEX is achieved, reductions of $0.10/W in manufacturing cost and up to $0.14/W in MSP could be achieved. 80% of the total manufacturing cost savings come from reductions in materials (46%) and CAPEX costs (34%). As with mc-Si, material

costs, in $/W, are reduced because the cost of materials is either fixed with area or increases at lower rate than the rated module power output. Because we assume the same j-box is used for the reference and Gen 6 cases, the reduction in j-box material costs is even more pronounced for CdTe compared to mc-Si.

The decrease in CAPEX with the larger module is significant - $0.40/W/year compared to $0.66/W/year. Unfortunately, because insufficient data could be obtained on the CAPEX of each tool for the Gen 6 case, we have little insight into the main drivers of this reduction. It is likely that the mechanisms observed for mc-Si also apply for CdTe - cycle time (per watt) is decreased, reducing the number of required tools to meet the throughput requirement, while the price per tool increases at a slower rate than the throughput (W/year) per tool. Because the CAPEX required for manufacturing CdTe modules is much larger than that required for assembling mc-Si modules, the potential for CAPEX savings is larger.

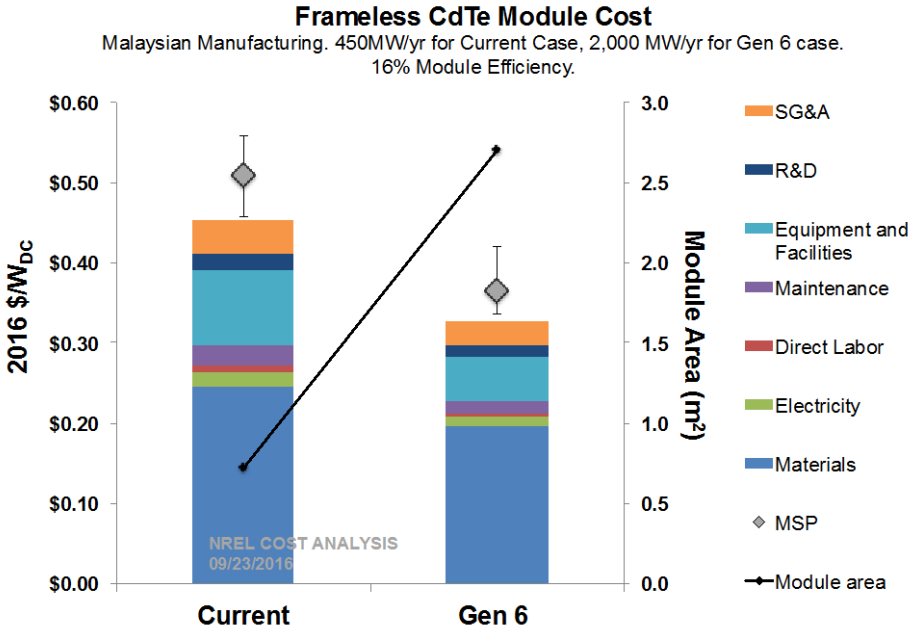


**Figure 3. Effect of module size on CdTe module manufacturing cost and MSP based on CAPEX data reported in [2].**

Shipping and logistics costs are not included. The black line connecting the module area data points is only meant as a guide for the eye.

In our model, annual maintenance costs are assumed to be a fixed percentage of CAPEX costs, and so the lower CAPEX results in proportionally lower maintenance costs. Smaller savings were also observed in labor costs, because of the reduced number of equipment stations required per watt to meet throughput requirements, and in electricity costs, because of economies of scale in electricity usage.

Sensitivity of this cost savings to ± 20% changes in key input parameters is shown in Figure 4. Again, the yield loss multiplier is applied equally to all manufacturing steps. As with mc-Si, some savings are achieved over a wide range of possible input values. Savings of more than $0.03/W, mostly in materials costs, is achieved even if the total plant CAPEX is double what First Solar has suggested. Based on our interviews with equipment vendors and industry members, we consider this scenario extremely unlikely. Sensitivity to efficiency is examined in detail in Section III, where we account for efficiency effects on both the module and system level.

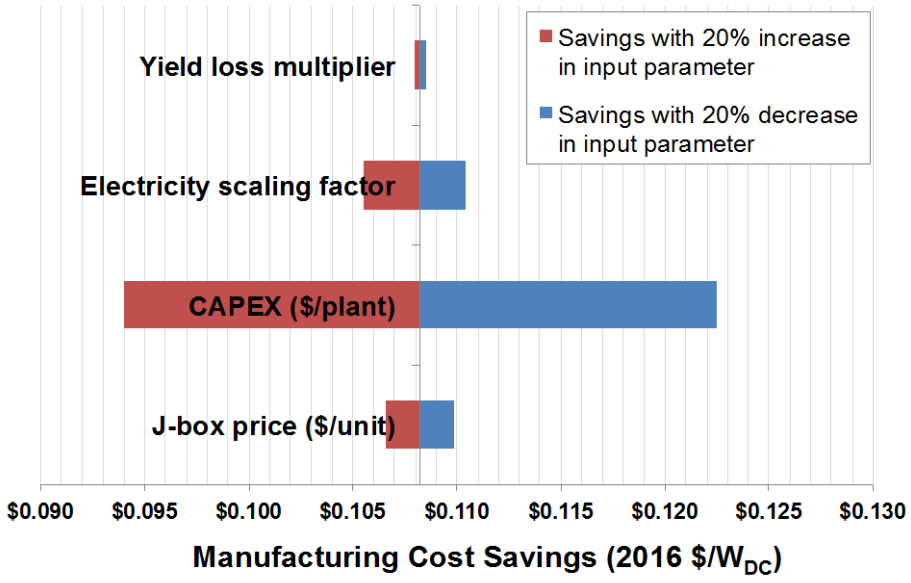


**Figure 4. Sensitivity of CdTe modules manufacturing cost savings with Gen 6 modules (Gen 6 cost minus reference case cost) to ±20% changes in key input assumptions.**

## 2.3 Analysis of CIGS Modules

### *2.3.1 Methods and Assumptions*

The CIGS analysis assumes a two-step sputtering and a batch selenization process is employed; this process is described in detail in [7]. We also assume the same device stack as in [7]. Data on the potential effect of increased module area on the manufacturing process and cost for CIGS were obtained via interviews with equipment suppliers and members of industry. In many cases, equipment suppliers were only able to provide limited or qualitative data, because either (1) they lacked adequate experience with large area modules to provide good data or (2) such data were proprietary or business sensitive. It is also difficult to predict how the significant amount of investment required from equipment vendors to design, test, and build very large new tools, combined with lower equipment order volumes, would impact tool pricing. Equipment shipping costs could also increase as module area scales, but a premium for shipping large tools is not included in our current model. Any increases in equipment shipping costs are highly uncertain at this time, as they depend on the location of the CIGS module manufacturer and the equipment manufacturer, and, if shipping costs are very high, the equipment

manufacturer may choose to locate production close to their customer(s). Assumptions in our analysis include:

- We assume the rated module efficiency is the same for all module sizes; this assumption is discussed in Sections III and IV.
- We assume that the modules move through continuous, rotary sputtering tools with the long-edge leading. When the width of the module exceeds the width of the conveyer on the sputtering equipment, we assume a new tool is required, and the cost per tool increases as (new tool width/previous tool width)$^{0.6}$. We assume that the same sputtering tool is used for the Gen 10 and Gen 10.5 cases. The total cost of ownership for the sputtering steps (in $/W) decreases with increasing module size.
- The total cost of ownership for the selenization step is constant with increasing module area. Module manufacturers would typically use the same furnace as in the base case, which uses large trays accommodating either a greater number of small modules or fewer large modules.
- The same tool can be used for the chemical bath deposition (CBD) step for each module size, with a decreasing batch size as module area scales, but a constant throughput (in $m^2$/hour) and constant CAPEX. No data could be obtained on this.
- Laser scribe equipment cost per tool is increased by 10%, 15%, 30%, and 40%, for the Gen 6, Gen 8, Gen 10, and Gen 10.5 sizes, respectively. We assume that the throughput in modules per hour is constant; in other words, additional tool cost; in other words, we assume that equipment required for maintaining throughput (e.g. any additional laser sources and beam splitters to enable a greater number of parallel scribes) is added to the larger tools. This, along with the increased width of the scribing equipment, is what drives the increase in price per tool.
- We make the same assumptions about the need for and cost of a modified flash tester as we made for mc-Si (described in Section II(A)).
- We make the same assumptions about the increase in auxiliary equipment costs for the bus bar assembly, glass washing and handling, module layup, final assembly (which includes adding the j-box), and testing steps as we did for mc-Si (described in Section II(A)).
- The j-box price per unit is assumed to be the same for all module sizes.
- We assume the manufacturing yield is maintained as module area scales. As with CdTe, it is currently uncertain what yields could be achieved for CIGS over large area substrates, as fabrication of very large area modules has not yet been demonstrated.

In general, the total cost of ownership for each processing step depends on many different variables, and multiple approaches that can be taken. CIGS processing and device designs vary significantly more between companies than mc-Si processes and designs; for CdTe, there is only one high-volume manufacturer (First Solar). Selected approaches to manufacturing larger area modules for this technology would depend on the CAPEX, total cost of ownership, and return on investment requirements of the customer, as well as

the rest of the factory layout and throughput of other processes. Costs will also depend on which tools are used for processing at a given size, whether the tool was designed for large area substrates, the tool length, and the configuration of the substrates in the tool.

### 2.3.2 Results

Figure 5 shows the results of our CIGS cost modeling. In order to protect business sensitive information, a more detailed cost breakdown could not provided. This analysis indicates CIGS may hold the potential for the greatest decreases in cost with larger areas, with savings of up to $0.136/W in manufacturing cost and $0.147/W in MSP. There are three separate sputtering steps in this CIGS manufacturing process – sputtering of the molybdenum (Mo) back contact layer, the intrinsic and aluminum-doped zinc oxide (i-ZnO/AZO) front contact stack, and the copper (Cu), indium (In), and gallium (Ga) precursors – all of which experience cost of ownership reductions as module area increases. These cost reductions include lower equipment costs, electricity usage, and labor requirements per watt, as well as the potential for increased substrate collection efficiency and material utilization, depending on the configuration of the modules in the tool and the tool design. Very large area sputtering tools are already employed in the manufacture of some displays and architectural glass coatings. In addition to this, the same economies of scale in the lamination, j-box, and busbar attachment steps, described above for CdTe and mc-Si, exist.

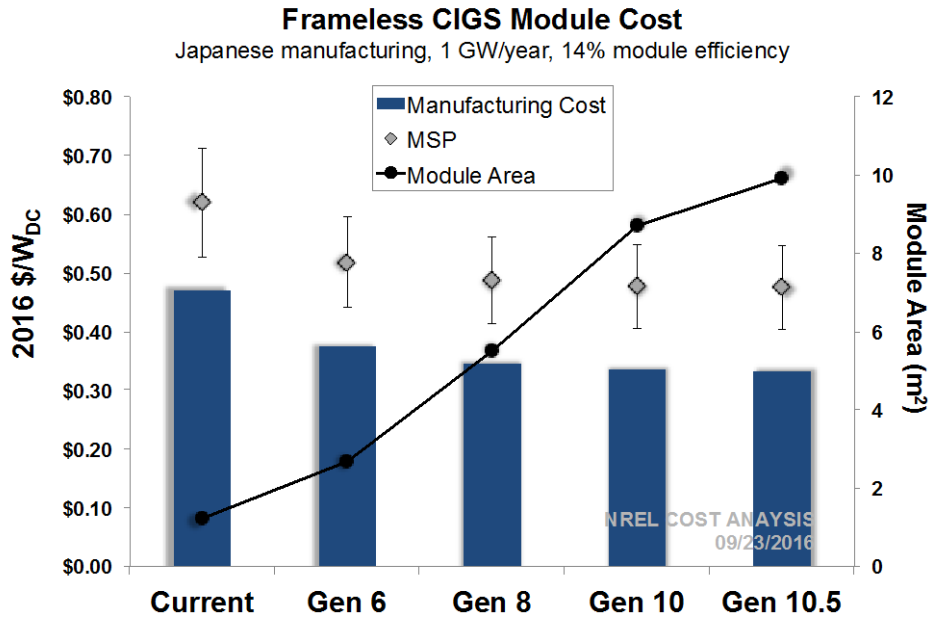


**Figure 5. Effect of module size on CIGS module manufacturing cost and MSP.**

Cost breakdown is not shown in order to protect business sensitive information. Shipping and logistics costs are not included. The black line connecting the module area data points is only meant as a guide for the eye.

As we observed for mc-Si, as the size extends beyond Gen 8, the cost of the j-box and busbars becomes increasingly small (j-box is reduced from $0.048/W in the reference case to $0.009/W in the Gen 8 case), and other costs that do not scale with module area begin to dominate. 71% of the manufacturing cost reduction is achieved by moving to Gen 6 sizes, with 91% of the savings realized with Gen 8 modules.

These cost savings are contingent on the ability to maintain manufacturing yield and efficiency as area scales. Currently, no data on uniformity and manufacturing yields for CIGS processes over very large substrate areas exists. The sensitivity of savings to manufacturing yield and other key input parameters is shown in Figure 6, below; the sensitivity to efficiency is discussed in Section III. For purposes of this sensitivity analysis, the yield loss multiplier was applied equally to yield losses at each step. Savings are most sensitive to differences in the selenization process, including the price per tool and the throughput. We believe that, for batch processes using currently available tools, throughputs that are at least similar to those of the reference case in watts per hour could be achieved, because a similar total module area could be packed into the batch furnace. However, sputtering and selenization has not been demonstrated on these very large area modules, and it is unclear whether modifications to the selenization process will be needed in order to maintain good performance. Any process changes that may be required could affect the throughput of each step.

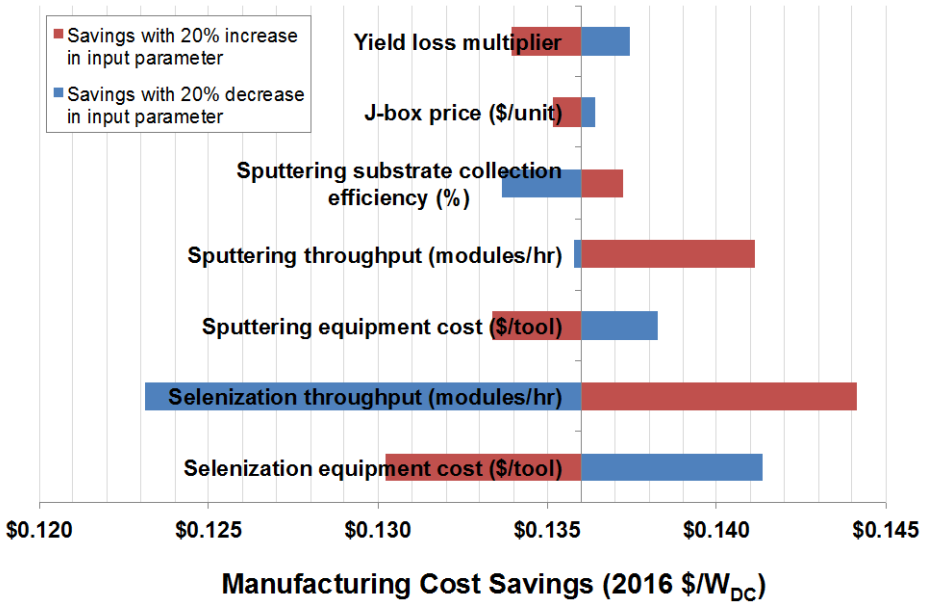


**Figure 6. Sensitivity of CIGS modules manufacturing cost savings with Gen 10.5 modules (Gen 10.5 cost minus reference case cost) to ±20% changes in key input assumptions.**

# 3 Effect of Module Area on Balance-of-System Costs and Total System Installed Cost per Watt

We evaluated the effect of module area on balance-of-system (BOS) costs for utility-scale systems using NREL's established bottom-up cost model [15–16]. In this model, we benchmarked both (1) soft costs (e.g., installation labor costs and engineering, procurement, and construction/developer overhead) and (2) hardware costs (e.g., structural/electrical BOS and inverter costs).

A modified system architecture will likely be employed for very large area modules. Several different system architectures for large area modules have been proposed; due to limited field experience, the relative merits of different proposed designs are not well understood. Here, we explore the costs associated with one possible approach, wherein flexible flanges and adhesive material are used in place of traditional fixed clamp connections between modules. This system design was used for our analysis of all large modules (Gen 6 through Gen 10.5). We assume that this configuration allows for the use of one less vertical mounting rail for each module assembly.

Based on our interviews and existing NREL data, we believe that installation of these large modules would require a machine to assist with lifting and placing the modules. In our model, we assume the cost of this machine is equal to that of a standard crane truck used in construction (a truck with a small crane mounted on the bed) plus a 20% premium for the appropriate robots, end effectors, etc. to interface with the module. Our results assume that the machine-assisted module mounting takes approximately the same amount of time as manual module mounting; this process could be sped up, additional cost savings could be realized. However, as discussed below, the installation labor cost associated with module mounting is a small fraction of the total installation labor costs, so these savings would likely be modest.

Figure 7 shows the system cost modeling results for Gen 6 and Gen 10/10.5 module sizes. Several factors drive these cost reductions. Material cost savings are observed by replacing typical clamps for glass-glass modules, which cost approximately $2.65/module, with flanges and adhesives, which are estimated to cost $0.80/module. The reduced module count and modified system architecture also result in labor and structural/electrical BOS savings. The reduced module count results in a significant, proportional reduction in module mounting time, but because much of the installation labor is spent on other tasks (e.g. installing the structure, racking, and inverter), the savings as a percent of total installation labor costs are modest. There is also a small additional cost associated with the use of an additional machine to assist with large module placement.

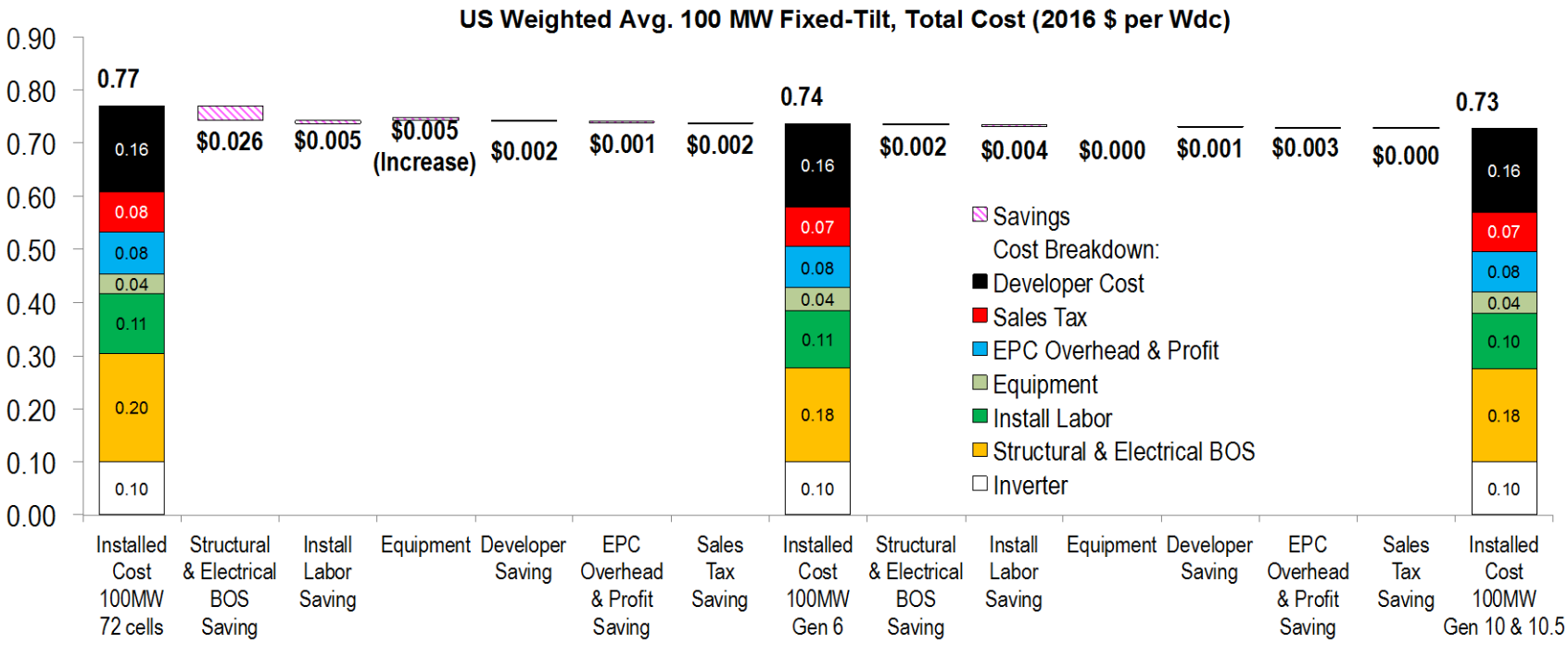


**Figure 7. Modeled impact of module area on BOS costs.**

Inputs to our cost model were collected via our interviews with industry members. The number of data points was extremely limited, as very few companies have installed large area modules. Additionally, while we only consider the case of utility-scale costs here, this same concept could potentially be employed for residential or commercial applications with the use of a specialized machine (e.g. a small crane).

In Figure 8, we combine these BOS costs with the module MSPs computed for each technology in Section II. Decreasing returns to scale are observed for both mc-Si and CIGS beyond Gen 8, but some additional module cost savings are still realized moving from Gen 8 to Gen 10 glass size. Increasing the size from Gen 10 to Gen 10.5 results in less than $0.005/W of additional savings in total installed cost for both mc-Si and CIGS.

Because mc-Si cells are typically binned by performance before they are integrated into a module, we do not expect a significant effect of module area on module efficiency for that case, although energy yield could be affected, as discussed in Section IV. The larger number of cells per module may also influence the binning process and number of bins. However, as discussed above, it is currently unclear whether efficiencies of thin-film, monolithic modules can be maintained as area scales. Figure 9 shows the sensitivity of total installed system cost savings to module efficiency CdTe and CIGS modules. We can see from Figure 9 that some cost savings compared to the reference case are still achieved for large area module efficiencies above ~12.5% for CdTe and above ~11% and CIGS. Savings decrease proportional to the reduction in large module efficiency compared to the reference case. This plot assumes that the module MSP in $/m$^2$ does not vary with efficiency. However, in reality, higher efficiency modules may be associated with cost and/or price premiums, and vice versa. Figure 9 can inform module cost and efficiency targets that must be achieved in order to realize a savings in total installed system cost with large modules.

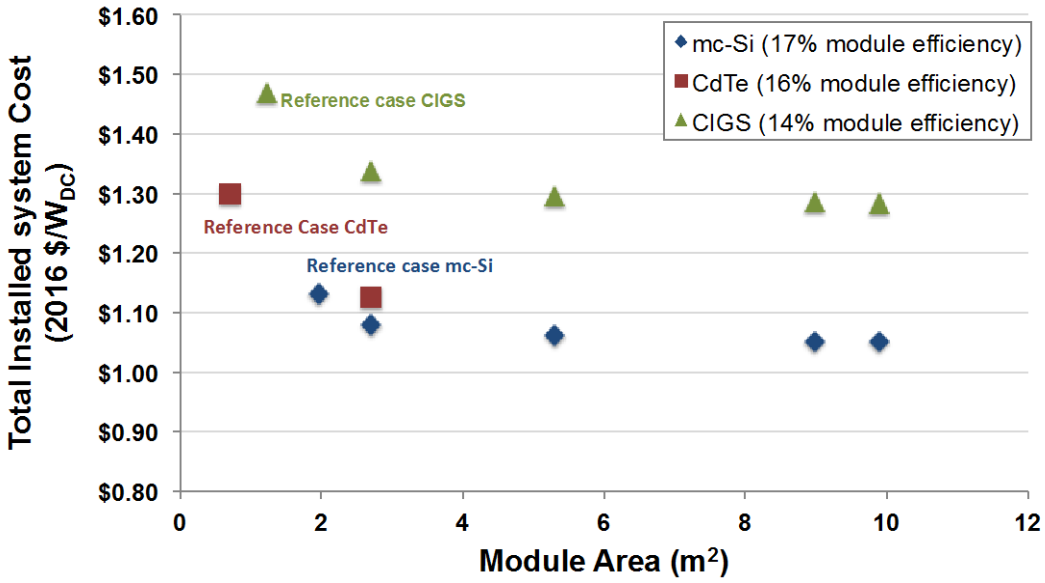


**Figure 8. Effect of module area on our modeled U.S.-weighted average total installed system price by technology.**

Assumes a 100MW utility-scale installation with fixed tilt. The primary goal of this plot is to illustrate how increasing module area may allow for cost reductions for each technology — caution should be exercised when making conclusions about absolute technology cost differences based on these results for reasons described in Section II.

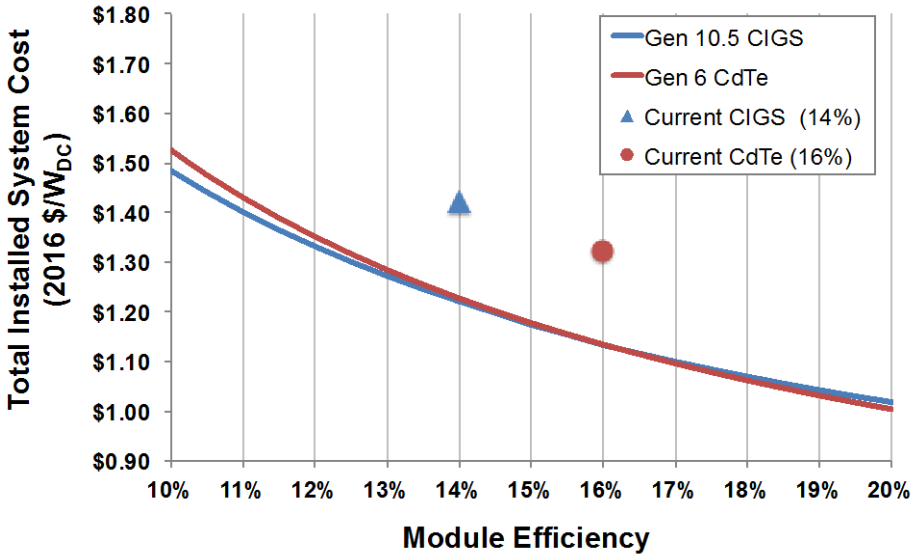


**Figure 9. Effect of module efficiency on realized cost savings with large module sizes for thin-film technologies.**

# 4 Potential Effect of Increased Module Size on Energy Yield

Effects of increased module area on rated module efficiency and energy production are not well understood due to a lack of data measuring the performance of large area modules. While some large area a-Si modules have been produced [1], mc-Si, CIGS, and CdTe modules of the sizes analyzed in this work have not yet been fabricated. In this section, we provide an overview of mechanisms that may result in performance effects for modules with increased area for each of these three technologies.

Based on interviews with industry and experts in module performance and reliability, we believe performance of standard mc-Si modules will not be significantly affected by size. Even with modules employing cells that were binned prior to assembly, there may be uneven degradation of the cells. There may also be greater variation in cell output within a larger module with a greater number of cells due to partial shading. The effect of these factors on energy yield, if observed, could be mitigated somewhat in wafer-based module architectures by rewiring the modules, employing additional bypass diodes, or module-level power electronics.

Module area might affect the energy production of monolithic thin-film modules by many more mechanisms. First, nameplate efficiency, degradation, or both could be affected if non-uniformities in the manufacturing processes over large areas could not be addressed. The process employed for the vast majority of current CIGS and CdTe manufacturing does not allow for cell binning, which reduces the ability to mitigate the effect of any cell-to-cell non-uniformities. It is currently unclear how difficult it will be to achieve high uniformity over large areas with the vapor phase transport process for CdTe and the selenization process for CIGS; although uniform, high quality sputtered layers for many materials can already be achieved over large area substrates. Additionally, non-uniform cell output, which could be caused by manufacturing non-uniformities or temperature non-uniformities in the field, may reduce energy yield. In current monolithic architectures, this cannot be mitigated by the use of bypass additional diodes.

It has been reported that one of the main causes of non-uniformity of thin-film solar modules (e.g., CIGS and CdTe) is the lognormal distributed shunt [17], which contributes significantly to the cell-to-module efficiency gap [18]. The lognormal distribution of shunt can be inherent in thin-film technologies, which originated from the fact that grain size in poly-crystalline films is lognormal distributed regardless of the choice of materials. Using the physics-based module simulation framework [19-20], we performed Monte Carlo simulation for CIGS modules with different sizes given a lognormal distribution of shunt to investigate the effect of module area on the efficiency (Figure 10). One important observation from the simulation is that modules with a larger size have a narrower distribution of efficiency (i.e., smaller variance). This occurs due to the screening effect of poorly shunted cells (at the tail of the log-normal distribution) on the well-performing neighboring cells is reduced as the area of the module increases, which lowers the possibility of producing very inefficient modules. Moreover, as the size of modules expands, it is also less likely to produce a defect-free module with exceptionally high efficiency. Eventually, the efficiency is limited by the mean of shunts for very large

modules. Hence, production of monolithic solar modules with greater areas will affect the binning strategy of the manufacturers (i.e., more uniform power rating and pricing). However, it can reduce the market flexibility of selling solar modules to customers with different needs. For example, at the utility-scale, it is not favorable to deploy expensive solar modules with excessively high efficiency, as it does not offset the BOS cost. In contrast, those highly efficient solar modules are more popular at the residential scale.

In addition to the potential effects discussed above, degradation may also be affected by other factors in the case of thin-film, monolithic modules. However, no data on this are currently available, and the effect may not always be negative. For example, it is known that partial shading events can cause reverse bias conditions, leading to strong electric fields, high current density, and high dissipated power density, and, ultimately, permanent module damage in some cases [21-22]. Large modules with longer cells may reduce the probability that the full length of one cell is shaded, while other cells are illuminated, a damaging partial shade condition. . However, more cells would be damaged during each partial shade event due to the larger number of cells per module. Issues with module ribbons or busbars are also common sources of module degradation or failure, and increased module area could potentially affect the probability of such events. For example, the use of longer ribbons in larger modules may result in increased stress or loading in the busbar and thus increased probability of broken ribbons. Similarly, greater stress may be seen in the solder bonds, which could result in shorter solder bond lifetimes. These issues could exist for both mc-Si and thin-film modules. Changes in module design to reduce stress (e.g., the use of thicker glass) may be able to address some of these challenges if they were indeed observed in practice.

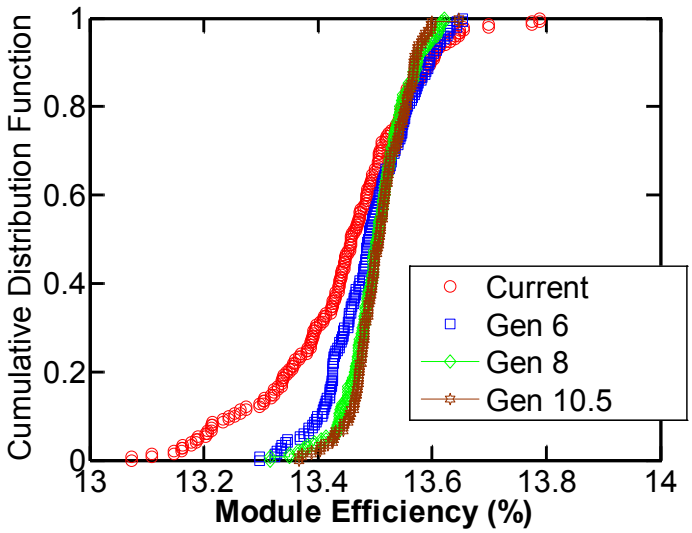


**Figure 10. Effect of module area on the distribution of module efficiency.**

Prior work suggests that although shunts or partial shading result in unsatisfactory degradation of module efficiency, novel geometry design and post-process scribing could be employed to enhance shadow tolerance for better reliability and isolate defects to improve overall module performance [18].

A complete understanding of the reliability of glass-glass modules in general is also still being developed. Module manufacturers have touted the ability of this architecture to reduce soiling and snow coverage, resist micro-cracks and snail trails, frame corrosion, and potential induced degradation (PID). However, the consequences of using impermeable backsheets are not well documented, and may depend on the encapsulant used.

Both module efficiency and lifetime energy yield are important drivers of LCOE. To evaluate fully the potential for large area modules to reduce LCOE, a better understanding of area-based effects on energy output is required.

# 5 Small Modules

We also explored the potential effects of decreasing module area via industry interview and our bottom-up cost models. We found that decreasing module size increased the cost at both the module and system levels for all technologies presented here. No industry members we interviewed thought small modules made sense for large-scale PV installations. Some smaller markets may value smaller size for other reasons (e.g., portable small-scale power in developing countries, consumer electronics, and small and irregularly shaped residential installs), but we found that this smaller form factor does not provide a benefit in terms of per watt cost or LCOE. Small modules may be more suitable for very volume manufacturing, including prototyping and product development, where a very expensive, high throughput tool is not required to meet demand and would not be fully utilized.

# 6 Discussion and Conclusions

We explored the potential for module area to influence module manufacturing and installed system cost per watt, and we provided an overview of the potential effects of module area on efficiency and energy yield. We found that small modules increase both module-level and system-level cost per watt, and are only relevant for low-volume manufacturing or niche applications. Large area modules, however, have the potential to result in significant savings at the module and system levels, especially for thin-film technologies. We observed diminishing returns to scale for sizes above Gen 8 or Gen 10 for module manufacturing cost and for sizes above Gen 6 for BOS and installation costs. While there is still uncertainty in many of our assumptions, our overall conclusions are robust over a wide range of potential input values, and provide bounds on these potential savings assuming that module efficiency, manufacturing yield, and energy yield can be maintained. The exact manufacturing cost savings realized will depend on the specific process steps and factory layout involved, whether large modules are manufactured in a new facility or in an upgraded, existing facility, and what equipment is used. Relative savings achieved with larger module size will also depend on the price of materials at any given point in time. Finally, for Gen 10 and Gen 10.5 glass, significant challenges around logistics and shipping will need to be addressed in order to achieve low-cost.

We have seen that the effect of module area on efficiency and energy production, especially for thin-film modules, is not well understood. While we have provided some initial analysis of how the effects of shunts might scale with module size, additional research is required to verify the effects of module area on energy output and thus LCOE. The ability to uniformly deposit thin-film devices over the areas we explored with high manufacturing yield has not yet been demonstrated, and it is unclear how challenging this might be. Further research on this topic is also required.

Additionally, there could be some barriers to manufacturing very large modules that are unrelated to cost per watt. For thin films in particular, a very high CAPEX would be required to build up the necessary capacity to manufacture large modules at competitive scale, given the large manufacturing capacity that already exists for mc-Si. The highly competitive nature of the current PV market makes smaller CAPEX investments, like upgrading existing mc-Si lines, preferable, and it makes it difficult to invest significant amounts in R&D, which encourages relatively near-term thinking. Any technology must also compete not with the current cost of the incumbent but with its cost at the time of market entry, and mc-Si costs continue to decline, creating a risk for potential investors. Finally, downstream suppliers may be slow to adopt large area modules if they require additional investment themselves. Increased module size would also require new investments from equipment manufacturers to develop new tools and processes suitable for large-areas. In some cases, knowledge can be borrowed from other industries, as with sputtering equipment currently used in display manufacturing.

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# Appendix. Junction Box Cost Calculations

We calculate the number of required diodes as follows, using a standard methodology outline in [18]:

$V_{oc\_cell}$ ~ 0.5 – 0.59 V

$V_c$ = cell breakdown voltage, assume to be 12V

$V_{bypass}$ = VF = forward voltage of typical bypass diode, assume to be

0.5V [cite]

$N_{max}$ = max # of solar cells bridged by the bypass diode < $(V_c\text{-}V_F)/V_{oc\_cell}$ +1

→ (12-0.5)/0.5 + 1 = 24 → Nmax = 23

→ (12-0.5)/0.59 + 1 = 20.49 → Nmax = 20

Divide # cells by 24 and round up to get required # of diodes

- Assume each bypass diode costs $0.3/unit
  - Price varies significantly depending on type of diode and supplier
- Assume $0.5 additional cost added to junction box price for larger housing, additional potting and encapsulant for each additional bypass diode
  - This assumption needs to be reviewed/validated.
  - Ran sensitivity analysis to this assumption in this report
- Assume same wire cost
- Assumes the basic junction box design is the same (no innovation in junction box design occurs as module size scales up)

**Table 3. Calculated Junction Box Parameters for the mc-Si Case**

| Module Size | Reference | Gen 6 | Gen 8 | Gen 10 | Gen 10.5 |
|---|---|---|---|---|---|
| # bypass diodes | 3 | 5 | 9 | 14 | 17 |
| Junction box price ($/unit) | 6 | 7.60 | 10.80 | 14.80 | 17.20 |

Note that in current practice, both 60-cell and 72-cell modules typically use the same junction box, with about three bypass diodes.