An Implementation of Automatic Washing Machine Control System Using Verilog HDL

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***Abstract*—This paper proposes to demonstrate the capabilities and scope of Verilog HDL by implementing the control system of an automatic washing machine. This paper accomplishes the above mentioned objective by implementing the Control System of an automatic washing using the Finite State Machine model. The Control System generates the control signals to control the overall operation of the washing machine. The Digital Design is simulated using Xilinx 14.1 ISE. The Verilog code for the Control System is then synthesized and implemented on Spartan 6 FPGA development board to verify its operation. This paper also demonstrates the reduction in Development Cycle by the use of Hardware Description Languages and FPGAs.**

***IndexTerms*— Verilog HDL, FPGA, Washing Machine Control System, Finite State Machine (FSM) model.**

I. INTRODUCTION

A finite-state machine (FSM) or finite-state automaton (plural: automata), or simply a state machine, is a mathematical model of computation used to design both computer programs and sequential logic circuits. There are two types: Mealy machine & Moore machine. Mealy machine is a finite state machine whose output values are determined both by its current state and current inputs. This is a deterministic finite state transducer: for each state and input, at most one transition is possible. Moore machine, is a finite state machine whose output values are determined solely by its current state. In this paper, Mealy State Machine is used to implement the control system of washing machine. The washing machine control system generates all the control signals required for the operation of washing machine and is designed using Verilog HDL. The digital design is implemented on Spartan 6 FPGA. Use of FPGAs facilitates the reduction in development cycle.

II. RELATED WORK

Chen Xizhen et. al [1] have proposed design of Control System for Washing Machine using Verilog HDL which involved use of its powerful language structure and concise code to describe the complex control logic. The proposed method used simulation tool to display the result.

P. Usha et. al [2] have proposed to demonstrate the practicality of HDL by implementing Automatic Washing Machine Control System using Verilog HDL as an example. The proposed work not only reduced the hardware development cycle but also greatly reduced development costs.

III. SYSTEM DESIGN

The washing machine controller has the following functionalities:

1. The wash machine has the following states: idle, soak, wash, rinse, spin.
2. There are three modes of operation i.e mode1, mode2 and mode3.
3. Different time durations are allocated to each mode of operation.

The controller is composed of two blocks: a finite - sate machine (FSM) block and a timer block. The FSM block receives some signals from the user, from the timer, and from other hardware parts such as the door sensor. FSM block output control the timer block and other hardware components of the washing machine. Table1 identifies the FSM input and output signals and their functionality. The timer block generates the correct time periods required for each cycle after it has been reset. The timer block is composed of an up- counter and combinational logic to give the correct time signals once certain count values have been achieved. The timer values will be determined by the clock frequency being used in the system.

Table 1: Alphabetical listing of input and output signals for the FSM (All signals are active high)

Variables	Input/output	Operation
CLK	IN	Main Clock for the System
Lid	IN	Machine door (lid) is open.
Coin	IN	Start wash machine.
Cancel	IN	Cancels the washing process

mode1/mode2/mode3	IN	Select Washing modes
idle_op	OUT	Do not perform any process
ready_op	OUT	Machine is ready to start the process
soak_op	OUT	Soaking operation
wash_op	OUT	Washing operation
rinse_op	OUT	Rinsing operation
spin_op	OUT	Spinning operation
coin_rtrn	OUT	Return the coin
water_inlet	OUT	Water intake

The working of the washing machine control system is described in the flow chart as shown in figure 1.

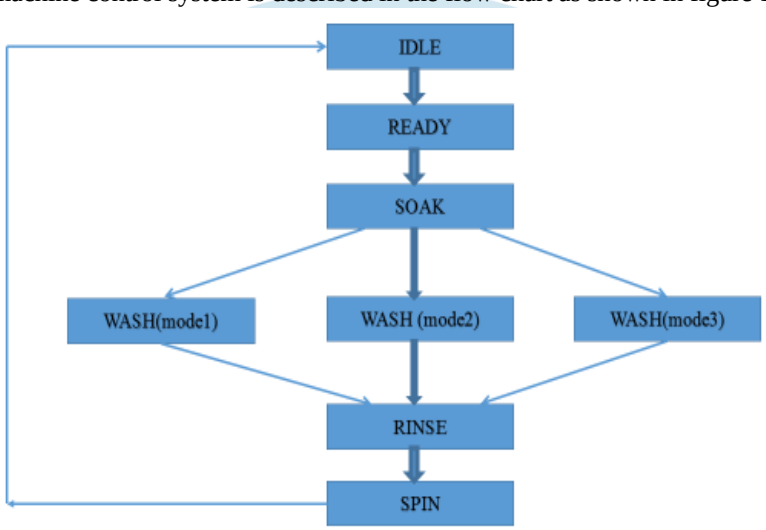

Figure 1: System flow chart of Washing Machine Controller

The FSM has 6 states as shown in figure 1. State transitions take place according to the timing control signals generated by the timer block and inputs given to a particular state. The processing in the next state depends on outputs produced in the previous state. Different wash times are selected by using the 3 different mode switches.

Figure 2 shows the State diagram of Washing Machine Control System which is based on Mealy Machine. It has following states: IDLE, READY, SOAK, WASH, RINSE, SPIN. Initially the FSM is in the idle state. Once the coin is inserted, the FSM will go to the READY state. Once in ready state, any of the 3 modes for washing can be selected. The selected mode decides the timing allocated to each state. If no mode is selected, it will remain in the READY state itself. In case the process is cancelled now, the coin is returned as the washing process has not yet started and the FSM returns to the IDLE state. But once the washing process starts, cancellation results in loss of the coin.

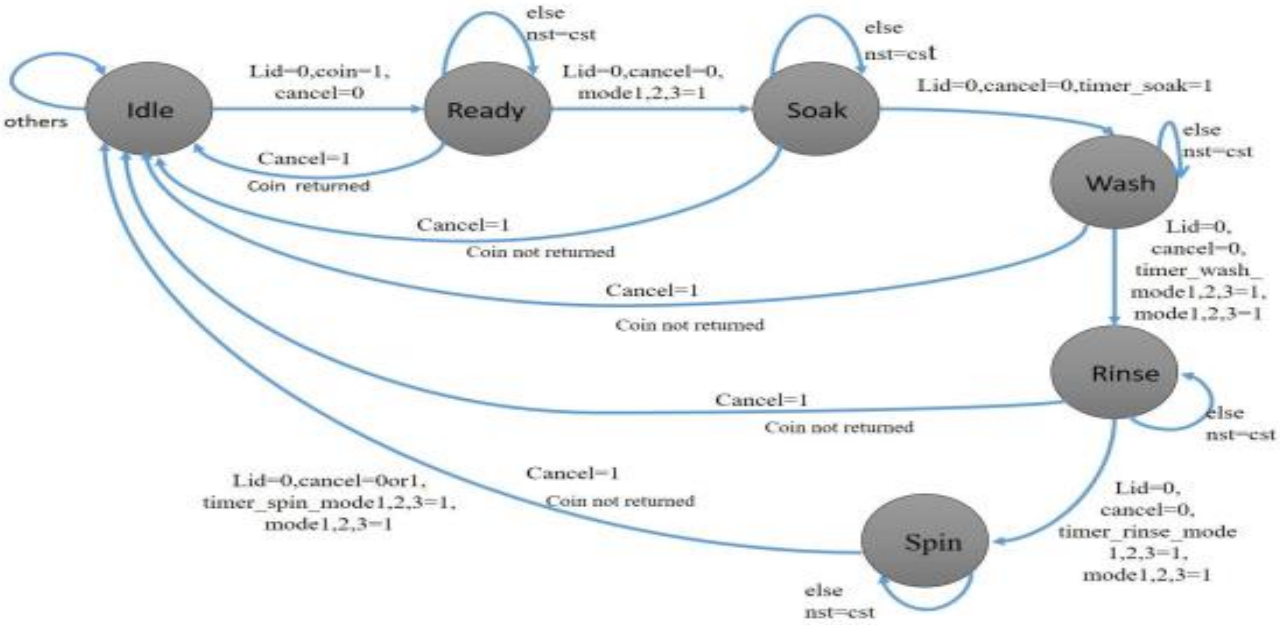

Figure 2: State Diagram of Washing Machine Control System

Once the washing process starts, the state transitions take place according to the control signals generated by the Timer unit. The Timer unit generates the control signals once the timers corresponding to the states elapse. The control signal to activate the water intake is generated during both the SOAK and RINSE states, as both the operations require fresh intake of water. The FSM transits from state READY to SPIN through the states - SOAK, WASH, RINSE, in an order. Once the last state i.e., SPIN is completed, the FSM transits back to IDLE state to take orders for the new wash cycle. If in between the washing process, the LID is opened to add or remove cloths or detergent, the washing process is paused for safety reasons.

The present state of the FSM is displayed using the 7 segment displays available on the SPARTAN 6 development board. The data and control signals for the 7 segment display are generated by the FSM itself according to the present states of the FSM.

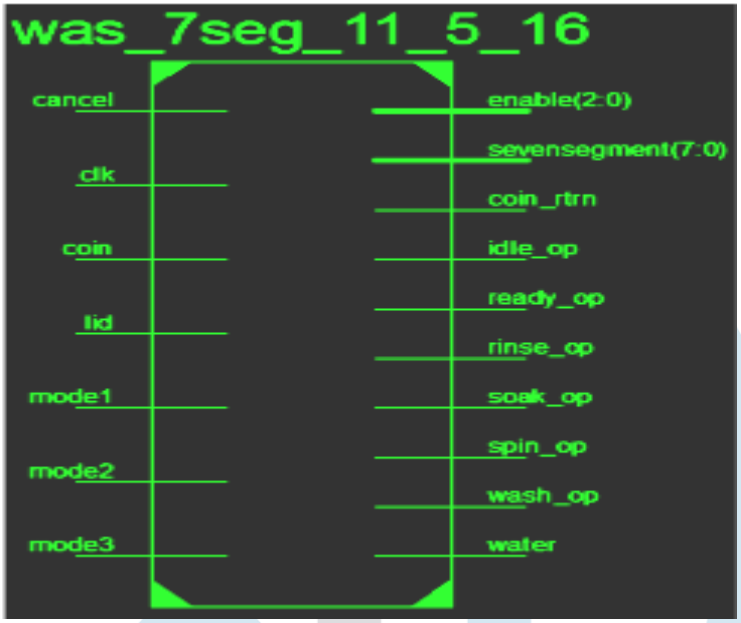

Figure 3: Xilinx generated Technology Schematic

Figure 3 shows the RTL schematic of the washing machine control system. The figure shows all the input and output signals associated with the control system. Totally 7 input signals and 10 output signals are visible. The output signals also include the control and data signals to output the state information on the 7 segment display.

IV. RESULTS

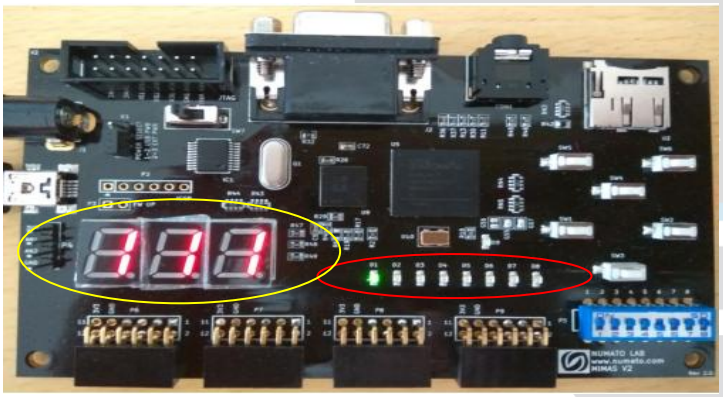

Figure 4: FSM in Idle State

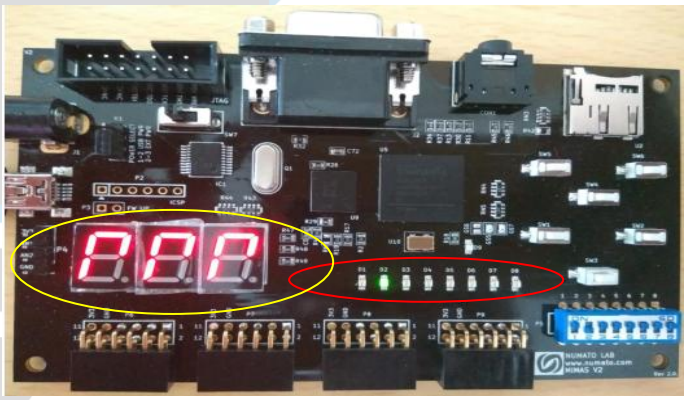

Figure 5: FSM in Ready State

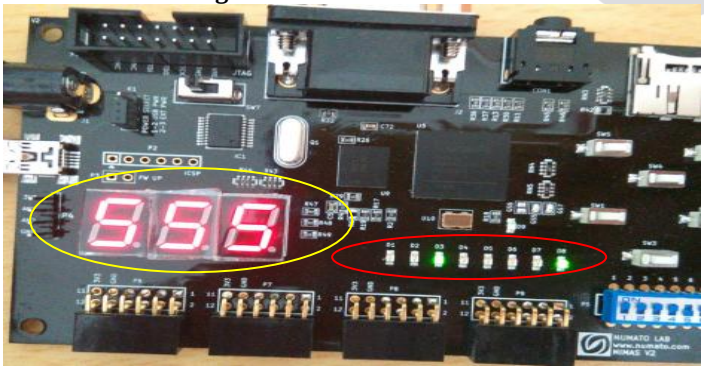

Figure 6: FSM in Soak State with water inlet ON

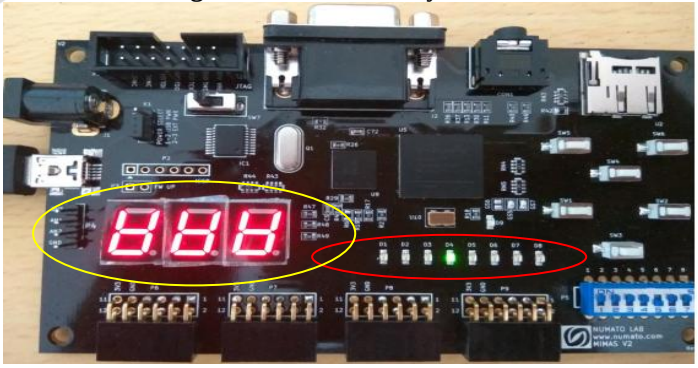

Figure 7: FSM in Wash State

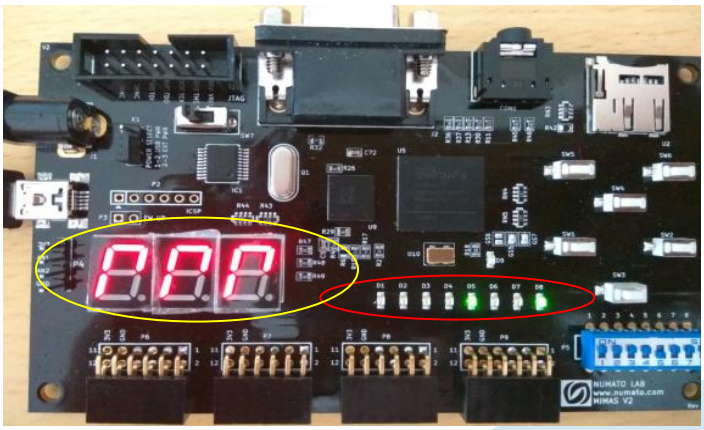

Figure 8: FSM in Rinse State

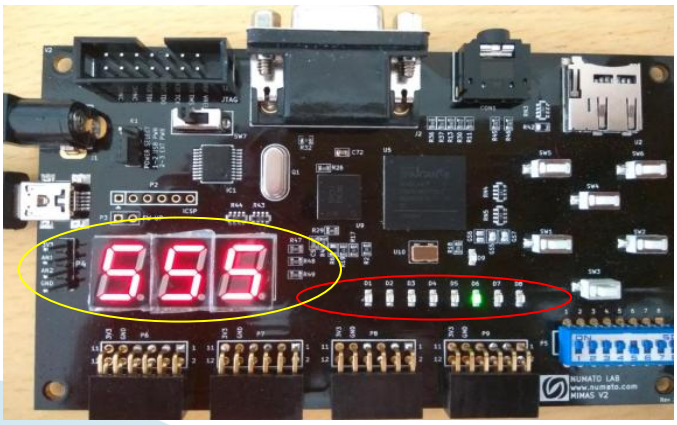

Figure 9: FSM in Spin State

The results of washing machine control system FSM are shown in figures 4 - 9. The 7 segment display & LEDs of the FPGA board indicate the respective state of the FSM.

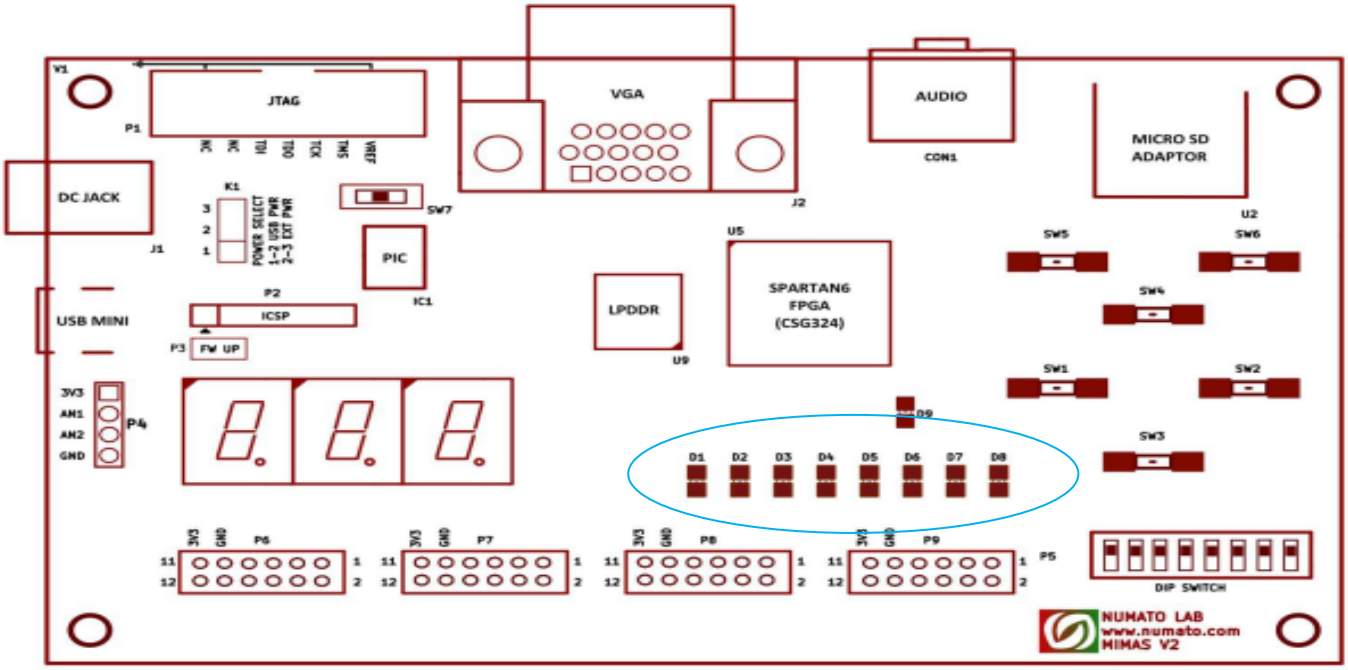

Figure 10: Skeletal Structure of Spartan 6 FPGA Board indicating output LEDs.

Figure 10 shows the output LEDs used for representing different state. The state assignment to the LEDs is shown in table 2.

Table 2: State Assignment to Output LEDs

LED	State
D1	Idle
D2	Ready
D3	Soak
D4	Wash
D5	Rinse
D6	Spin
D7	Not Used
D8	Water Intake

V. Conclusion and Future Scope

A FSM for washing machine control system was designed in Verilog HDL and implemented on Spartan 6 FPGA. The FSM designed has 6 states which perform different operations of a washing machine. The digital design of washing machine control system using Verilog HDL reduces the development cycle time.

In future, the number of states of the FSM can be increased for additional operations if required. Actuators like DC motor, stepper motor and solenoid valves can be interfaced with the FPGA to realize the real time operation and functioning of the washing machine control system.

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