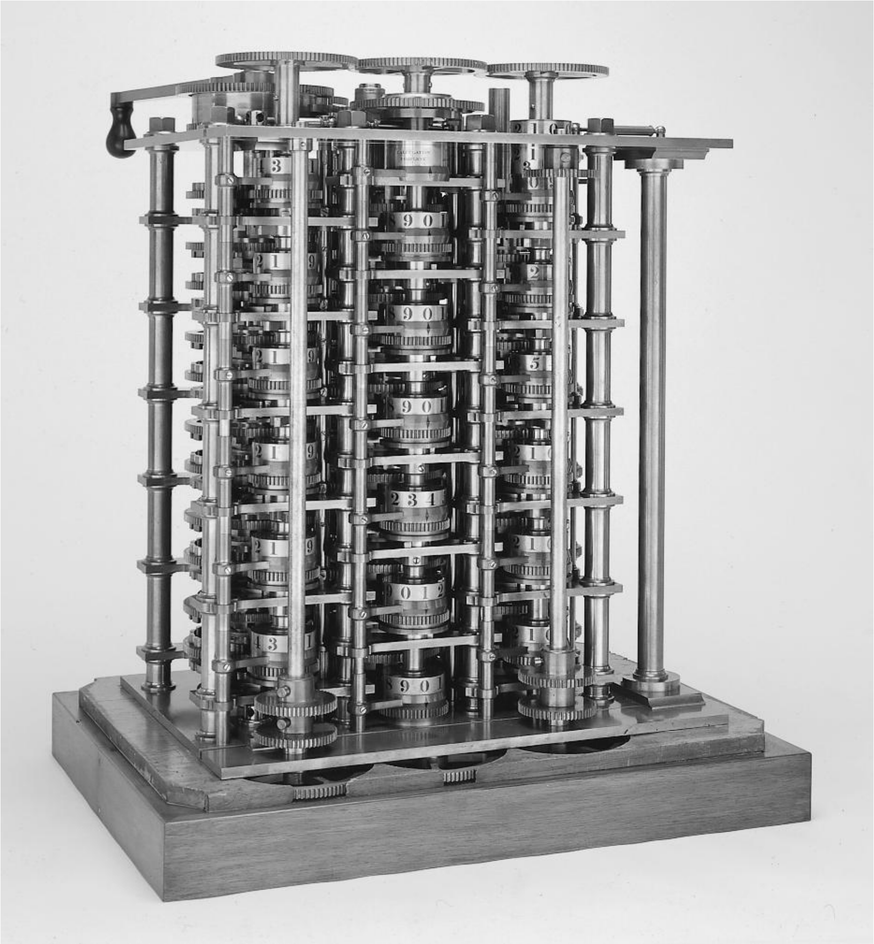
An Introduction to VLSI (Very Large Scale Integrated) Circuit Design

Presented at EE1001
Oct. 16th, 2012

By Hua Tang

The First Computer

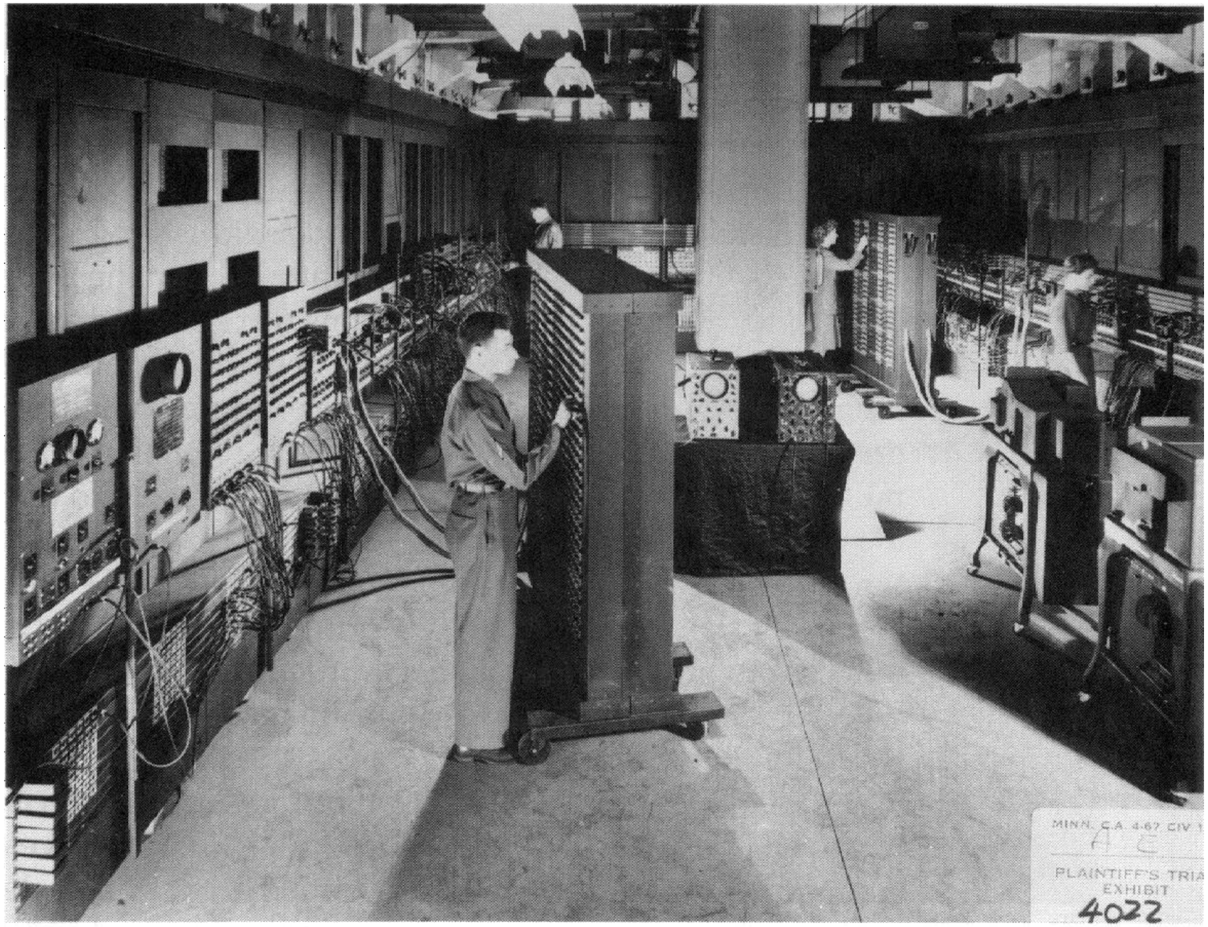


The Babbage Difference Engine (1832)

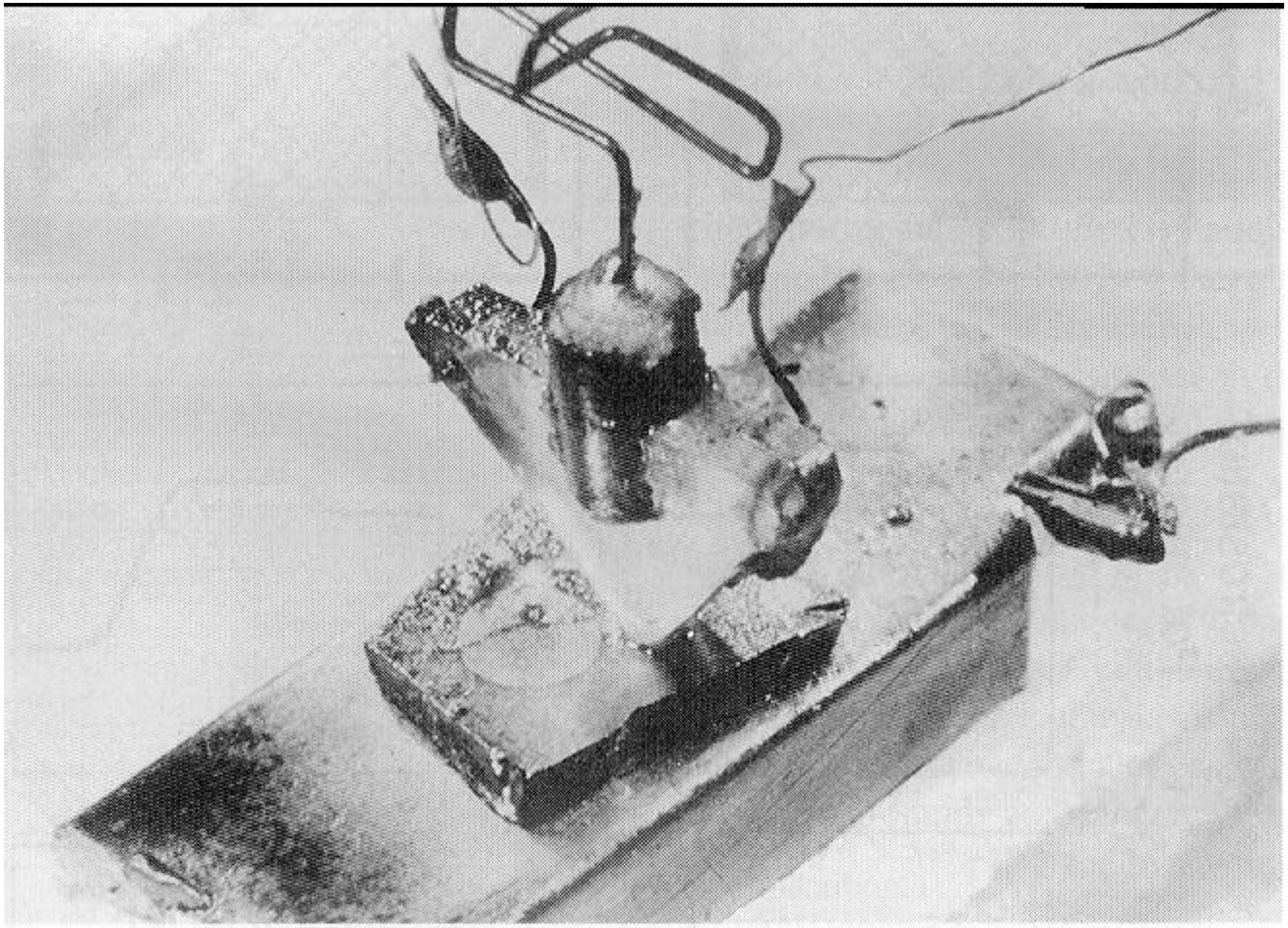
25,000 parts

cost: £17,470

The first electronic computer (1946)

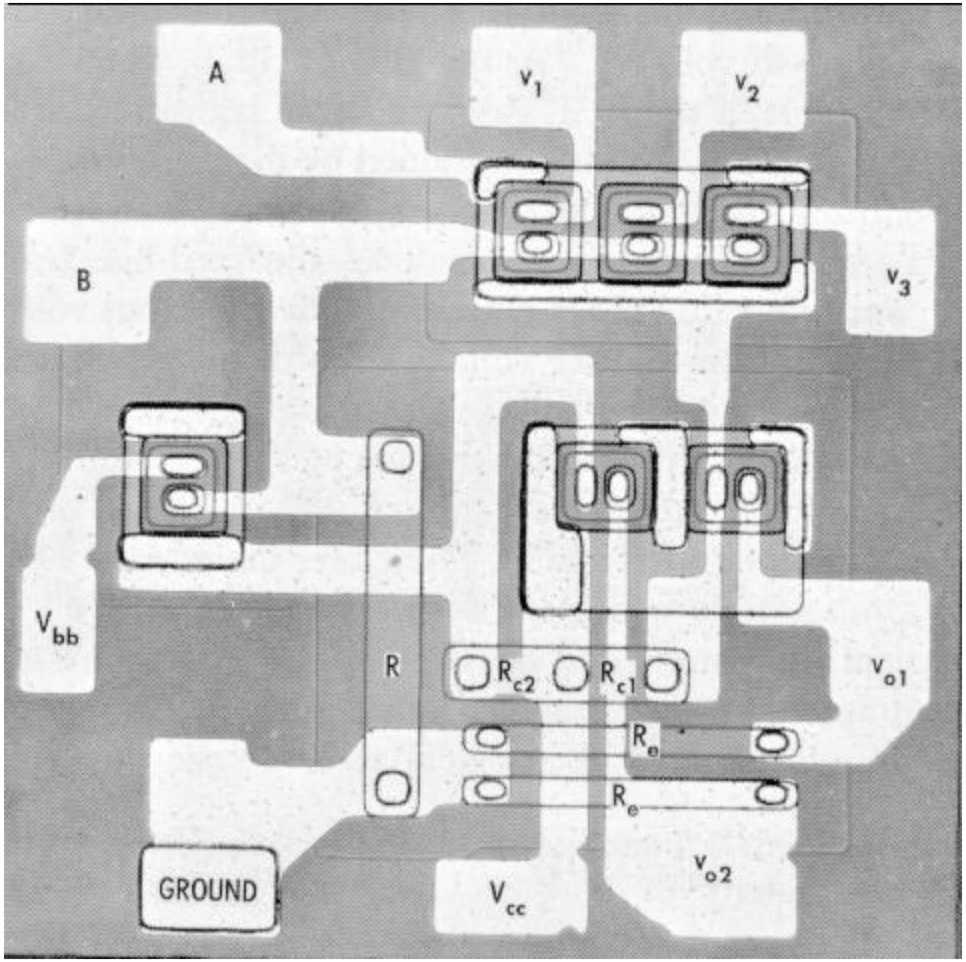


First Transistor (Bipolar)



First transistor
Bell Labs, 1948

The First Integrated Circuits

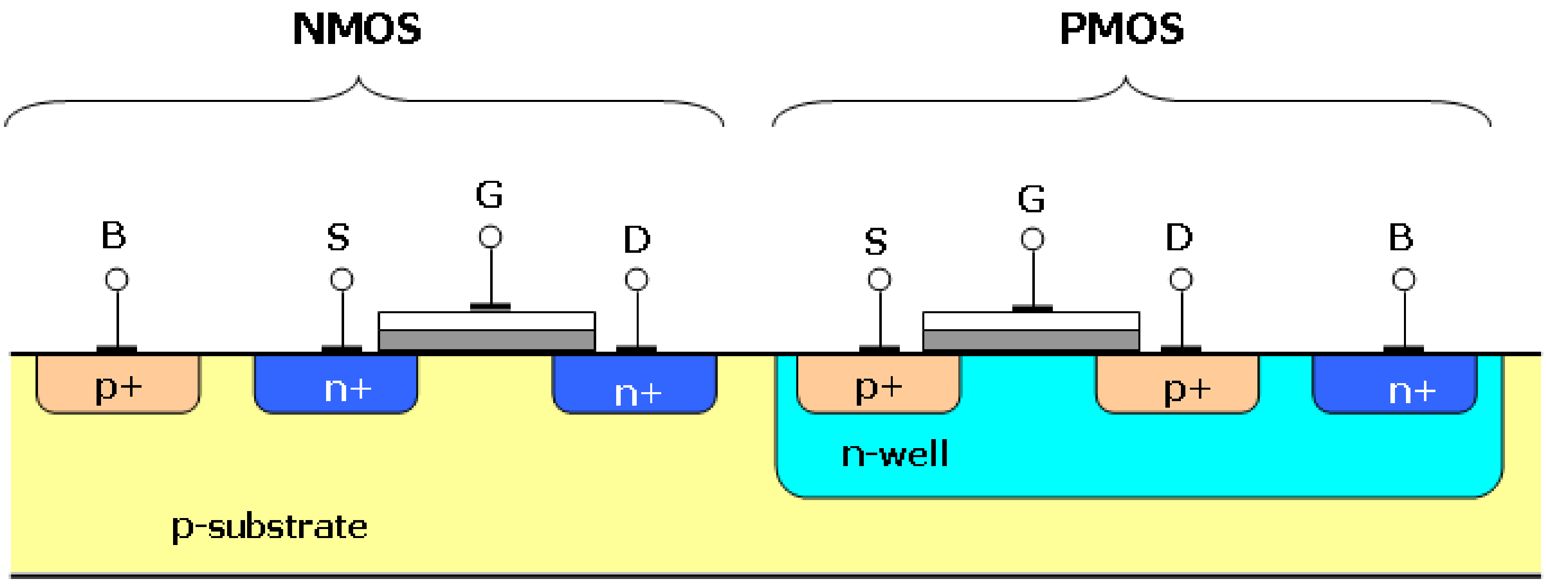


Bipolar logic
1960's

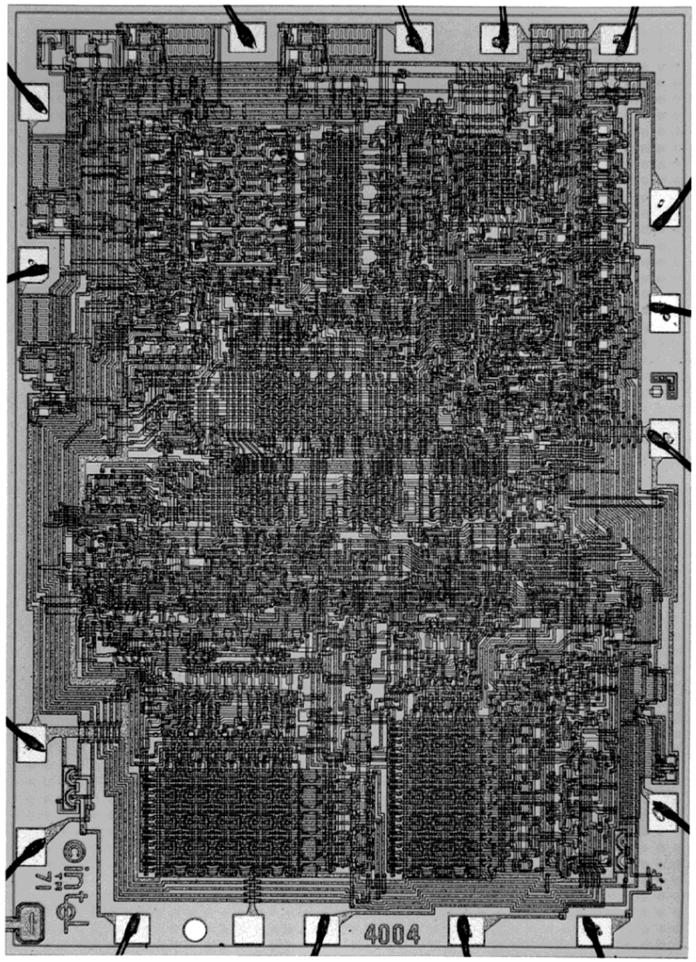
ECL 3-input Gate
Motorola 1966

Basic IC circuit component: MOS transistor

MOS: Metal Oxide Semiconductor

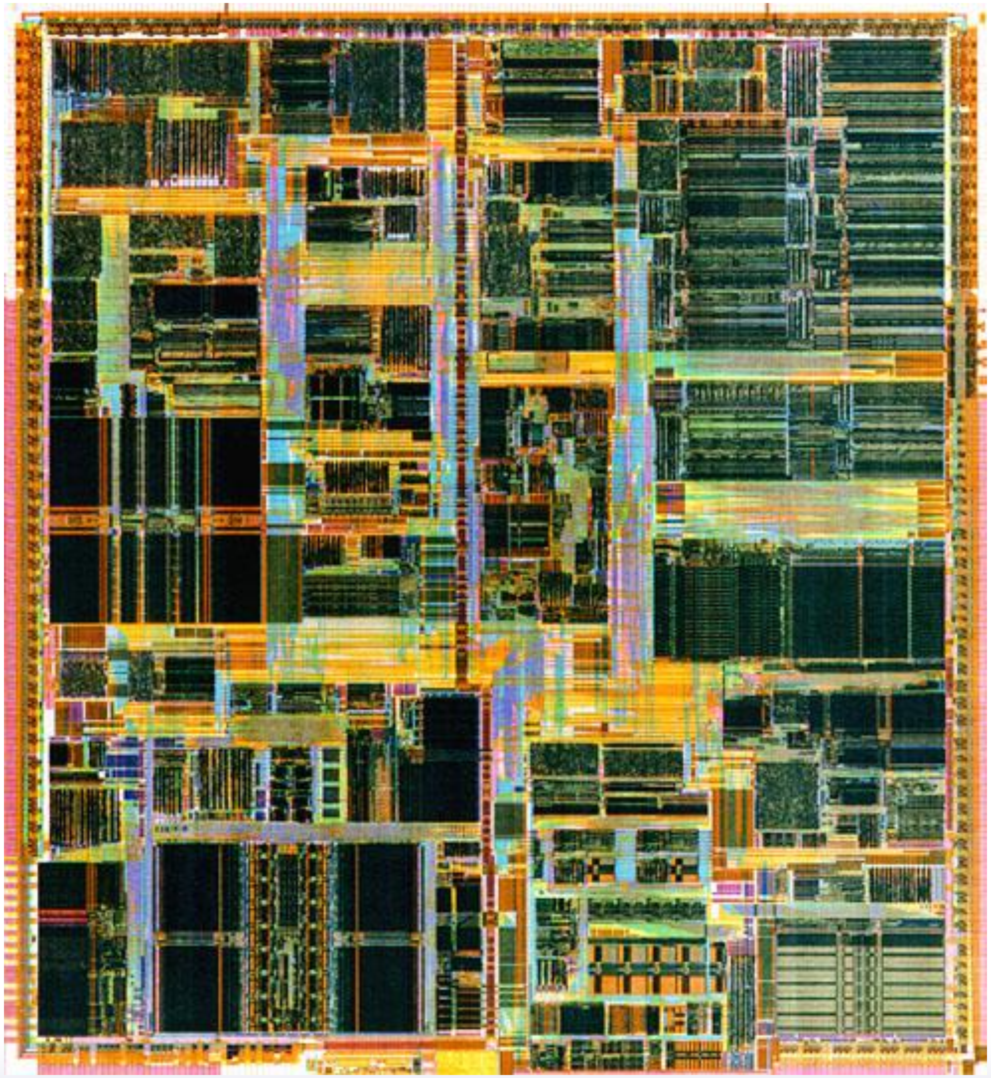


Intel 4004 Micro-Processor



1971
1000 transistors
< 1MHz operation
10μm technology

Intel Pentium (IV) microprocessor



2001
42 Million transistors
1.5 GHz operation
0.18µm technology

More recent Processors

2006
291 Million transistors
3 GHz operation
65nm technology

2007
800 Million transistors
2 GHz operation
45nm technology (the biggest change in CMOS transistor technologies in 40 years)

2010 Core i7
1.2 Billion transistors
3.3 GHz operation
32nm technology

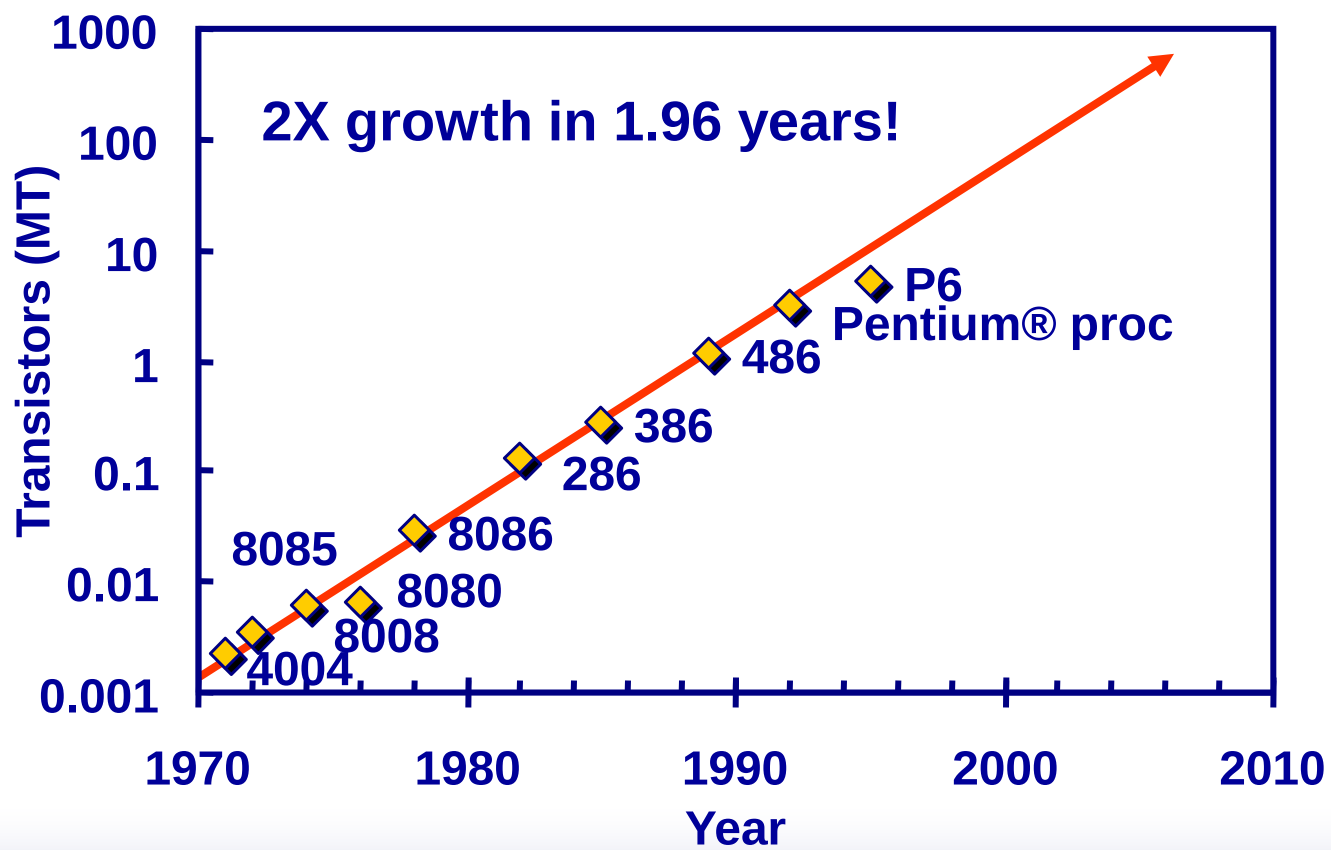
Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

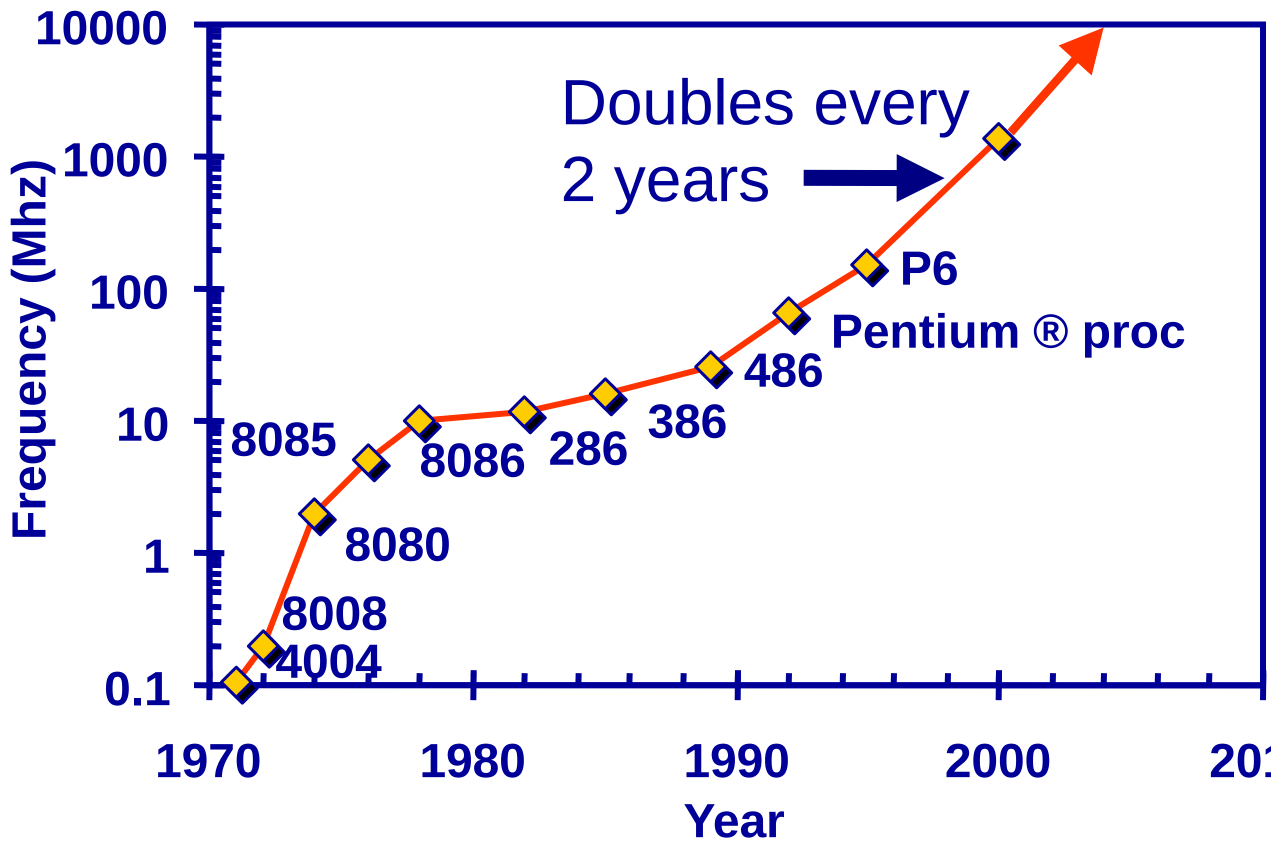
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's law in Microprocessors

Transistors on Lead Microprocessors double every 2 years



Frequency



Lead Microprocessors frequency doubles every 2 years

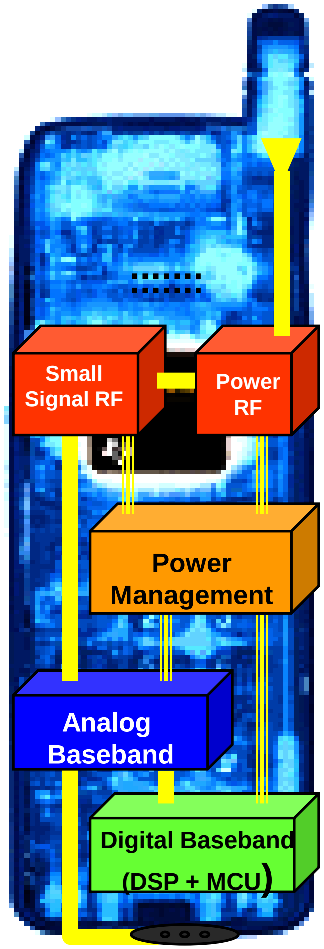
Not Only Microprocessors

Cell Phone

HDTV

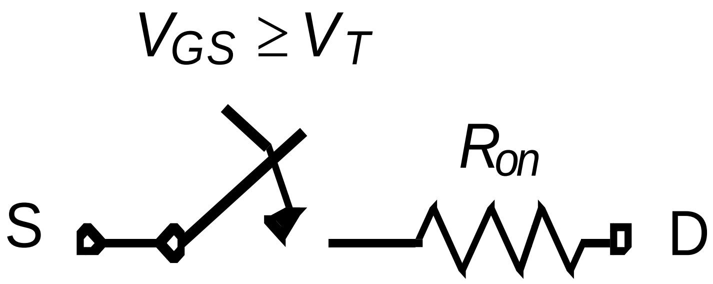
PDA

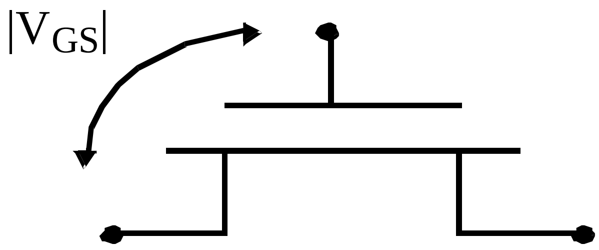
….



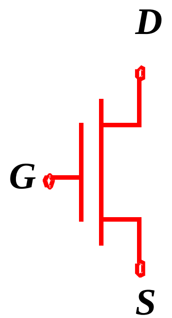
What is a MOS Transistor?

A Switch! An MOS Transistor



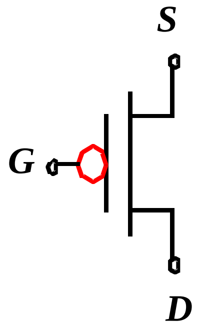


MOS Transistors - Types and Symbols



NMOS

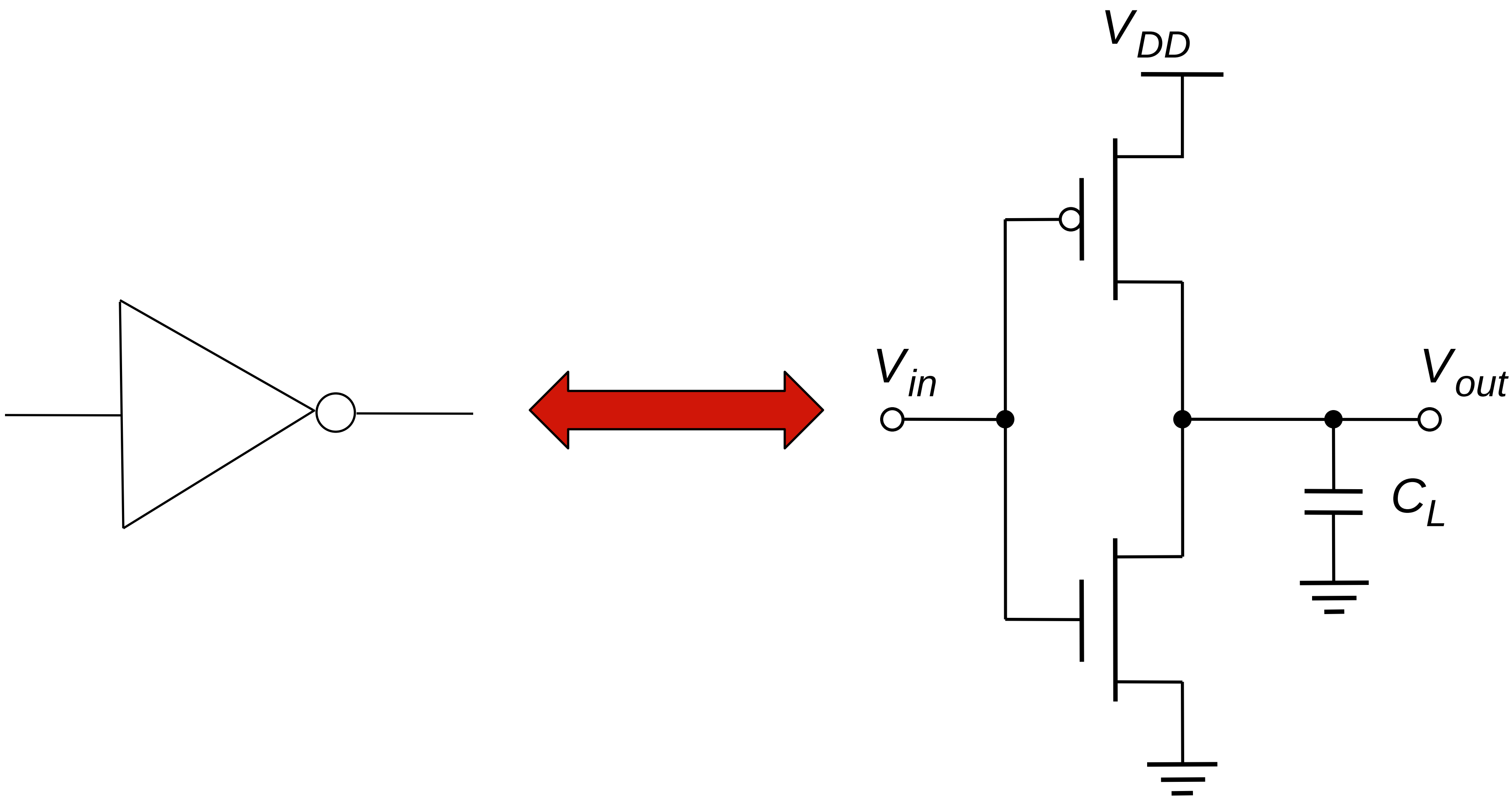
if *G*="1" or V_{dd}
switch on



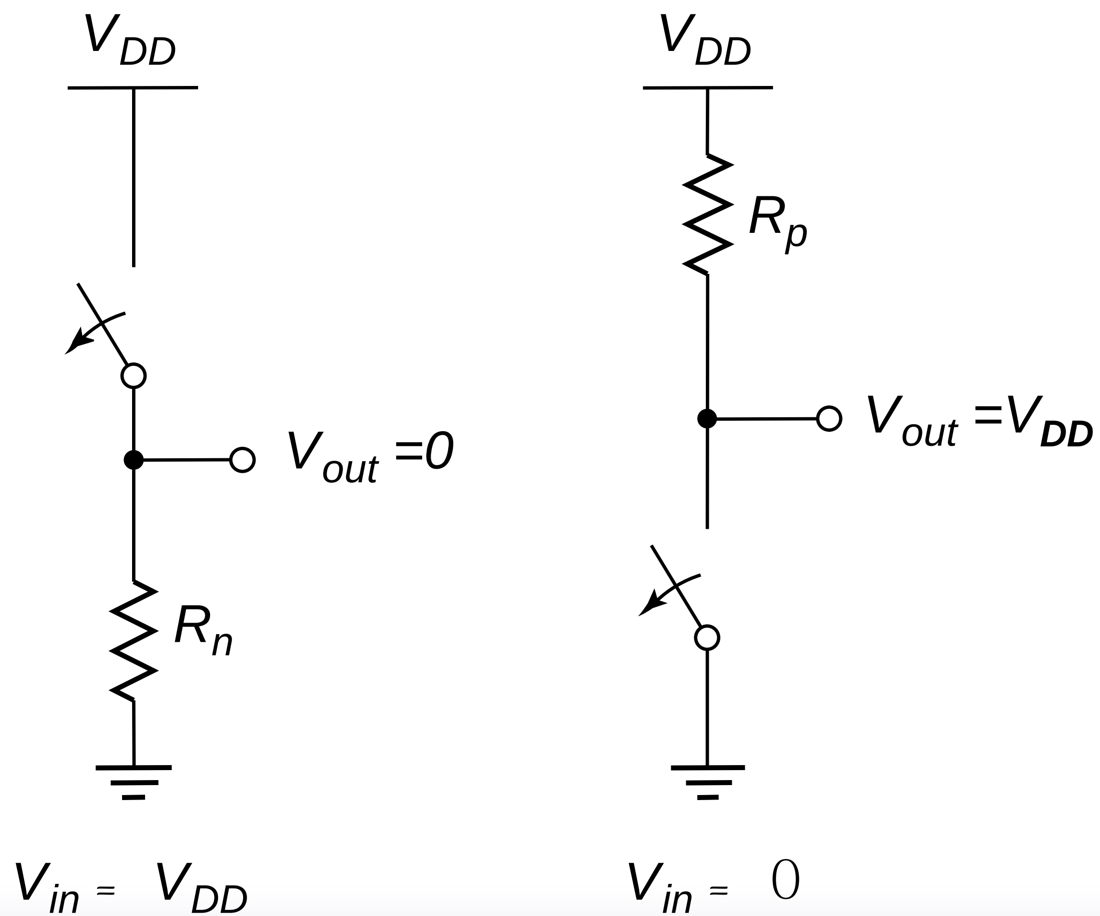
PMOS

if *G*="0" or ground
switch on

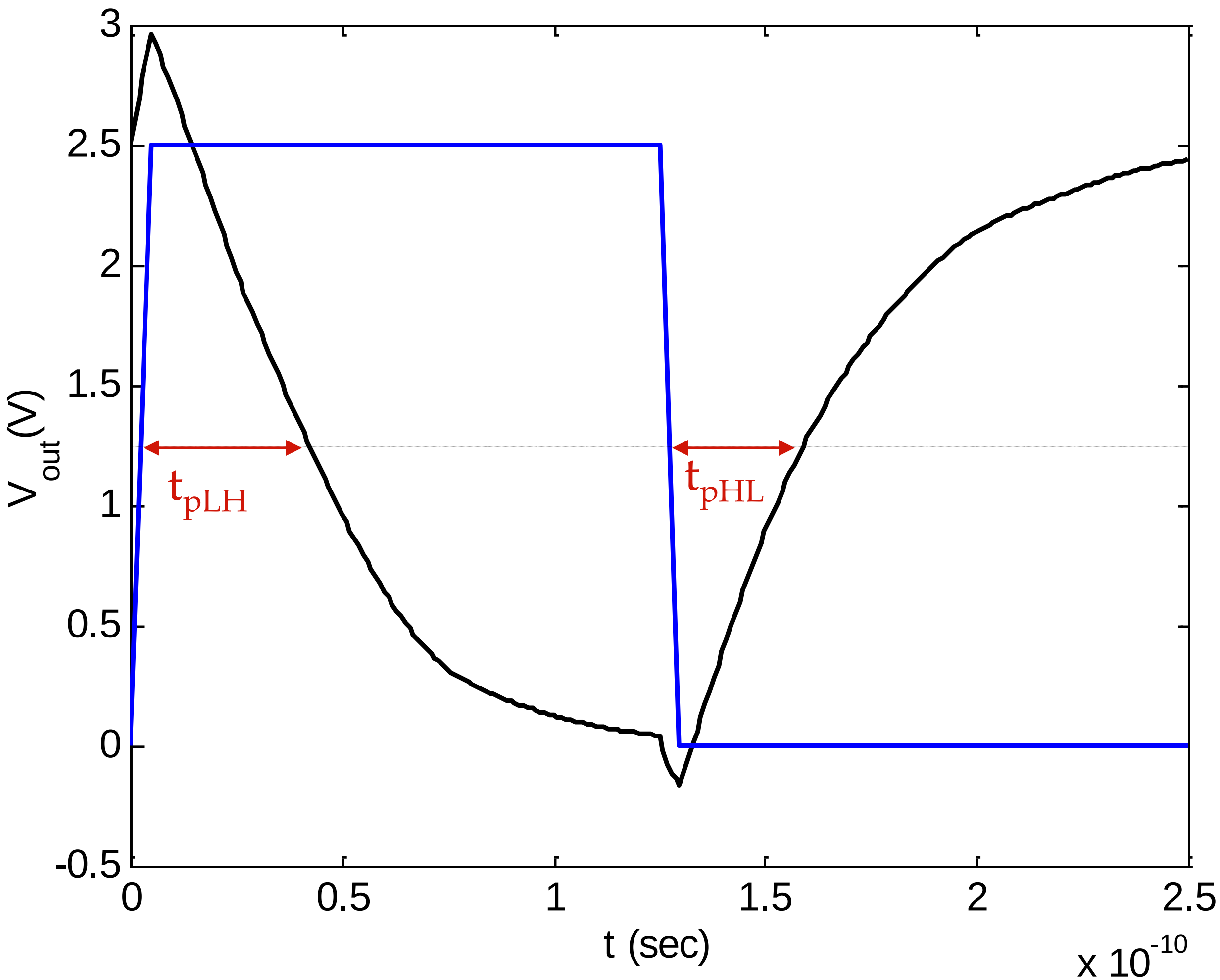
The CMOS Inverter: A First Glance



CMOS Inverter
First-Order DC Analysis

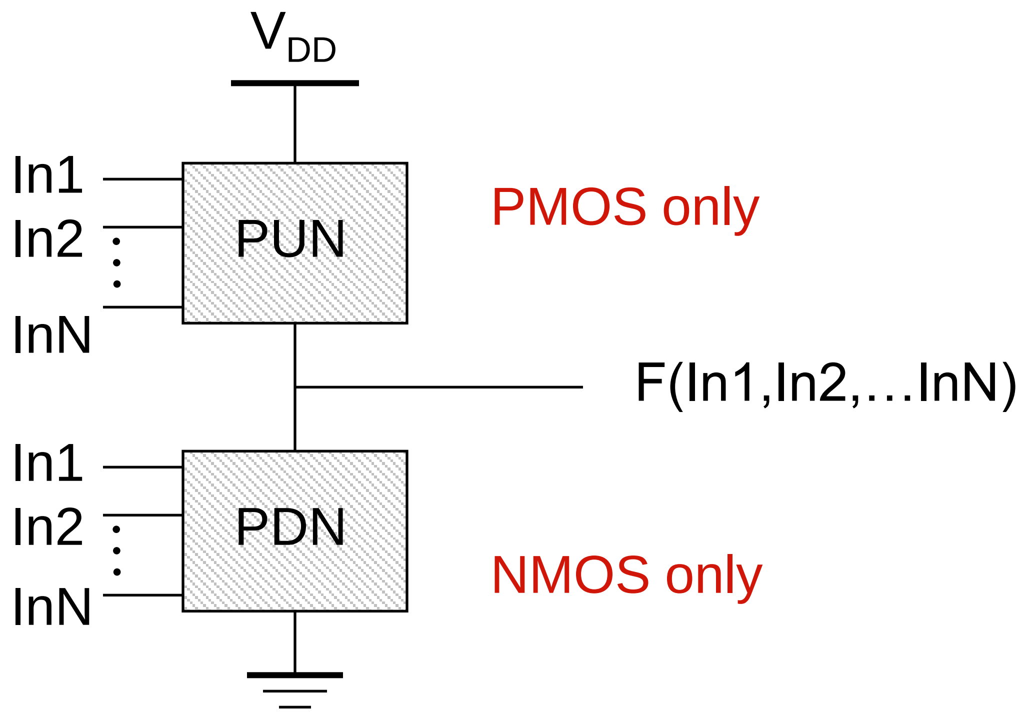


Transient Response



The delay Essentially determines the clock speed of the processor

Static CMOS (Complementary MOS)

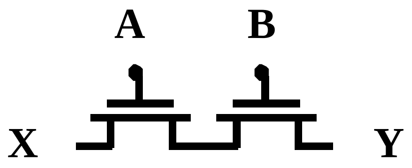


PUN and PDN are dual logic networks

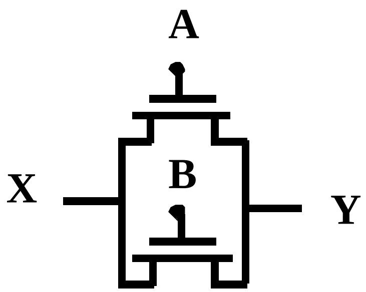
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

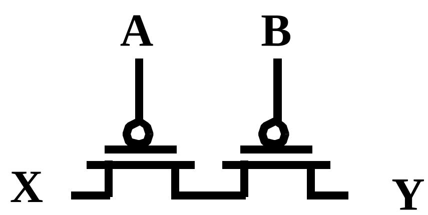


Y = X if A OR B

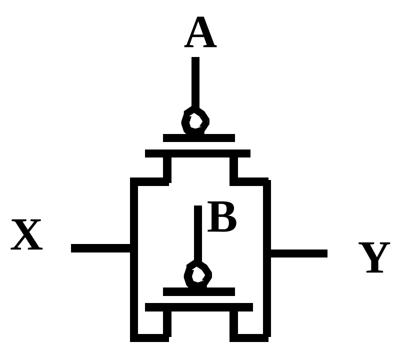
NMOS Transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\bar{A}$ AND $\bar{B} = \overline{A + B}$



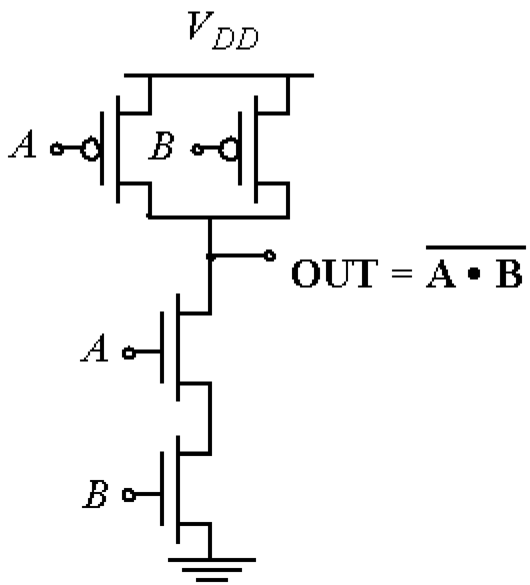
$Y = X$ if $\bar{A}$ OR $\bar{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: $G = A\,B \Rightarrow$ Conduction to GND

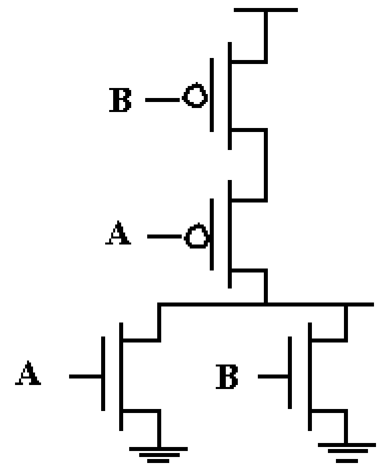
PUN: $F = \overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

Example Gate: NOR

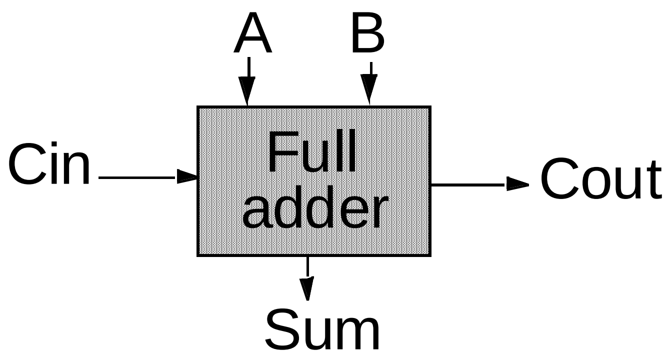
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



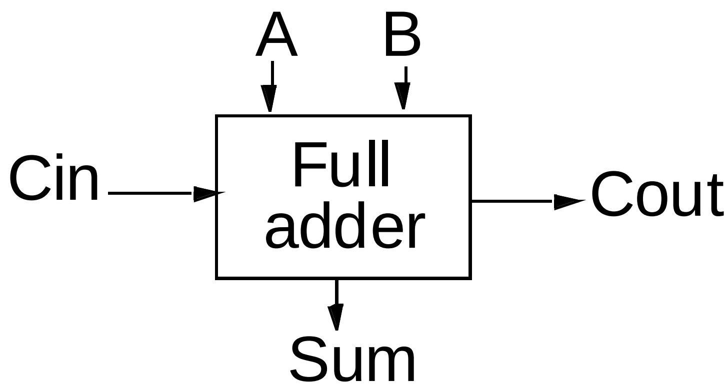
$$OUT = \overline{A + B}$$

Full-Adder



A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Binary Adder

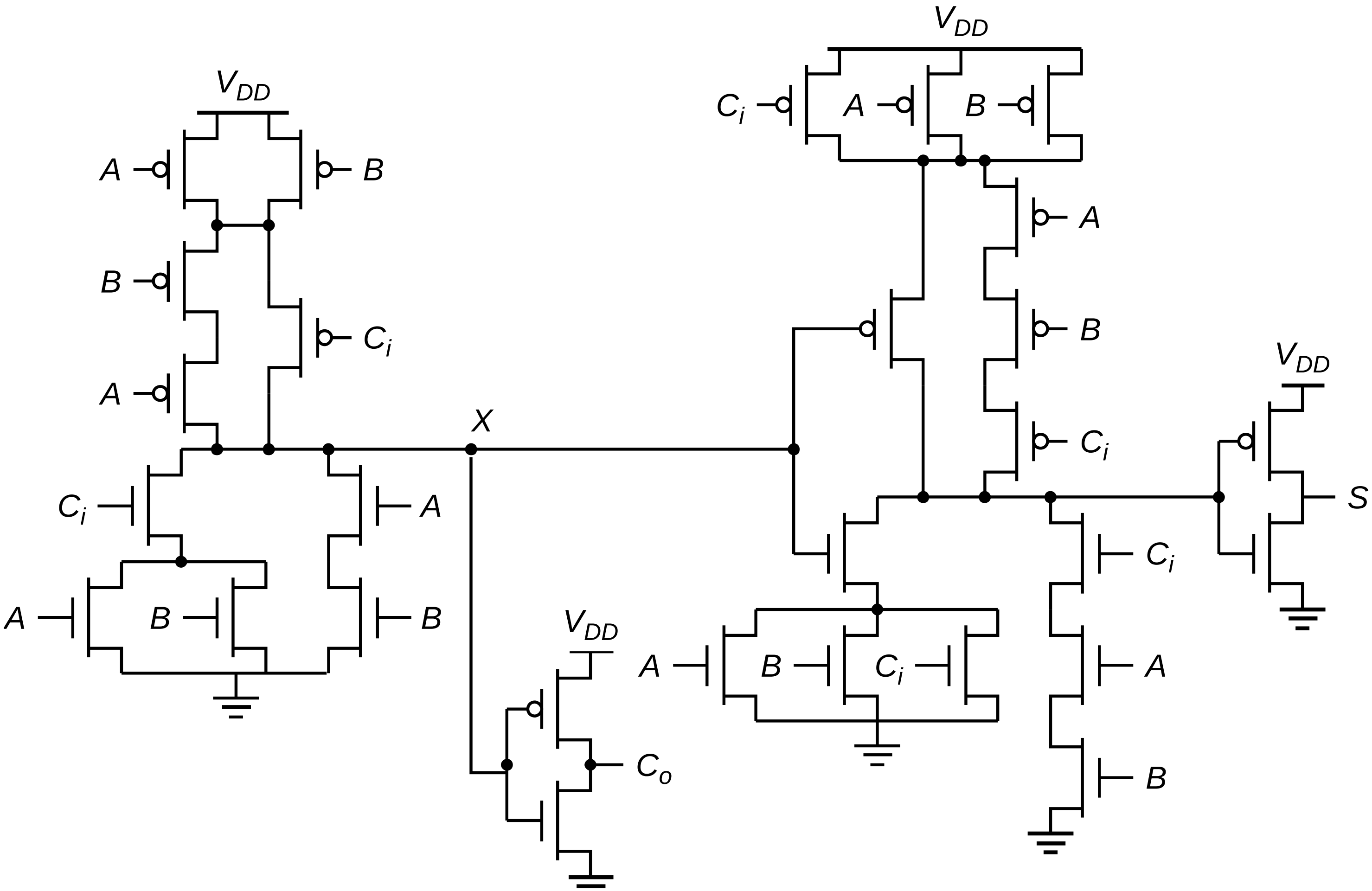


$$S = A \oplus B \oplus C_i$$

$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$

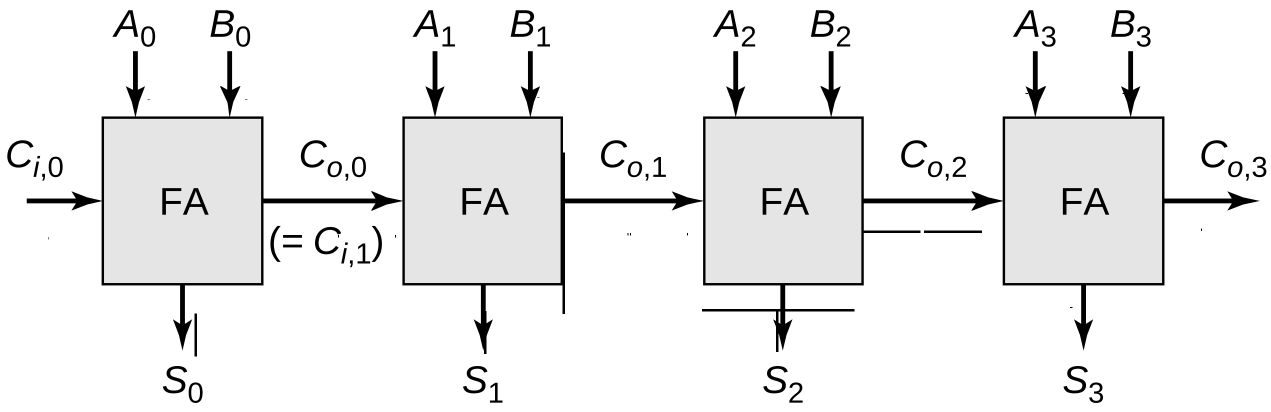
$$C_o = AB + BC_i + AC_i$$

Complimentary Static CMOS Full Adder

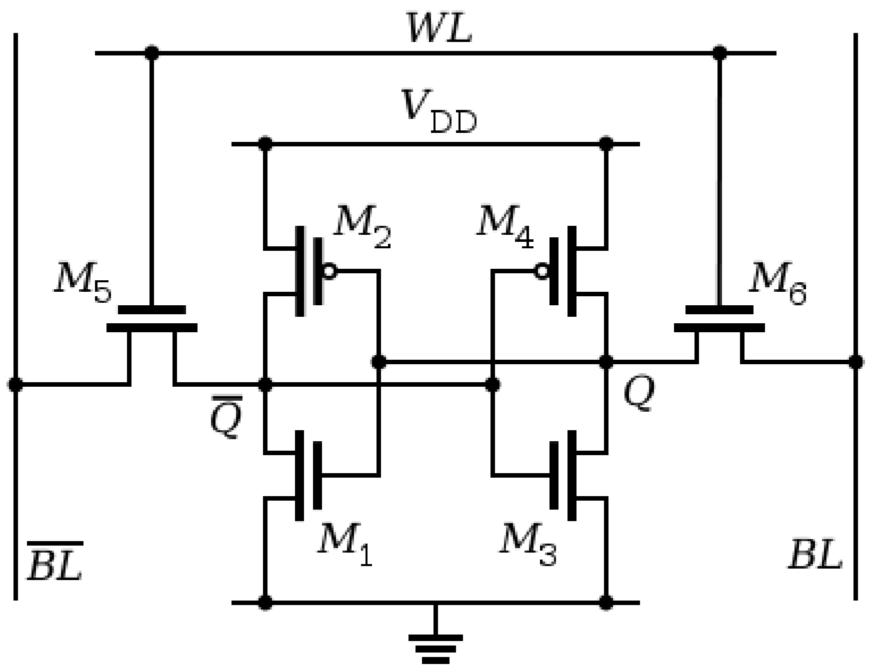


28 Transistors

The Ripple-Carry Adder



SRAM Memory cell



The add-up

32-bit adder:	>3,000
32-bit comparator:	>3,000
32-bit multiplier:	>50,000
1k SRAM:	6,000

…

Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

Future Design Challenges

- Processor architecture (multiple-core; interconnections)
- Semi-conductor materials (current leakage; process variation)
- Power consumption (power density; thermal dissipation)

Career in VLSI design

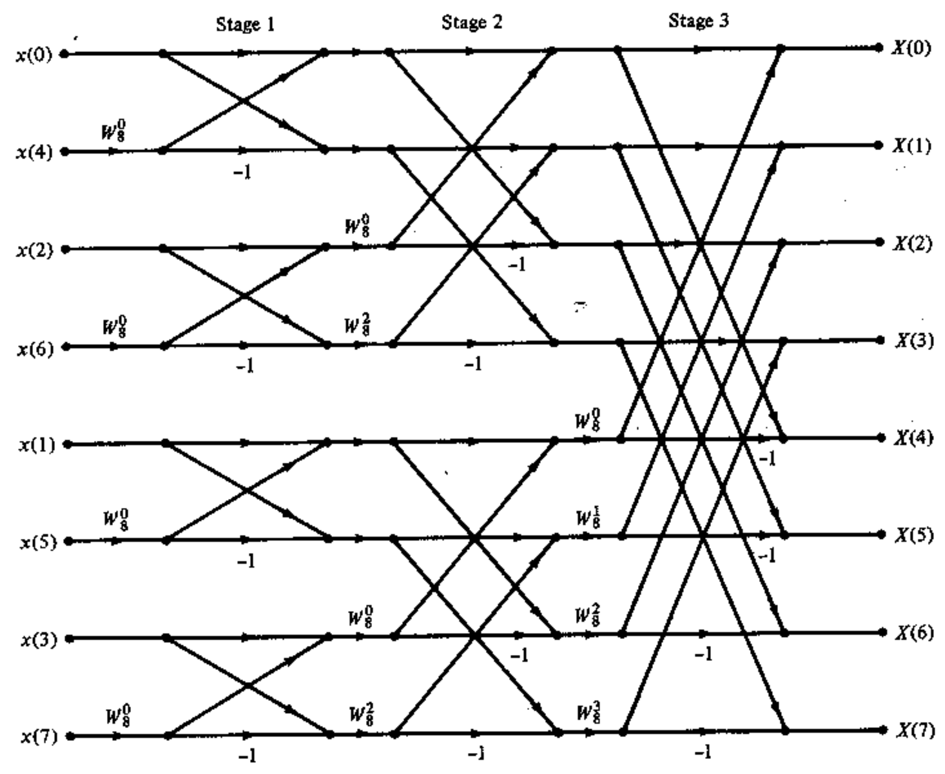
VLSI circuit design and design automation

- Intel, IBM, AMD, Texas Ins., Agilent,…
- Qualcomm, Broadcom, Samsung,…
- Micron, Seagate, WesternDigital…
- Cadence, Synopsys, MentorGraphics…
- Xilinx, Altera, ….

....

VLSI Design: FFT Butterfly

- Widely used in signal processing
- Design Butterfly Unit for 2-point FFT
- Components include multiplier, adder, subtractor, and data management

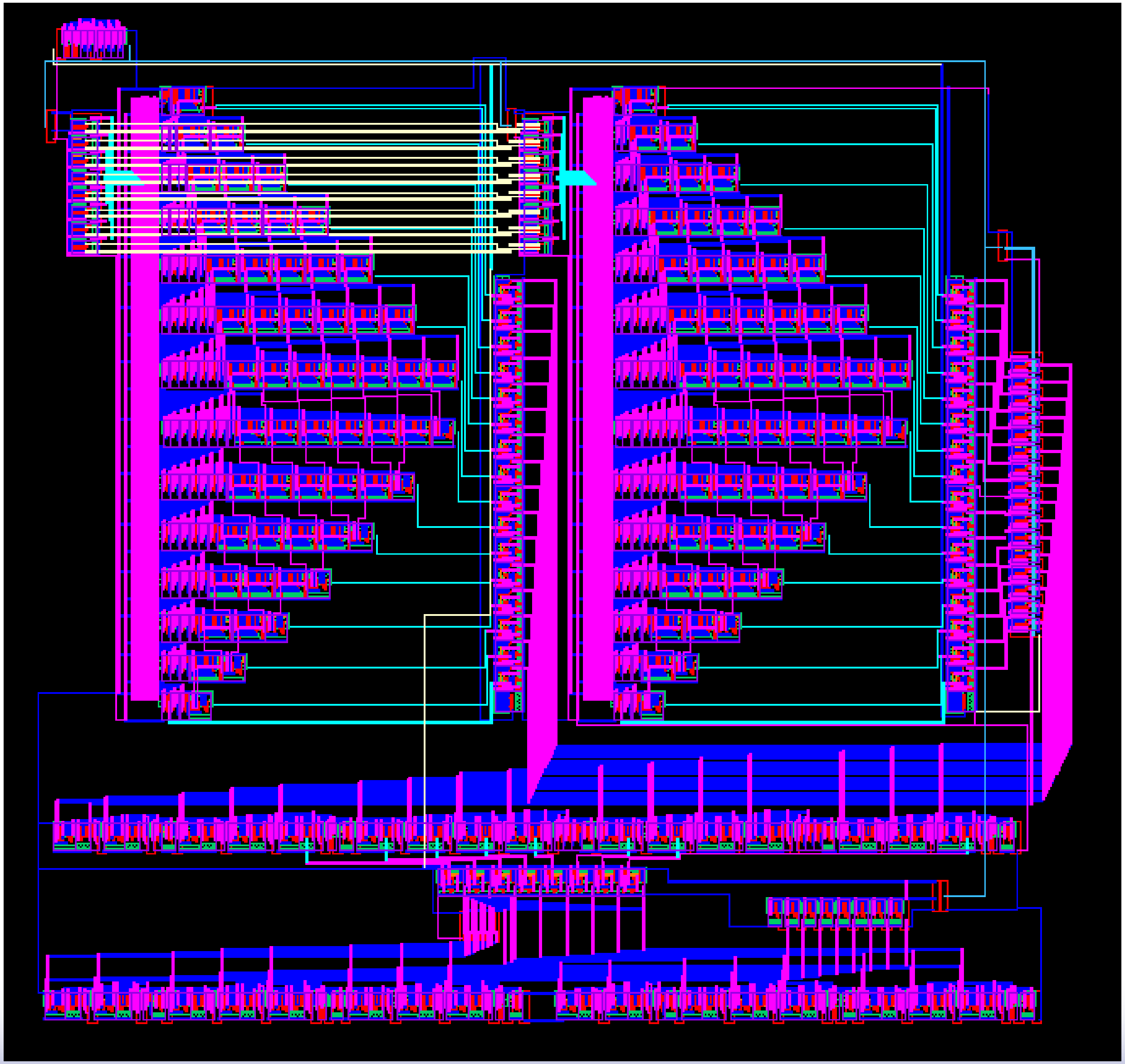


8-point FFT composed of 12 butterflies

Image from www.cmlab.csie.ntu.edu.tw/cml/dsp/training/coding/transform/fft.html

By: Spencer Strunic
Matt Webb

FFT Butterfly Unit Layout

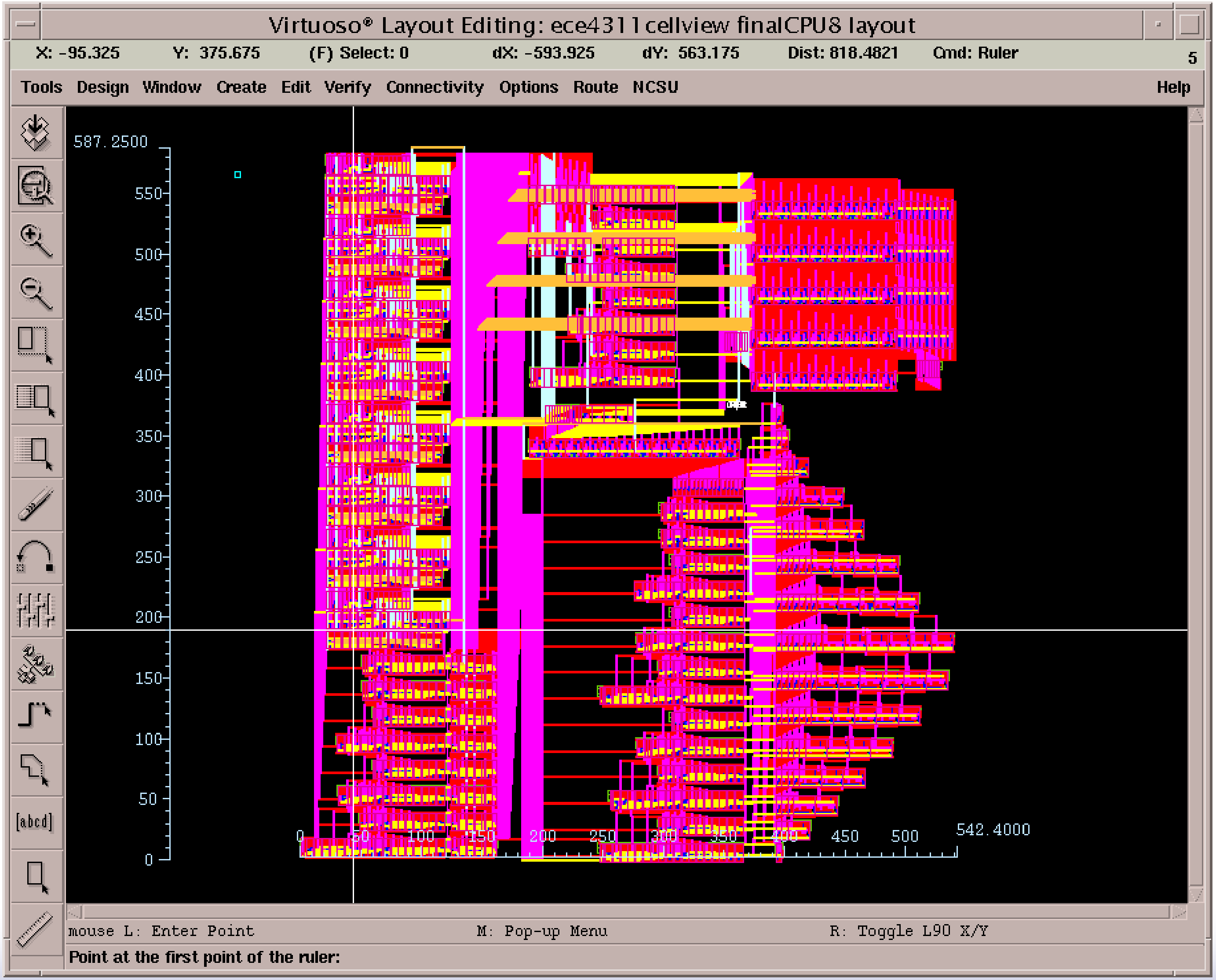


VLSI Design: 8-bit CPU

- Registers
  - Store data
  - Manipulate data
- ALU
  - Select between many different operations to output
- Adder
  - Adds two 8-bit numbers
- Multiplier
  - Multiplies two 8-bit numbers

By: Brian Linder
Matt Leines

8-bit CPU Layout



FIR Filter

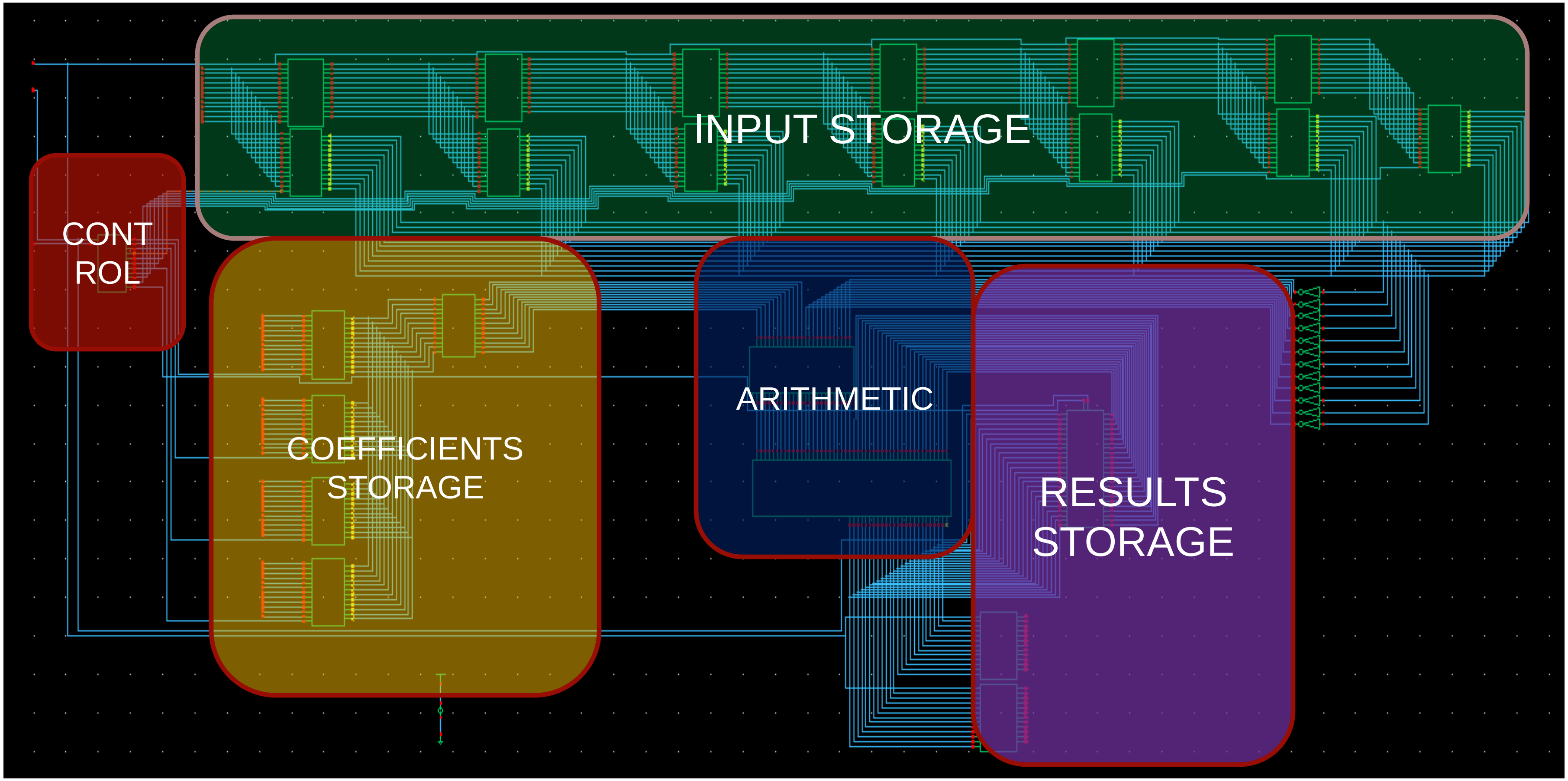
- FIR – Finite-Impulse Response
- Involves calculations of finite convolution sums in discrete-time systems
- Useful for Digital Signal Processing
- Equation -

$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k]$$

- *x* is the input signal, *h* is the finite impulse response, *y* is the sum output and *N* is the order of the filter

By: Craig Bristow
Joliot Chu

FIR Filter System Design



Module 1 – Control Module

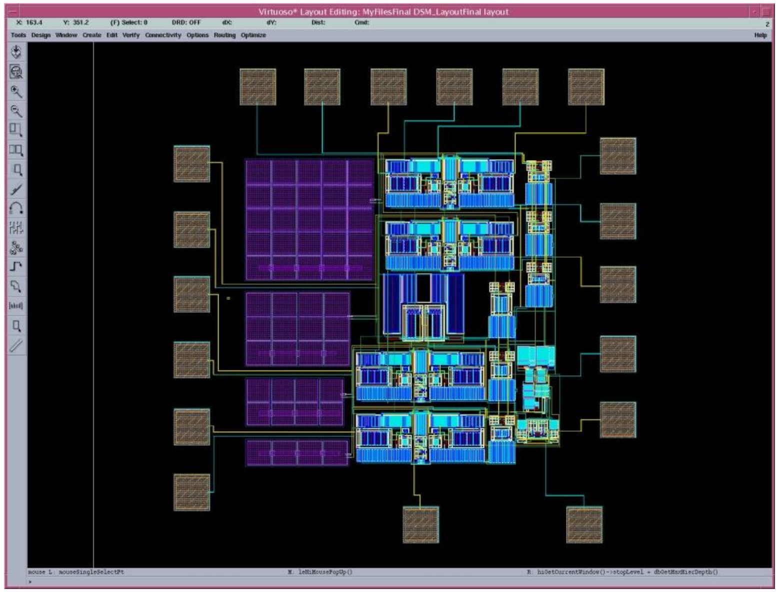
Module 2 – Input Module

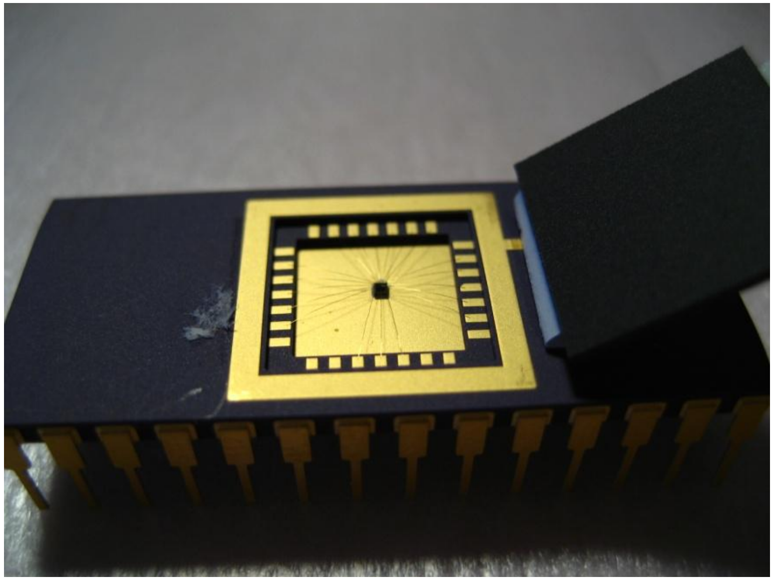
Module 3 – Coefficients Module

Module 4 – Arithmetic Module

Module 5 – Results Storage

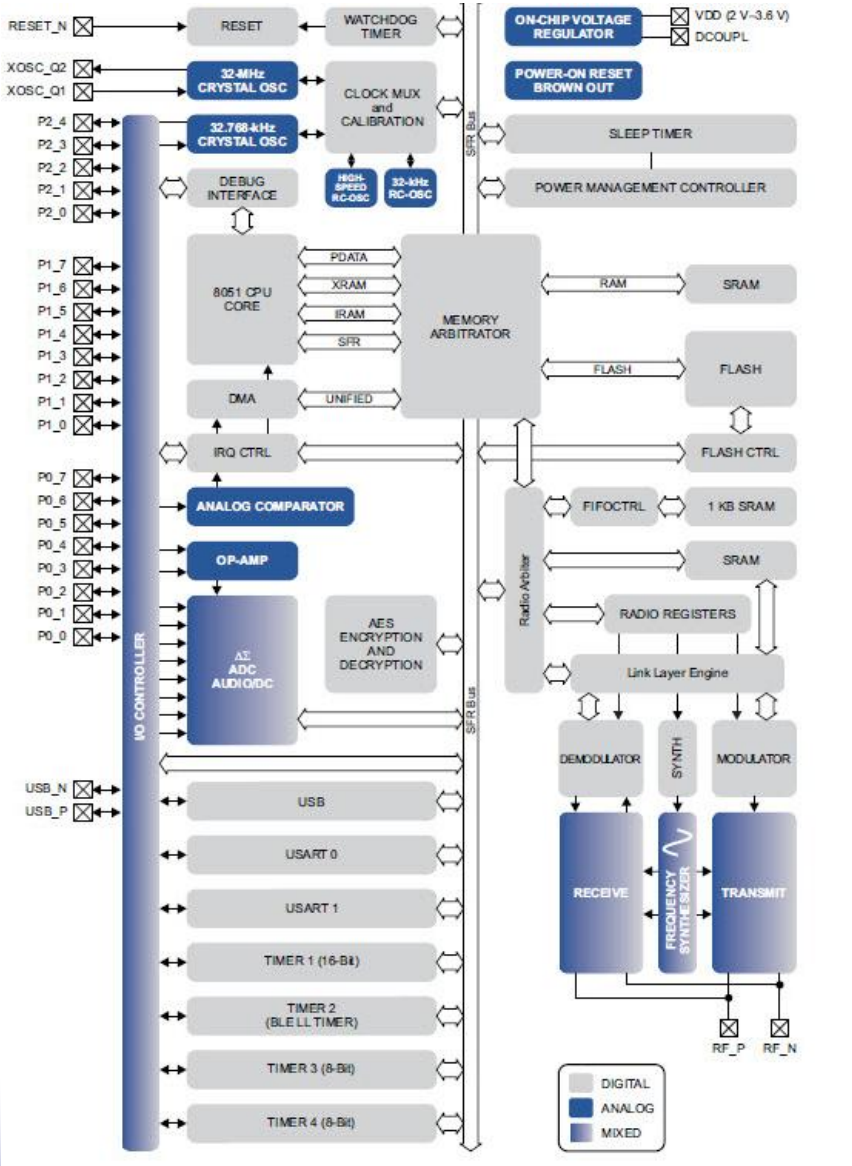
A Delta-Sigma Converter for WCDMA

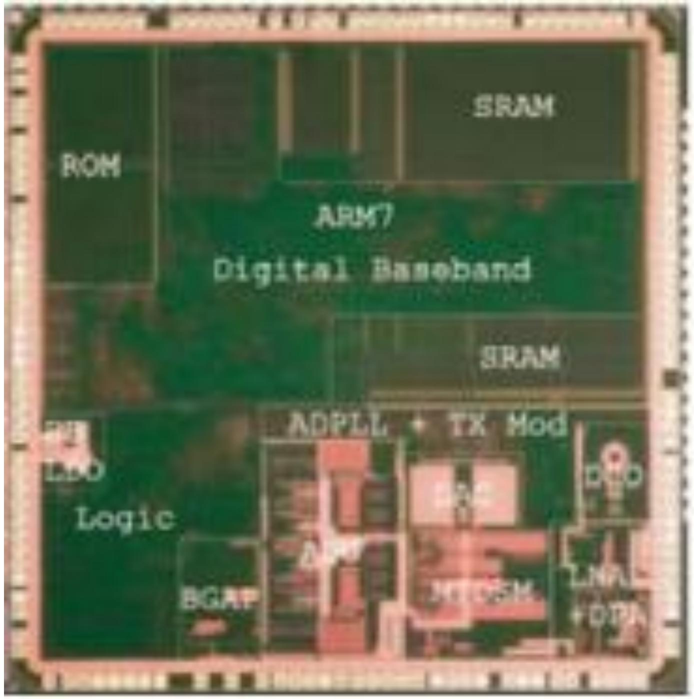




By: Matt Webb, Hairong Chang

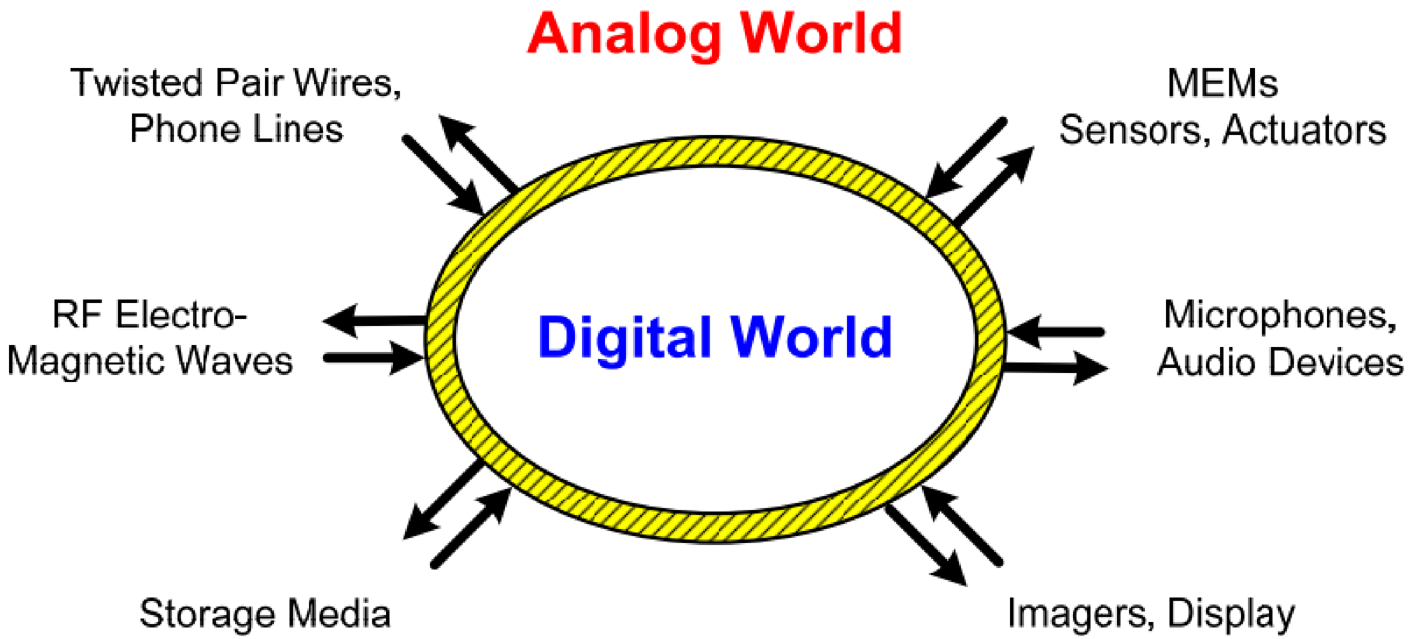
Nowdays, many electronic systems on a single chip have both analog and digital (called Mixed-signal SoC (System on Chip))





From Texas Instruments

Why A-D Interface?



- Nature is analog, not digital.
- A-D interface's role is "translator".

Contact Information:

Office:	MWAH 276
Hour:	3-5pm MW
Phone:	726-7095
Email:	htang@d.umn.edu
Http:	www.d.umn.edu/~htang