Thermal effects and junction temperature evaluation of Power MOSFETs

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Introduction

In modern power supply design, more and more attention is given to the electrical efficiency of the overall system and to the junction temperature of semiconductor devices, which handle the conversion of power to a usable form.

Among all semiconductor devices, the transistor is by far the most important category. Nearly all of them are three-pin devices (MOSFETs, BJTs, IGBTs) and unlike diodes, they have a driving section which makes them more sensitive to issues related to the interaction between power handling and the input signal. The aim of this application note is to illustrate the method to evaluate the thermal stress on power MOSFET devices when they are used in switch mode power supplies. By this computation and with the physics characteristics of the device, it is possible to predict the temperature reached inside the junction, and the allowable margin or heatsink required to assure that the system has a suitable thermal margin during operation. This approach is fundamental because correct computation allows more accurate evaluation of system lifetime and assures working operation within the SOA.

Contents

1 Description

Since the purpose of this application note is to illustrate a method to evaluate the thermal stress generated on power MOSFET devices during normal or accidental operation, it is important to begin with some discussion on MOSFET structure. In order to simplify the theoretical approach, a planar structure is used as a reference [1]. Here, it is possible distinguish the gate, source, and drain regions. These areas are easily identified, but since the interfaces between them are functions of the voltage applied, an equivalent electrical circuit reports static and variable parameters.

Figure 1: Power MOSFET structure
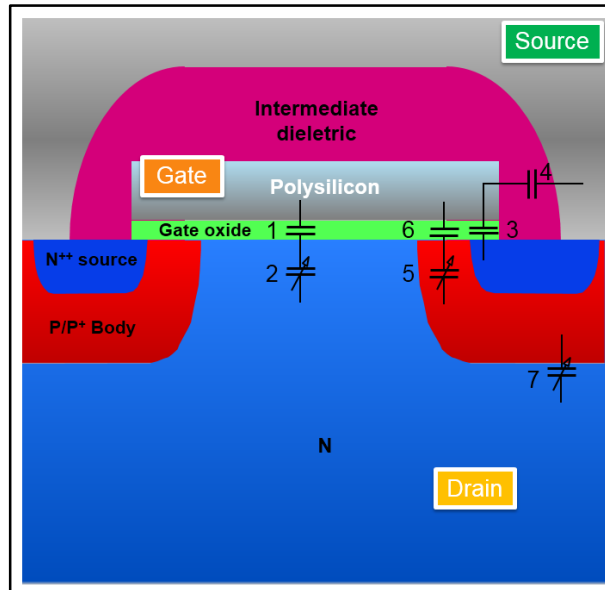
Although in *Figure 1*, the gate, source and drain regions are easily identified, it is difficult and inaccurate to represent them with a fixed capacitance value. Due to the relationship to the applied Vds voltage, which modulates the depletion layers, the capacitances have a variable component, so on an electrical equivalent circuit, a series of fixed and variable capacitances are used to emulate the behaviors of the gate, source and drain pins. This type of model perfectly describes the usual capacitance graphs reported by semiconductor manufacturers on their MOSFET datasheets. In *Figure 2*, those parameters are highlighted.

Figure 2: Power MOSFET intrinsic capacitance
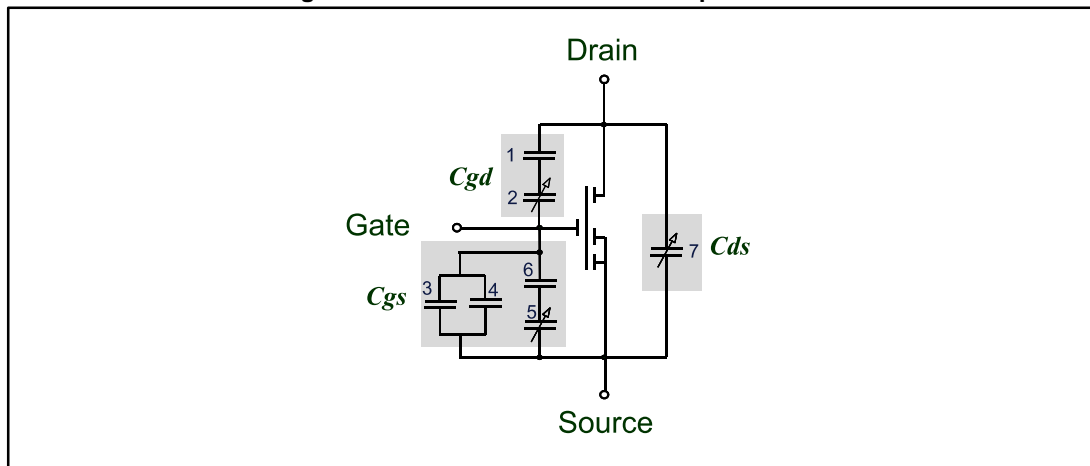
The diagram above summarizes and simulates the behaviors of the parasitic capacitances of the MOSFET.

The analysis of the MOSFET structure help us to understand the mode of operation of the device when used as a switch, and then to better explain its losses. In particular, in their technical documents semiconductor manufacturers report some electrical measurements performed under standard conditions. With those parameters, using a theoretical approach, it is possible to estimate the power losses on a MOSFET device when used as a switch. Before proceeding, it is important to note that the behaviors of the devices are strongly linked to the circuit where the device operates, and then to the type of load (resistive, inductive or capacitive).

2 Thermal considerations

The term "junction temperature" became popular in the early days of semiconductor thermal analysis when semiconductor devices became the prominent power technology. With the concept "junction temperature", it is assumed that the die's temperature is uniform across its top surface; in other words, the whole die's surface has the same temperature. This is a simplified approach because it ignores the fact that x-axis and y-axis thermal gradients always exist and can be large during high power conditions or when a single die has multiple heat sources or source connections.

The basic principles of thermal analysis are similar to those in the electrical domain. It is possible to make a comparison between the thermal domain and the electrical domain by identifying the main parameters on each single domain. As in an electrical circuit, it is possible to model the thermal behaviors using voltage sources, resistance and capacitance. These elements, connected in a suitable ways, can be used to predict and evaluate the thermal performances of semiconductor devices. Before going deeper into the details, another very important aspect must be highlighted. In a thermal study, the mode cannot be omitted as the heat is transferred from the source to the ambient. Since the goal of this document is to provide a thermal overview for semiconductor devices used in electronic applications, to complete the analysis the thermal transfer mode must also be investigated. In this specific ambient, the thermal transfer can be summarized in two main modes, convection and radiation. These two thermal transport mechanisms will be discussed later.

3 Rth as thermal resistance

As introduced previously, it is possible to do a mirrored analysis on the thermal domain by studying an electrical network where voltage sources, resistance and capacitance represent and simulate the thermal behaviors of physics components.

Figure 3: Dualism of electric resistance with thermal impedance
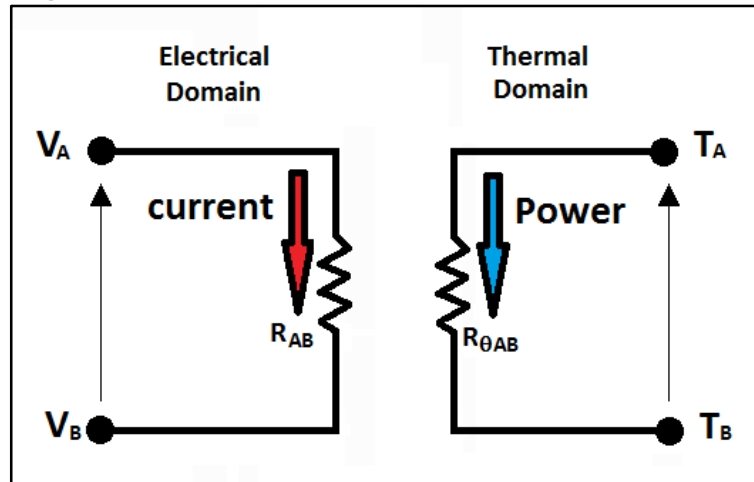
Each single domain is characterized by two main physical characteristics. In the electrical domain, current and electrical potential are the main parameters. The current, I, represents the flux of electrical carriers measurable when they move from a point A with electrical potential V_A to point B with V_B through a path characterized by an electrical resistance, R. The difference between them is indicated as V_A-V_B and the relationship between these physics characteristic is represented by the Ohm's law.

Equation 1

$\Delta V_{AB} = V_A - V_B = I \times R_{AB}$

A similar approach can be taken in the thermal domain where P represents the heat flux moving from a place with temperature T_A to another with T_B. The resistance that impedes the flow is indicated as $R_{\Theta AB}$.

The thermal domain is regulated by Fourier's law, but given the duality with the electrical domain, the relationship can be delivered and summarized in:

Equation 2

$\Delta T_{AB} = T_A - T_B = P \times R_{\Theta AB}$

The following table summarizes and compares the physics characteristics on the two domains.

Table 1: Physics characteristics of the two domains

Electrical domain			Thermal domain		
Variable	**Symbol**	**Unit**	**Variable**	**Symbol**	**Unit**
Current	I	A	Thermal power	P_D	W
Voltage	V	V	Temperature	T_X	°C
Electrical resistance	R	Ω	Thermal resistance	$R_{\Theta XY}$	°C/W
Electrical capacitance	C	F	Thermal capacitance	C_Θ	J/°C
$\Delta V_{AB} = I \times R_{AB}$			$\Delta T_{AB} = P_\Theta \times R_{\Theta AB}$		

This approach considerably simplifies the thermal study when semiconductor devices are used. For the thermal analysis it is very popular to refer to the following schematic:

Figure 4: Thermal model for silicon structure
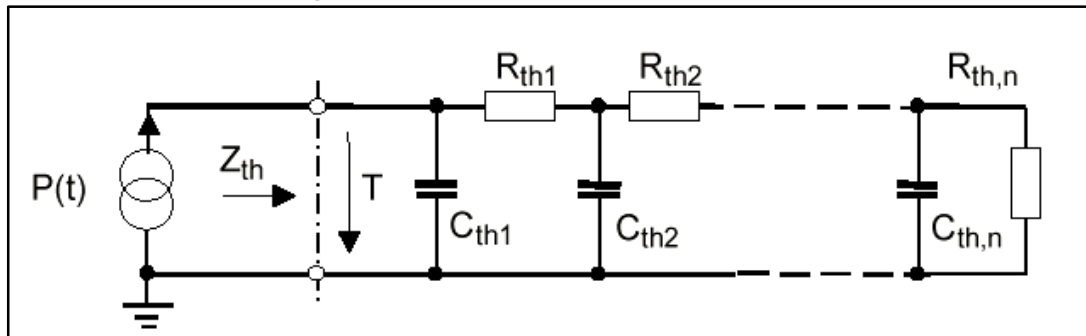
The thermal components take into consideration the physics factors of the semiconductor structure and the other physics elements that make up the component (MOSFET, IGBT, Bipolar). In particular, when the heat flows through a layer, we can model the thermal resistance offered by the layer with a relationship between the length (thickness), the area, and the thermal conductivity of the layer crossed by the heat flow.

Equation 3

$$R_{Th-layer} = \frac{Length}{k \cdot Area}$$

This relationship is true with thermal equilibrium. Instead, when a system is forced by a power pulse, the material thermal inertia of the structure does not allow temperature to rise instantaneously. This behavior is modeled by a layer thermal capacitance function of the volume (V), specific heat (c_p) and material density (ρ) of the layers crossed by the heat flow.

Equation 4

$C_{Th-layer} = \rho \cdot C_p \cdot V$

These two characteristics can summarize and describe the thermal aspect of a structure, and through them designers can make the right choice to manage the thermal aspect of their systems.

4 Thermal factors

As previously mentioned, there are several factors that influence the thermal behavior of silicon devices. In datasheets, usually thermal impedance and resistance are reported. Since the former describes the behaviors for fast transients, it is reported as a graph normalized with the thermal resistance. Fast transients are always considered instants wherein the structure involved in the thermal process can be restricted only to the package of the device. Using the K factor correction given by the graph, it is possible to estimate the increasing junction temperature due to a power pulse. In other cases, the time is longer. In this case, if the power pulse is enough to impact the external structure of the devices also, the thermal resistance must be taken into account.

**Figure 5: Thermal impedance for MOSFET devices**
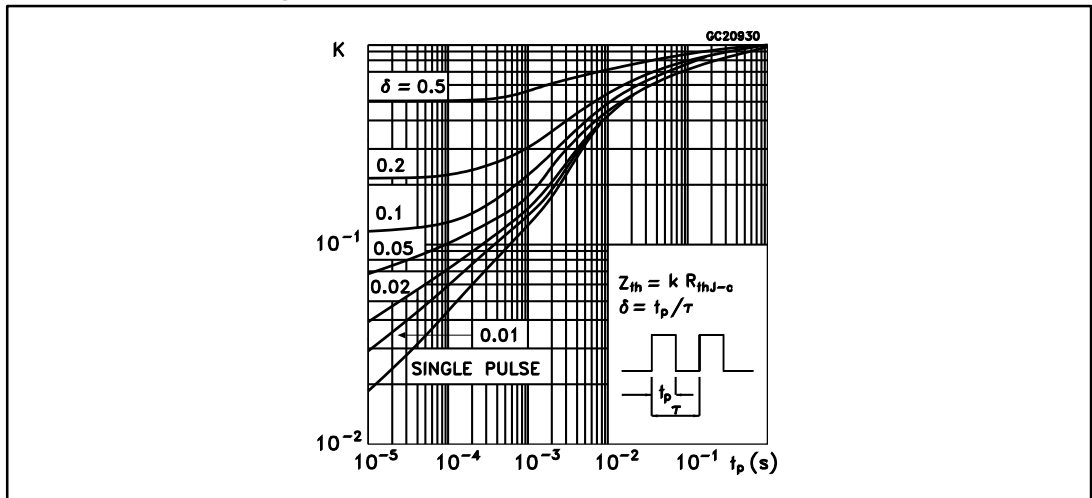
It is interesting to study what happens inside a device when the power pulse is very short. In the die model below, a MOSFET structure in a TO220 package is shown.

Figure 6: MOSFET die model
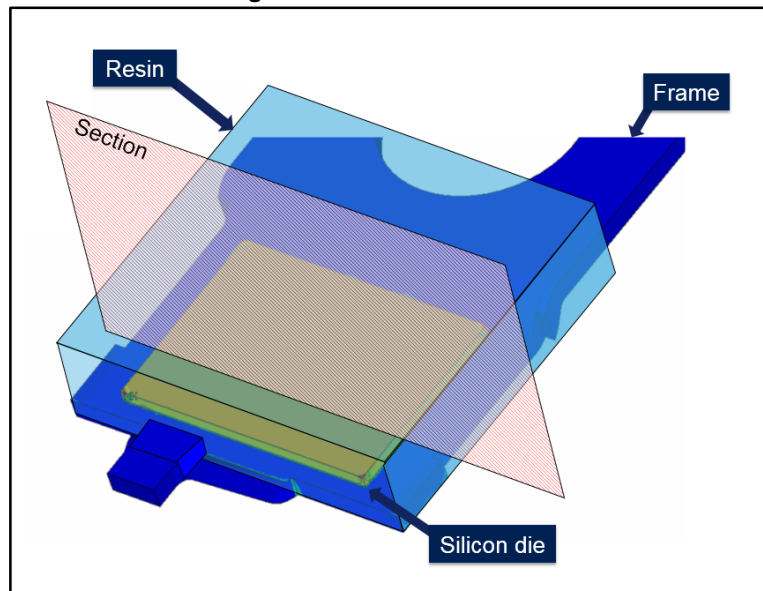
As it is possible to note, the silicon die is attached to the frame by a preform and the whole structure is encapsulated in a resin. Hereafter, all analyses will be referred to the section as reported below.

Figure 7: Section of a MOSFET structure
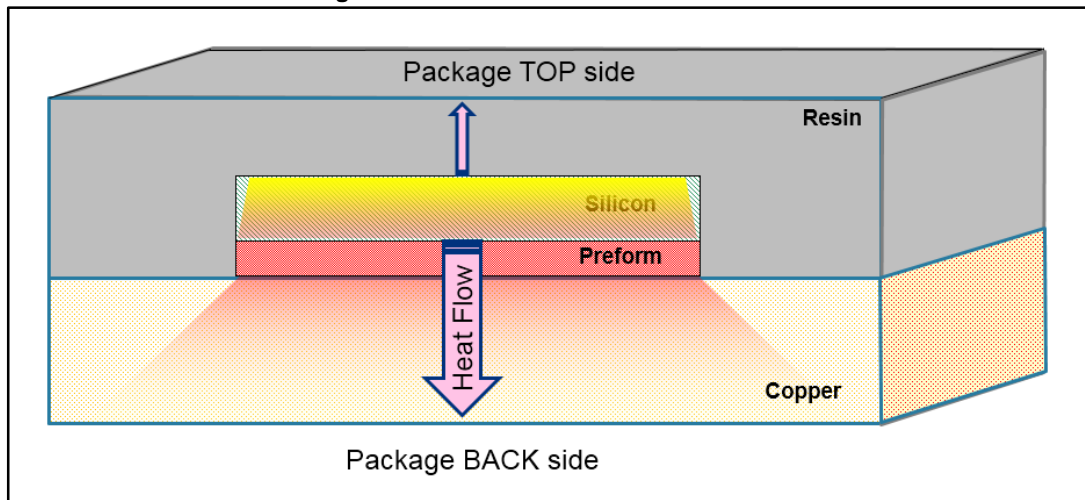
Since the conductivity of the resin is very low, the heat generated by the silicon die has as its preferred path the back side where the conductivity of the copper is higher. The power generated within the die changes the device temperature, increasing it according to the thermal capacitances and resistances of the layers involved, from the silicon to the package back side. As a thermal model, one similar to that reported in *Figure 4* can be used.

The behaviors of the structure can be derived by the previous model and the time power pulse helps to choose the right parameter to use.

If the power pulse applied to the MOSFET is very short (lower than 1 msec), the power generated is limited to the die. On it, the channel temperature starts to increase according to the specific heat and the thermal conductivity of the silicon structure only. Since the time is very short, the structure involved is only the die and the temperatures of the preform and frame remain substantially unchanged.

Figure 8: Cross section when Tpulse is lower than 1 msec
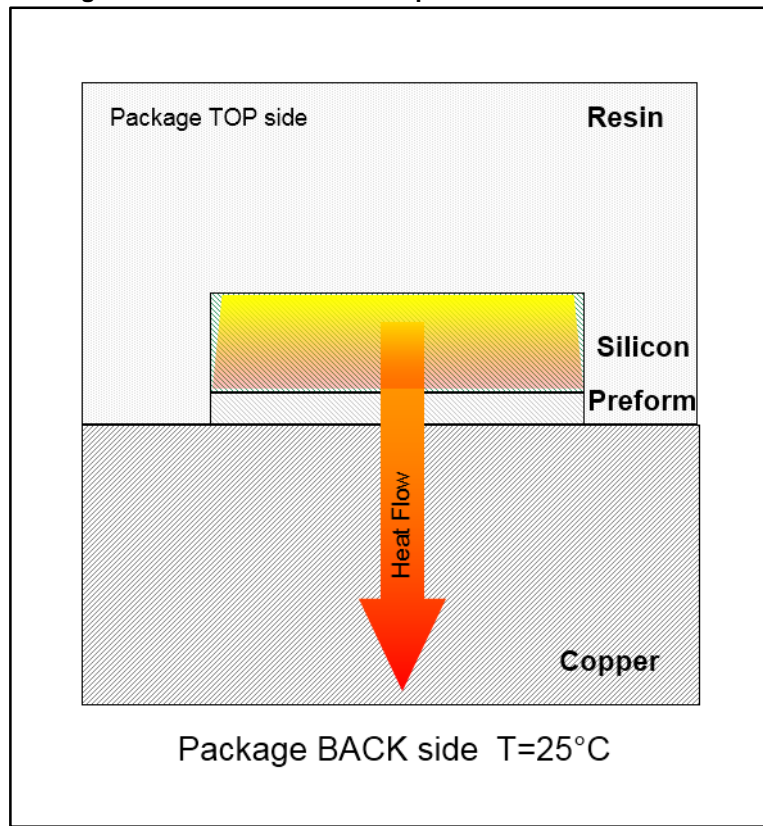
In these conditions, the Zth parameter must be used to evaluate the T_j reached on the die after the power pulse. Its value can be obtained using the curves reported in the datasheet.

Figure 9: Thermal impedance section for Tpulse lower than 1 msec
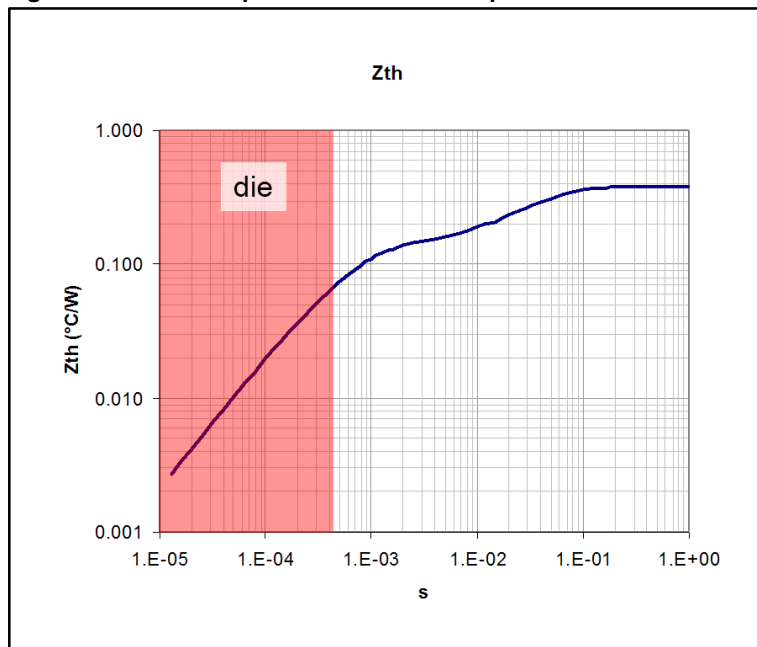
Referring to the thermal impedance (the case temperature is set at a fixed temperature), the first part of the curve is only related to the die dimension and silicon physical properties.

If the time pulse is long enough to saturate the thermal capacitance of the silicon, the temperature of the channel rises according to the thermal conductivity of the silicon and the thermal capacitance and conductivity of the preform.

The temperature significantly rises in the preform layer. The temperature of the frame is lightly increasing.

Before going on with the study, it is important to underline that the phenomenon is strongly linked to the die and package dimensions. For this reason, the definition of "short power pulse" or "lower than 1 msec" used in this application note is related only to the device used for this analysis.

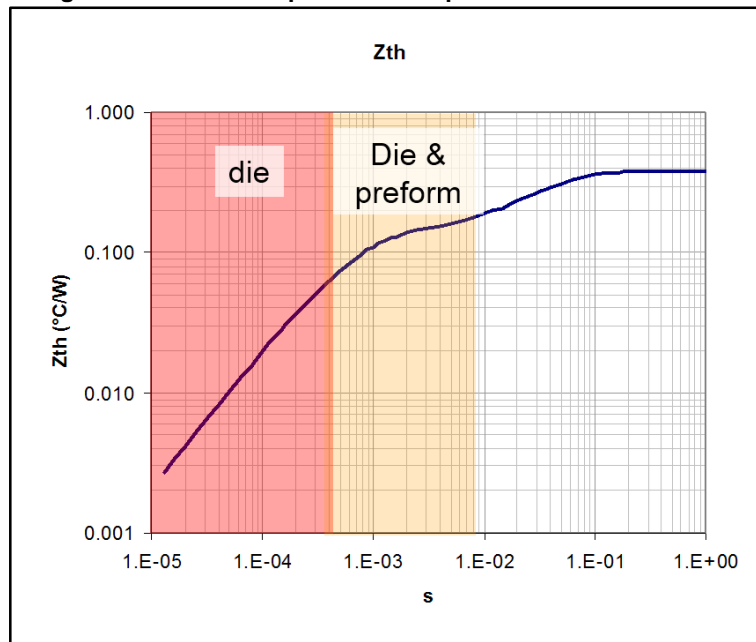**Figure 10: Cross section when Tpulse is lower than 10 msec**
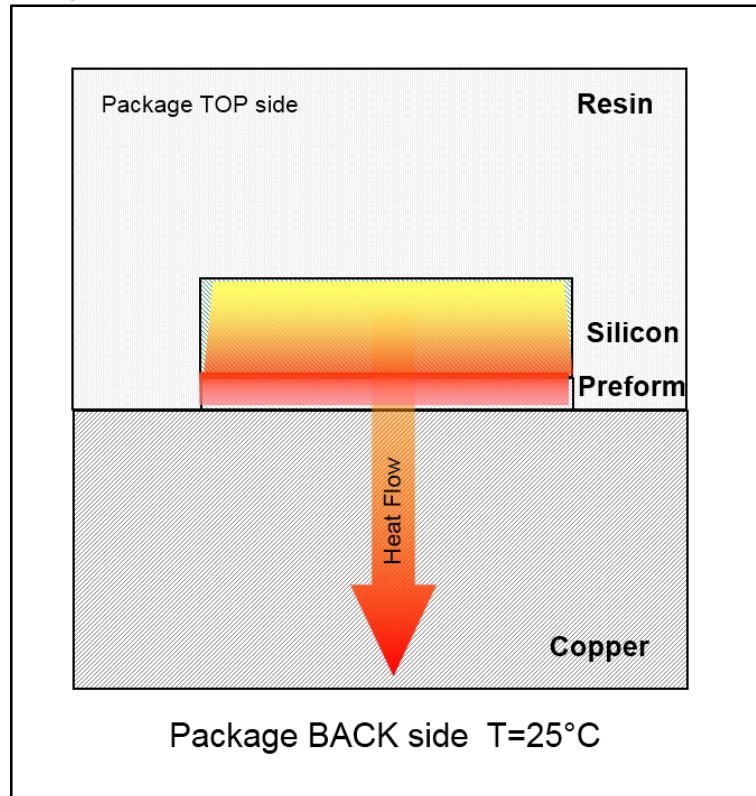
Figure 11: Thermal impedance for Tpulse lower than 10 msec

In this case, the structure involved is represented by the die and the preform, and its temperature increases according to its thermal parameters.

When the power pulse is very long, even the thermal capacitance of the preform saturates: the temperature rises significantly in the frame also. In this case, the temperature of the channel rises according to the thermal conductivity of the silicon, preform and the thermal capacitance and conductivity of the frame.

Figure 12: Cross section when Tpulse is lower than 1 sec
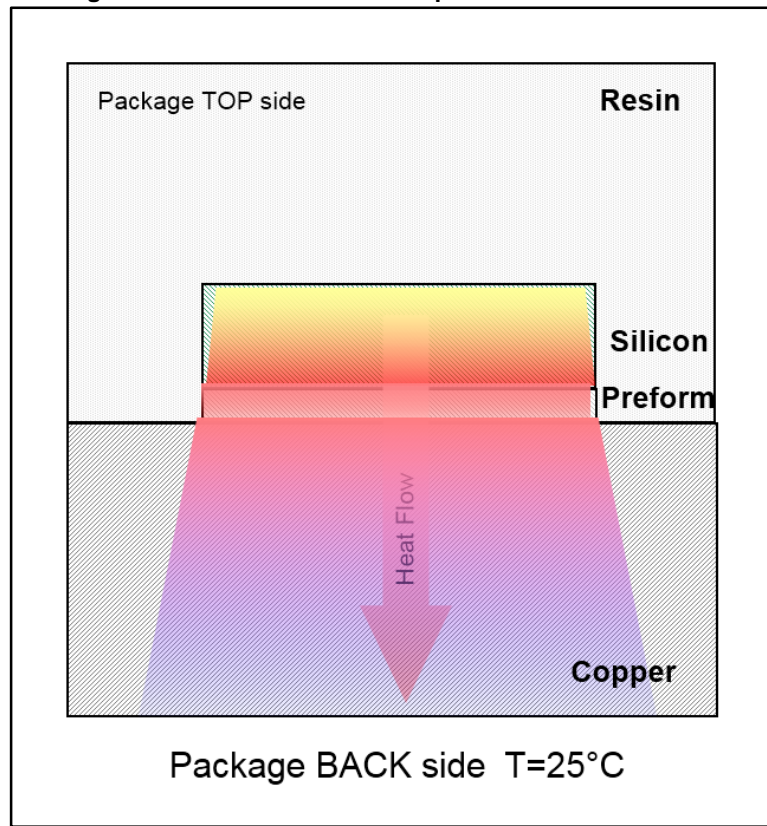
In the previous illustration, the majority of the heat is indicated with a red arrow but it is obvious that some small quantities go in other directions also. The red arrow represents, then, the preferred direction due to the small thermal resistance.

Figure 13: Thermal impedance section for Tpulse lower than 1 sec
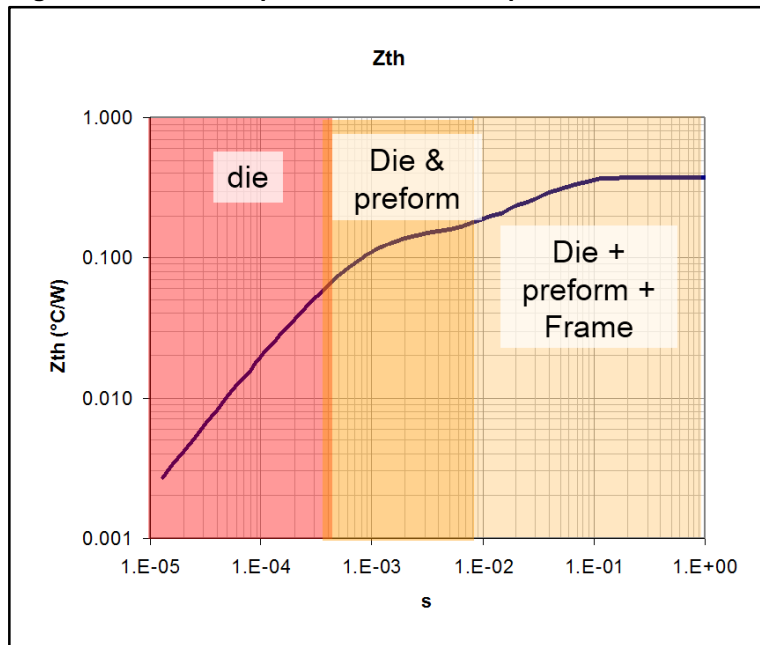
When the thermal capacitance of the frame saturates also, thermal equilibrium is reached and the total thermal resistance depends on all the layers of the package.

The thermal behavior of the package is mainly dependent on die area and the thickness of the several layers which form the structure. Other parameters, such as the copper backside extension, has a second order effect on that. So, since the TO220 and TO247 have similar copper frames and preform thickness, the thermal response of the same die assembled in both frame appears similar.

**Figure 14: Thermal impedance comparison between TO220 and TO247**
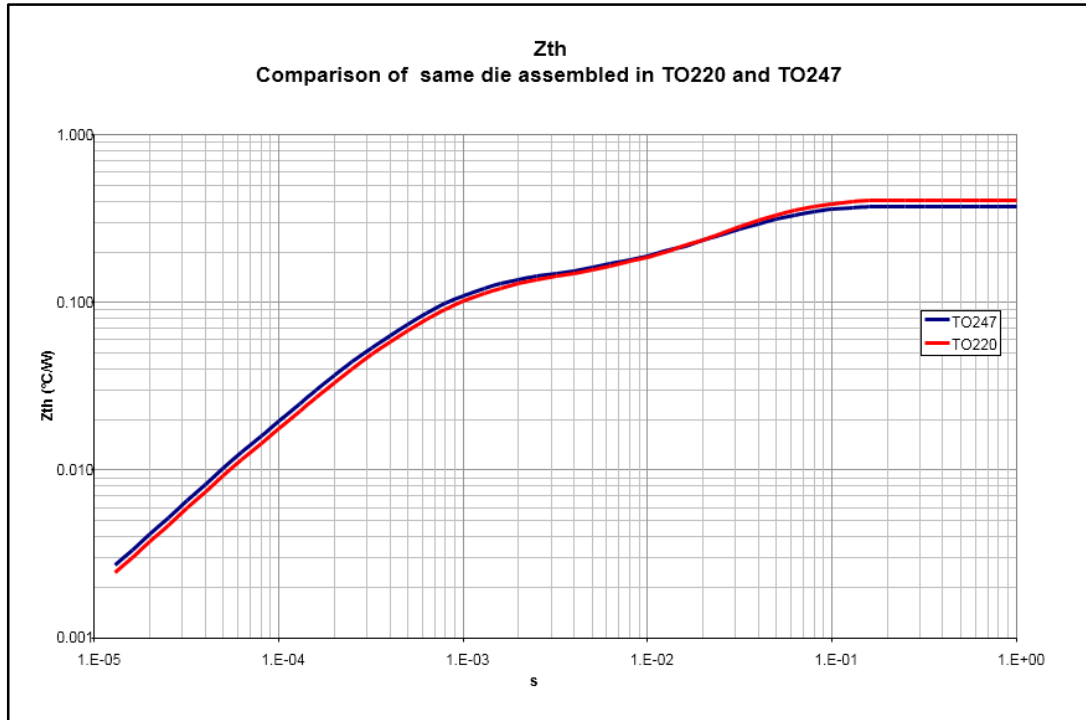
It is important to underline that in *Figure 14* the Zth is reported without any differentiation between Z_{thj-c} and Z_{thj-a}. This approximation can be done because, as described previously, when a short power pulse is forced, only the structure formed by die, preform and frame is involved, therefore Z_{thj-c} and Z_{thj-a} are represented by the same curve.

When the thermal stress involves the external structure, R_{thj-c} or R_{thj-a} must be computed. Usually semiconductor manufacturer's report these two parameters in their datasheets.

Referring to *Figure 15*, the equivalent thermal circuit is composed by:

Figure 15: Equivalent thermal model
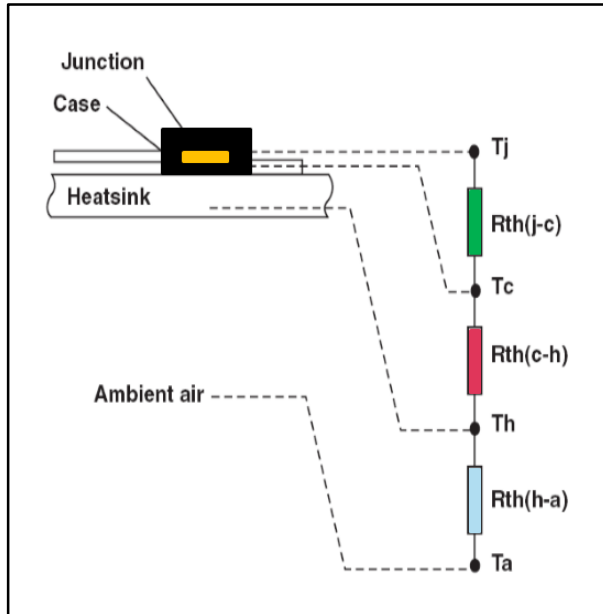
The thermal resistance reported in datasheets is only referred to the package die R_{thj-c}, while the R_{thj-a} is only referred to the condition at thermal equilibrium without any additional heatsink and with the T_{case} locked to T_{amb}.

The R_{thj-c} can be seen as the thermal resistance when the package is mounted on the infinite heatsink by an ideal case-to-heatsink interface. This situation is only an ideal. In real cases, the operations can be seen as:

- finite contact thermal resistance case-heatsink $R_{th(c-h)}$
- finite heatsink to ambient resistance $R_{th(h-a)}$

Thus the total thermal resistance can be summarize as:

Equation 5

$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$

Additional thermal resistance is introduced when the device is mounted on a heatsink due to real contact surfaces. Sometime grease is used or an isolator layer (such as mica, ceramic or silicon) is inserted, for non-insulated packages, between package and heatsink.

This thermal resistance can be minimized by contact grease and an appropriate pressure force. Just for reference, for TO220/TO220FP packages, a torque of 0.4 Nm is recommended.

As the previous relationship highlights, the thermal behaviors are linked to the total R_{thj-a}, thus, when a device is mounted on a heatsink, its thermal characteristics are fundamental. The choice of heatsink involves several parameters because its thermal resistance is function of:

- Material
- Shape
- Finishing
- Orientation
- Temperature, and whether the cooling is or is not forced by air or liquid

Figure 16: Thermal model for heatsink
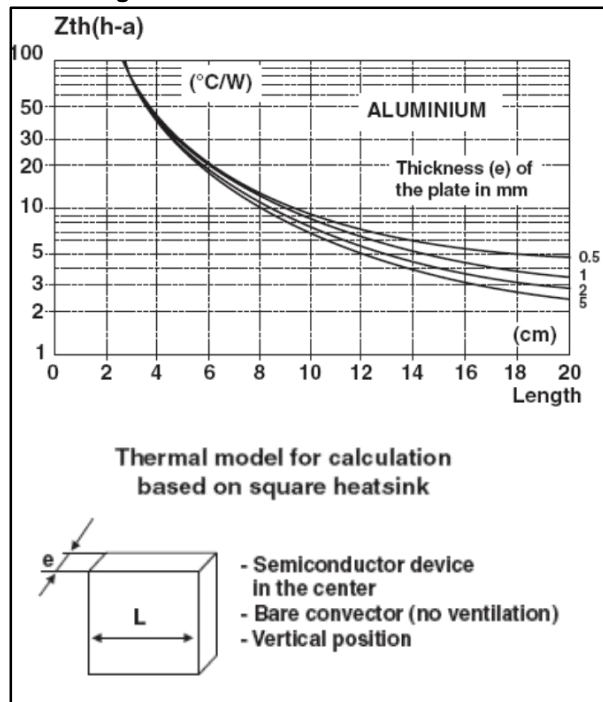
While pure thermal conduction is impacted by the thermal conductivity of the material and somewhat by the shape, the other parameters are strictly related to the method of heat transferal.

5 Transfer heat modes

When a hot body is put into a cooler ambient, there is a transfer of energy from the hot body to the external ambient. The ambient can be represented by a solid, liquid or gaseous state. In the electronics ambient, the transferring modes can be summarized mainly into:

- convection (natural or forced)
- radiation

The thermal **convection** take place when two bodies are put in contact and at least one of them exchanges heat by fluid. In order for the phenomenon to occur, a fluid must be placed between the two bodies and/or to be in relative motion with respect to the bodies between which heat is exchanged. Therefore the convection can take place between a solid and a liquid, between a solid and a gaseous material, between a liquid and a gaseous material, but also between two liquids. In general it can be said that convection takes place within the fluid in a limited space which begins at the interface between the fluid and the other body and end at a distance that depends on the case, but is still somewhat reduced.

It is the most difficult heat transfer mode to mathematically predict.

Figure 17: Schematic for convection
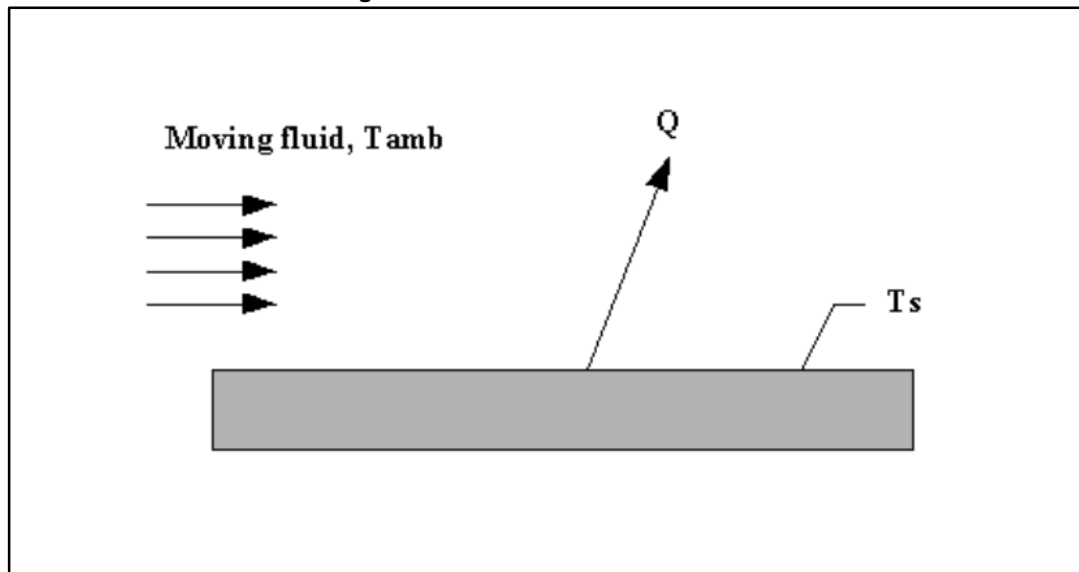
There are two types of convection according to relative motion between the two bodies:

- **Natural** is the fluid flow induced by buoyant forces, which arises from different densities caused by temperature variations in the fluid.
- **Forced** is the fluid flow caused by external means (e.g., fans, pumps, etc.)
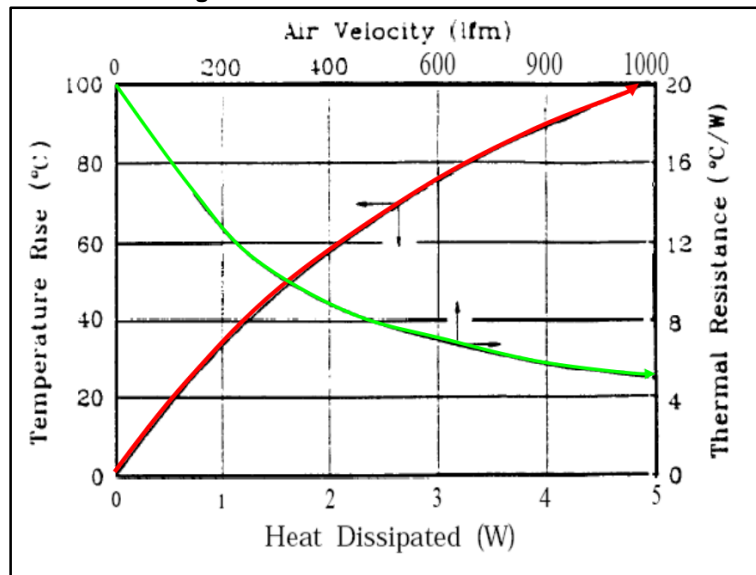
Figure 18: Convection modes
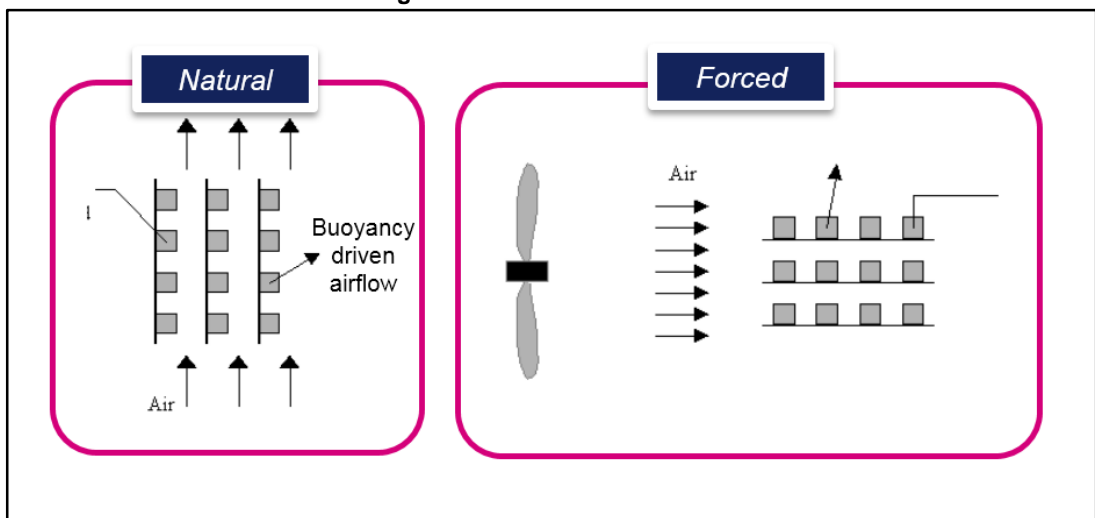
For convection mode, the thermal resistance can be summarize in:

Equation 6

$R_{th} = 1/ (h_c * A_S)$

Where $\mathbf{h_c}$ is the heat transfer coefficient and $\mathbf{A_s}$ the surface area. Heatsink maker usually provide some thermal curves.

**Figure 19: Thermal curve for heatsink**

For this kind of transmission, some recommendations can be made:

- Fins on extruded heatsinks should be vertically aligned when natural convection cooling is used
- Altitude impacts negatively on natural convection
- Care should be taken not to block the flow of air to heatsinks
- Heat-generating devices should be placed near the top of the cabinet, while cooler, heat-sensitive components should be located lower in the cabinet
- Forced-air cooling should be arranged to follow natural-convection air paths

The thermal **Radiation** is a consequence of Maxwell's, Hertz's and Planck's laws applied to heat transmission. The explanation is due to the fact that, when no material (i.e. in a vacuum) is between two bodies at different temperatures, no convection or thermal conduction can occur. The only way to transfer heat is through radiation of electromagnetic waves between the surfaces.

Figure 20: Schematic for radiation
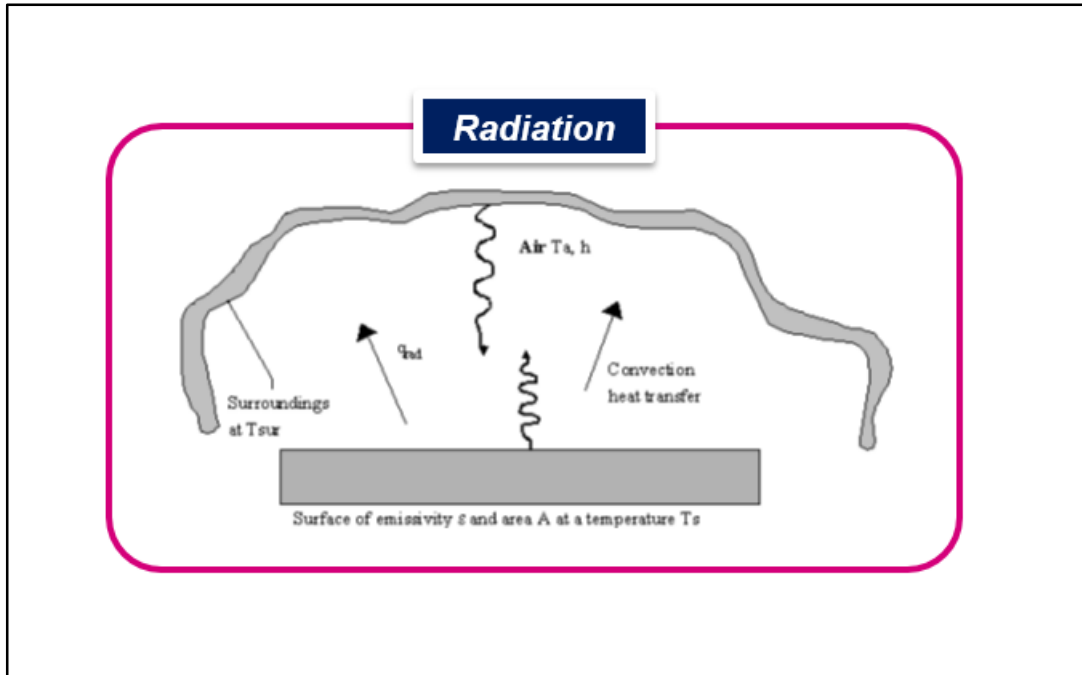
As noted several times, heat exchange by radiation depends on both the length of the wave and the direction and temperature. However, in the practical applications generally an approximation is used and in particular, it is supposed that the emitting surfaces emit in a perfectly diffuse (i.e. the radiation emitted does not depend on the direction) and the material properties (absorption coefficient, reflection and transmission) are considered independent of the wavelength. For radiation mode, the thermal resistance can be summarized in:

Equation 7

$R_{th} = 1/ (h_r * A_R)$

Where **h_r** is the radiative heat transfer coefficient and **A_r** the radiative surface area, **h_r** can be summarized using the Stefan-Boltzmann equation:

Equation 8

$h_r = \varepsilon\ \sigma\ (T_S + T_a)*(\ T_{S^2} - T_{a^2})$

Where ε is emissivity, σ is the Stefan-Boltzmann constant, T_S is the surface temperature and T_a the ambient temperature.

As for convection, for radiation some recommendations can also be made:

- Maximize surface emissivity
- The only radiative surfaces are those in plain view (not total surface area). The area between fins radiates into each other
- Use high conductivity heatsink and interface materials to minimize thermal resistance from case to radiating surface and increase the temperature difference between dissipating surface and ambient
- When forced cooling is adopted, irradiation contribution is negligible; when natural, if the heatsink is well designed, approximately 30% of the heat is transferred by radiation.

To complete the overview, in *Table 2*, some emissivity coefficients are reported.

Table 2: Emissivity coefficients

Material and finish	Emissivity
Aluminum - polished	0.04
Aluminum - rough	0.06
Aluminum - anodized (any color)	0.8
Copper - commercial polished	0.03
Copper - machined	0.07
Copper - thick oxide coating	0.78
Steel - rolled sheet	0.55
Steel - oxidized	0.78
Stainless steel - alloy 316	0.28
Nickel plate - dull finish	0.11
Silver - polished	0.02
Tin - bright	0.04
Paints & lacquers - any color - flat finish	0.94
Paints & lacquers - any color - gloss finish	0.89

5.1 MOSFET power losses

When a power MOSFET is used as a switch in an electronic application, it is submitted to thermal stress due to the electrical power dissipated on it. In order to design a robust project, designers evaluate the power losses starting from the specifics of the electrical application, topologies implemented, and modes to dissipate the heat. This study allows a choice of the right components to operate in a safe manner. By restricting the area of the power losses in the switch device, the power losses dissipated inside the device during operation can be categorized in two main classes:

- Conduction losses (related to the ohmic characteristics of the device)
- Switching losses divided into:
    - Turn-on/turn-off losses
    - Output capacitance stored energy loss
    - Gate driving loss
    - Freewheeling diode additional losses

Thus the total losses can be written as:

Equation 9

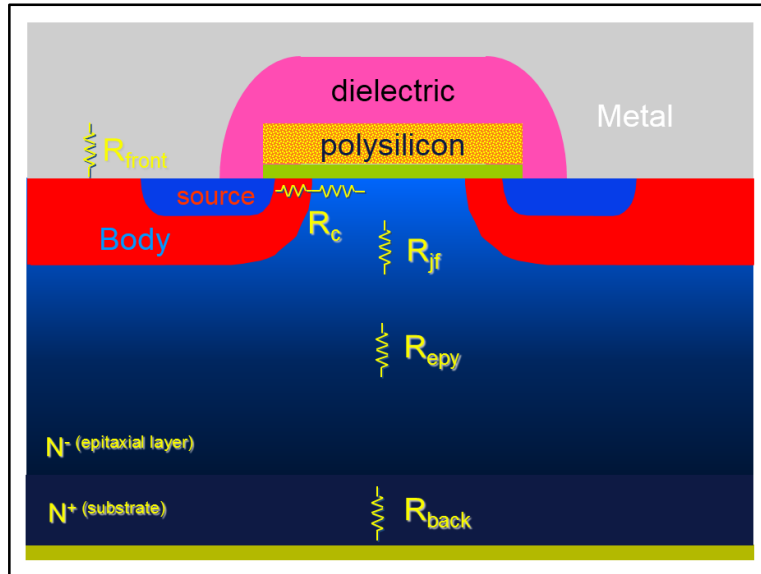$P_{tot} = P_{cond} + P_{sw} + P_{Coss} + P_{driving} + P_{diode}$

Each single contribution is linked to a specific working operation, then we analyze them.

5.1.1 Conduction losses

When the device is fully on, the only electrical resistance is represented by the resistance of the structure. This resistance is due to many contributions, as *Figure 21* shows:

Figure 21: Power MOSFET structure

Since some contribution is linked to the temperature, also the total $R_{DS(on)}$ shows a value variable with the temperature as usually reported in the datasheet. So, restricting the area analysis to the conduction phase, the power losses are due to the Joule's effect in the structure:

Equation 10

$P_{cond} = I^2_{RMS} \cdot R_{DS(ON)} \,(Temp)$

Then, in order to perform the computation of this contribution, it is necessary to evaluate or know the I_{RMS} value of the current forced into the device. If the device supplies a resistive load, the relationship between voltage and current is constant. The theoretical waveforms can be described as:

Figure 22: Resistive load: ideal waveforms
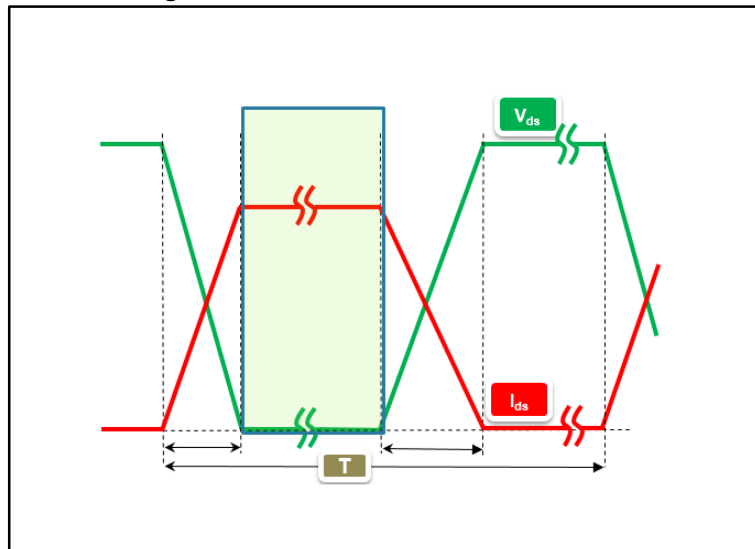
In this condition, the estimated conduction power losses will be:

Equation 11

$P_{cond} = [(I_d)^2 \cdot t_{ON}/T] \cdot R_{DS(ON)} \,(Temp)$

If the system supplies an inductive load, the current waveform is delayed compared to the voltage waveform. Furthermore, CCM or DCM perform in different ways. The following relationship summarizes the whole condition referring to *Figure 23*.

Figure 23: Inductive load: ideal waveforms
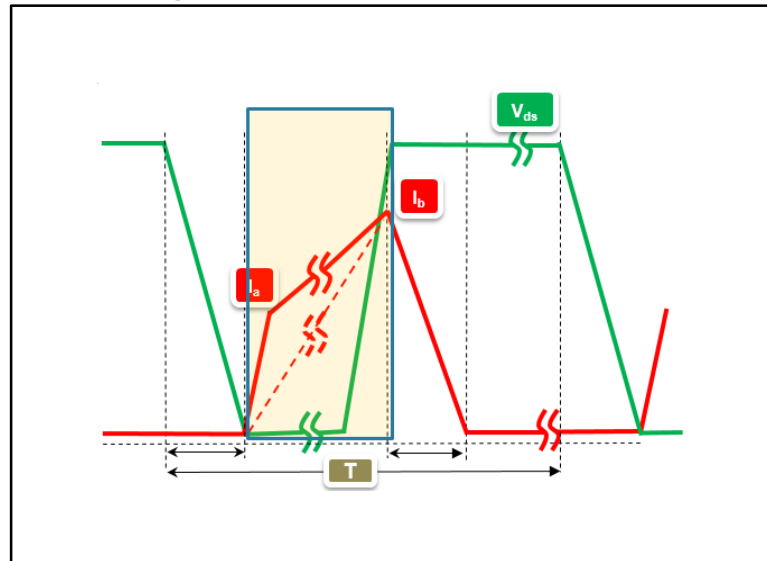
I_a is the current value at turn-on while I_b is thevalue at turn-off. In DCM mode, I_a is equal to zero, therefore:

Equation 12a

$P_{cond} = 1/3 \cdot I^2_b \cdot R_{DS(ON)} \, (Temp) \cdot t_{ON}/T$

If the system operates in CCM, the new relationship will be:

Equation 12b

$P_{cond} = 1/3 \cdot (I^2_a + I^2_b + I_a \cdot I_b) \cdot R_{DS(ON)} \, (Temp) \cdot t_{ON}/T$

The above formulas allow evaluation of the power losses due to the Joule's effect on the structure.

To complete the overview, some typical current waveforms and the relative I_{RMS} values are reported.

Figure 24: Triangular current waveforms

$$I_{RMS} = I_{peak} * \sqrt{\left(\frac{1}{3} * \frac{t_{ON}}{T}\right)}$$
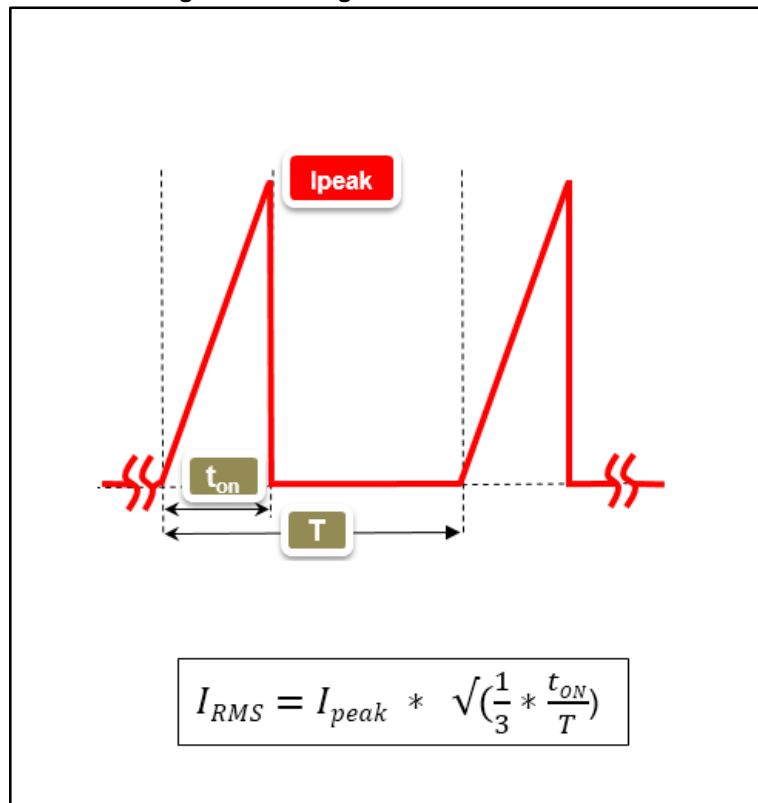
Figure 25: Trapezoidal current waveforms

$$I_{RMS} = \sqrt{\left(\frac{1}{3} * (I_a^2 + Ia * Ib + Ib^2) * \frac{t_{ON}}{T}\right)}$$
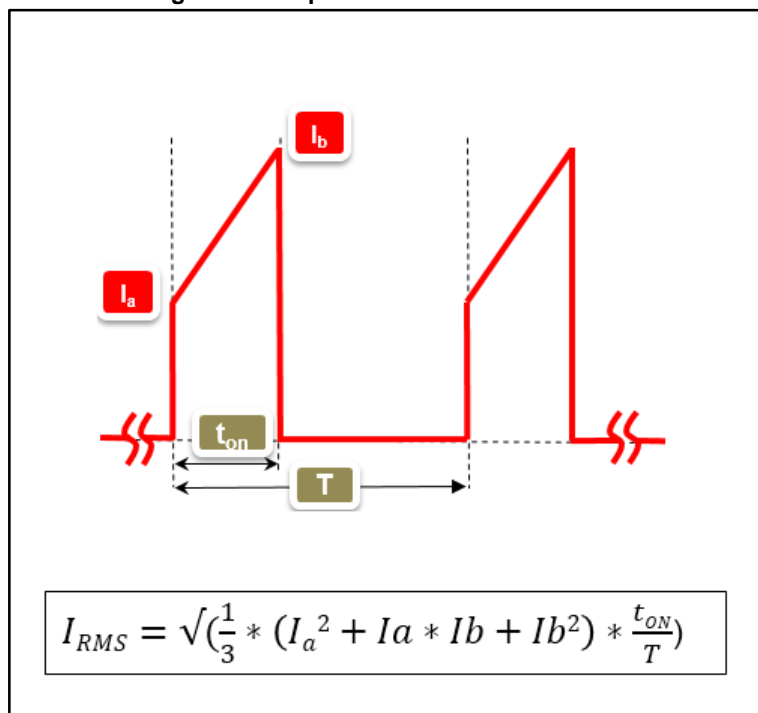
Figure 26: Full sine current waveforms

$$I_{RMS} = \frac{I_{peak}}{\sqrt{2}}$$
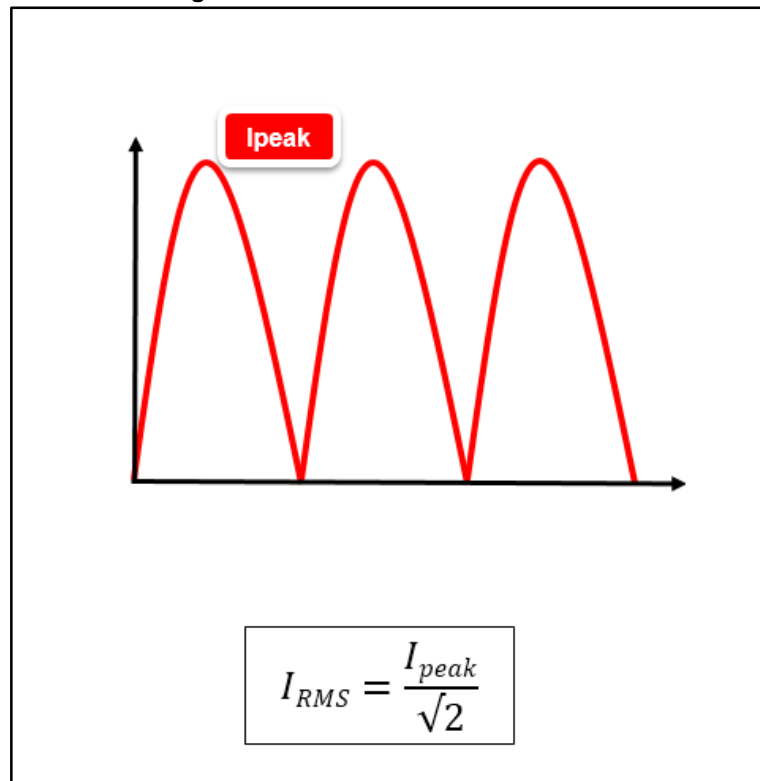
Figure 27: Half sine current waveforms

$$I_{RMS} = \mathrm{I}_{peak} * \sqrt{\frac{t_{ON}}{2T}}$$
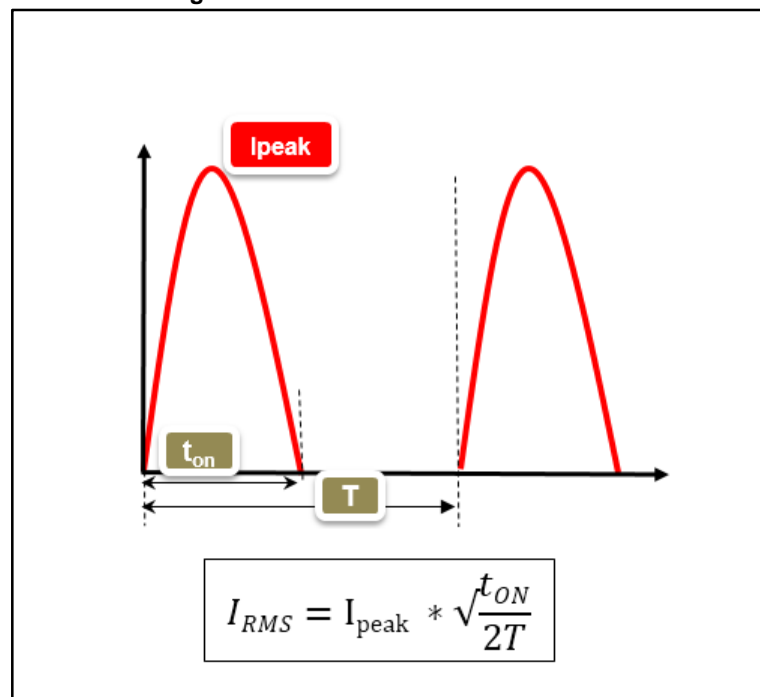
5.1.2 Switching losses

Turn-on/turn-off

During the ON-OFF and OFF-ON transitions, some power losses are present. As shown in the previous paragraph, the behavior and the losses of the switching devices are linked to the load. A differentiation must be made if a resistive or inductive load is powered.

If the device supplies a resistive load, the relationship between voltage and current is constant and the switching power losses can be described by:

Figure 28: Resistive load: ideal waveforms
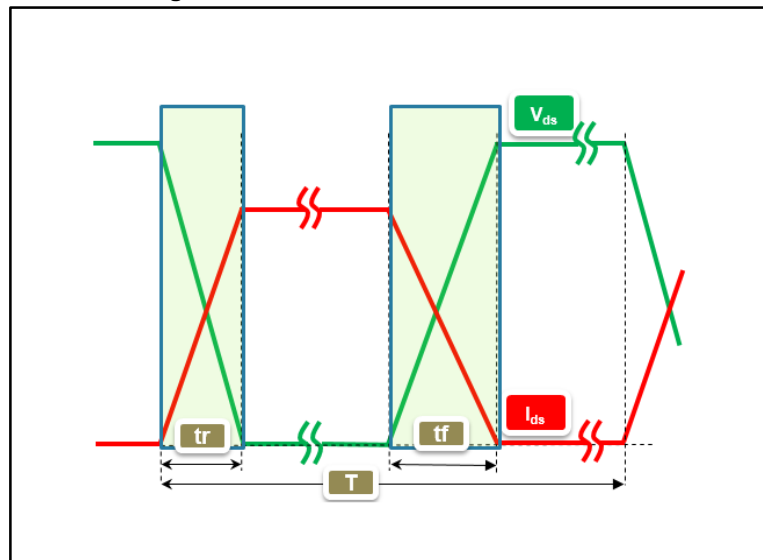
During the switching ON operations, the power losses can be calculated as:

Equation 13

$P_{sw(on)}=1/6\cdot(V_{ds}\cdot I_d)\cdot t_r/T$

While for turn OFF:

Equation 14

$P_{sw(off)}=1/6\cdot(V_{ds}\cdot I_d)\cdot t_f/T$

In the case of inductive load, there is not a linear relationship between voltage and current. The variation of the last parameter is always delayed compared to the voltage.

If no energy is stored inside the reactive component, the turn-on commutation happens at zero current (dotted line *Figure 29*).

Figure 29: Inductive load: ideal waveforms
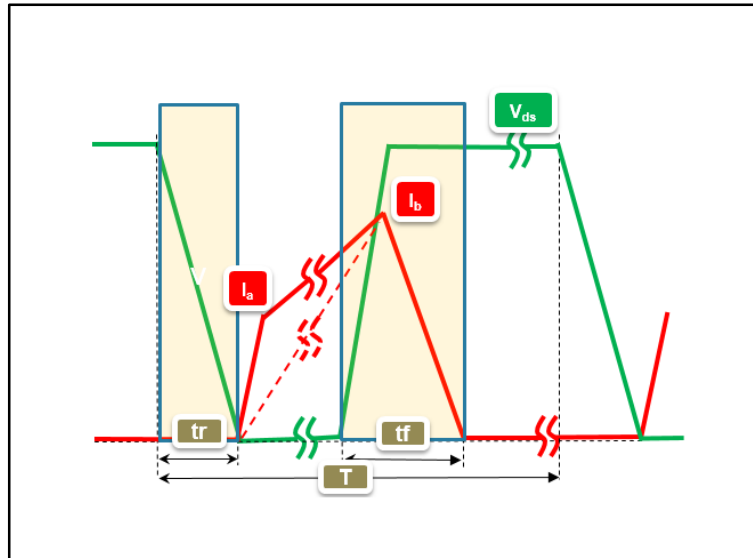
$P_{sw(on)}$=*negligible*

while for the turn-off:

**Equation 15**

$P_{sw(off)}=1/2\cdot(V_{dsmax}\cdot I_{dpeak})\cdot t_f/T$

The previous formulas help designers to investigate the losses during the startup phase of the project because, using some parameters like t_f, t_r or $R_{DS(ON)}$(Temp), they can predict the T_{jmax} of the MOSFET. However this is false because, they cannot predict the real parameter values due to the different working operation compared to the data reported in the datasheet.

A correct approach is to measure the energies involved during switching operations. Using the data measured it is possible to evaluate the switching power dissipated during operation. *Figure 30* shows turn-on details on an inductive load.

Figure 30: Turn-on details during steady-state conditions
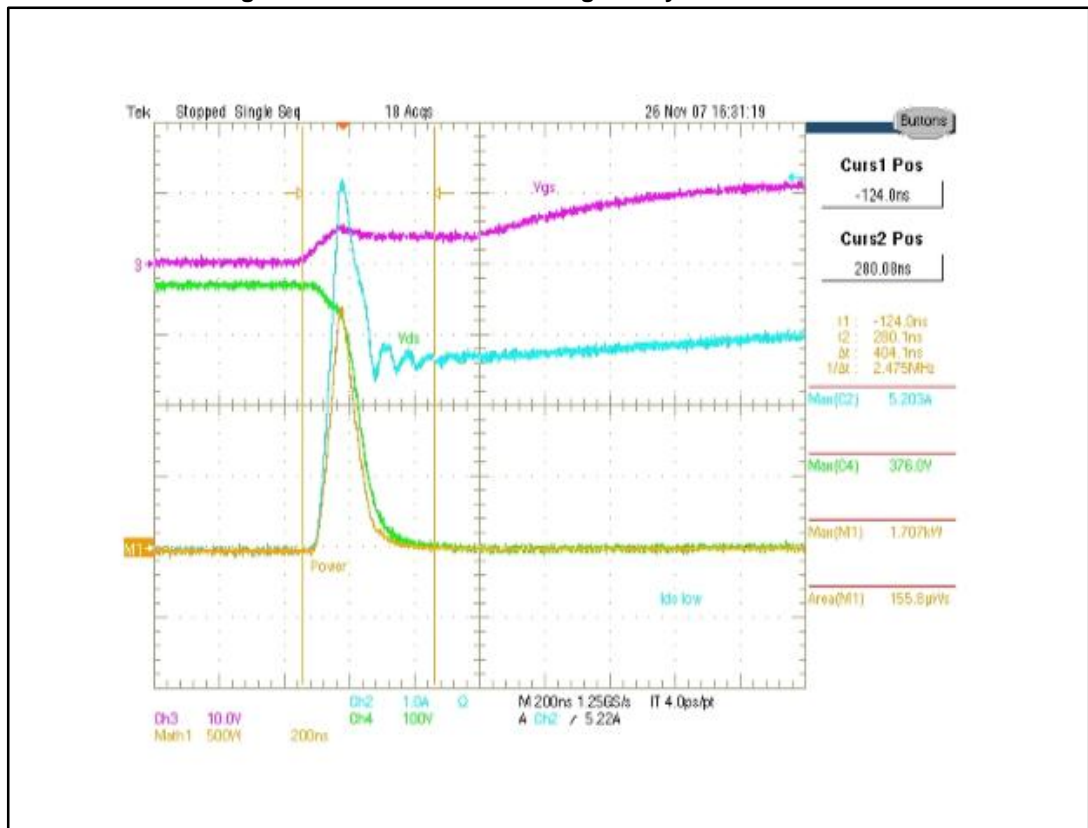
It is possible to generalize the instant summarizing in two parts the component of the losses, and in particular:

Figure 31: Turn-on waveform analysis
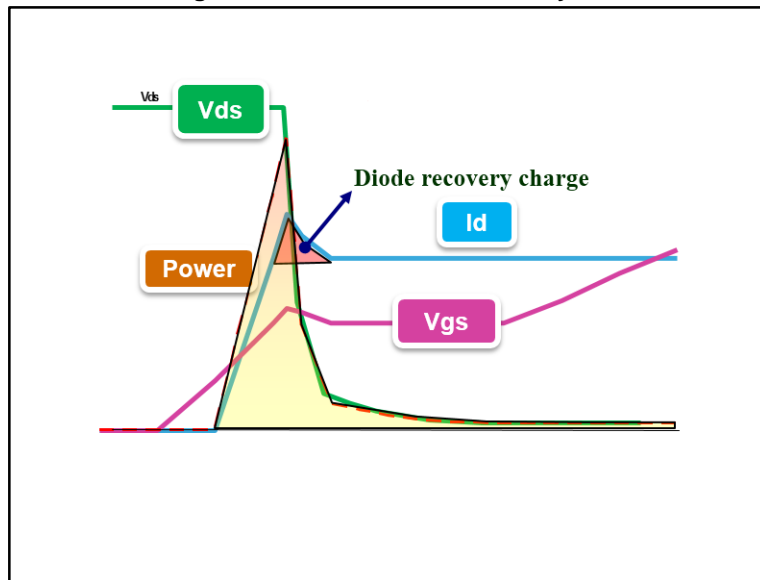
The small peak of the current is due to the recovery of the diode if it is applied. The power losses can be written as:

Equation 16
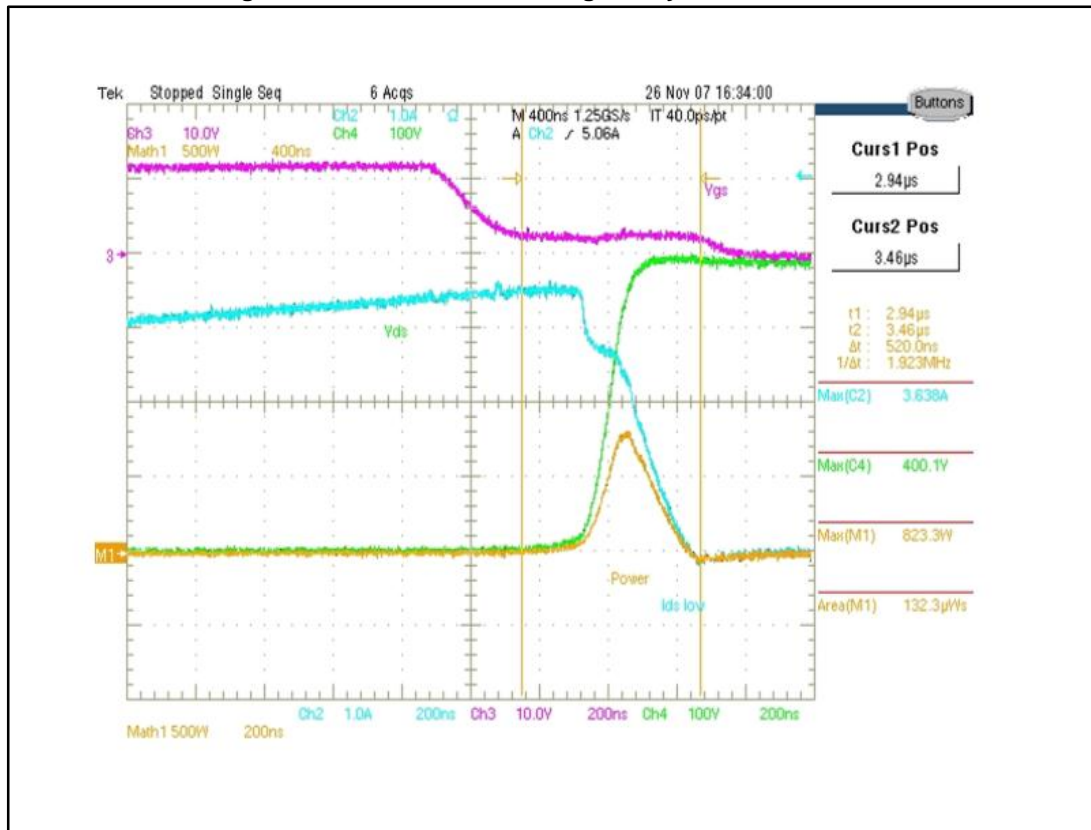
$$P_{sw(on)}=E_{on}\cdot f_{sw}$$

where f_{sw} is the switching frequency. The power losses due to the diode and included in Equation 16 are:

Equation 17

$$P_{diode}=Q_{rr}\cdot V_{ds}\cdot f_{sw}$$

Regarding the turn-off operations, the same approach can be applied:

Figure 32: Turn-off details during steady state conditions

The turn-off operations are not affected by the influence of the diode as in the turn-on operations. It is important to underline that in some topologies there is not a linear link between the E_{off} measured and the real energies dissipated. This aspect is especially evident in resonant topologies.

As for the turn-on case, the switching power losses during the OFF transition can be described by:

Figure 33: Turn-off waveform analysis
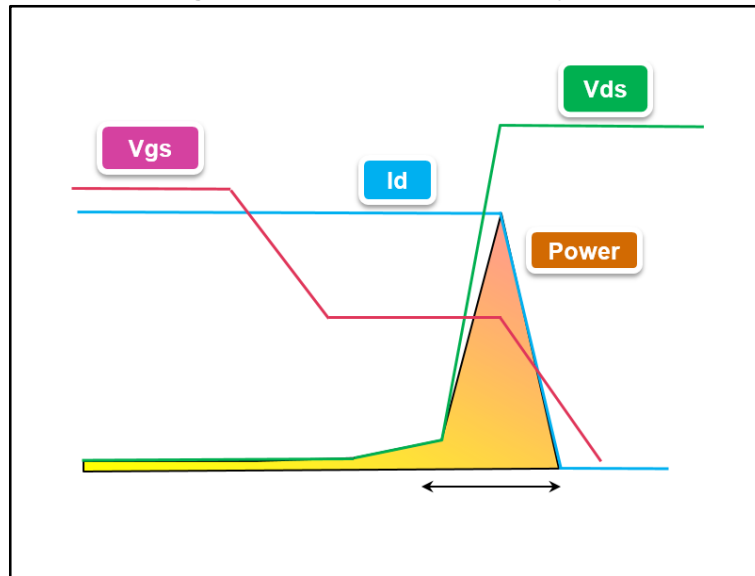
The energy losses can be determined as:

Equation 18

$$P_{sw(on)} = E_{off} \cdot f_{sw}$$

where f_{sw} is the switching frequency and E_{off} the energy measured.

The relationships reported for turn-on and off operations are valid to calculate the power losses if the stress is constantly repetitive as in the converters as flyback topology where current waveform is constant if the load is fixed. If the real stress is variable according to a law or a control, a correction factor must be applied.
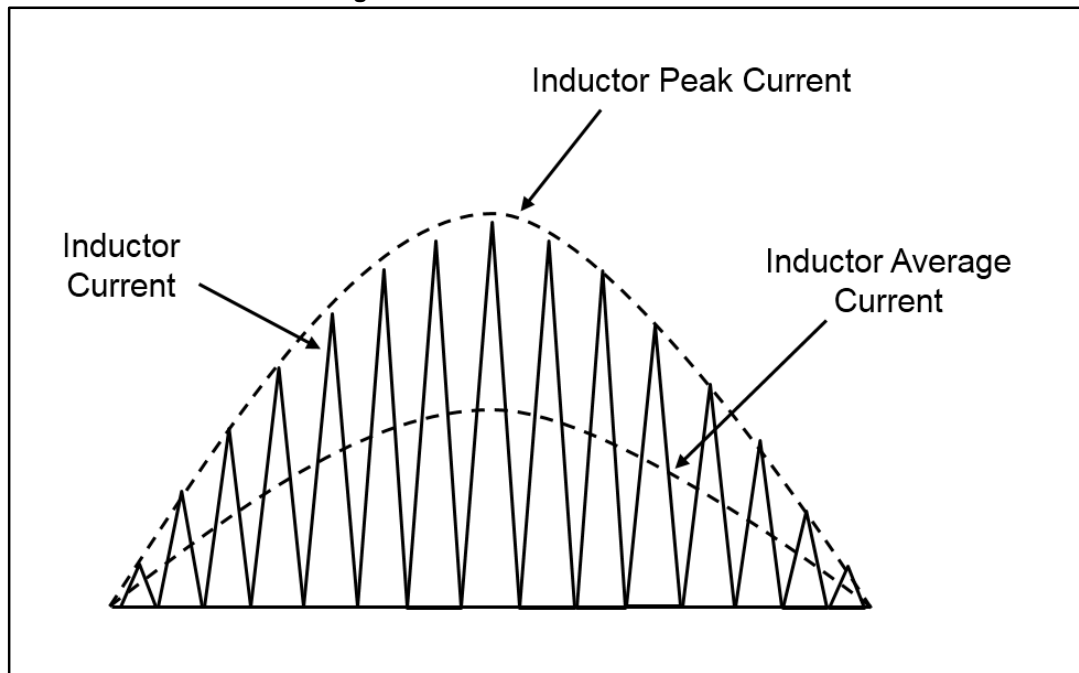
Equation 19

$$P_{sw(on)} = E_{off} \cdot f_{sw} \cdot \alpha$$

Just as an example, if the analysis is performed on a PFC section, the α parameter will be equal to:

Equation 20

$$\alpha \cong \frac{1}{\sqrt{2}}$$

Figure 34: Current waveform on DCM

Output capacitance stored energy loss

During each switch-off operation, the output capacitance (C_{oss}) is charged to V_{bulk}, storing Energy. This energy is given back when C_{oss} is discharged during switch on operations. If the capacitance C is an ideal component, a simple relationship allows to determine the energy E stored inside it when a voltage V is applied across it. This relation is noted as:

Equation 21

$$E = \frac{1}{2} \cdot C \cdot V^2$$

When a semiconductor device is analyzed, due to the strong non linearity of its structure, the evaluation of the energy stored inside C_{oss} is not simply, because the C value is a function of the voltage applied.

Equation 22

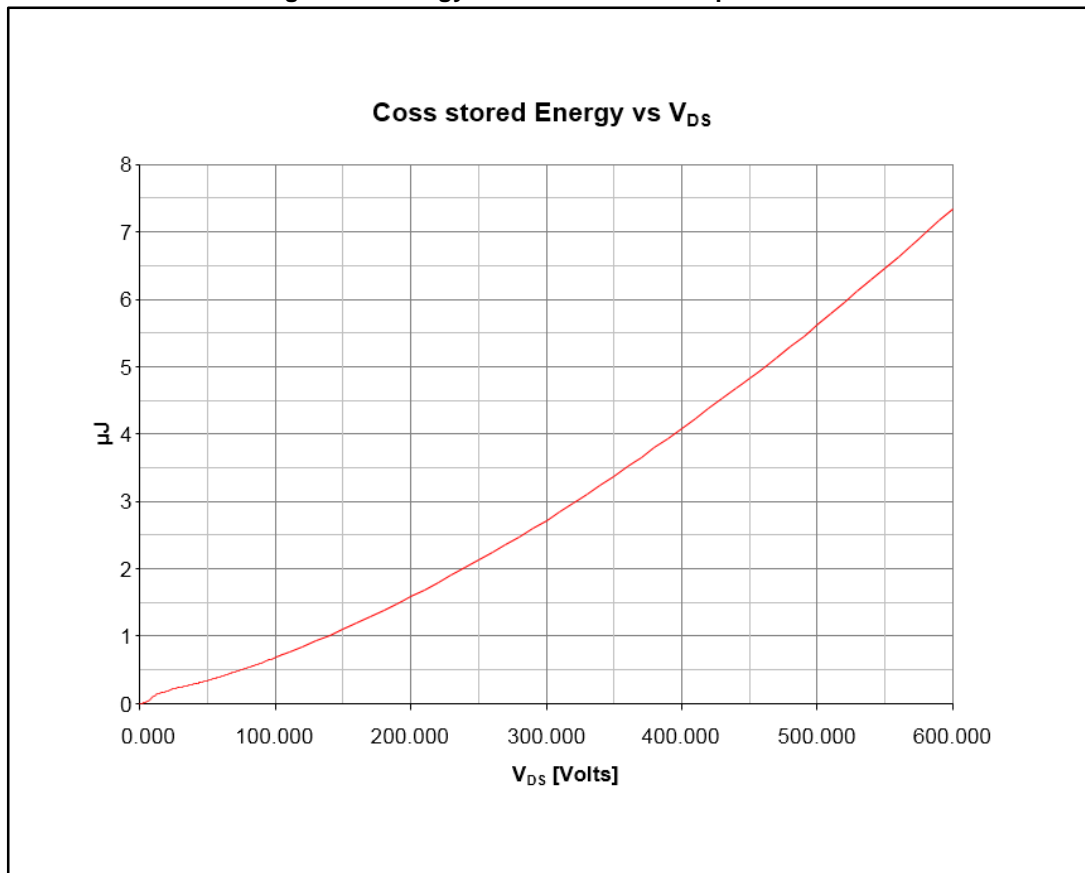$$E(v_{ds}) = \int_0^{V_{ds}} C_{oss}(v) \cdot v dv$$

If a graph is furnished as reported in *Figure 35*, the power losses can be evaluated as:

Equation 23

$$P_{Coss} = E_{Coss} \cdot f_s$$

This energy is dissipated within the device during turn-on, if Vds is not zero.

Figure 35: Energy stored in the Coss capacitance

Gate driving loss

The switching operations of a power device are usually controlled by a driver. The driver provides control of the turn-on and turn-off time, properly charging and discharging the capacitance of the gate of the power device. Since the control gate of the device does not play a role in the power line, the charge furnished by the driver is lost through the dissipative elements at each switch operation. This charge can be evaluated starting from the gate charge curve reported in a MOSFET datasheet.

Equation 24

$$P_{drive} = Q_g V_g f_s$$

Where V_g is the max output driver voltage applied and f_s the switching frequency. If the driving is implemented with a simple resistor R_{ext}, the power loss can be evaluated as:

Equation 25

$$P_{Rgint} = \frac{R_{gint}}{R_{gext}+R_{gint}} P_{drive}$$
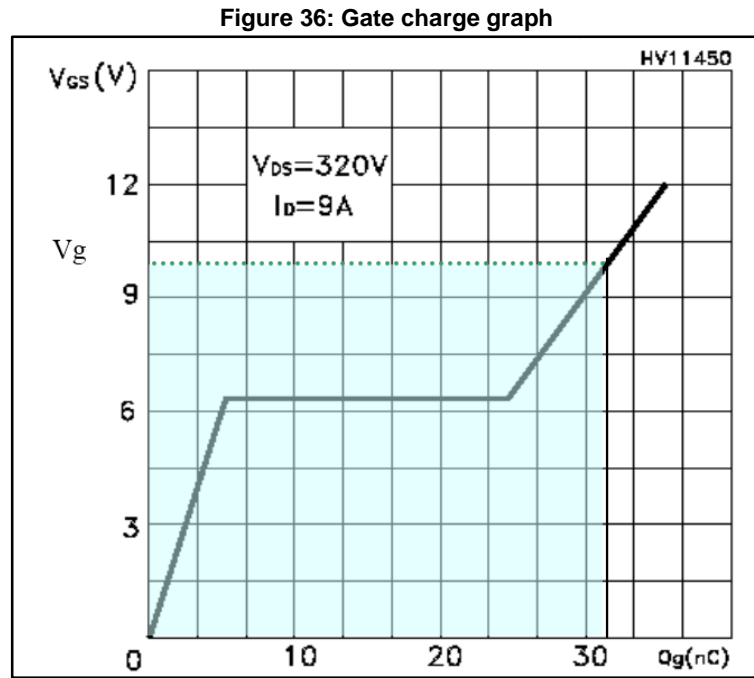
Figure 36: Gate charge graph

Figure 36 above reports the gate charge graph for the device used in the examples that follow.

6 Example 1

In the following example, starting from a real case and measurements performed on it, computations are made to assure the safe operation of the semiconductor device. To guarantee the spec reported in the datasheet and the safe condition of the operations of the semiconductor device, it is necessary to know the maximum junction temperature reached by the device during the power stress. In order to evaluate it, we need to summarize all the data.

Table 3 reports the test conditions.

Table 3: Test conditions

| Parameter	Value
$R_{DS(ON)}$ (25 °C)	1.06 Ω
Mode	CCM
T_{amb}	25 °C
Heatsink	No
R_{thj-a}	62.5 °C/W
R_{thj-c}	6.25 °C/W
T_c	115 °C

To evaluate T_j it is necessary to know the P_{tot} dissipated by the device. Then, as reported in the previous paragraphs, we can evaluate the power losses due to the conduction phase, those due to the switching, due to the C_{oss} and due to the P_{driver}. Then, starting from the

Example 1   AN4783

analysis of the details of the working operations, it is possible to determine the P_{tot} forced inside the power device.

Equation 26

Tj = Tamb + [Ptot * Rthj-a]

Figure 37: Electrical waveforms at steady-state conditions
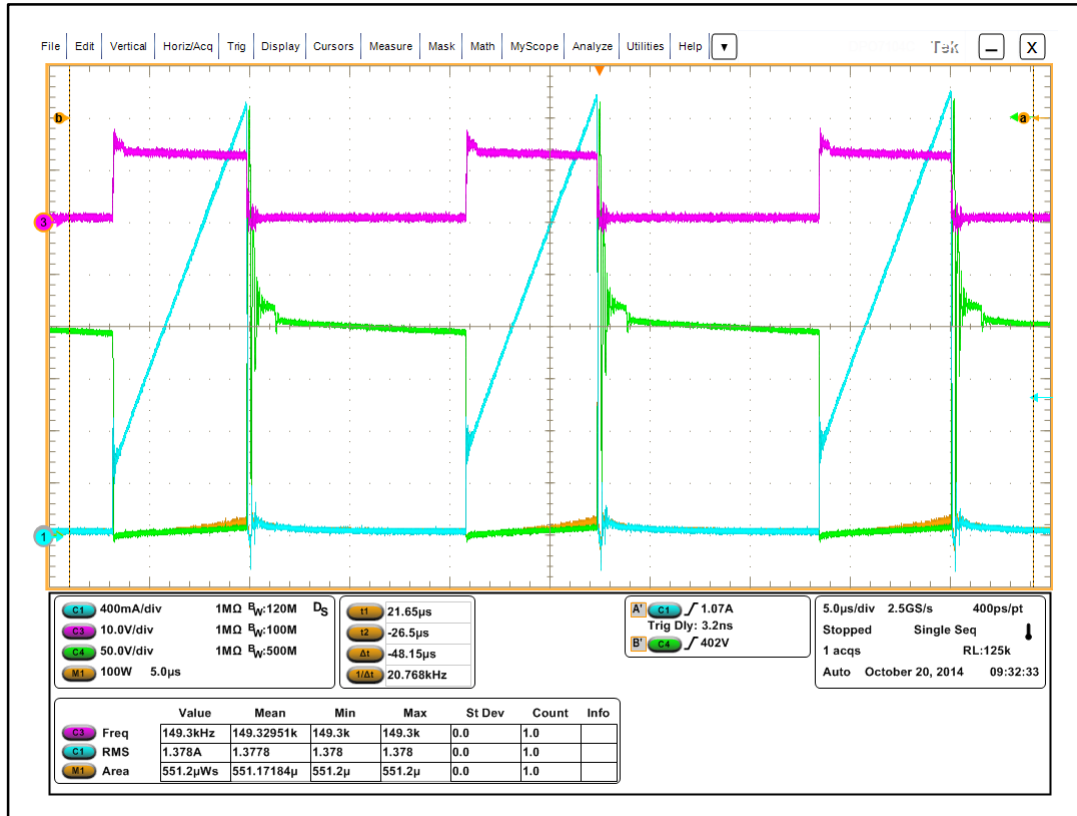
In *Figure 37*, using an oscilloscope, it is possible to measure some parameters as the working frequency and I_{RMS}.

Figure 38: Turn-off details at steady-state conditions
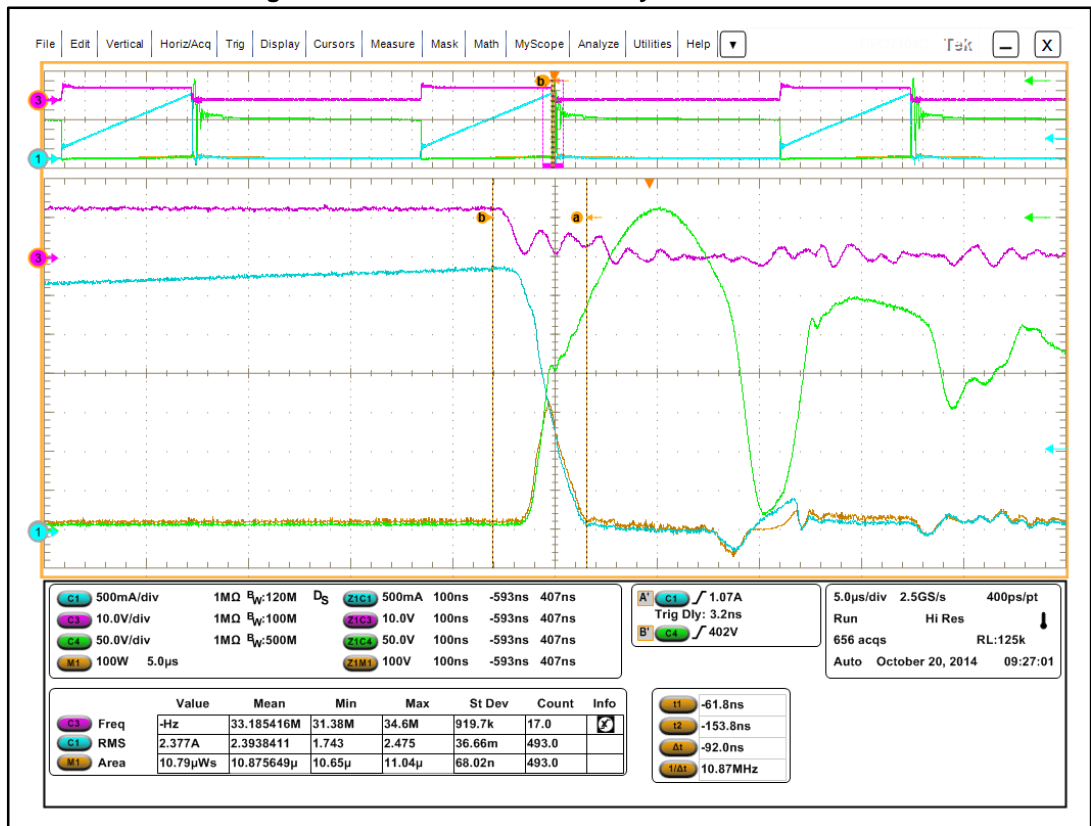
Figure 38 reports the details of the turn-off operations where it is possible to measure the energy losses.

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Figure 39: Turn-on details at steady-state conditions
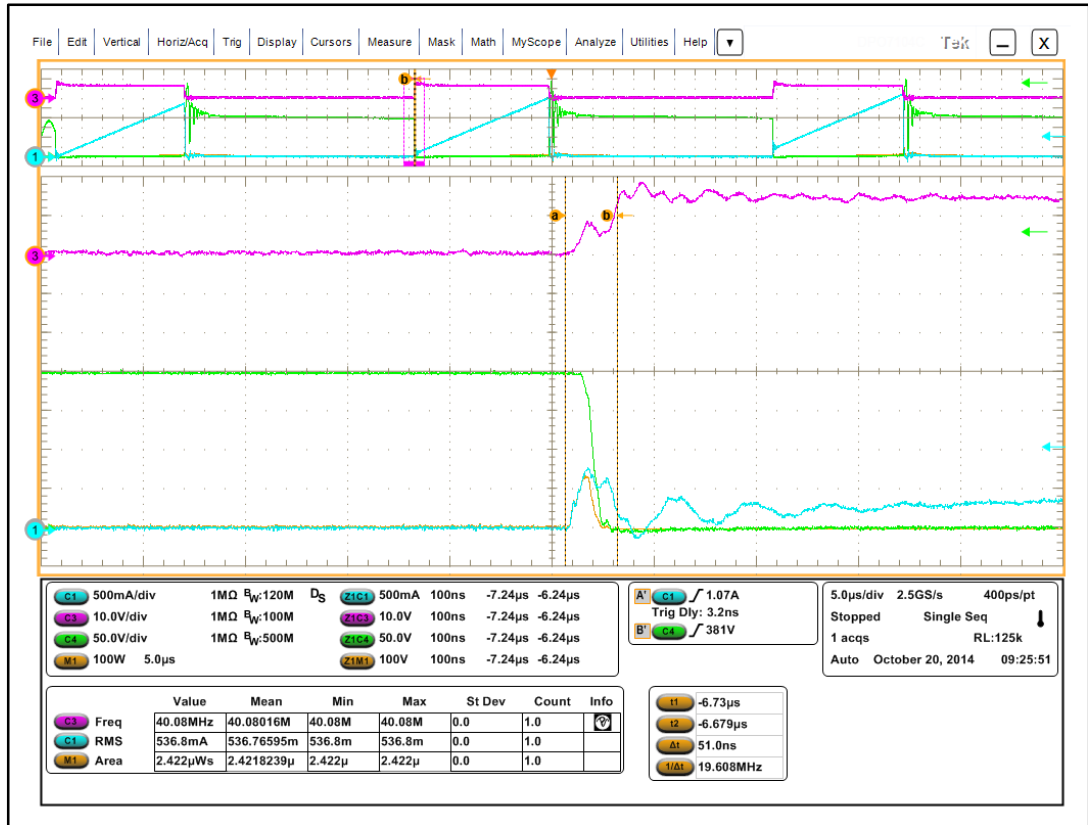
From the data and the relationships previously introduced, it is possible to write:
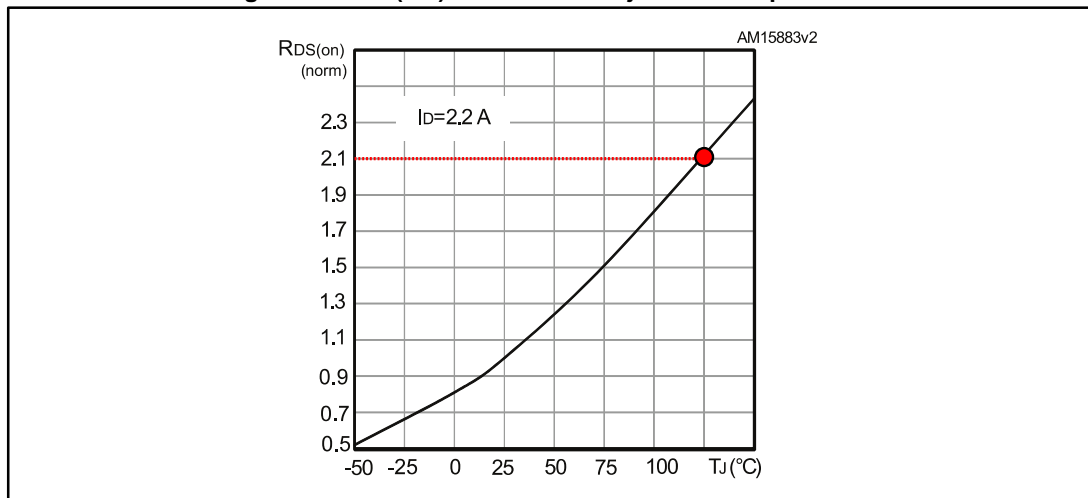
E_{OFF}=6.65 µJ

E_{ON}=1.49 µJ

I_{RMS}=7.7 A

Freq= 57 kHz

From the datasheet of the device [2] it is possible to obtain the data related to $R_{DS(ON)}$ (T_c=115 °C). This data can be obtained from the following graph:

Figure 40: RDS(ON) function of the junction temperature

Then:

$R_{DS(ON)}$ (Tc=115 °C) = K $R_{DS(ON)}$ (Tc=25 °C) = 2.1* 1.06= **2.226 Ω**
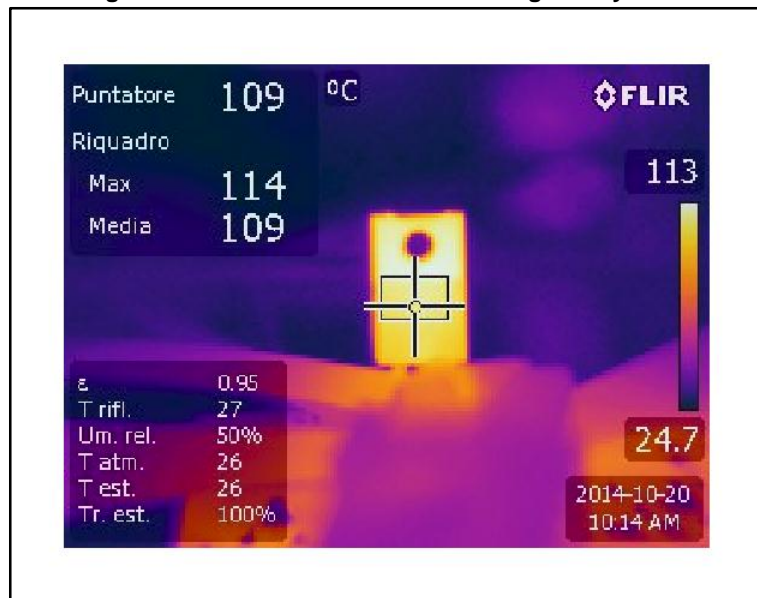
And summarizing:

P_{cond}= 1.15 W

P_{sw}= 0.47 W

P_{coss}= 1.47 µW

$P_{tot} = P_{cond} + P_{sw} + P_{coss}$ = 1.62 W

$T_j = T_{amb} + P_{tot} * R_{thj-a}$ = 25 +1.62 * 62.5 = 126 °C

$T_c = T_j - P_{tot} * R_{thj-c}$ = 126-1.62 * 6.25 = 116 °C

The data estimated for the T_c is very similar to the real data as confirmed by the thermal measurement performed by thermo camera.

Figure 41: Thermal measurement during steady-state

The small difference between the data measured and the data estimated is due to the real value of some parameters reported in the datasheet such as $R_{DS(ON)}$, R_{thj-a}, R_{thj-c}.

Example 2   **AN4783**

7   Example 2

A similar approach can be performed if the power stress is represented by a single event. In this case, the parameters involved must take into account the fast transient of the event. This aspect is represented by the use of the Z_{th} parameter. Following the theory introduced in the previous paragraphs it is possible to evaluate the thermal stress when an accidental event occurs. In *Figure 42* an overstress is present when a system is submitted to a short-circuit of the output. It is possible to note that the system swaps from normal steady-state condition to an extra current before the action of the protection circuit. For the case reported, the system uses an STMicroelectronics MOSFET and in particular the STF6N60M2 [2].

Figure 42: Waveform analysis during short-circuit event
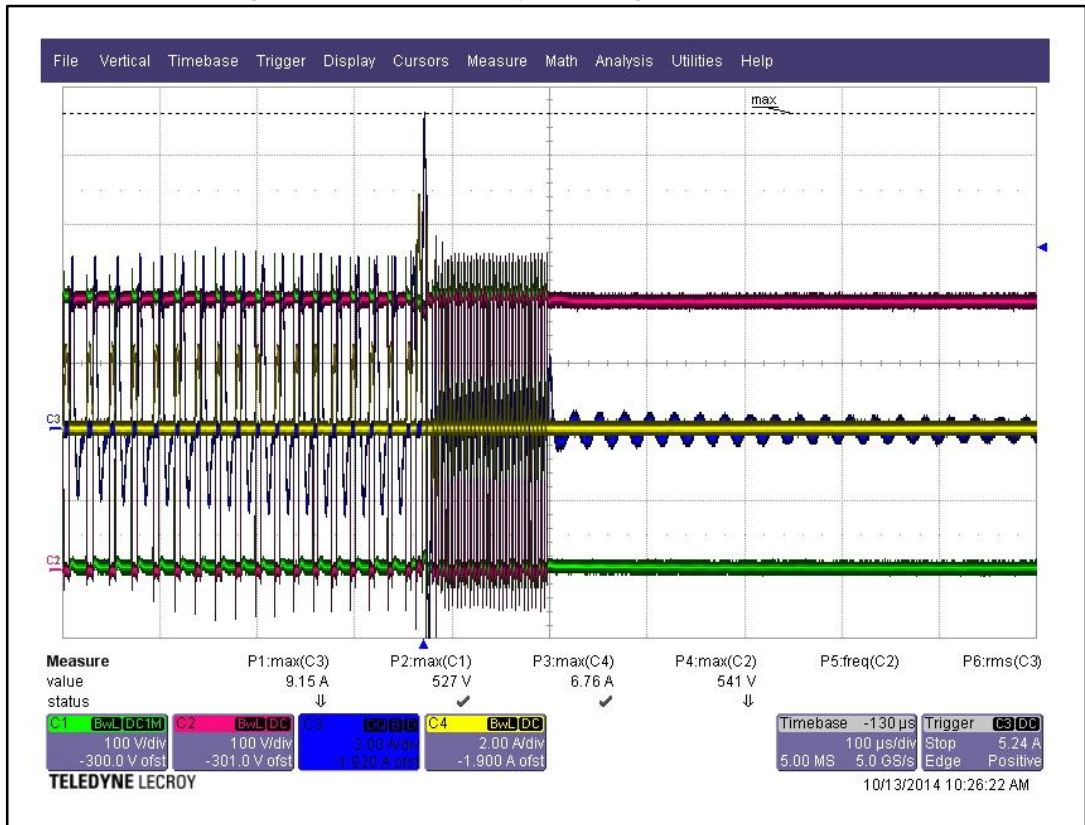
During the short-circuit event, the system operates with very high current only for a few pulses. If the stress is present for a single event, we can approach the study in the following way:

Figure 43: Waveform analysis during the single power pulse
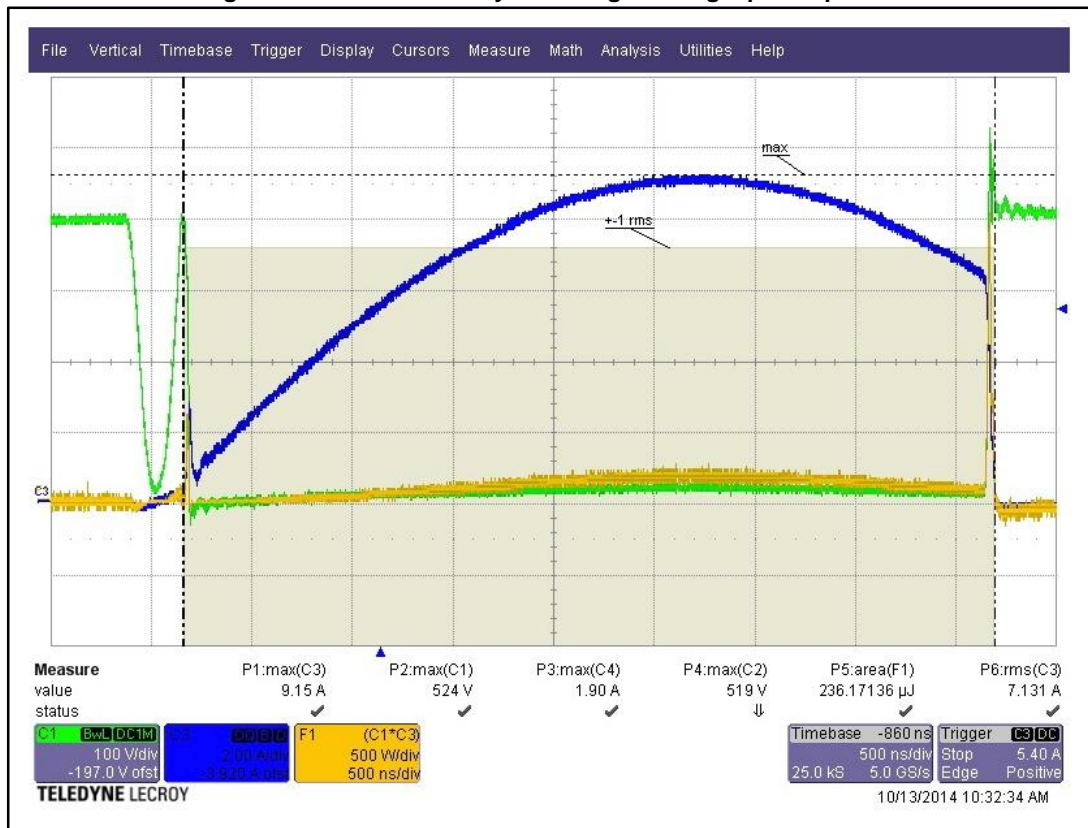
Evaluating the average current during the time when the event is present and noted the $R_{DS(ON)}$ of the device, it is possible to obtain the extra power forced inside the device.

Equation 27

$P_{pulse} = I^2_{RMS} * R_{DS(ON)}(Temp)$

Where I_{RMS} is the value measured and the $R_{DS(ON)}(T)$ is the value estimate of the $R_{DS(ON)}$ when the junction temperature is that of the final computation.

Similar results can be obtained if the power stress is noted measuring the energy during the test and the time of the pulse. In this case the data are:

Equation 28

$P_{pulse} = E_{Cond} / T_{pulse}$

$T_{pulse} = 4 \ \mu s$

Referring to *Figure 43* it is possible to summarize:

$P_{pulse} = 59 \ W$

The energy limit for semiconductor devices is represented by the junction temperature reached when it is submitted to an electrical stress. For this reason, semiconductor manufacturers put into the technical document of the device the limit (i.e. for STF6N60M2 T_{jmax}=150 °C) giving a graph (SOA) or some absolute maximum ratings for specific parameters. Each single limit reported in the datasheet guarantees that the T_j is lower than the T_{jmax} allowed. If it is not possible to find in the datasheet the conditions under investigation, it is possible to estimate the T_j using the graphs of the thermal impedance Z_{th}.

We need to evaluate the derating factor K and apply the formula (4.0). Let's start, referring to *Figure 44*, and considering T_c = 38 °C:

Figure 44: Thermal impedance for STF6N60M2 in TO220FP
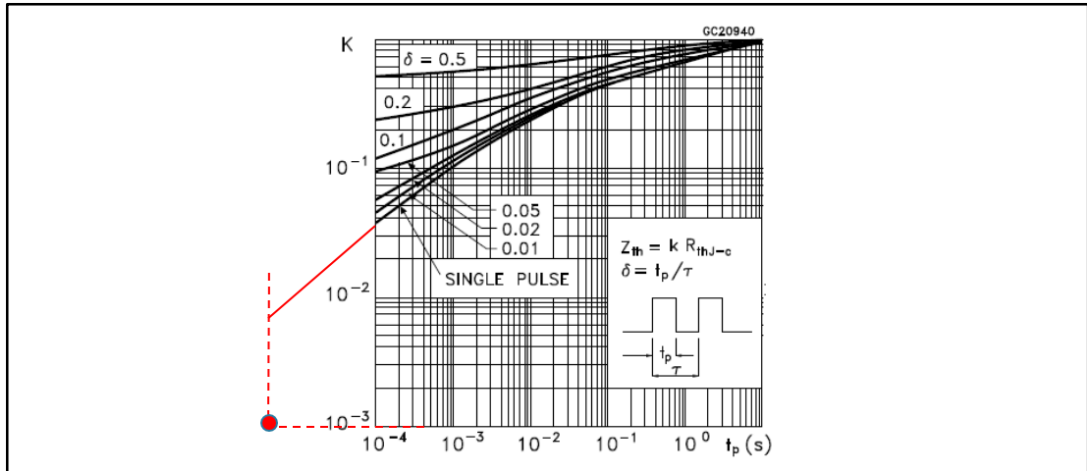
Taking into account the properties of the log-log Zth graph it is possible to extrapolate the K (4 µs) value:

Equation 29

$K_{(4µs)} = K_{(100µs)} * SQRT(4*10^{-6}/100^{*10-6})$

Then

$Z_{thj-c} = K_{(4µ)} * R_{thj-c} = 0.008*6.25 = 0.05$ °C/W

$T_j = T_c + P_{pulse} * Z_{thj-c} = 38 + (59* 0.05) = 40.95$ °C

Since the T_j reached during the stress is lower than the max T_{jmax} (for this case 150 °C), the device will operate in a safe manner.

The same approach can be used in case of avalanche phenomenon where a power pulse is forced into the device only for a single event.

8   References

1. N. Mohan, T. M. Undeland, W. P. Robbins: "*Power Electronics: converters, applications, and design*", Second edition, John Wiley & Sons, New York, 1995.
2. STF6N60M2 datasheet
3. Agnone, A. ; Chimento, F. ; Musumeci, S. ; Raciti, A. ; Privitera, G.*: "A New Thermal Model for Power MOSFET Devices Accounting for the Behavior in Unclamped Inductive Switching" Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*

9 Revision history

Table 4: Document revision history

Date	Version	Changes
20-Nov-2015	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY