AN946: PCI-Express 4.0 Jitter Requirements

PCI-Express (PCIe) is a point-to-point serial communication standard that supports 2.5 GB/s, 5 GB/s, 8 GB/s and 16 GB/s data rates. All of these standards require a 100 MHz ± 300 ppm reference clock (Refclk). Given the evolution and refinement of these PCIe standards, 4.0 specifically, there has been the addition of the 16 GB/s (base 4.0 standard), the removal of separate clock, and expansion of Gen1 and Gen2 transfer functions that creates additional requirements for the reference clocks to be used in the system at all data rates. In particular, the peaking value for 2.5 G and 5 G data rates has been lowered to 0.01 dB to be in alignment with the 8 G and 16 G data rates. This specification also increases the number of possible filter scenarios for Gen1 (2.5 G) data rates. Currently, this document is based on the PCI-Express Base Specification 4.0. Since the generation 4 PCI-Express specifications are still pending finalization, this documentation will undergo updates as appropriate.

KEY POINTS

- Describes new PCIe Gen 4 Requirements
- Demonstrates how to determine the filter functions to process your data for compliance
- Provides recommended test setup to make your measurements

1. Clocking Architectures

In the application note, "AN562: PCI Express 3.0 Jitter Requirements", there are three different clocking architectures supported by previous PCI-express specifications. Each one of these clocking architectures comes with very different jitter filtering characteristics which will impact the overall jitter performance of the system. For the PCI-Express 4.0 specification, there are only two types of architectures supported: Common Refclk (CC) and Independent Refclk.

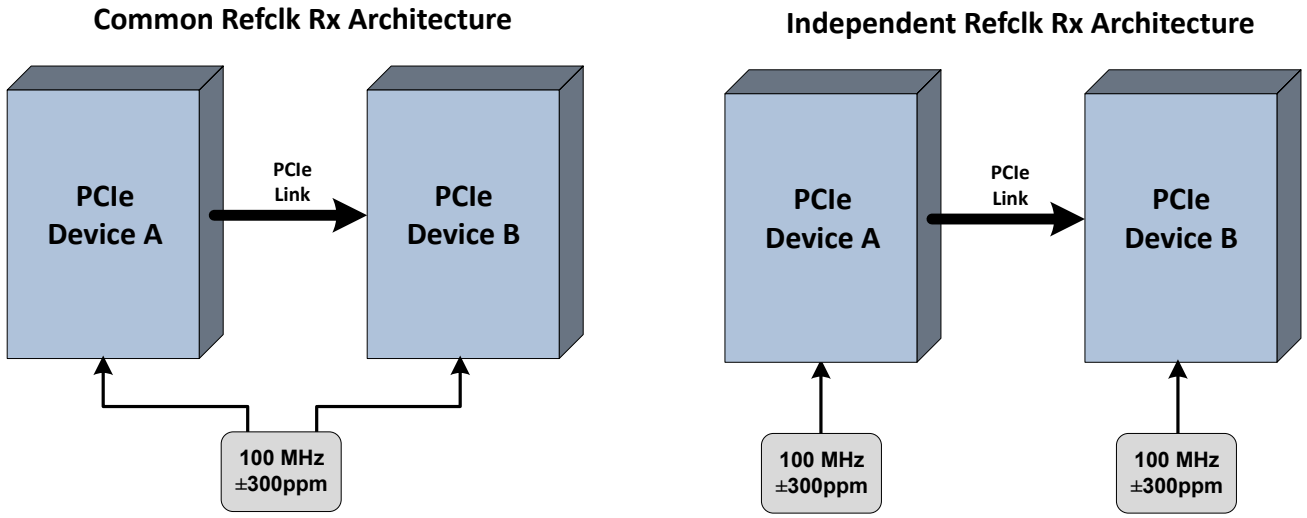


Figure 1.1. Clocking Architectures

2. Filters Applied to Data

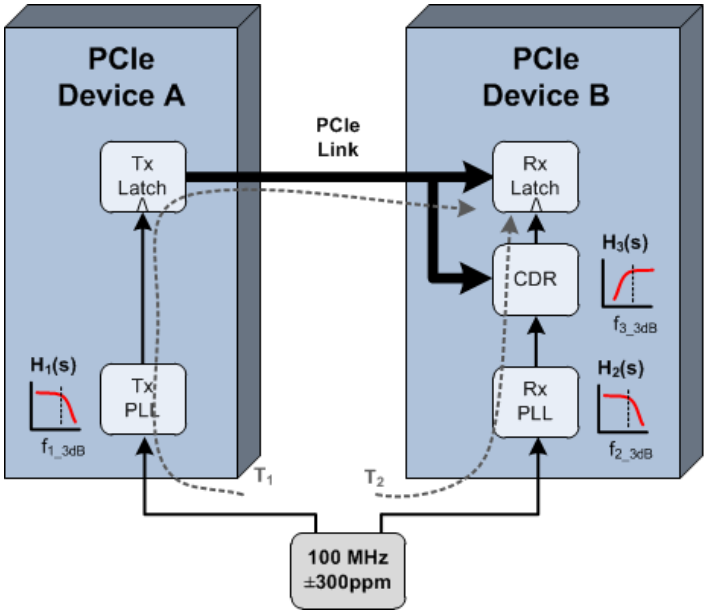
The PCI-Express specifications have traditionally specified multiple types of filtering to be applied to raw data. For Gen4, two types of filtering are required. The first is edge filtering of the raw data, which minimizes jitter caused by the finite sampling rate of the test equipment. This filtering is typically implemented by applying a 5 GHz bandwidth filter to the data. The second type of filtering, which is the primary topic of this application note, is through the use of PLL difference functions that are inherent in the combination of RX PLL, TX PLL, and CDR that are part of the PCI-Express system. The proper use of these filters will yield the effective Refclk jitter as it appears at the sample latch of the receiver.

3. Reference Clock Jitter Requirements

PCI-Express has very strict requirements for bit error rate of the system that is directly impacted by the jitter of the system. This jitter can be in the form of both random and deterministic components that originate from various parts of the system. The most direct and complex contributor to the jitter in the system is the Refclk. As such, the PCI-Express standards impose specific performance requirements on the Refclk to ensure that bit errors in the system are minimized. Because the Refclk can have such a major impact on the system, a Refclk with low jitter can easily improve the overall performance of the system.

3.1 Gen4 Common Clocked Requirements

In the common clocked architecture, the Refclk is distributed to both the transmitter and receiver of the two PCI-Express devices in the system. In this case, the overall transfer function for the Refclk that impacts the amount of jitter appearing at the receiver latch is defined by the difference function between the transmitter and receiver PLLs multiplied by the receiver latch high pass characteristic. This is further impacted by the transport delay difference between the two inputs to the RX and TX PLLs. Since the delay impacts the transfer function, thus affecting the jitter seen by the CDR, the delay should be applied to the TX PLL and the RX PLL transfer function separately and the worst case jitter from the two scenarios would be the result.



PLL and CDR Transfer Functions	
Tx PLL	$H_1(s) = \frac{2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}{s^2 + 2 \cdot s \cdot \zeta_1 \cdot \omega_{n1} + \omega_{n1}^2}$
Rx PLL	$H_2(s) = \frac{2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}{s^2 + 2 \cdot s \cdot \zeta_2 \cdot \omega_{n2} + \omega_{n2}^2}$
CDR	$H_3(s) = \frac{s}{s + \omega_{n3}}$ $\omega_{n3} = 2 \cdot \pi \cdot f_{3\_3dB}$
Refclk Path Delay Difference: T = | T1 – T2 |	

Figure 3.1. Gen4 Common Clock Requirements

$$H(s) = \left(H_1(s) \cdot e^{-s.T} - H_2(s)\right) \cdot H_3(s) \; H_{(s)} = \left(H_2(s) \cdot e^{-s.T} - H_1(s)\right) \cdot H_3(s)$$

PCI-Express 4.0 has modified the filter scenarios for 2.5 G and 5 G, bringing them in alignment with the minimum 0.01 dB peaking seen in the 8 G and 16 G specifications.

Table 3.1. PLL and CDR Characteristics for All Data Rates Based on the PCI-Express 4.0 Specification

<table>
<tr><th></th><th>Overall Jitter Transfer Functions</th><th>Transfer Function Parameters Defined</th></tr>
<tr><td>PCIe 2.5G</td><td rowspan="3">$H(s) = \left(H_1(s)\cdot e^{-s\cdot T} - H_2(s)\right)\cdot H_3(s)$
$H(s) = \left(H_2(s)\cdot e^{-s\cdot T} - H_1(s)\right)\cdot H_3(s)$
where T = 12 ns max</td><td>
<table>
<tr><th></th><th>.01 dB Peaking</th><th>3.0 dB Peaking</th></tr>
<tr><td>f_{1_3dB}, f_{2_3dB}
1.5 MHz</td><td>$\omega_{n1} = .0535\cdot 2\pi$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = .810\cdot 2\pi$ Mrad/s
$\zeta_1 = 0.54$</td></tr>
<tr><td>f_{1_3dB}, f_{2_3dB}
22.0 MHz</td><td>$\omega_{n1} = .785\cdot 2\pi$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = 74.68\cdot 2\pi$ Mrad/s
$\zeta_1 = 0.54$</td></tr>
</table>
f_{3_3dB} 1.5 MHz
16 Combinations
</td></tr>
<tr><td>PCIe 5G</td><td>
<table>
<tr><th></th><th>0.01 dB Peaking</th><th>1.0 dB Peaking</th></tr>
<tr><td>f_{1_3dB}
5.0 MHz</td><td>$\omega_{n1} = 1.12$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = 11.01$ Mrad/s
$\zeta_1 = 1.16$</td></tr>
<tr><td>f_{1_3dB}
16.0 MHz</td><td>$\omega_{n1} = 3.58$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = 35.26$ Mrad/s
$\zeta_1 = 1.16$</td></tr>
</table>
<table>
<tr><th></th><th>0.01 dB Peaking</th><th>3.0 dB Peaking</th></tr>
<tr><td>f_{2_3dB}
8.0 MHz</td><td>$\omega_{n2} = 1.79$ Mrad/s
$\zeta_2 = 14$</td><td>$\omega_{n2} = 26.86$Mrad/s
$\zeta_2 = .54$</td></tr>
<tr><td>f_{2_3dB}
16.0 MHz</td><td>$\omega_{n2} = 3.58$ Mrad/s
$\zeta_2 = 14$</td><td>$\omega_{n2} = 53.73$ Mrad/s
$\zeta_2 = .54$</td></tr>
</table>
f_{3_3dB} 5.0 MHz
64 Combinations
</td></tr>
<tr><td>PCIe 8G and 16G</td><td>
<table>
<tr><th></th><th>0.01 dB Peaking</th><th>2.0 dB Peaking</th></tr>
<tr><td>f_{1_3dB}
2.0 MHz</td><td>$\omega_{n1} = 0.448$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = 6.02$ Mrad/s
$\zeta_1 = 0.73$</td></tr>
<tr><td>f_{1_3dB}
4.0 MHz</td><td>$\omega_{n1} = 0.896$ Mrad/s
$\zeta_1 = 14$</td><td>$\omega_{n1} = 12.04$ Mrad/s
$\zeta_1 = 0.73$</td></tr>
</table>
<table>
<tr><th></th><th>0.01 dB Peaking</th><th>1.0 dB Peaking</th></tr>
<tr><td>f_{2_3dB}
2.0 MHz</td><td>$\omega_{n2} = 0.448$ Mrad/s
$\zeta_2 = 14$</td><td>$\omega_{n2} = 4.62$ Mrad/s
$\zeta_2 = 1.15$</td></tr>
<tr><td>f_{2_3dB}
5.0 MHz</td><td>$\omega_{n2} = 1.12$ Mrad/s
$\zeta_2 = 14$</td><td>$\omega_{n2} = 11.53$ Mrad/s
$\zeta_2 = 1.15$</td></tr>
</table>
f_{3_3dB} 10.0 MHz
64 Combinations
</td></tr>
</table>

The jitter specifications in the table below continue to be the same values given in past specifications. The most notable difference being that the Gen1 (2.5 GB/s) specification is expressed as a pk-pk value rather than an RMS like the rest of the generations of the specifications. This is due to the combination of the PLL to CDR bandwidths that exist. In particular with the CDR bandwidth being low at 1.5 MHz and the PLL bandwidths being equal or higher, then that allows SSC effects to pass through to the CDR as deterministic jitter. So, in that case it makes more sense to specify the jitter in terms of pk-pk rather than RMS.

Table 3.2. Jitter Limits for Common Clock Architecture

Data Rate	CC Jitter Limit
2.5 G	108 ps pk-pk
5.0 G	3.1 ps RMS
8.0 G	1.0 ps RMS
16.0 G	0.5 ps RMS

3.2 PCI-Express 4.0 Independent Refclk Requirements

Currently the PCI-Express 4.0 specification does not define the jitter transfer function and jitter limits for the Independent Refclk architecture. Instead, the approach taken is to allow the implementation and associated reference clock jitter and transfer function trade-offs that impact the overall transmitter jitter to be handled by the implementer. However, to minimize potential issues related to the system clock, Skyworks recommends that the maximum PLL BW and CDR filters be used as outlined in PCI-Express 3.1 specification to filter the reference clock jitter and that this result be less than the common clock jitter budgets divided by sqrt(2). The reason for dividing the limit by sqrt(2) is that if both the separate transmit and receive clocks each meet this rms jitter limit, then their combined rms jitter (which adds as the sqrt of the sum of the squares) will be less than the maximum system budget for Refclk jitter listed above.

4. Spread Spectrum Clocking and Bit Rate Tolerance

PCIe devices are specified to reliably transmit data when using a Refclk with a spread spectrum modulation rate of 30–33 kHz and modulation amplitude of 0 to –0.5% (i.e., downspread 0.5% in reference to the carrier frequency). Because each PCIe device must transmit within a bit rate of ±300 ppm of each other, the same Refclk must be supplied to both devices if SSC is used. In some system implementations, separate clocking architecture will therefore not work if SSC is turned on unless both clocks are synchronized to a common source. When the system is SRIS capable, the CDRs will be designed with loop filter characteristics such that the SSC can be tracked independently by the receiver allowing for SRIS support. Using SSC is possible for the Separate Reflck, Common Clocked RX Architecture, and Data Clocked RX Architecture. In addition to the SSC modulation rate and modulation amplitude, there is also a requirement for the maximum rate of change of the frequency on a Refclk with SSC active at 1250 ppm/µs. Refclks with the SSC active will need to meet additional phase jitter requirements at low frequency as shown in the table below.

Table 4.1. Limits for Phase Jitter from the Reference Clock with SSC Active

Frequency	Maximum Peak-to-Peak Phase Jitter (ps)
30 kHz	25000
100 kHz	1000
500 kHz	25

5. Refclk Test Setup

The reference clock test setup as defined in the 3.1 specification assumes that only the reference clock generator is present. It takes the approach of measuring with the worst case system degradation in place using a 12-inch differential trace that is terminated by two 2 pF capacitors. GEN 4.0 has refined the specification to a 15 dB loss at 4 GHz and a 2 pF load.

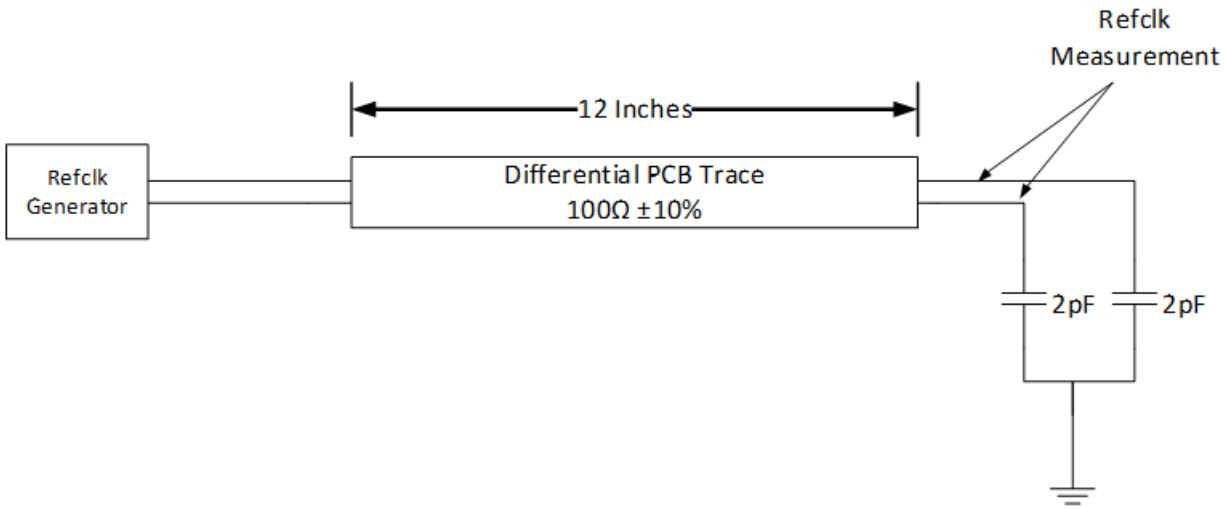


Figure 5.1. Refclk Test Setup

6. A Typical PCI Express Application

Skyworks offers a variety of clock devices that allows for flexible PCIe Refclk distribution. For example, the Si5338 I2C Programmable Any-Frequency, Any-Output Quad Clock Generator is an ideal device for generating PCIe clocks:

- Compliant with PCI Express 4.0 and legacy standards (2.1, 1.1)
- PCI Express 4.0 jitter = 0.12 ps RMS (4x lower than the requirement)
- Generates up to four 100 MHz HCSL output clocks but is programmable with other frequencies and signal formats. This allows one clock device to generate PCIe Refclks and other board clocks of different frequencies and signal formats.
- Output frequencies are programmable per output from 5 MHz to 710 MHz.
- Independent VDDO for each output clock enables integrated level translation.
- Output signal formats are programmable per output as HCSL, LVDS, LVPECL or LVCMOS.
- Excellent jitter performance allows Refclk generation for Common Refclk RX, Data Clocked RX, and Separate Clock Architectures.
- Spread spectrum can be enabled or disabled per output with programmable modulation rate and modulation amplitude per output.
- Built-in HCSL terminations.
- Small 4x4 mm package

A typical use of the Si5338 in a PCIe application is shown in the figure below. In this example the Si5338 replaces a 100 MHz clock oscillator with spread spectrum, a 1:2 HCSL buffer, a 66.6667 MHz clock oscillator, and a 125 MHz clock oscillator.

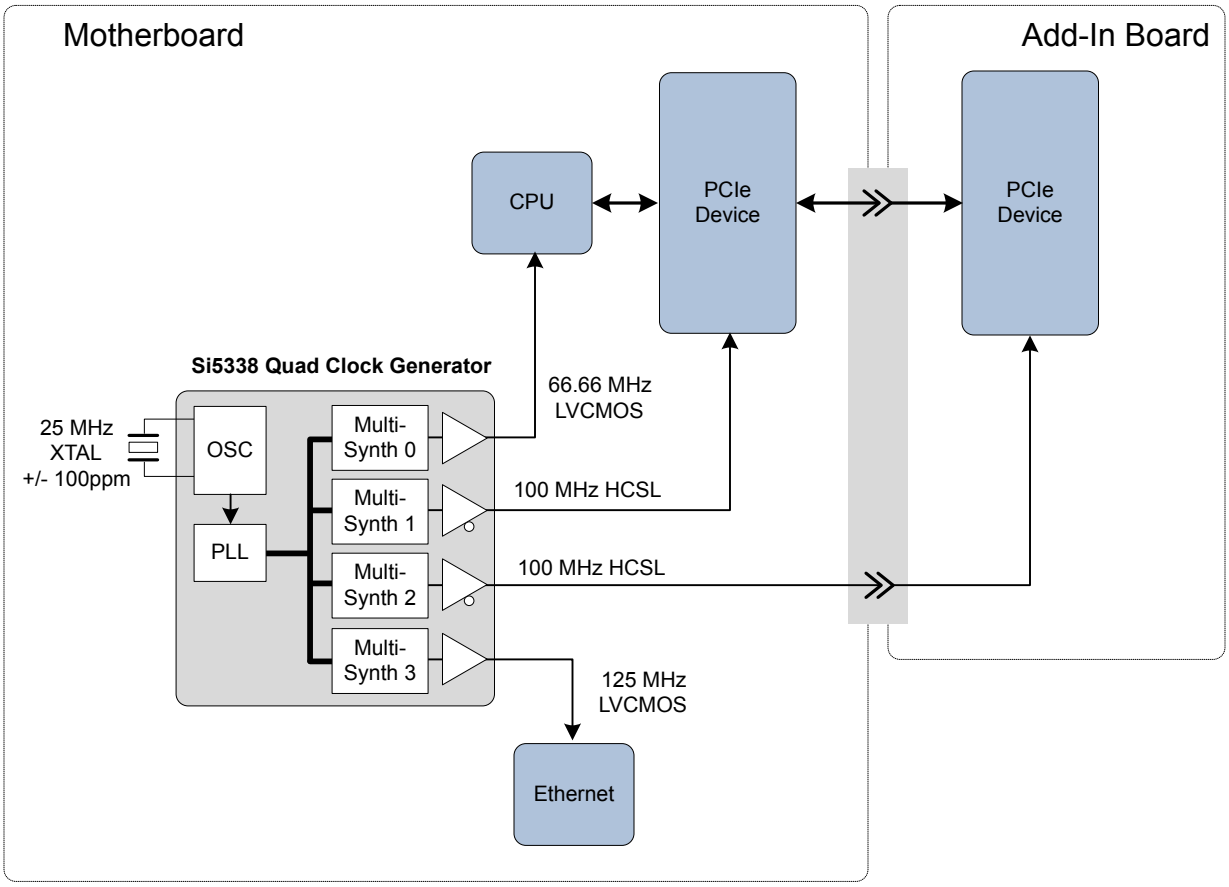


Figure 6.1. PCIe Application Using the Si5338 as the Refclk Generator

Appendix 1. PCI Express Compliance Report

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