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of Engineering and Management
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**DEPARTMENT OF ELECTRONICS & COMMUNICATION
ENGINEERING**

**ANALOG ELECTRONICS LABORATORY
LAB MANUAL – 15ECL37
III-SEMESTER
2016-2017**

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SYLLABUS

1. Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency:
Full Wave Rectifier (b) Bridge Rectifier
2. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).
3. Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.
4. Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.
5. Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain bandwidth product from its frequency response.
6. Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
7. Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.
8. Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
9. Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.
10. Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.
11. Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.
a) Hartley Oscillator (b) Colpitts Oscillator
12. Design and set-up the crystal oscillator and determine the frequency of oscillation.

Course objectives:

This laboratory course enables students to get practical experience in design, assembly, testing and evaluation of

- Rectifiers and Voltage Regulators.
- BJT characteristics and Amplifiers.
- JFET Characteristics and Amplifiers.
- MOSFET Characteristics and Amplifiers.
- Power Amplifiers.
- RC-Phase shift, Hartley, Colpitts and Crystal Oscillators

Course outcomes:

Through this course, the students:

- Acquire a basic knowledge in solid state electronics including diodes, MOSFET, BJT, and operational amplifier.
- Develop the ability to analyze and design analog electronic circuits using discrete components.
- Observe the amplitude and frequency responses of common amplification circuits.
- Design, construct, and take measurement of various analog circuits to compare experimental results in the laboratory with theoretical analysis.

LAB INSTRUCTIONS

Do's

- Ensure your presence five minutes before the commencement of the lab.
- Attend all the lab sessions without fail.
- Come well prepared for every lab session.
- Complete and Bring the Lab records regularly.
- Ensure the proper polarity of cables before connecting the kits.
- Ensure the checking of the circuit of circuit connections before turning ON the circuit.
- Tuck in your shirts and not to play with instruments laid on the bench.
- Wearing loose garments inside the lab is strictly prohibited.
- You have to wear shoes compulsorily.
- Keep the space around you clear for others.

Don'ts

- Don't bring the Cell phone and food items to Lab.
- Don't switch ON voltage supplies after making circuit connections in the absence of the teacher.
- Don't rotate the Knobs unnecessarily.

LIST OF EXPERIMENTS

Sl No	Title	Page No
1	Rectifiers	1
2	Clippers and Clampers	7
3	Zener Diode	20
4	BJT Amplifiers	23
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6	Hartley and Colpitts oscillator	31
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Experiment No : 1**DATE :****FULL WAVE RECTIFIER****AIM:**

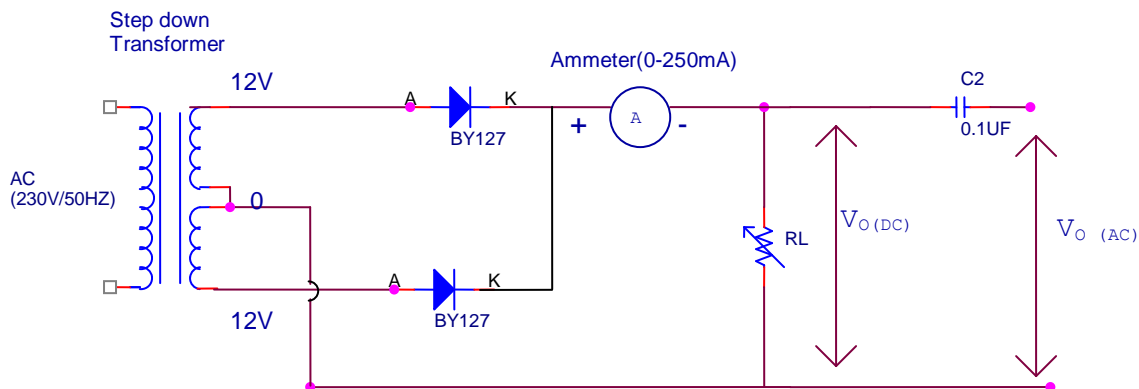
To study the full wave rectifier and to calculate ripple factor and efficiency and Regulation with filter and without filter.

COMPONENTS REQUIRED:

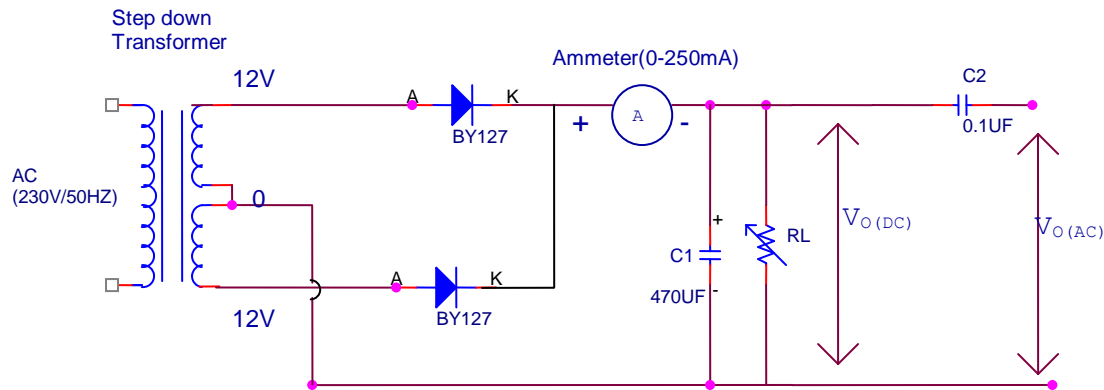
Sl. No.	Components Details	Specification	Qty
1.	Diodes	BY127	2 Nos.
2.	Capacitor	0.1 μ f, 470 μ f	Each 1 No.
3.	Power Resistance Board		1 No.
4.	Step down Transformer	12 V	1 No.
5.	CRO, Multimeter, Milliammeter, Connecting Board		

THEORY:

The center tapped full wave rectifier circuit is similar to a half wave rectifier circuit, using two diodes and a center tapped transformer. Both the input half cycles are converted into unidirectional pulsating DC.

CIRCUIT DIAGRAM:**FULL WAVE RECTIFIER WITHOUT FILTER CAPACITOR**

FULL WAVE RECTIFIER WITH FILTER CAPACITOR



DESIGN:

$V_{in\ rms} = 12V$

$$V_{in\ m} = \sqrt{2} V_{in\ rms} = 16.97V$$

$$V_{O\ DC} = 2V_m / \pi = 10.8V$$

Given $V_{O\ DC} = 10V$

$$I_{O\ DC} = 100mA$$

$$R_L = V_{O\ DC} / I_{O\ DC} = 100\Omega$$

$Ripple = r = V_{o\ rms} / V_{O\ DC} = 0.48$

Design for the filter capacitor

$$Ripple = 1 / (4\sqrt{3} f C R_L)$$

Given $r = .06$

$$C = 1 / (4\sqrt{3} f r R_L)$$

$$R_L = 100\Omega$$

$$f = 50Hz$$

$= 470UF$

Efficiency $\eta = P_{DC} / P_{AC} \Rightarrow (I_{DC}^2 * R_L) / [(I_{rms})^2 * (R_L + R_F)]$

Regulation $\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$

PROCEDURE:

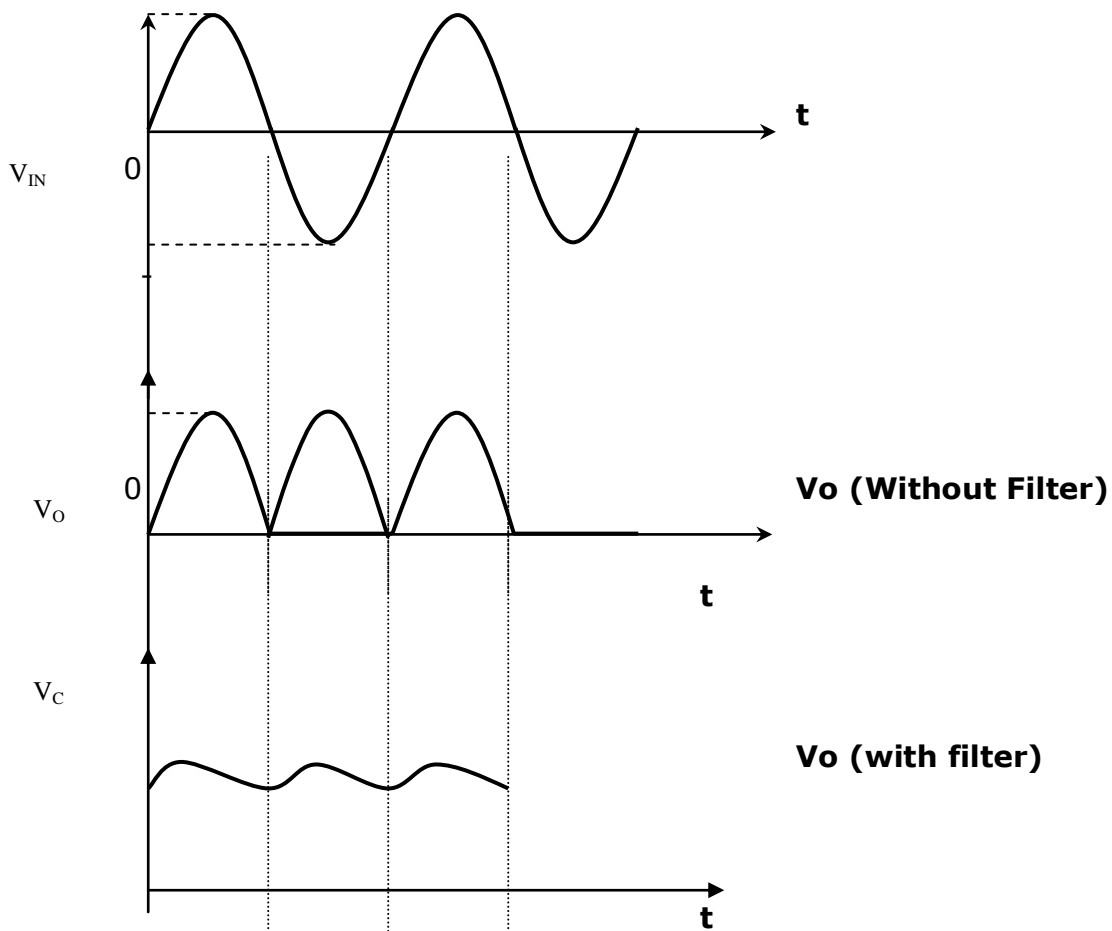
1. Connections are made as shown in the circuit diagram
2. Switch on the AC power supply

3. Observe the wave form on CRO across the load resistor and measure the o/p amplitude and frequency.
4. Note down R_L , I_{DC} , V_{ODC} , V_{INAC} , V_{OAC} in the tabular column for different load resistances.
5. Calculate the ripple and efficiency and regulation for each load resistance.
6. Repeat the above procedure with filter capacitor.

TABULAR COLUMN:

Sl. No.	R_L	I_{DC}	V_O (DC)	V_{IN} (AC)	V_O (AC)	Ripple	Efficiency	Regulation

WAVEFORMS:



Experiment No : 1b**DATE :****BRIDGE RECTIFIER****AIM:**

To study the bridge rectifier and to calculate ripple factor and efficiency and regulation with filter and without filter.

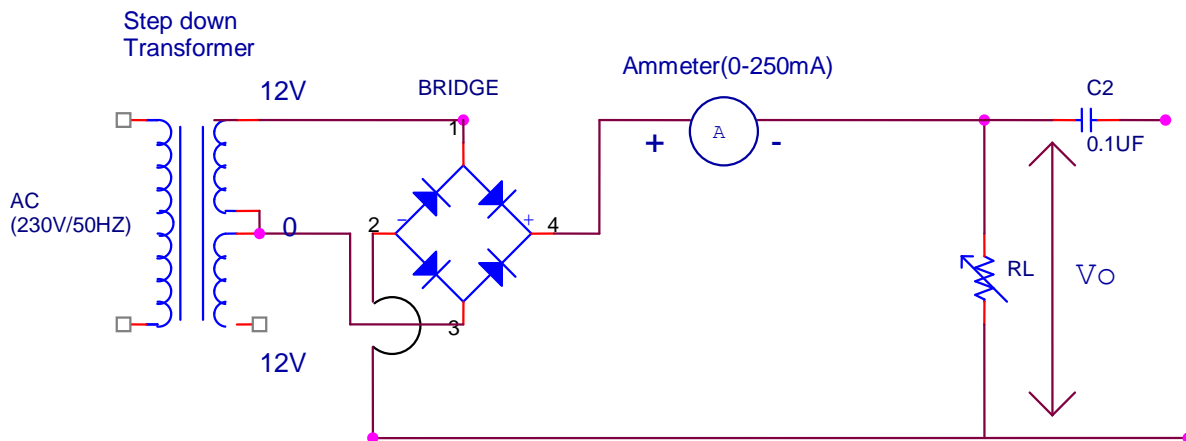
COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Diodes	BY127	4 Nos.
2.	Capacitor	$0.1\mu f$, $470\mu f$	Each 1 No.
3.	Power Resistance Board		1 No.
4.	Step down Transformer	12 V	1 No.
5.	CRO, Multimeter, Milliammeter, Connecting Board		

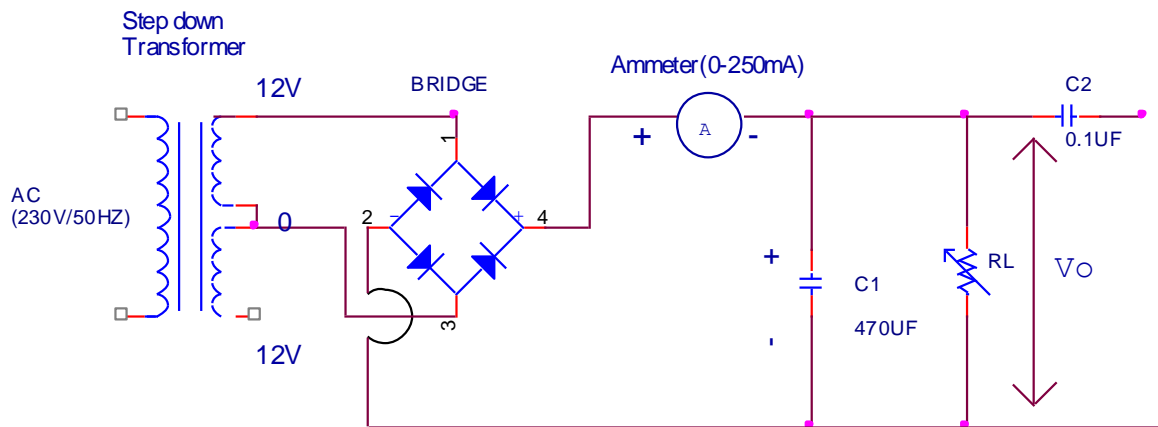
THEORY:

The bridge rectifier circuit is essentially a full wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge. To one diagonal of the bridge, the ac voltage is applied through a transformer and the rectified dc voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer; ac voltage can be directly applied to the bridge.

The bridge rectifier circuit is mainly used as a power rectifier circuit for converting ac power to dc power, and a rectifying system in rectifier type ac meters, such as ac voltmeter in which the ac voltage under measurement is first converted into dc and measured with conventional meter.

CIRCUIT DIAGRAM:**BRIDGE RECTIFIER WITHOUT FILTER CAPACITOR**

BRIDGE RECTIFIER WITH FILTER CAPACITOR



DESIGN:

$V_{in\ rms} = 12V$

$$V_{in\ m} = \sqrt{2} V_{in\ rms} = 16.97V$$

$$V_{O\ DC} = 2V_m / \pi = 10.8V$$

Given $V_{O\ DC} = 10V$

$$I_{O\ DC} = 100mA$$

$$R_L = V_{O\ DC} / I_{O\ DC} = 100\Omega$$

$Ripple = r = V_{o\ rms} / V_{O\ DC} = 0.48$

Design for the filter capacitor

$$Ripple = 1 / (4\sqrt{3} f C R_L)$$

Given $r = .06$

$$C = 1 / (4\sqrt{3} f r R_L)$$

$$R_L = 100\Omega$$

$$f = 50Hz$$

$= 470UF$

Efficiency

$$\eta = P_{DC} / P_{AC}$$

$$= (I_{DC}^2 * R_L) / [(I_{rms})^2 * (R_L + R_F)]$$

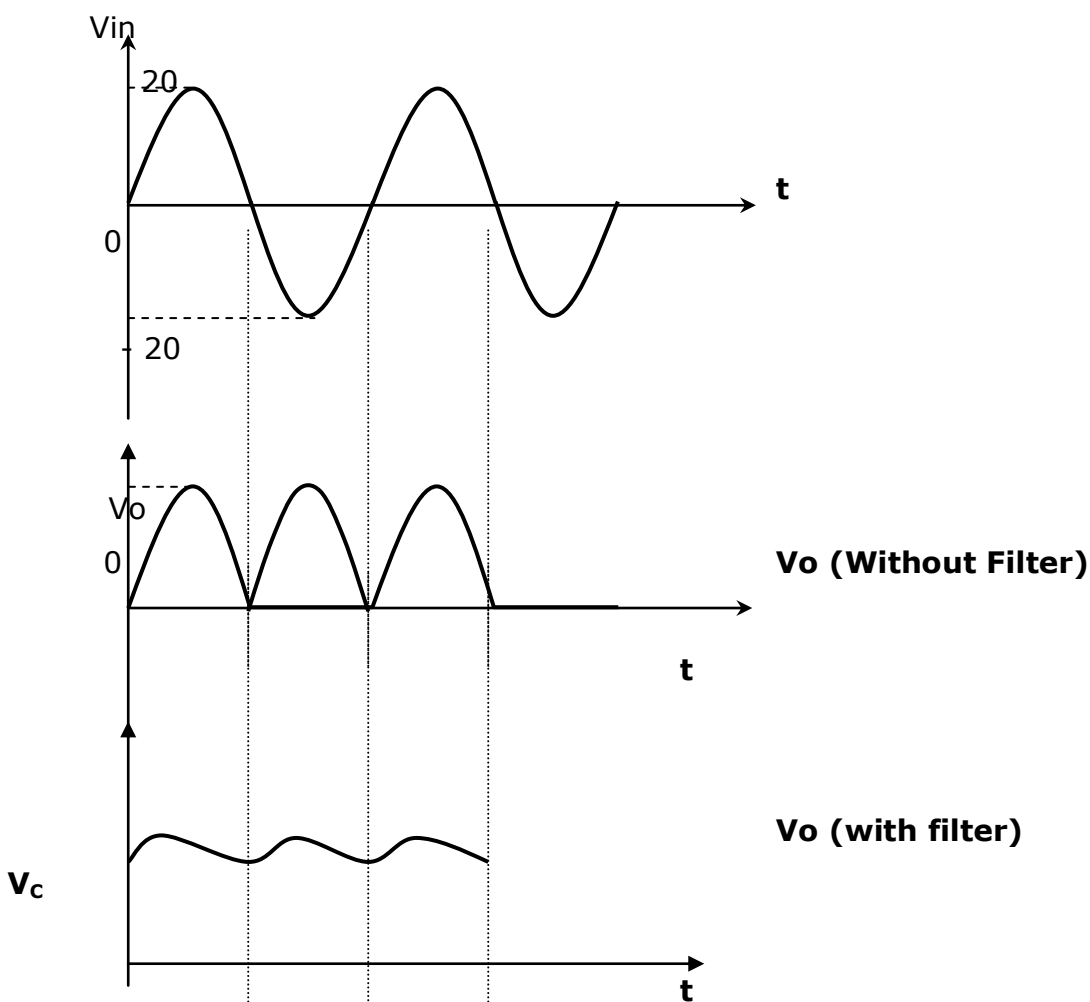
Regulation $\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$

PROCEDURE:

1. Connections are made as shown in the circuit diagram
2. Switch on the AC power supply
3. Observe the wave form on CRO across the load resistor and measure the o/p amplitude and frequency.
4. Note down R_L , I_{DC} , V_{ODC} , V_{INAC} , V_{OAC} in the tabular column for different load resistances.
5. Calculate the ripple factor, efficiency and regulation for each load resistance.
6. Repeat the above procedure with filter capacitor.

TABULAR COLUMN:

Sl. No.	R_L	I_{DC}	V_O (DC)	V_{IN} (AC)	V_O (AC)	Ripple	Efficiency	Regulation

WAVEFORMS:

Experiment No : 2a**DATE :****CLAMPING CIRCUITS****AIM:**

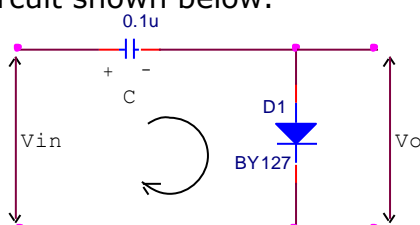
Design a clamping circuit for the given output.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Diodes	BY127	1 No
2.	Capacitors	0.1 μ F	1 No
	Signal generator, Cathode Ray Oscilloscope (CRO) with Probes, Dual Power Supply, Connecting Board		

THEORY:

A clamper is one, which provides a D.C shift to the input signal. The D.C shift can be positive or negative. The clamper with positive D.C shift is called positive clamper and clamper with negative shift is called negative clamper. Consider a clamper circuit shown below.



In the positive half cycle as the diode is forward biased the capacitor charges to the value $(V_{IN} - V_D)$ with the polarity as shown in the figure. In the negative half cycle the diode is reverse biased. Hence the output is $V_O = V_{IN} - V_C$.

Initially let us assume that the capacitor has charged to $(V_{IN} - V_D)$ i.e.
 $(5 - 0.5) = 4.5V$

Then in the positive half cycle diode is forward biased and applying KVL to the loop,

$$\therefore V_{in} - V_C - V_0 = 0 \quad V_0 = V_{in} - V_C$$

$$\text{When } V_{in} = 0 \quad V_0 = 0 - 4.5 = -4.5V$$

$$V_{in} = 5V \quad V_0 = 5 - 4.5 = 0.5V$$

In the negative half cycle

$$\text{When } V_{in} = -5V \quad V_0 = -5 - 4.5 = -9.5V$$

The output shifts between 0.5V and -9.5V. Here the output has shifted down by 4.5V

The peak to peak voltage at the output of a clamper is the same as that of the input.

CIRCUIT DIAGRAM AND DESIGN:

Given $V_{in} = 10V$ (p-p)

A] In the positive half cycle:

Diode is forward biased.

Applying KVL to loop 1

$$V_{in} - V_C - V_D = 0$$

$$\begin{aligned} V_C &= V_{in} - V_D \\ &= 5 - 0.5 \Rightarrow 4.5V \end{aligned}$$

In the negative half cycle:

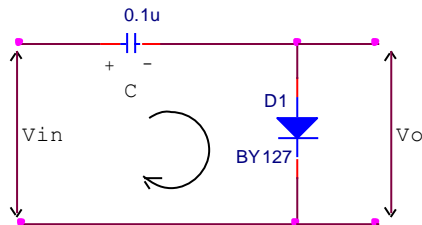
$$V_{in} - V_C - V_0 = 0$$

$$V_0 = V_{in} - V_C$$

$$\text{When } V_{in} = 0 \quad V_0 = -4.5V$$

$$\text{When } V_{in} = 5V \quad V_0 = 0.5V$$

$$\text{When } V_{in} = -5V \quad V_0 = -9.5V$$



B] In the negative half cycle:

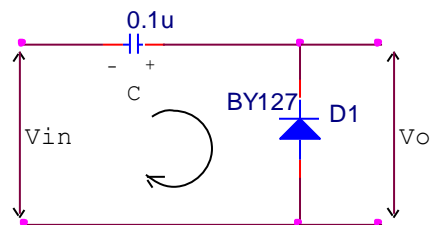
Diode is forward biased

Applying KVL to loop 1

$$V_{in} + V_C + V_D = 0$$

$$V_C = - (V_{in} + V_D)$$

$$\begin{aligned} V_C &= - (-5 + 0.5) \\ &= 4.5V \end{aligned}$$



In the positive half cycle:

Diode is reverse biased.

Apply KVL to the loop

$$V_{in} + V_C - V_0 = 0$$

$$V_0 = V_{in} + V_C$$

$$\text{When } V_{in} = 0 \quad V_0 = 4.5V$$

$$\text{When } V_{in} = 5V \quad V_0 = 5 + 4.5 = 9.5V$$

$$\text{When } V_{in} = -5V \quad V_0 = -0.5V$$

C] Assume $V_R = 2V$

In the positive half cycle:

Diode is forward biased.

Apply KVL to loop 1

$$V_{in} - V_C - V_D - V_R = 0$$

$$V_C = V_{in} - V_D - V_R$$

$$= 5 - 0.5 - 2$$

$$= 2.5V$$

In the negative half cycle:

Diode is reverse biased

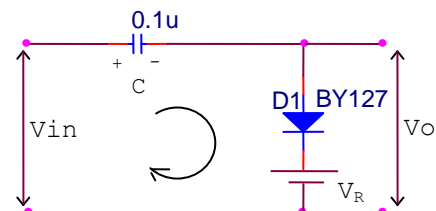
$$V_{in} - V_C - V_0 = 0$$

$$V_0 = V_{in} - V_C$$

$$\text{When } V_{in} = 0V \quad V_0 = -2.5V$$

$$\text{When } V_{in} = 5V \quad V_0 = 2.5V$$

$$\text{When } V_{in} = -5V \quad V_0 = -7.5V$$



D] Assume $V_R = 2V$

In the positive half cycle:

Diode is forward biased and the capacitor charges.

Apply KVL to loop 1

$$V_{in} - V_C - V_D + V_R = 0$$

$$V_C = V_{in} - V_D + V_R$$

$$= 5 - 0.5 + 2$$

$$= 6.5V$$

In the negative half cycle:

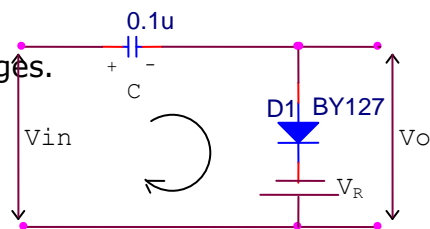
$$V_{in} - V_C - V_0 = 0$$

$$V_0 = V_{in} - V_C$$

$$\text{When } V_{in} = 0V \quad V_0 = -6.5V$$

$$\text{When } V_{in} = 5V \quad V_0 = -1.5V$$

$$\text{When } V_{in} = -5V \quad V_0 = -11.5V$$



E] In the negative half cycle:

Assume $V_R = 2V$

Diode is forward biased and capacitor charges.

Apply KVL to the loop1

$$V_{in} + V_C + V_D + V_R = 0$$

$$V_C = - (V_{in} + V_R + V_D)$$

$$= - (-5 + 0.5 + 2)$$

$$= 2.5V$$

From the fig. we see that

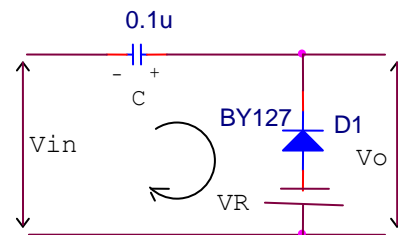
$$V_{in} + V_C - V_O = 0$$

$$V_O = V_{in} + V_C$$

$$\text{When } V_{in} = 0 \quad V_O = 2.5V$$

$$\text{When } V_{in} = 5V \quad V_O = 7.5V$$

$$\text{When } V_{in} = -5V \quad V_O = -2.5V$$

**F] $V_R = 2V$** **In the negative half cycle:**

Diode is forward biased and capacitor charges.

Apply KVL to loop 1

$$V_{in} + V_C + V_D - V_R = 0$$

$$V_C = - (V_{in} + V_D - V_R)$$

$$= - (-5 + 0.5 - 2)$$

$$= 6.5V$$

From the circuit we see that,

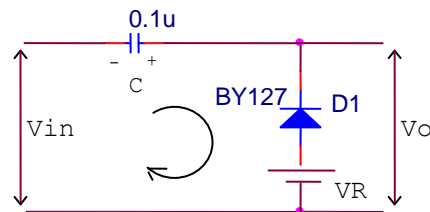
$$V_{in} + V_C - V_O = 0$$

$$V_O = V_{in} - V_C$$

$$\text{When } V_{in} = 0V \quad V_O = 6.5V$$

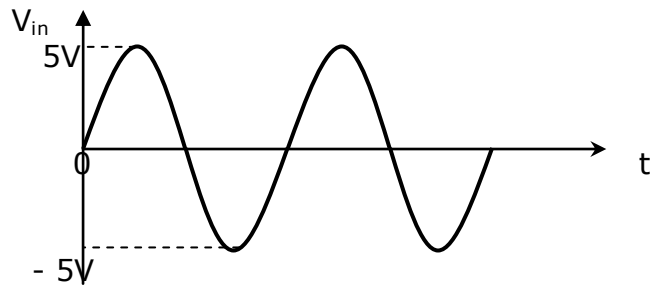
$$\text{When } V_{in} = 5V \quad V_O = 11.5V$$

$$\text{When } V_{in} = -5V \quad V_O = 1.5V$$

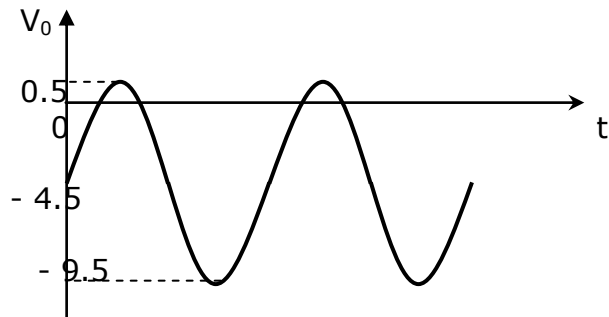
**PROCEDURE:**

1. Rig up the circuit as shown in the circuit diagram.
2. Give a sinusoidal input of 10V peak to peak
3. Check and verify the output.

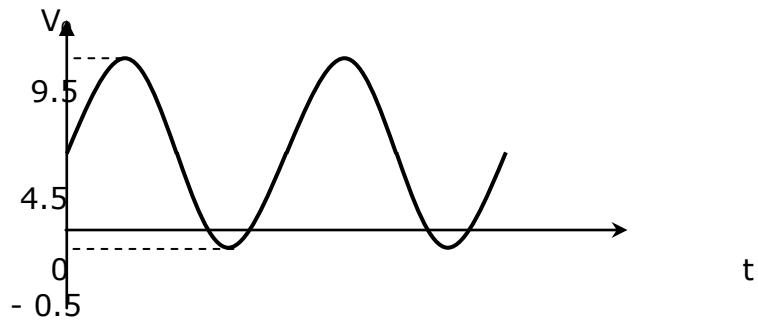
WAVEFORMS:



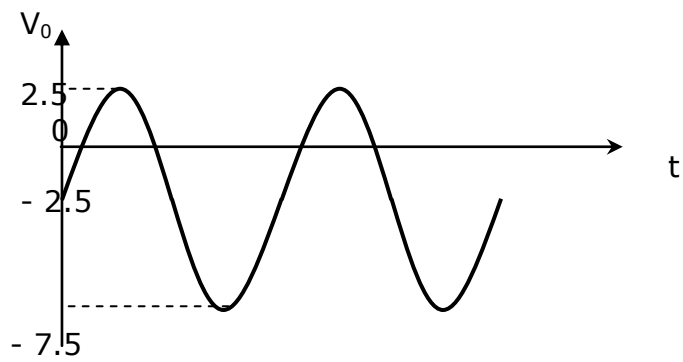
[A]

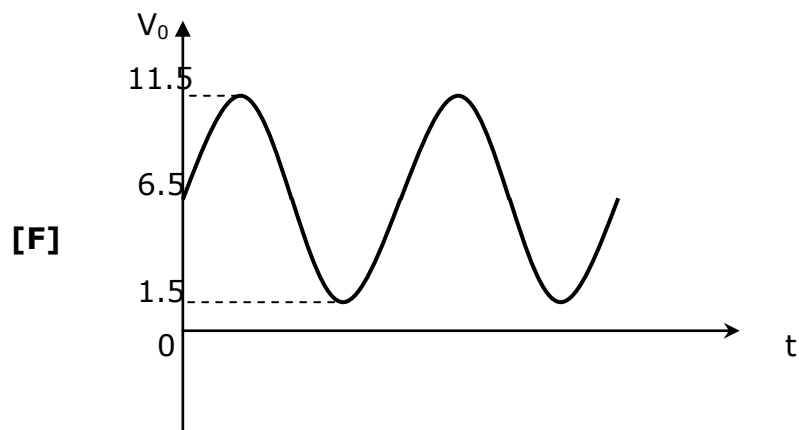
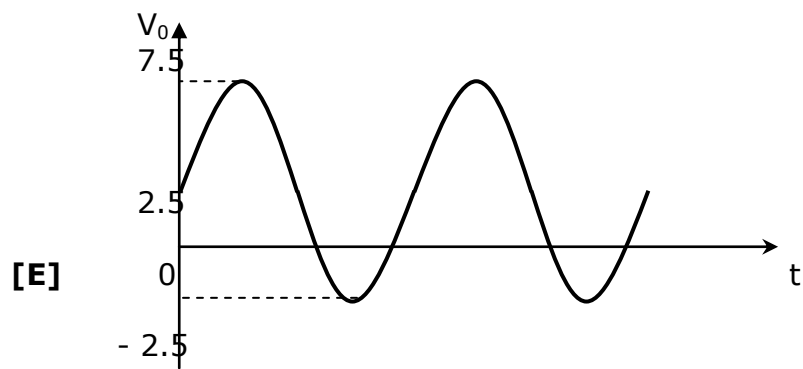
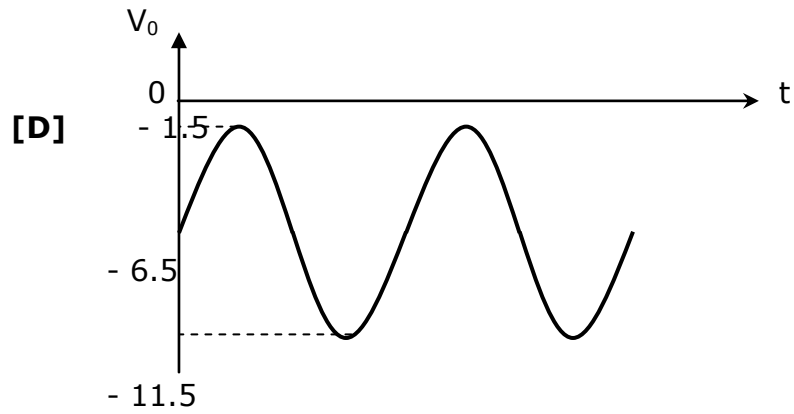


[B]



[C]





RESULT :

Experiment No : 2b**DATE :****CLIPPING CIRCUITS****AIM:**

Design a clipping circuit for the given values.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Diodes	BY127	1 No
2.	Resistors	10 K Ω	1 No

THEORY:

The process by which the shape of a signal is changed by passing the signal through a network consisting of linear elements is called linear wave shaping. Most commonly used wave shaping circuit is clipper. Clipping circuits are those, which cut off the unwanted portion of the waveform or signal without distorting the remaining part of the signal. There are two types of clippers namely parallel and series. A series clipper is one in which the diode is connected in series with the load and a parallel clipper is one in which the diode is connected in parallel with the load.

CIRCUIT DIAGRAM AND DESIGN:

Assume $V_{in} = 10V$ (Peak to Peak)

(a) Consider the circuit in fig. 1

In the **positive half cycle** D is forward biased

$$\therefore V_0 = V_{in} - 0.5 = 5 - 0.5 = 4.5 \text{ (0.5V is the diode drop)}$$

In the **negative half cycle** D is reverse biased

$$\therefore V_0 = 0V$$

(b) Consider the circuit in fig. 2

In the **positive half cycle** D is reverse biased

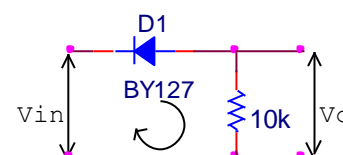
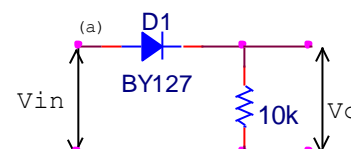
$$\therefore V_0 = 0V$$

In the **negative half cycle** D is forward biased

Applying KVL to the loop

$$\therefore V_{in} + V_D - V_0 = 0$$

$$\therefore V_0 = V_{in} + V_D = -5 + 0.5 = -4.5V$$



(c) Consider the circuit in fig. 3

Given $V_R = 2.5V$

In the **positive half cycle**

(i) When $|V_{in}| > |V_D + V_R|$, D is forward biased

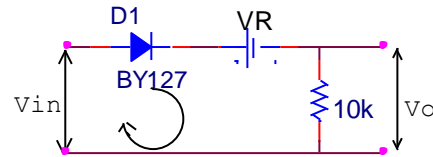
Applying KVL, we get

$$V_{in} = V_D + V_R + V_0$$

$$V_0 = V_{in} - V_D - V_R$$

$$V_0 = 5 - 0.5 - 2.5$$

$$V_0 = 2V$$



(ii) When $|V_{in}| < |V_D + V_R|$, D is reverse biased

$$V_0 = 0V$$

In the **negative half cycle**, D is reverse biased

$$V_0 = 0V$$

(d) Consider the circuit in fig. 4

Assume $V_R = 3V$

In the **positive half cycle**, D is reverse biased

$$V_0 = 0V$$

In the **negative half cycle**

(i) When $|V_{in}| > |V_D + V_R|$, D is forward biased

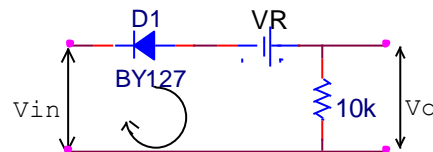
Applying KVL, we get

$$V_{in} = -V_D - V_R + V_0$$

$$V_0 = V_{in} + V_D + V_R$$

$$V_0 = -5 + 0.5 + 3$$

$$V_0 = -1.5V$$



(ii) When $|V_{in}| < |V_D + V_R|$, D is reverse biased

$$V_0 = 0V$$

(e) Consider the circuit in fig. 5

Assume $V_{R1} = 2.5V$ and $V_{R2} = 3V$

In the **positive half cycle**, D_2 is reverse biased

(i) When $|V_{in}| > |V_{D1} + V_{R1}|$, D_1 is forward biased

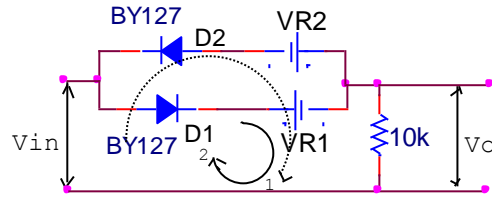
Applying KVL, we get

$$V_{in} = V_{D1} + V_{R1} + V_0$$

$$V_0 = V_{in} - V_{D1} - V_{R1}$$

$$V_0 = 5 - 0.5 - 2.5$$

$$V_0 = 2V$$



(ii) When $|V_{in}| < |V_{D1} + V_{R1}|$, D_1 is reverse biased

$$V_0 = 0V$$

In the **negative half cycle**

(i) When $|V_{in}| > |V_{D2} + V_{R2}|$, D_2 is forward biased

Applying KVL, we get

$$V_{in} = -V_{D2} - V_{R2} + V_0$$

$$V_0 = V_{in} + V_{D2} + V_{R2}$$

$$V_0 = -5 + 0.5 + 3$$

$$V_0 = -1.5V$$

(ii) When $|V_{in}| < |V_{D2} + V_{R2}|$, D_2 is reverse biased

$$V_0 = 0V$$

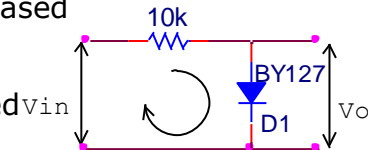
(f) Consider the circuit in fig. 6

During the **positive half cycle**, D is forward biased

$$V_0 = V_D = 0.5V$$

During **negative half cycle**, D is reverse biased

$$V_0 = V_{in}$$



(g) Consider the circuit in fig. 7

During positive half cycle,

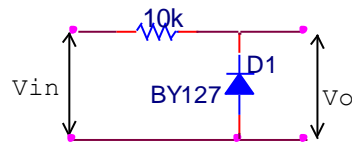
D is reverse biased

$$V_0 = V_{in}$$

During negative half cycle,

D is forward biased

$$V_0 = -V_D = -0.5V$$



(h) Consider the circuit in fig. 8

During positive half cycle

(i) When $|V_{in}| > |V_D + V_R|$,

D is forward biased

$$V_0 = V_D + V_R = 0.5 + 2.5$$

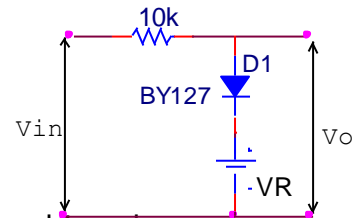
$$V_0 = 3V$$

(ii) When $|V_{in}| < |V_D + V_R|$, D is reverse biased

$$V_0 = V_{in}$$

During negative half cycle, D is reverse biased

$$V_0 = V_{in}$$



(i) Consider the circuit in fig. 9

Assume $V_R = 2.5V$

During positive half cycle,

D is reverse biased

$$V_0 = V_{in}$$

During negative half cycle

(i) When $|V_{in}| > |V_D + V_R|$,

D is forward biased

Applying KVL to the loop, we get

$$V_0 = -V_D - V_R = -0.5 - 2.5$$

$$V_0 = -3V$$

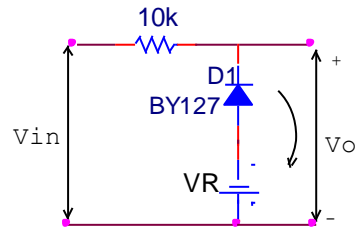
(ii) When $|V_{in}| < |V_D + V_R|$,

D is reverse biased

$$V_0 = V_{in}$$

During negative half cycle, D is reverse biased

$$V_0 = V_{in}$$



(j) Consider the circuit in fig. 10

Assume $V_{R1} = V_{R2} = 2.5V$

During positive half cycle, D_2 is reverse biased.

(i) When $|V_{in}| > |V_{D1} + V_{R1}|$, D_1 is forward biased

$$V_0 = V_{D1} + V_{R1} = 0.5 + 2.5$$

$$V_0 = 3V$$

(ii) When $|V_{in}| < |V_{D1} + V_{R1}|$,

D_1 is reverse biased

$$V_0 = V_{in}$$

During negative half cycle,

D_1 is reverse biased

(i) When $|V_{in}| > |V_{D2} + V_{R2}|$, D_2 is forward biased

Applying KVL to the loop, we get

$$V_0 = -V_{D2} - V_{R2} = -0.5 - 2.5$$

$$V_0 = -3V$$

(ii) When $|V_{in}| < |V_{D2} + V_{R2}|$, D_2 is reverse biased

$$V_0 = V_{in}$$

(k) Consider the circuit in fig. 11

Assume $V_{R1} = 3.5V$ and $V_{R2} = 2V$

During positive half cycle

(i) When $|V_{in}| > |V_{D1} + V_{R1}|$

D_1 is forward biased and

D_2 is reverse biased

$$V_0 = V_{D1} + V_{R1} = 0.5 + 3.5 = 4V$$

(ii) When $|V_{in}| < |V_{R2} - V_{D2}|$

D_1 is reverse biased and

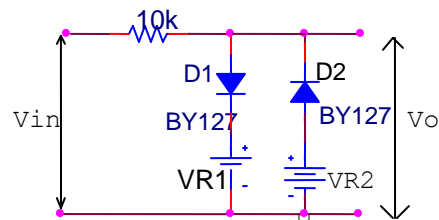
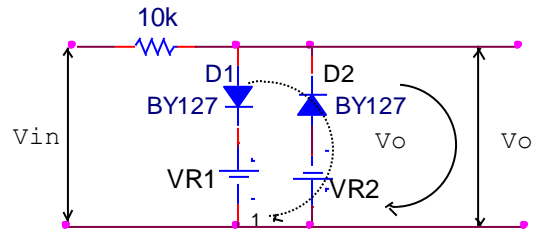
D_2 is forward biased

$$V_0 = -V_{D2} + V_{R2} = -0.5 + 2 \Rightarrow 1.5V$$

During negative half cycle,

D_1 is reverse biased and D_2 is forward biased

$$V_0 = -V_{D2} + V_{R2} = -0.5 + 2 \Rightarrow V_0 = 1.5V$$

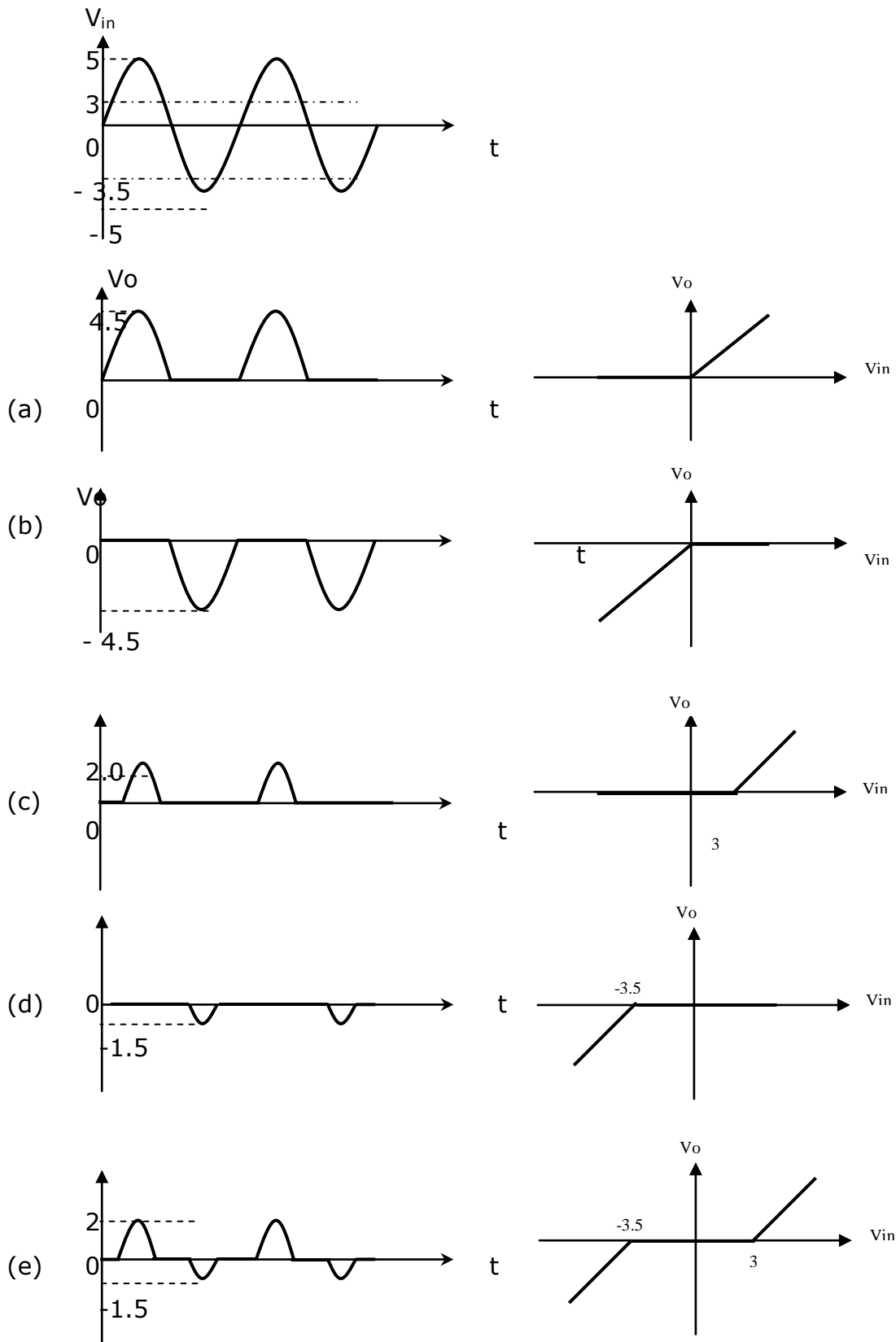


PROCEDURE:

1. Rig up the circuit as shown in the fig.
2. Give a sinusoidal input of 10V peak to peak.
3. Check the output at the output terminal.
4. To plot the transfer characteristics, connect channel 1 of the CRO to the output and channel 2 to the input and press the XY knob
5. Adjust the grounds of both the channels to the centre.
6. Measure the designed values.

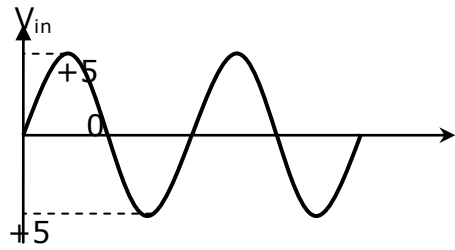
WAVEFORMS:

Series Clipper

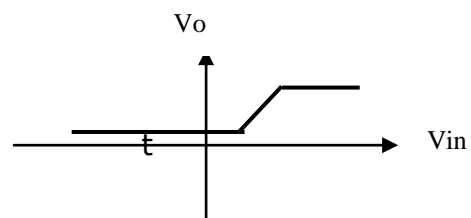
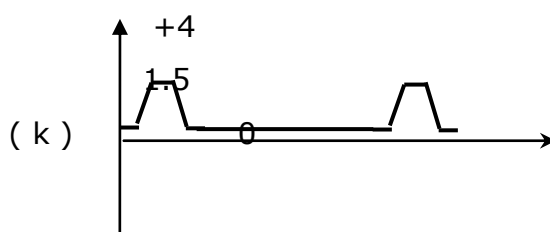
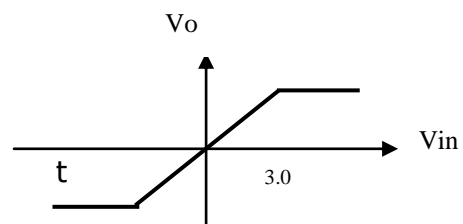
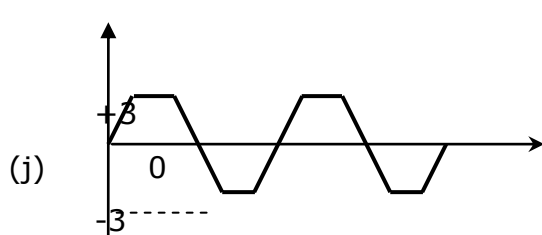
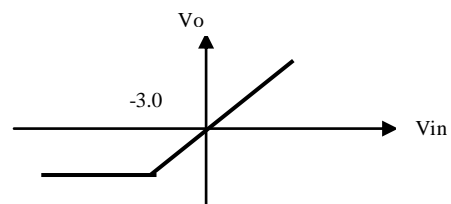
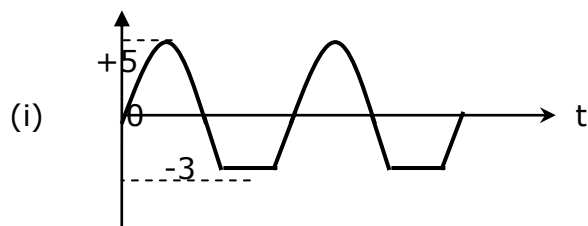
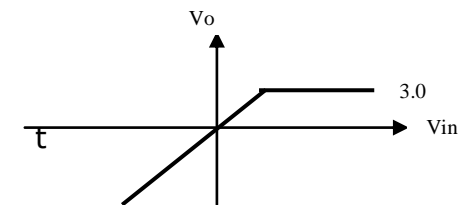
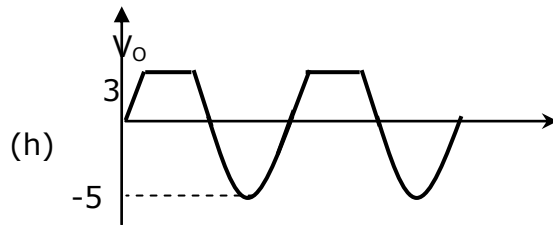
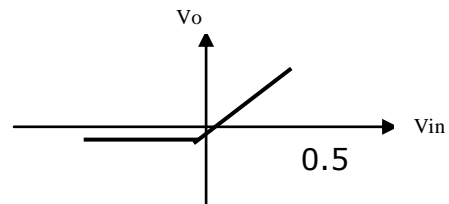
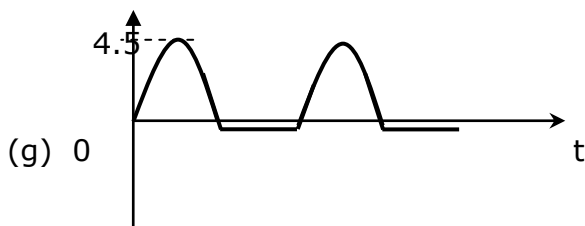
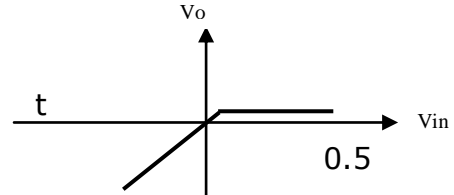
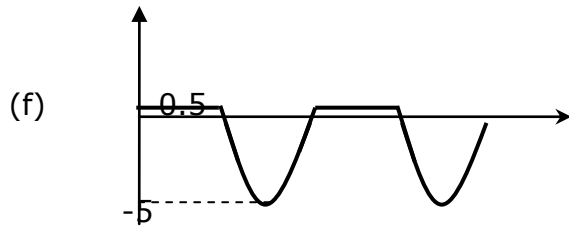


RESULT :

Shunt Clipper



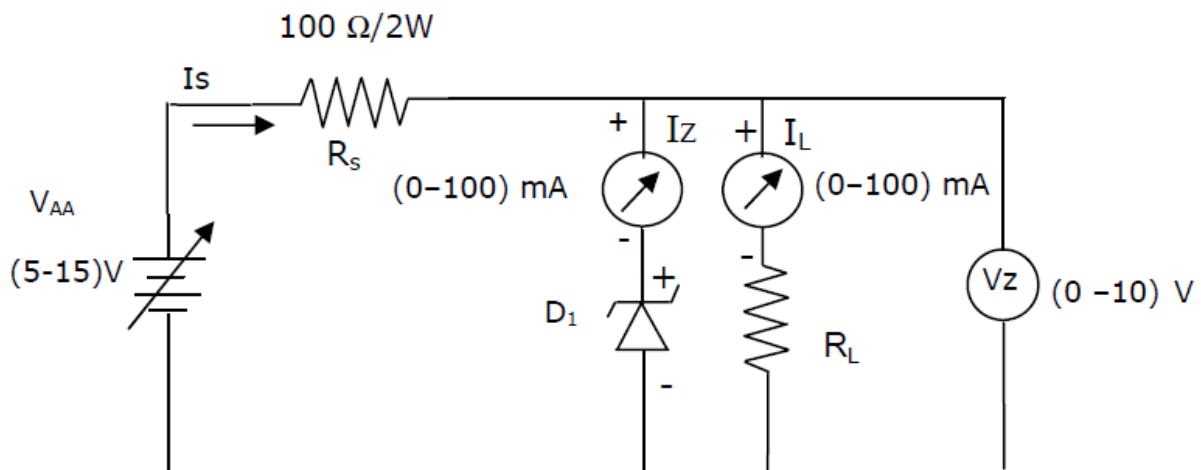
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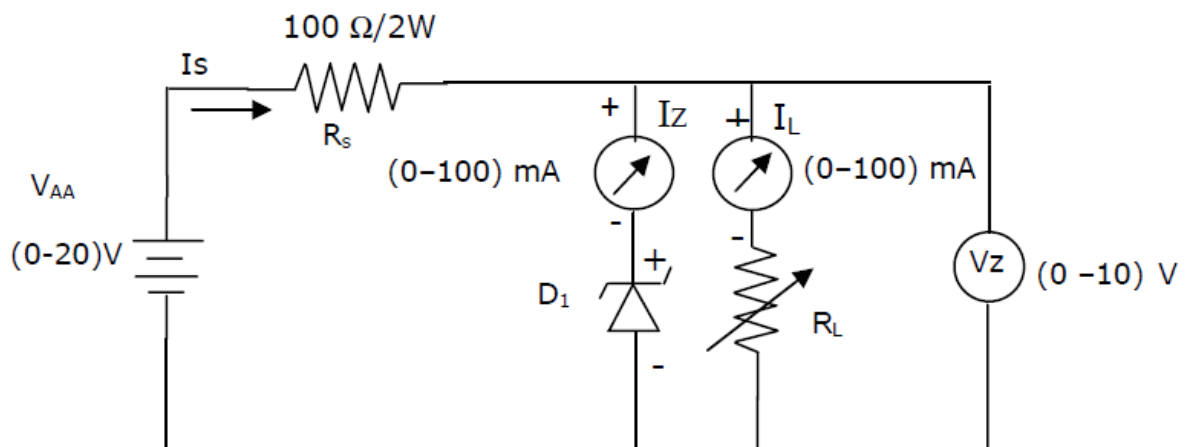
Experiment : 03**DATE :****ZENER DIODE****AIM:**

To study zener diode as voltage regulator, To calculate % line regulation, To calculate % load regulation.

APPARATUS: Zener diode, Resistors, Power supply, Multi meter.

CIRCUIT DIAGRAM:

Line Regulation: Zener Regulator



Load Regulation: Zener Regulator

THEORY:

Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. It is acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode break downs while reverse biased. In the case of normal diodes the diode damages at the break down voltage. But Zener diode is specially designed to operate in the reverse breakdown region.

The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, its depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction. And the electron hole pair generation takes place. Thus heavy current flows. This is known as Zener break down.

So a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage across it remains constant. This principle is used in voltage regulator using Zener diodes. The figure shows the zener voltage regulator, it consists of a current limiting resistor R_S connected in series with the input voltage V_S and zener diode is connected in parallel with the load R_L in reverse biased condition. The output voltage is always selected with a breakdown voltage V_Z of the diode.

The input source current, $I_S = I_Z + I_L$ (1)

The drop across the series resistance, $R_S = V_{in} - V_Z$ (2)

And current flowing through it, $I_S = (V_{in} - V_Z) / R_S$ (3)

From equation (1) and (2), we get, $(V_{in} - V_Z) / R_S = I_Z + I_L$ (4)

Regulation with a varying input voltage (line regulation): It is defined as the change in regulated voltage with respect to variation in line voltage. It is denoted by 'LR'. In this, input voltage varies but load resistance remains constant hence, the load current remains constant. As the input voltage increases, from equation (3) I_S also varies accordingly. Therefore, zener current I_Z will increase. The extra voltage is dropped across the R_S . Since, increased I_Z will still have a constant V_Z and V_Z is equal to V_{out} .

The output voltage will remain constant. If there is decrease in V_{in} , I_Z decreases as load current remains constant and voltage drop across R_S is reduced. But even though I_Z may change, V_Z remains constant hence, output voltage remains constant.

Regulation with the varying load (load regulation): It is defined as change in load voltage with respect to variations in load current. To calculate this regulation, input voltage is constant and output voltage varies due to change in the load resistance value. Consider output voltage is increased due to increasing in the load current. The left side of the equation (4) is constant as input voltage V_{in} , I_S and R_S is constant. Then as load current changes, the zener current I_Z will also change but in opposite way such that the sum of I_Z and I_L will remain constant. Thus, the load current increases, the zener current decreases and sum remain constant. From reverse bias characteristics even I_Z changes, V_Z remains same hence, and output voltage remains fairly constant.

PROCEDURE:-

A) Line Regulation:

1. Make the connections as shown in figure below.
2. Keep load resistance fixed value; vary DC input voltage from 5V to 15V.
3. Note down output voltage as a load voltage with high line voltage 'VHL' and as a load

Voltage with low line voltage 'VLL'.

4. Using formula, % Line Regulation = $(V_{HL} - V_{LL}) / V_{NOM} \times 100$, where V_{NOM} = the nominal load voltage under the typical operating conditions. For ex. $V_{NOM} = 9.5 \pm 4.5$ V

B) Load Regulation:

1. For finding load regulation, make connections as shown in figure below.
2. Keep input voltage constant say 10V, vary load resistance value.
3. Note down no load voltage 'VNL' for maximum load resistance value and full load voltage 'VFL' for minimum load resistance value.
4. Calculate load regulation using, % load regulation = $(VNL - VFL) / VFL \times 100$.

Calculations:

% Line Regulation = $(V_{HL} - V_{LL}) / V_{NOM} \times 100 = \text{-----} \%$

% voltage regulation = $(V_{NL} - V_{FL}) / V_{FL} \times 100 = \text{-----} \%$

RESULT:

Experiment No : 4**DATE :****BJT AMPLIFIER****AIM:**

Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain bandwidth product from its frequency response.

APPARATUS REQUIRED:

Sl.No	APPARATUS	RANGE	QUANTITY
1	AFO	(0-1)MHz	1
2	CRO	(0-20)MHz	1
3	Resistors	1.5K Ω , 6K Ω , 2K Ω , 14k Ω , 2.3K Ω , 10K Ω	Each one
4	Power supply	(0-30V)	1
5	Transistors	BC 107	1
6	Capacitors	28pF, 10pF, 720pF	1

THEORY:

Negative feedback in general increases the bandwidth of the transfer function stabilized by the specific type of feedback used in a circuit. In Voltage shunt feedback amplifier, consider a common emitter stage with a resistance R' connected from collector to base. This is a case of voltage shunt feedback and we expect the bandwidth of the Trans resistance to be improved due to the feedback through R' . The voltage source is represented by its Norton's equivalent current source $I_s = V_s / R_s$.

Design :

Given specifications:

$V_{CC} = 10V$, $I_C = 1.2mA$, $A_V = 30$, $f_i = 1\text{ kHz}$, $S = 2$, $h_{FE} = 150$, $\beta = 0.4$

The feedback factor, $\beta = -1/R_F = +1/0.4 = 2.5K\Omega$

(i) To calculate R_C :

The voltage gain is given by,

$$A_V = -h_{fe} (R_C \parallel R_F) / h_{ie}$$

$$h_{ie} = \beta r_e$$

$$r_e = 26mV / I_E = 26mV / 1.2mA = 21.6$$

$$h_{ie} = 150 \times 21.6 = 3.2K$$

Apply KVL to output loop,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \text{ ----- (1)}$$

Where $V_E = I_E R_E$ ($I_C = I_E$)

$$V_E = V_{CC} / 10 = 1V$$

$$\text{Therefore } R_E = 1 / 1.2 \times 10^{-3} = 0.8K = 1K\Omega$$

$$V_{CE} = V_{CC} / 2 = 5V$$

From equation (1), $R_C = 3K\Omega$

(ii) To calculate R_1 & R_2 :

$$S = 1 + (R_B / R_E)$$

$$R_B = (S - 1) R_E = R_1 \parallel R_2 = 1K\Omega$$

$$R_B = R_1 R_2 / (R_1 + R_2) \text{ ----- (2)}$$

$$V_B = V_{BE} + V_E = 0.7 + 1 = 1.7V$$

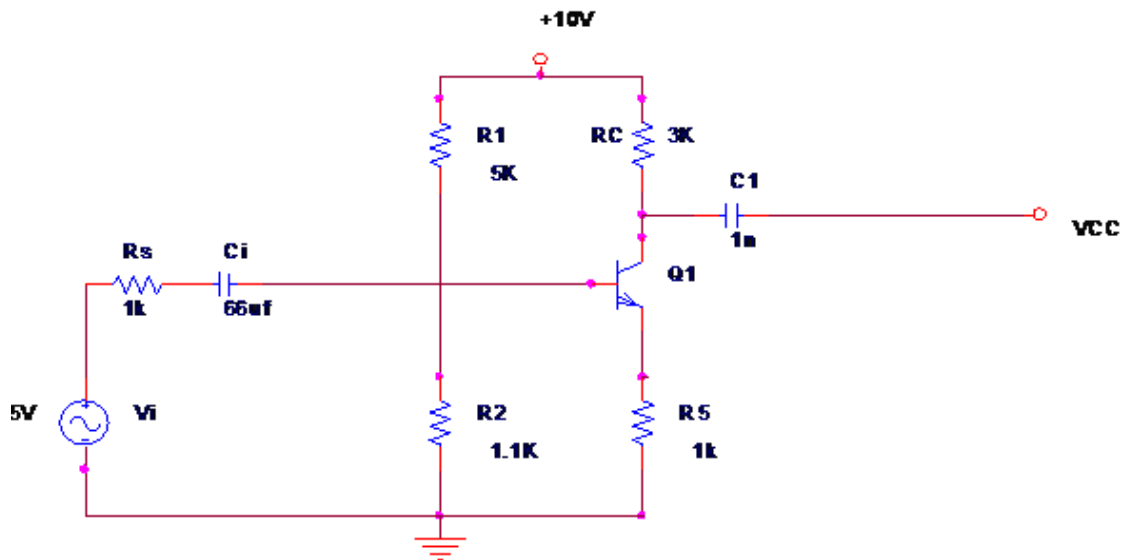
$$V_B = V_{CC} R_2 / (R_1 + R_2) \text{ ----- (3)}$$

Solving equation (2) & (3),

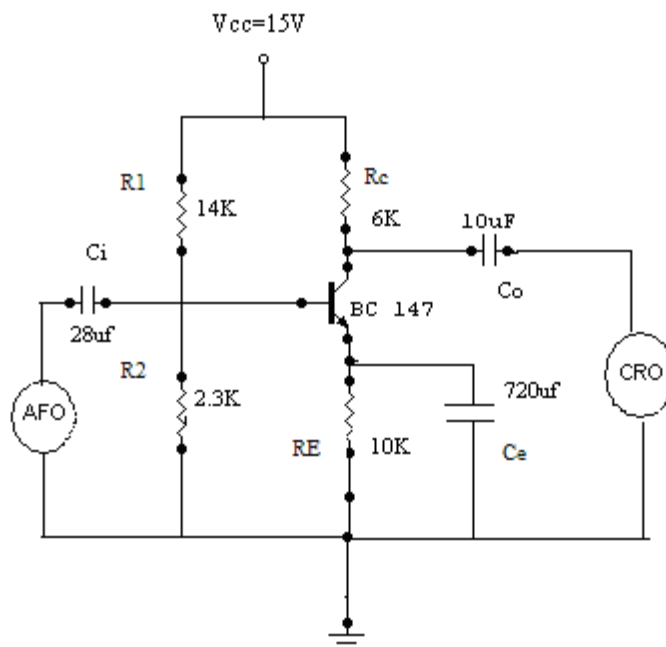
$$R_1 = 5K\Omega \text{ \& } R_2 = 1.1K\Omega$$

CIRCUIT DIAGRAM

WITHOUT FEEDBACK:



WITH FEEDBACK:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set VCC = 10V; set input voltage using audio frequency oscillator.
3. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.
4. Calculate the gain in dB
5. Plot gain Vs frequency curve in semi-log sheet.
6. Connect the circuit as per the circuit diagram.
7. Set VCC = 10V; set input voltage using audio frequency oscillator.
8. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.
9. Calculate the gain in dB
10. Plot gain Vs frequency curve in semi-log sheet.
11. Compare this response with respect to the amplifier without feedback.

TABULATION:**(With or without feedback)**

FREQUENCY	OUTPUT VO(V)	Vin(V)	Gain = $20\log(V_o/V_{in})$ dB

(iii) To calculate Resistance:

Output resistance is given by,

$$R_O = R_C \parallel R_F$$

$$R_O = 1.3K\Omega$$

input impedance is given by,

$$R_i = (R_B \parallel R_F) \parallel h_{ie} = 0.6K\Omega$$

Trans-resistance is given by,

$$R_m = -h_{fe} (R_B \parallel R_F) (R_C \parallel R_F) / (R_B \parallel R_F) + h_{ie}$$

$$R_m = 0.06K\Omega.$$

AC parameter with feedback network:**(i) Input Impedance:**

$$R_{if} = R_i / D \text{ (where } D = 1 + \beta R_m)$$

$$\text{Therefore } D = 25$$

$$R_{if} = 24$$

Input coupling capacitor is given by,

$$X_{ci} = R_{if} / 10 = 2.4 \text{ (since } X_{Ci} \ll R_{if})$$

$$C_i = 1 / 2\pi f X_{Ci} = 66\mu f$$

(ii) Output impedance:

$$R_{of} = R_O / D = 52$$

Output coupling capacitor:

$$X_{CO} = R_{of} / 10 = 5.2$$

$$C_O = 1 / 2\pi f X_{CO} = 30\mu f$$

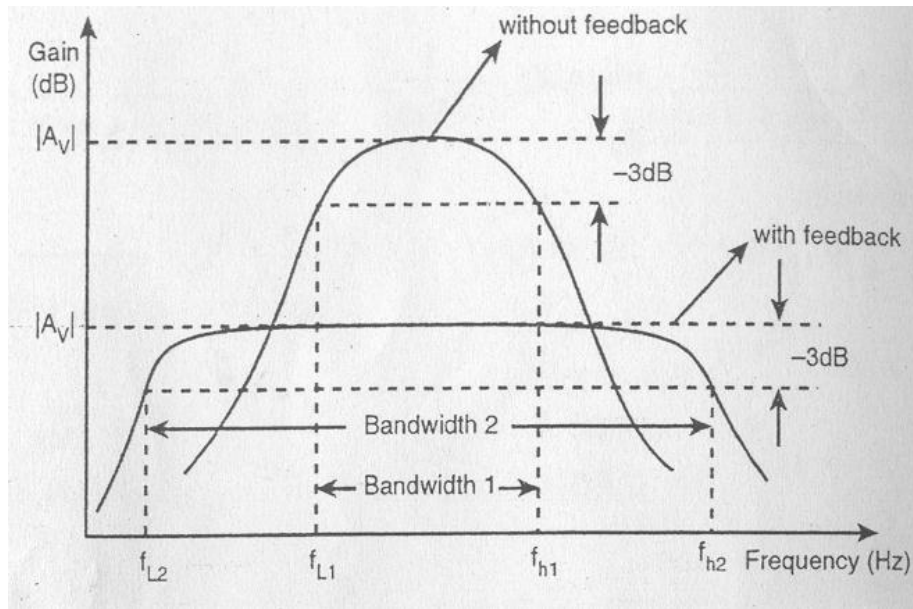
(iii) Emitter capacitor:

$$X_{CE} \ll R'_E = R'/10$$

$$R'_E = R_E \parallel \{ (h_{ie} + R_B) / (1 + h_{fe}) \}$$

$$X_{CE} = 2.7$$

$$\text{Therefore } C_E = 58 \mu\text{f.}$$

Model Graph:**RESULT:**

Experiment No : 5**DATE :****BJT DARLINGTON EMITTER FOLLOWER****AIM:**

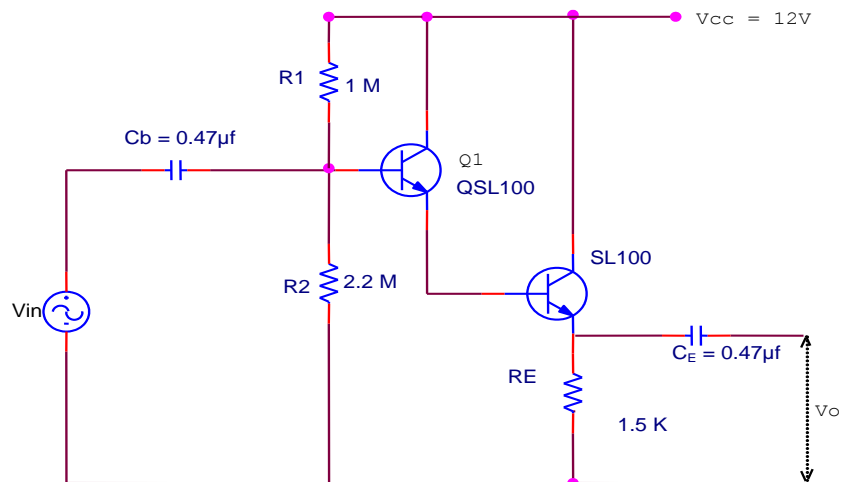
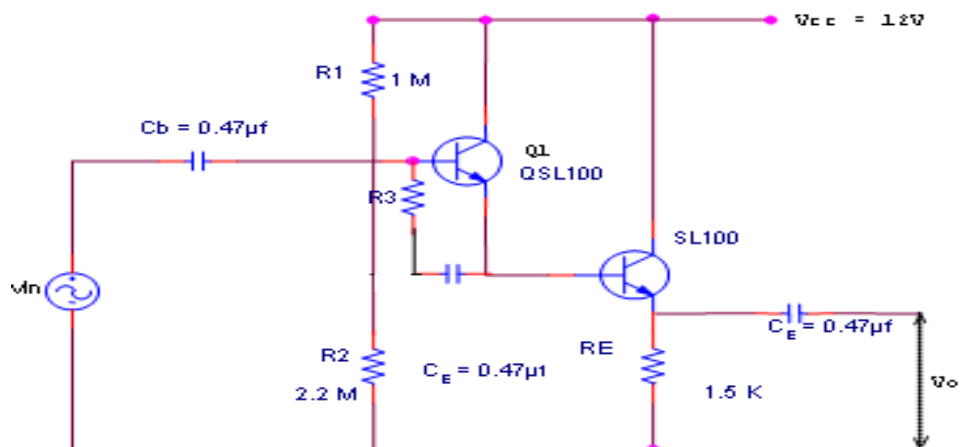
To design and test a Darlington emitter follower circuit with and without boot strapping and determine the gain, input and output impedance.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	2 Nos.
2.	Capacitors	10 μf	1 No
		0.47 μf	2 Nos.
3.	Resistors	1 M Ω , 2.2 M Ω , 1.5 K Ω , 10 K Ω , 47K Ω	Each 1 No
	DC Supply, CRO with Probe, Signal generator, AC millivoltmeter		

THEORY:

Normally transistors are used as amplifiers. But there are some applications in which, matching of impedance is required between two circuits without any gain or attenuation. In such applications emitter followers are used. Emitter followers have large input impedance and small output impedance. Darlington emitter follower has two transistors connected in cascade such that the emitter of first transistor is connected to the base of second transistor. The voltage gain of the darlington emitter follower is close to unity. The major drawback of this circuit is that the second transistor amplifies leakage current of the first transistor and overall leakage current becomes high. The output is observed at the emitter terminal of the second transistor. Hence it is called an emitter follower.

CIRCUIT DIAGRAM:
Darlington emitter follower without bootstrapping

Darlington emitter follower with bootstrapping

DESIGN:

Given $I_C = 4\text{mA}$, $V_{CC} = 12\text{V}$, $V_{BE} = 0.6\text{V}$, $\beta_1 = \beta_2 = 100$

To find R_E :

Applying KVL to the output loop of the second transistor, we get

$$V_{CC} = V_{CE} + V_{RE}$$

$$\text{Therefore } V_{RE} = V_{CC} - V_{CE} = 12 - 6$$

$$\text{Therefore } V_{RE} = 6\text{V}$$

$$\text{W.K.T } R_E = V_{RE} / I_{E2}$$

$$\text{Here } I_{E2} = I_{C2}$$

$$\text{Therefore } R_E = 6 / 4 \times 10^{-3}$$

$$\mathbf{R_E = 1.5k\Omega}$$

To find R_1 & R_2 :

From the circuit we have

$$\begin{aligned}V_A &= V_{BE1} + V_{BE2} + V_{RE} \\&= 0.6 + 0.6 + 6 = 7.2V\end{aligned}$$

W.K.T. $I_C = \beta I_B$

Therefore $I_B = (4 \times 10^{-3}) / 100 = 40 \mu A$

Let $10I_B$ be the current through R_1 and $9I_B$ be the current through R_2 .

From the fig. we see that

$$R_1 = (V_{CC} - V_A) / 10I_B$$

Therefore **$R_1 = 12K\Omega$**

From the fig. $R_2 = V_A / 9I_B$

Therefore **$R_2 = 20 K\Omega \approx 22K\Omega$**

W.K.T. $C_C = 10 / X_{RE} = 10 / (2\pi f R_E)$

Assume $f = 50Hz$

Therefore **$C_C = 21.2\mu F \approx 47 \mu F$**

W.K.T. $C_b = 10 / X_{RB} = 10 / (2\pi f R_B)$ where $R_B = R_1 || R_2 = 7.5k\Omega$

Therefore **$C_b = 4.2\mu F \approx 4.7\mu F$**

Chose **$R_3 = 10 K\Omega$, $C_B = 10\mu F$** for bootstrapping

PROCEDURE:

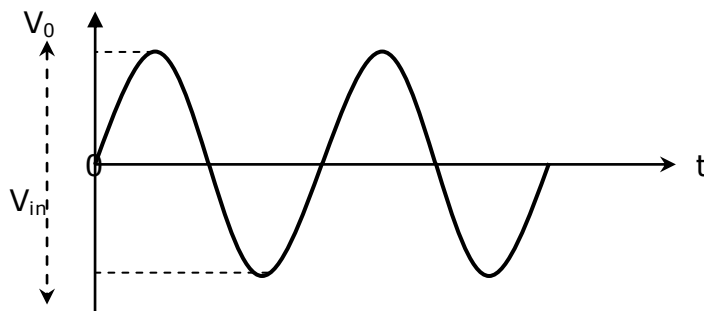
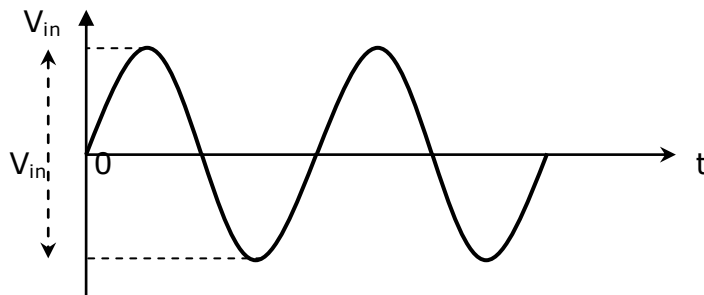
1. Rig up the circuit as shown in the fig.
2. Check the circuit for biasing, i.e. check V_{CE} , V_{CC} and V_{RE} .
3. Give a sinusoidal input signal of 1KHz from a signal generator.
4. Set the input signal to a value such that the output doesn't get clipped.
5. For different frequencies of the input signal, read the output on the voltmeter and verify that the gain is 1.
6. To measure input impedance, connect a resistor of $47k\Omega$ in series with the signal generator.
7. Measure the voltage at the input point (V_S) and at the point after the resistor (V_{IN}).
8. Current through the resistor is given by the expression **$I = (V_S - V_{IN}) / 47K$** .
9. Input impedance is given by **$Z_{IN} = V_{IN} / 47 K$**
10. To measure output impedance, connect a DRB in parallel with the output.
11. Adjust all the knobs of the DRB to maximum.
12. Start reducing the resistance in the DRB from a large value until the output reduces to half.
13. The resistance in the DRB is the output impedance.

TABULAR COLUMN:

$V_{IN} = \underline{\hspace{2cm}}$ constant

Frequency (Hz)	V_o (V)	A_v	A_v (dB)

WAVEFORM:



RESULT :

Experiment No : 6**DATE :****HARTLEY OSCILLATOR / COLPITT'S OSCILLATOR****AIM:**

Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	1 No
2.	Capacitors	0.1 μf , 1000 $p f$	2 No
		47 μf , 0.0023 μf	Each 1 No
3.	Resistors	22K Ω , 4.7K Ω , 1.2K Ω , 330 Ω 1 K Pot	Each 1 No
4.	Inductors	100 μH , 1mH, 5mH	Each 1 No
	DC Supply, CRO with Probe		

THEORY:

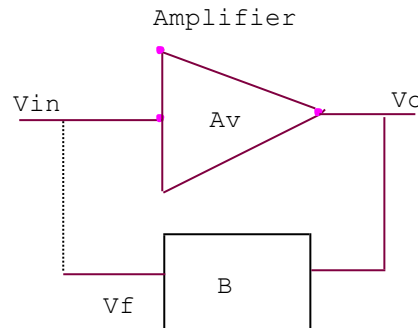
Oscillators are devices, which generate oscillations. The frequency of oscillations depends on the feedback network. Feedback may be of two types namely positive and negative. In positive feedback, the feedback signal is applied in phase with the input signal thus increasing it. In negative feedback, the feedback signal is applied out of phase with the input thus reducing it. The feedback used in oscillators is positive feedback. The oscillators work on the principle of Barkhausen criteria. This states that for sustained oscillations

- i) Loop gain $A_v\beta$ must be equal to 1.
- ii) The phase shift around the loop must be 0 deg or 360 deg.

Here A_v is the gain of the amplifier and β is the attenuation of the feedback network. Consider the feedback network shown in the fig (1) below. Assume an amplifier with input signal V_{in} . The output signal V_o will be 180 deg out of phase with V_{in} . So to get an in phase output, the feedback network provides 180-deg phase shift. Therefore the output V_f from the feedback network can be made in phase and equal in amplitude to V_{in} and V_{in} can be removed. Even then the oscillations continue. Practical oscillations do not need any input signal to start oscillations. They are self-starting due to thermally produced noise in resistors and other components. Only one frequency (f_o) of noise satisfies, Barkhausen

criteria and the circuit oscillates with that frequency. The magnitude of f_o keeps on increasing each time it goes around the loop. The amplification of f_o is limited by circuit's own non-linearities. Therefore to start oscillations $Av\beta > 1$ and to sustain it, the loop gain $Av\beta = 1$.

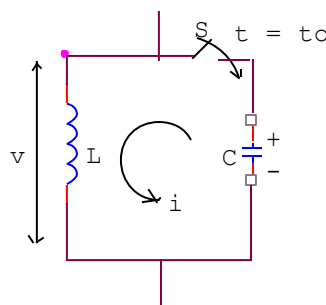
Fig 1.



The feedback network used here consists of L and C. Consider the circuit shown below fig 2. This circuit consists of L and C in parallel. The capacitor stores energy in its electric field whenever there is voltage across it and the inductor stores energy in its magnetic field whenever there is current through it. Initially let us assume that the capacitor has charged to V volts. When S is closed $c = 0$. When S is closed at $t = t_0$, capacitor starts charging through the inductor. Thus a voltage gets built up across the inductor due to the change in current through it. If the capacitor was charged with the polarity as shown in the fig 2 the current starts flowing from the positive plate of the capacitor to the negative plate of the capacitor. As shown the voltage across the capacitor reduces during the discharge time v reduces and I increases. At time t_1 v will be 0 and I will be maximum as c is fully discharged, the capacitor charges like sinusoidal oscillations. Thus the circuit oscillates with the frequency

$$f_o = 1 / 2\pi\sqrt{LC}$$

Fig.2



The Hartley oscillator consists of two inductors and a capacitor and Colpitts oscillator consists of two capacitors and an inductor.

The resonant frequency f_o for Hartley oscillator is

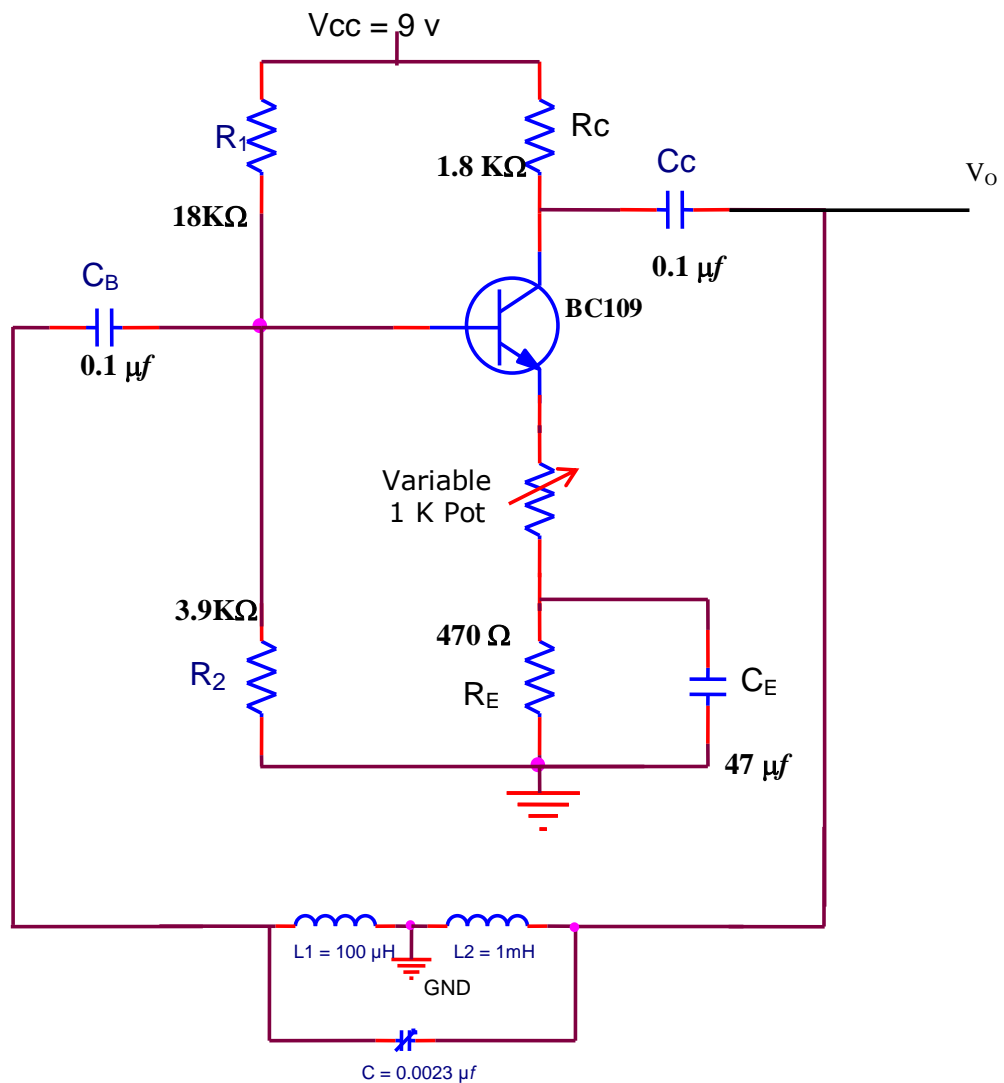
$$f_o = 1 / 2\pi \sqrt{L_{eq}C} \text{ -----where } L_{eq} = L_1 + L_2.$$

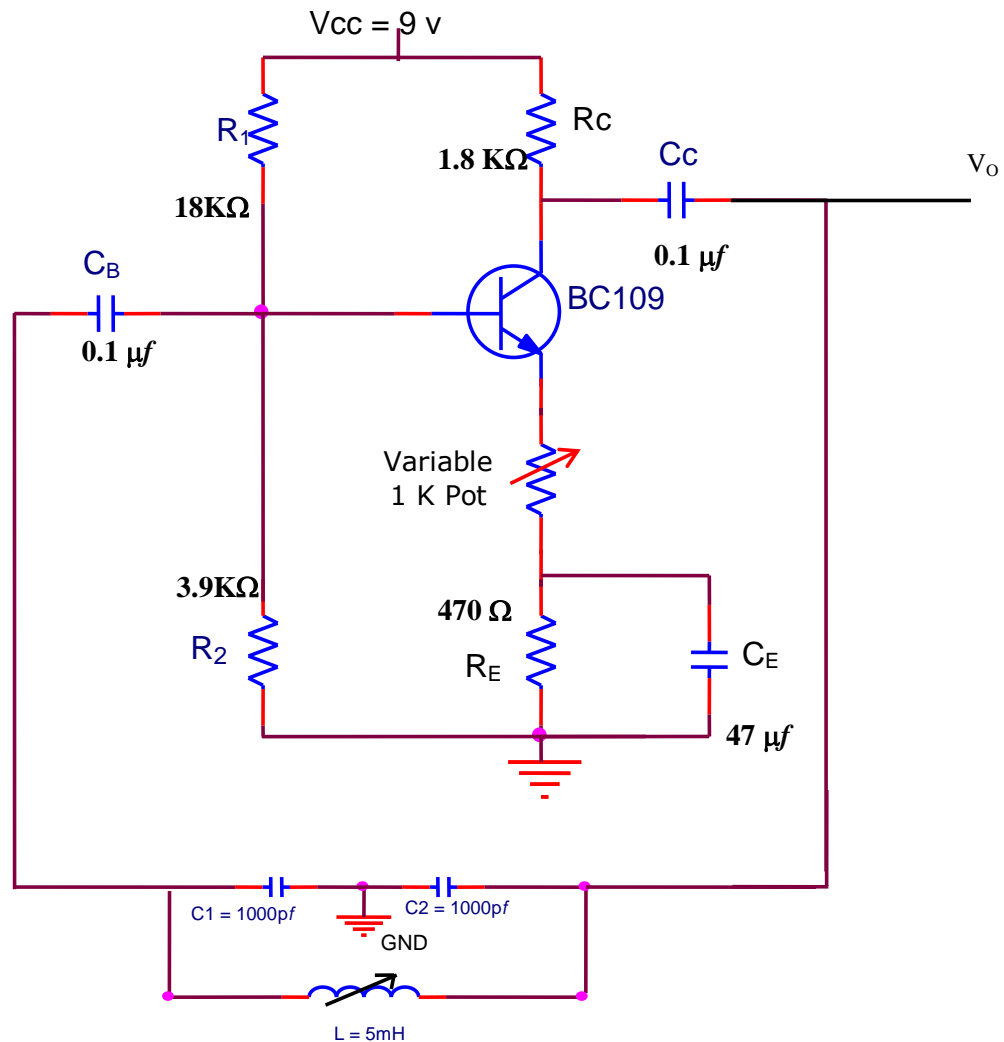
The resonant frequency f_o for Colpitts oscillator is

$$f_o = 1 / 2\pi \sqrt{LC_{eq}} \text{ -----where } C_{eq} = C_1C_2/(C_1 + C_2)$$

CIRCUIT DIAGRAM:

HARTLEY OSCILLATOR:



COLPITTS OSCILLATOR:

DESIGN:

Given $V_{CC} = 9V$, $I_C = 2mA$, $\beta = 50$

R_E : W.K.T. $V_{RE} = V_{CC} / 10 = 9 / 10 = 0.9V$ -----for biasing

$$I_E \approx I_C = 2 \text{ mA}$$

From the fig. We see that,

$$I_E R_E = V_{RE}$$

$$R_E = 0.9 / (2 \times 10^{-3}) = 450\Omega$$

Therefore **$R_E \approx 470\Omega$**

R_C : $V_{CE} = V_{CC} / 2 = 4.5V$ ----- for Q point to be in active region.

Applying KVL to output loop

$$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$$

$$9 - 2 \times 10^{-3} R_C - 4.5 - 0.9 = 0$$

Therefore **$R_C = 1.8k\Omega$**

R_1 & R_2 : From biasing circuit

$$\begin{aligned} V_B &= V_{BE} + V_{RE} \\ &= 0.7 + 0.9 \\ V_B &= 1.6V \end{aligned}$$

Assume $10 I_B$ flows through R_1 and $9 I_B$ flows through R_2 .

$$\text{W.K.T. } I_C = \beta I_B$$

$$2 \times 10^{-3} = 50 I_B$$

$$\text{Therefore } I_B = 40 \mu A$$

From the fig. we see that,

$$R_1 = V_{CC} - V_B / 10 I_B = 9 - 1.6 / (10 \times 40 \times 10^{-6}) = 18.5k\Omega$$

$$\text{Therefore } \mathbf{R_1 \approx 18k\Omega}$$

$$\mathbf{R_2 = V_B / 9I_B = 1.6 / (9 \times 40 \times 10^{-6}) = 4.44k\Omega}$$

$$\text{Therefore } \mathbf{R_2 \approx 3.9k\Omega}$$

C_E, C_C, C_B : Let $C_B = C_C = 0.1\mu F$

$$X_{CE} = R_E / 10$$

$$\text{Therefore } f = 10 / (2\pi C_E R_E)$$

Let $f = 100\text{Hz}$ and W.K.T $R_E = 470\Omega$

$$\text{Therefore } C_E = 10 / 2\pi f.R_E = 34\mu F$$

$$\text{Therefore } \mathbf{C_E \approx 47\mu F.}$$

HARTLEY OSCILLATOR:

$$\text{Attenuation } \beta = V_f / V_o = I_{X_{L1}} / I_{X_{L2}} = X_{L1} / X_{L2} = 2\pi f o L1 / 2\pi f o L2 = L1 / L2$$

$$\text{For sustained oscillations } A_v \beta = 1 \text{ ----- } A_v = 1 / \beta = L2 / L1$$

$$\text{For oscillations to start } A_v \beta > 1 \text{ ----- } A_v > L2 / L1$$

COLPITTS OSCILLATOR:

$$\text{Attenuation } \beta = V_f / V_o = I_{X_{C1}} / I_{X_{C2}} = X_{C1} / X_{C2} = (1 / 2\pi f o C1) / (1 / 2\pi f o C2) = C1 / C2$$

$$\text{For sustained oscillations } A_v \beta = 1 \text{ ----- } A_v = C1 / C2$$

$$\text{For oscillations to start } A_v \beta > 1 \text{ ----- } A_v > C1 / C2$$

DESIGN OF TANK CIRCUIT

Assume $f_o = 100 \text{ KHz}$

HARTLEY OSCILLATOR

$$f_o = 1 / (2\pi \sqrt{L_{eq} C}) \text{ -----where } L_{eq} = L_1 + L_2.$$

Assume $L_1 = 100 \mu\text{H}$, $L_2 = 1\text{mH}$

$$\therefore L_{eq} =$$

$$\therefore f_o = 1 / (2\pi \sqrt{2 \times 10^{-3} C})$$

$$\therefore C = 0.0023 \mu\text{f} \text{ (Decade capacitance box)}$$

COLPITTS OSCILLATOR

$$f_o = 1 / (2\pi \sqrt{L C_{eq}}) \text{ -----where } C_{eq} = (C_1 C_2) / (C_1 + C_2)$$

Assume $C_1 = C_2 = 1000 \text{ pF}$

$$\therefore C_{eq} =$$

$$\therefore f_o = 1 / 2\pi \sqrt{L \times .05 \times 10^{-6}}$$

$$\therefore L = 5 \text{ mH (Use decade inductance box)}$$

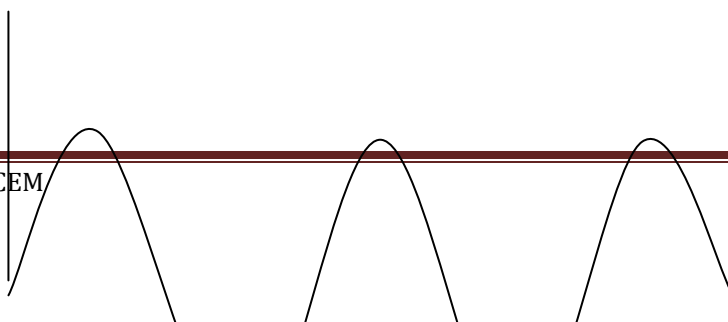
PROCEDURE:

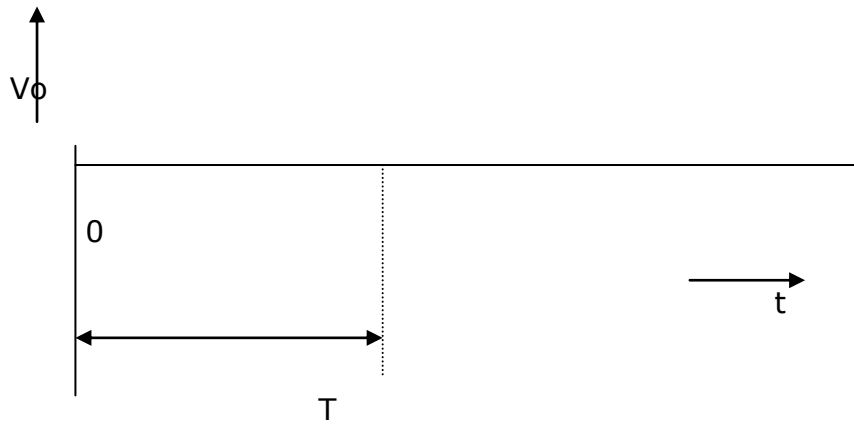
1. Rig up the circuit as shown in the circuit diagram.
2. Before connecting the feedback network, check the circuit for biasing conditions i.e. check V_{CE} , and V_{RE} .
3. After connecting the feedback network. Check the output.
4. Check for the sinusoidal waveform at output. Note down the frequency of the output waveform and check for any deviation from the designed value of the frequency.
5. To get a sinusoidal waveform adjust $1\text{K}\Omega$ potentiometer.
6. DCB/DIB can be varied to vary the frequency of the output waveform.

TABULAR COLUMN

HARTLEY OSCILLATOR		
SL NO	C	f _o

COLPITTS OSCILLATOR		
SL NO	L	f _o

WAVEFORM:



$$\therefore \text{frequency } f_o = 1/T$$

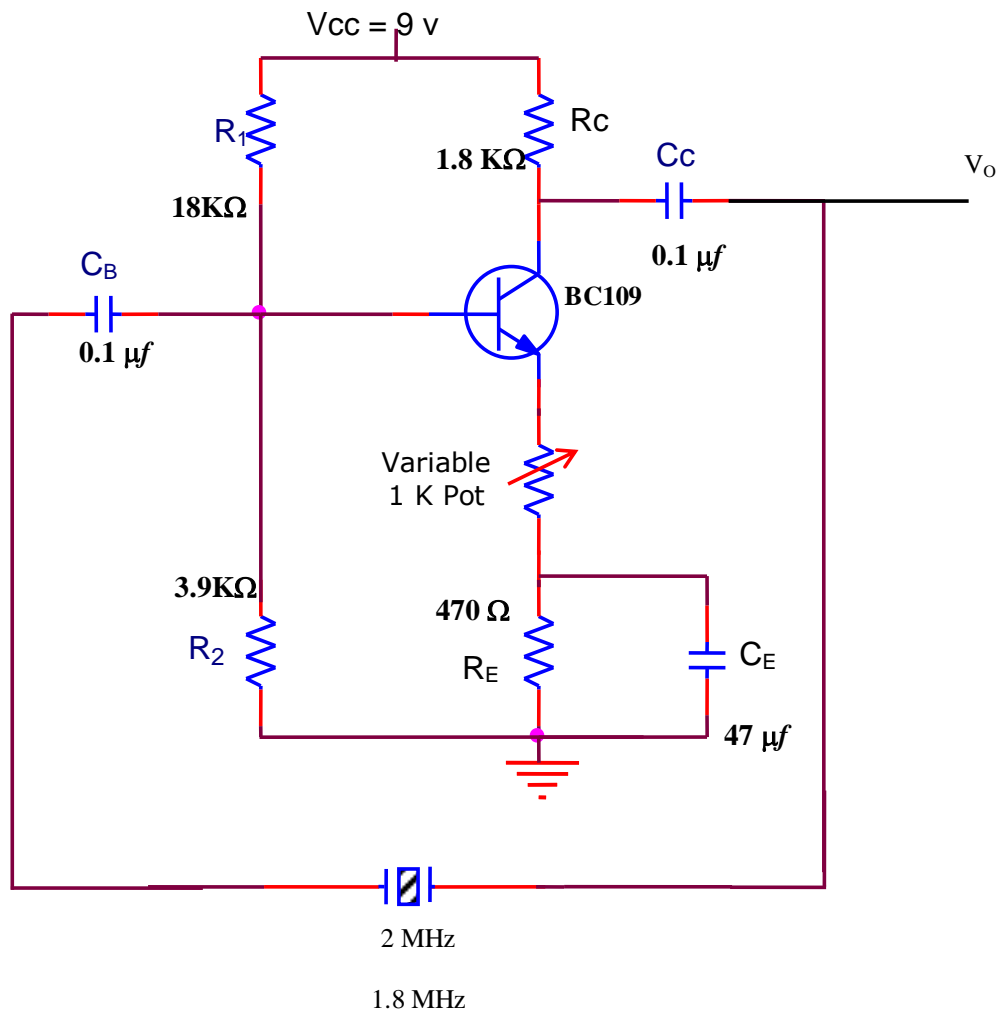
RESULT:

Experiment No : 7**DATE :****CRYSTAL OSCILLATOR****AIM:**

To design a crystal oscillator to oscillate at the specified crystal frequency.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	1 No
2.	Capacitors	$0.1\ \mu f$	2 No
		$47\ \mu f$	1 No
3.	Resistors	$22K\Omega$, $4.7K\Omega$, $1.2K\Omega$, 330Ω 1 K Pot	Each 1 No
4.	Crystal	2 MHz or 1.8 MHz	1 No
	DC Supply, CRO with Probe		

CIRCUIT DIAGRAM:

DESIGN:

Given $V_{CC} = 9V$, $I_C = 2mA$, $\beta = 50$

R_E : W.K.T. $V_{RE} = V_{CC} / 10 = 9 / 10 = 0.9V$ -----for biasing

$$I_E \approx I_C = 2 \text{ mA}$$

From the fig. We see that,

$$I_E R_E = V_{RE}$$

$$R_E = 0.9 / (2 \times 10^{-3}) = 450\Omega$$

Therefore **$R_E \approx 470\Omega$**

R_C : $V_{CE} = V_{CC} / 2 = 4.5V$ ----- for Q point to be in active region.

Applying KVL to output loop

$$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$$

$$9 - 2 \times 10^{-3} R_C - 4.5 - 0.9 = 0$$

Therefore **$R_C = 1.8k\Omega$**

R_1 & R_2 : From biasing circuit

$$V_B = V_{BE} + V_{RE}$$

$$= 0.7 + 0.9$$

$$V_B = 1.6V$$

Assume $10 I_B$ flows through R_1 and $9 I_B$ flows through R_2 .

$$\text{W.K.T. } I_C = \beta I_B$$

$$2 \times 10^{-3} = 50 I_B$$

$$\text{Therefore } I_B = 40 \mu A$$

From the fig. we see that,

$$R_1 = V_{CC} - V_B / 10 I_B = 9 - 1.6 / (10 \times 40 \times 10^{-6}) = 18.5k\Omega$$

Therefore **$R_1 \approx 18k\Omega$**

$$\mathbf{R_2 = V_B / 9I_B = 1.6 / (9 \times 40 \times 10^{-6}) = 4.44k\Omega}$$

Therefore **$R_2 \approx 3.9k\Omega$**

C_E , C_C , C_B : Let $C_B = C_C = 0.1\mu F$

$$X_{CE} = R_E / 10$$

$$\text{Therefore } f = 10 / (2\pi C_E R_E)$$

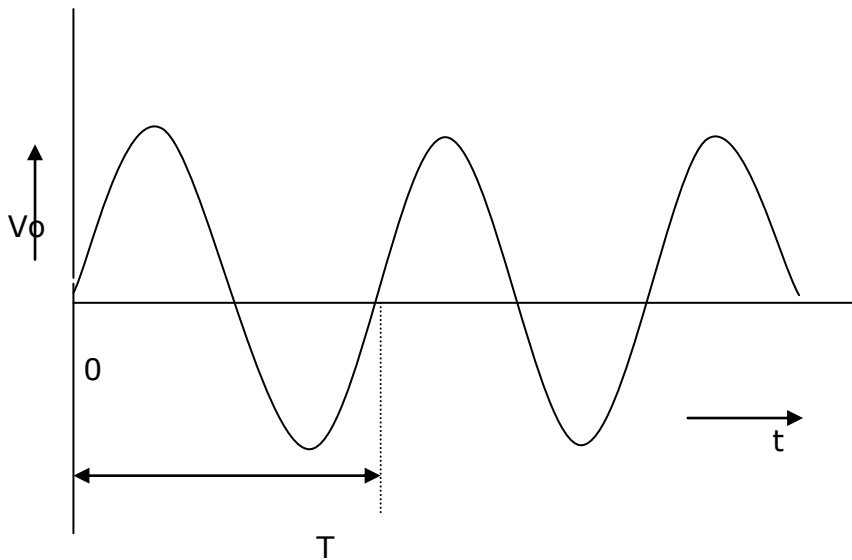
Let $f = 100Hz$ and W.K.T $R_E = 470\Omega$

$$\text{Therefore } C_E = 10 / 2\pi f.R_E = 34\mu F$$

Therefore **$C_E \approx 47\mu F$.**

PROCEDURE:

1. Rig up the circuit as shown in the circuit diagram.
2. Before connecting the feedback network, check the circuit for biasing conditions i.e. check V_{CE} , and V_{RE} .
3. After connecting the feedback network. Check the output.
4. Check for the sinusoidal waveform at output. Note down the frequency of the output waveform and check for any deviation from the designed value of the frequency.
5. To get a sinusoidal waveform adjust $1K\Omega$ potentiometer.

WAVEFORM:

$$\therefore \text{frequency } f_o = 1/T$$

RESULT:

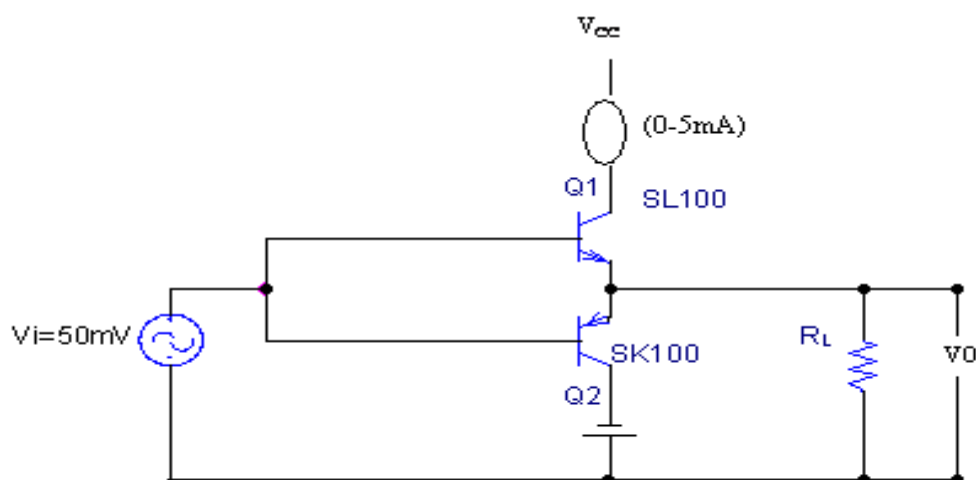
Experiment No : 8**DATE :****COMPLEMENTARY SYMMETRY CLASS-B PUSH PULL POWER AMPLIFIER****Aim:**

Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	1 No.
		SK100	1 No.
2.	Diode	BY127	2 Nos.
3.	Capacitors	47 μf	2 Nos.
		470 μf	1 No.
4.	Resistors	220 Ω	2 No
		DRB	1 No
	DC Supply, CRO with Probe, Signal generator, AC millivoltmeter		

Theory: In class B operation, to obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half cycle, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half cycle and the other part pulls the signal low during the other half cycle, the circuit is referred to as a push pull circuit.

Circuit diagram:

DESIGN:

Given $V_{CC} = 2.5V$; $R_L = 10\ \Omega$; $I_{DC} = 3mA$

To Find R_1 & R_2 :

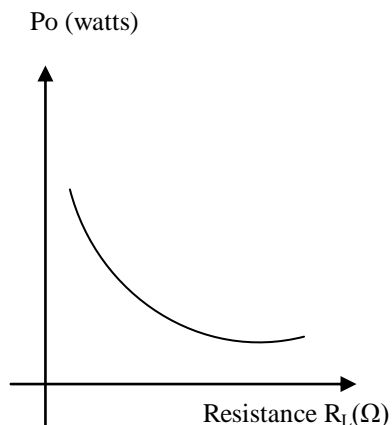
Applying KVL at the input circuit;

We get ; $V_{CC} = 2V_{R1} + 1.4$

Therefore; $V_{R1} = 0.55V$;

$V_{R1} = I_{DC}R_1 = 0.55V$; **$R_1 = 183\Omega$** .

Choose; $R_1 = R_2 = 220\Omega$.

**To Find C_i :**

Input coupling capacitor is given by, $X_{Ci} > Z_{ieff}/10 > 1.1K/10$

$X_{Ci} > 1/2\pi f C_i$; $C_i > 28\mu F$; Choose **$C_i = 47\mu F$**

To Find C_o :

Output coupling capacitor is given by, $X_{Co} = 10$

$X_{Co} > 1/2\pi f C_o$

$C_o > 318\mu F$; Choose; $C_o = 470\mu F$

$P_{oac} = V_o^2/8R_L$ $P_{idc} = V_{CC}I_{dc}$

Calculate circuit efficiency, $\eta = P_o(ac)/P_i(dc) = (\pi/4)V_o/V_{CC} = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set $V_i = 3V$, using the signal generator.
3. Keeping the input voltage constant, vary the load resistor and note down the readings of the ammeter and peak to peak output voltage.
4. Calculate P_{DC} , P_{AC} and % efficiency η .
5. Draw the plot of resistance versus output power.

Tabulation

$V_i = \text{-----}$

$R_L (\Omega)$	$V_o (v)$	$I_{DC}(mA)$	P_{AC}	P_{DC}	% η

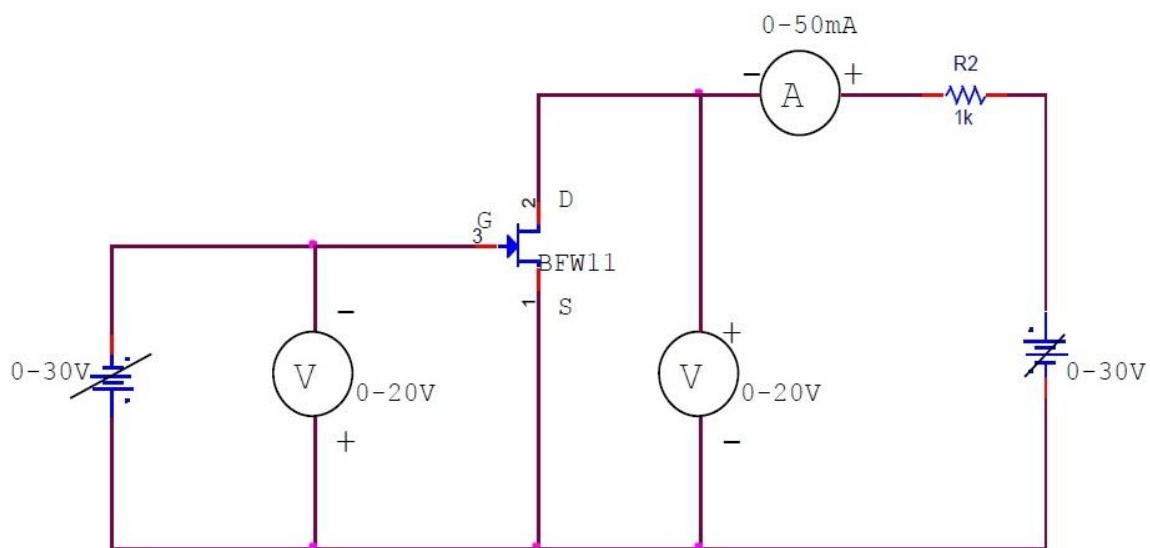
RESULT:

Experiment No : 9**DATE :****JFET CHARACTERISTICS**

AIM : Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.

EQUIPMENT REQUIRED :

- 1 Regulated Power Supply 0-30V
- 2 Voltmeter 0-20V
- 3 Ammeter 0-50mA
- 4 Bread Board
- 5 JFET.

CIRCUIT DIAGRAM:**SPECIFICATIONS:**

For **JFET BFW11**: -

Gate Source Voltage $V_{GS} = -30V$

Forward Gain Current $I_{GF} = 10\text{ mA}$

Maximum Power Dissipation $P_D = 300\text{ mW}$.

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the gate to source junction of the FET always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with v_{ds} . with increase in I_d the ohmic voltage drop between the and the channel region reverse biases the junction and the conducting position of the channel begins to remain

constant. The V_{ds} at this instant is called "pinch of voltage". If the gate to source voltage (V_{gs}) is applied in the direction to provide additional reverse bias, the pinch off voltage is decreased.

In amplifier applications, the FET is always used in the region beyond the pinch off.

$$I_{ds} = I_{dss} (1 - V_{gs} / V_p)^2.$$

PROCEDURE:

DRAIN CHARACTERISTICS

1. Make the connections as per circuit diagram.
2. Keep $V_{GS} = 0V$ by varying V_{GG} .
3. Varying V_{DD} gradually, note down both drain current I_D and drain to source voltage (V_{DS}).
4. Step Size is not fixed because of non linear curve and vary the X-axis variable (i.e. if
5. Output variation is more, decrease input step size and vice versa).
6. Repeat above procedure (step 3) for $V_{GS} = -1V$.

TRANSFER CHARACTERISTICS:

1. Keep $V_{DS} = 2V$ by varying V_{DD} .
2. Varying V_{GG} gradually from 0 – 5V, note down both drain current (I_D) and gate to source
3. Voltage (V_{GS}).
4. Step Size is not fixed because of non linear curve and vary the X-axis variable (i.e. if
5. Output variation is more, decrease input step size and vice versa).
6. Repeat above procedure (step 2) for $V_{DS} = 4V$.

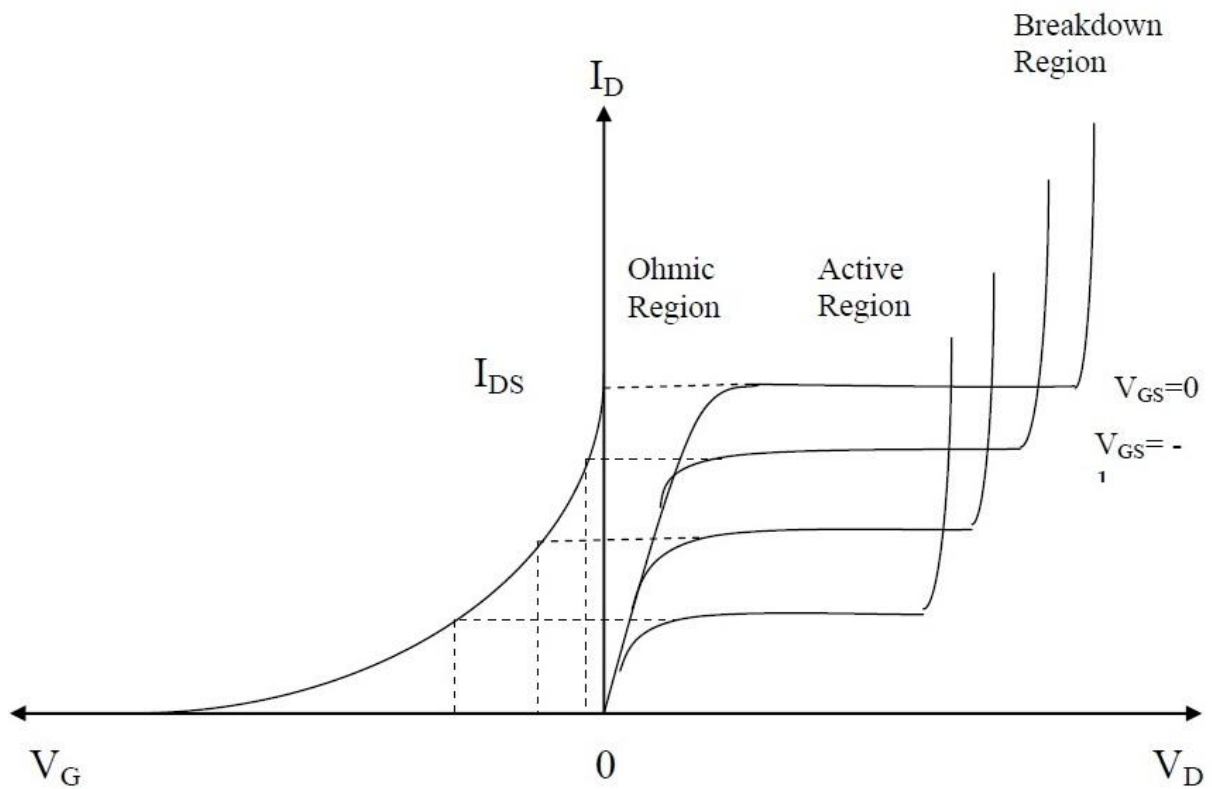
OBSERVATIONS:

DRAIN CHARACTERISTICS:

$V_{GS}(V)=0$		$V_{GS}(V)= -1$	
$V_{DS}(V)$	I_D (mA)	$V_{DS}(V)$	$I_D(mA)$

TRANSFER CHARACTERISTICS:

$V_{DS}(V) = 1$		$V_{DS}(V) = 3$	
$V_{GS}(V)$	$I_D (mA)$	$V_{GS}(V)$	$I_D(mA)$

MODEL GRAPH:**Transfer Characteristics****Drain Characteristics**

CALCULATIONS:

1. **Drain resistance r_d** $= \Delta V_{DS} / \Delta I_D =$
2. **Trans conductance g_m** $= \Delta I_D / \Delta V_{GS} =$
3. **Amplification factor μ** $= r_d \times g_m =$

RESULT:

1. Drain Resistance (r_d) =
2. Trans conductance (g_m) =
3. Amplification factor (μ) =

Experiment No : 10**DATE :****JFET COMMON SOURCE CHARACTERISTICS****AIM:**

Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

EQUIPMENT REQUIRED:

- 1 Regulated Power Supply 0-30V
- 2 Voltmeter 0-20V
- 3 Ammeter 0-50mA
- 4 Bread Board
- 5 JFET.

THEORY:

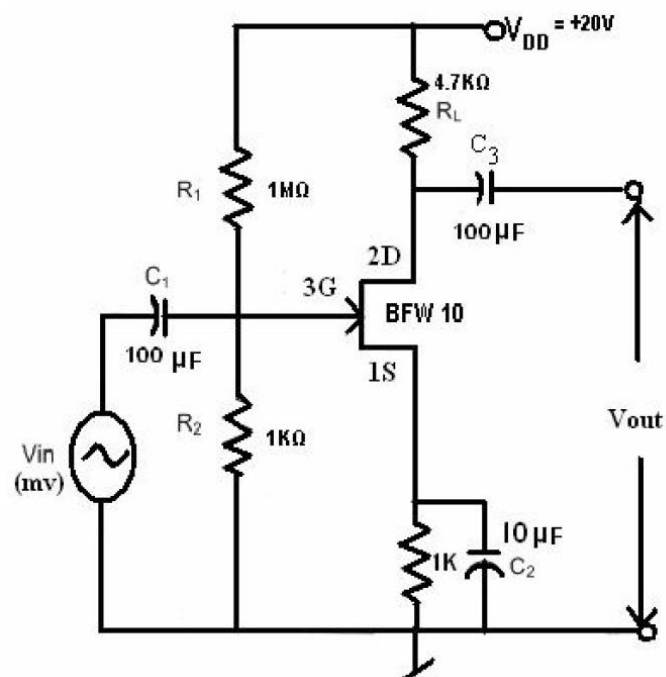
The Common Source Amplifier is one of the three basic FET transistor amplifier configurations. In comparison to the BJT common-emitter amplifier, the FET amplifier has much higher input impedance, but a lower voltage gain. The Junction Field Effect Transistor (JFET) offers very high input impedance along with very low noise figures. It is very suitable for extremely low-level audio applications as in audio preamplifiers. The JFET is more expensive than conventional bipolar transistors but offers superior overall performance. Unlike bipolar transistors, current can flow through the drain and source in any direction equally. Often the drain and source can be reversed in a circuit with almost no effect on circuit operation.

The bias levels in amplifiers based on BJTs are often stabilized using the emitter degeneration technique; that is, a resistor is placed between the transistor's emitter and ground. The resistor creates negative feedback, which forces the quiescent collector current to remain at its design value regardless of changes in the transistor's parameters (such as βF). A similar technique can be used to stabilize the biasing of FET amplifiers.

A common-source JFET amplifier in which a resistor R_S has been added between the source and ground. In this circuit the gate has been connected to ground through the resistor R_G ; thus, the gate is held at ground potential (0 V). If the drain current I_D begins to rise above its intended quiescent value, the voltage drop across R_S will increase. Since the gate-source voltage V_{GS} is the difference between the gate potential (fixed at 0 V) and the voltage across R_S , a rise in the voltage across R_S will cause V_{GS} to drop, lowering I_D back to its original value. The opposite chain of events occurs if I_D begins to drop below its design value. It is a common practice in the design of circuits based on JFETs to tie the gate to ground potential via a large-valued resistor (typically around $1M\Omega$)

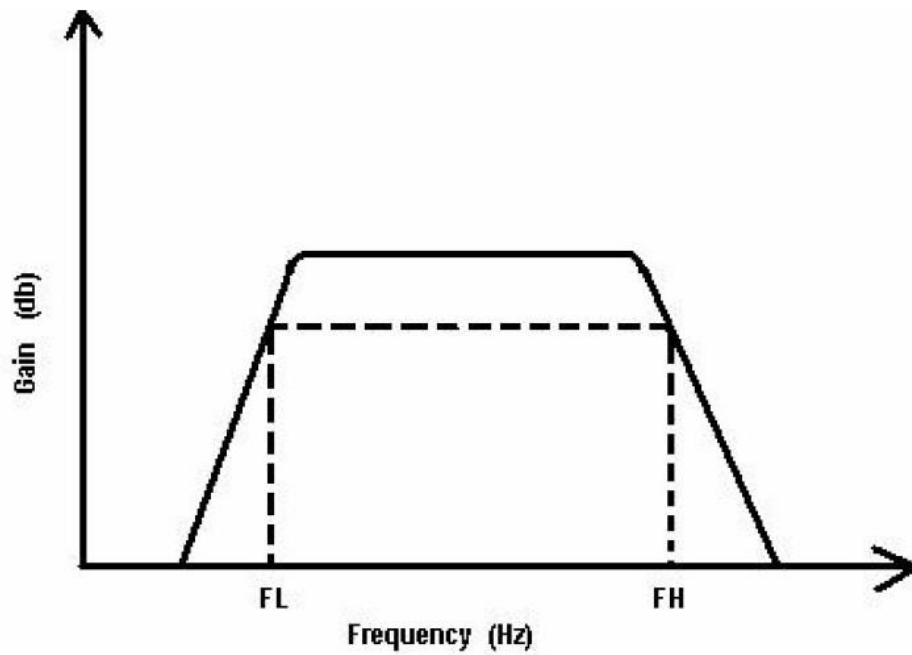
PROCEDURE:

1. Make the connections as per circuit diagram.
2. Keep $V_{GS} = 0V$ by varying V_{GG} .
3. Varying V_{DD} gradually, note down both drain current I_D and drain to source voltage (V_{DS}).
4. Step Size is not fixed because of non linear curve and vary the X-axis variable (i.e. if
5. Output variation is more, decrease input step size and vice versa).
6. Repeat above procedure (step 3) for $V_{GS} = -1V$.

CIRCUIT DIAGRAM:**TABULAR COLUMN:**

SI No	Input Voltage (V_i)	Input Frequency (f_i)	Output Voltage (V_o)	Gain (db)

GAIN VS FREQUENCY CURVE:



RESULT:

$F_H =$

$F_L =$

Gain (db) =

VIVA – QUESTIONS

1. What are Semiconductors? Give examples?
2. What are the types of Semiconductor?

3. What is Intrinsic Semiconductor?
4. What is Extrinsic Semiconductor?
5. What are the types of Extrinsic Semiconductor?
6. What is P-type Semiconductor?
7. What are break down diodes or zener diodes
8. What is break down? What are its types?
9. What is zener breakdown? What is avalanche break down?
10. What are the PIVs of three different filters
11. What are the advantages of bridge rectifier over center-taped full wave rectifier?
12. Define transformer utilization factor? What is the TUF for HWR and full wave center taped and bridge rectifier?
13. Why the CE configuration is commonly used for the amplifier circuits?
14. Why the I_b vs V_{be} plots move outwards for higher values of V_{ce} in C_e input characteristics?
15. What are the different types of clipping circuits?
16. Explain the different types of clipping circuits.

APPENDIX

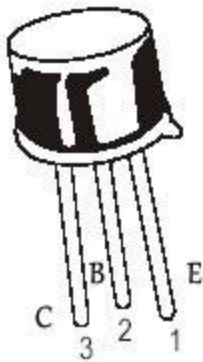
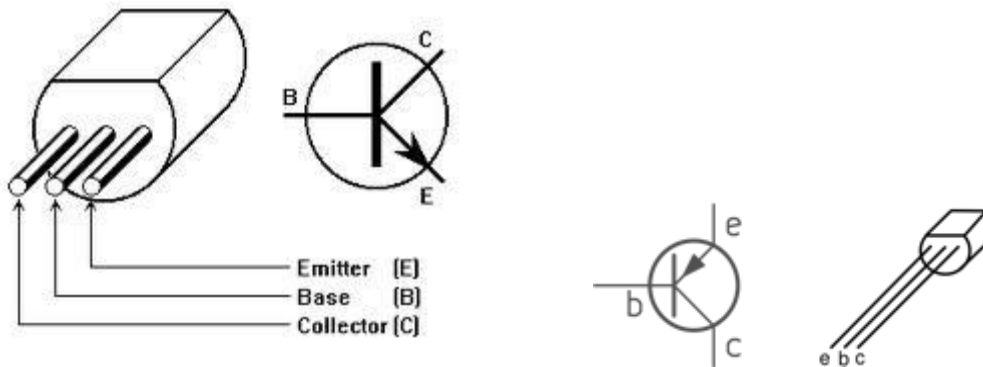
Pin Identification of Transistors

1. Bipolar Junction Transistor (BJT) Transistors

Transistors may be NPN or PNP which are available in Plastic casing or Metal Can package. In plastic casing,



one side of the transistor is Flat which is the front side and the pins are arranged serially. To identify the pins, keep the front flat side facing you and count the pins as one, two etc. In most NPN transistors it will be 1 (Collector), 2 (Base) and 3 (Emitter). Thus CBE. But in PNP transistors, the condition will be just reversed. That is EBC.



In Metal can types, the pins are arranged circularly. Just see a Tab in the rim. In NPN type, the pin close to the Tab is Emitter, the opposite one, the Collector and the middle one, base. In PNP type the pins are reversed. Pin close to the Tab is Collector.

But this is not a standard pin configuration. The pin arrangement may vary in some transistors. So to get an idea, the following table will help you

Transistor	Type	Pins 1 2 3	Transistor	Type	Pins 1 2 3
BC546,547,548,549 550, BC 337, AC 187	NPN	CBE	2N 2222A, 2N 3904	PNP	EBC
TIP 120,121,122	NPN	BCE	TIP 125,126,127	PNP	EBC
BD139	NPN	ECB	BD140	PNP	ECB
BF494,495	NPN	CEB	MPSA 92,42,44	PNP	EBC
C2570	NPN	BEC	BC636	PNP	BCE
C1730	NPN	ECB	SK/CK/BEL100P	PNP	EBC
BD677	NPN	BCE	AC188	PNP	EBC
D882 / 2SD882	NPN	ECB	BC557	PNP	EBC
D313/MJE 13005	NPN	BCE	BC558	PNP	EBC

2. Field Effect Transistor (FET)

To identify a Field Effect Transistor, one should keep the curved portion facing him/her and start counting in anti clockwise direction. The 1st one is the source, then the gate and then the drain.

3. MOSFET – Metal Oxide Semiconductor Field Effect Transistor

Usually in some cases the pins of MOSFET are accordingly labeled as G, S and D denoting Gate, Source and Drain. In some cases, it is recommended to consult the datasheet of the MOSFET. Normally making the flat side faced towards you, the pins are labeled as S, G, D starting from left to right.

