Analog IC Design 2010

Lecture 7 – CAD tools, Simulation and layout

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All images are taken from Gray, Hurst, Lewis, Meyer, 5th ed., unless noted otherwise.

Contents

Simulation:

- Netlist
- Transistor models
- Process corners
- Example

Layout:

- Design rules
- Comparing layout and schematic

Simulation - Netlist

Netlist and schematic

- Component models

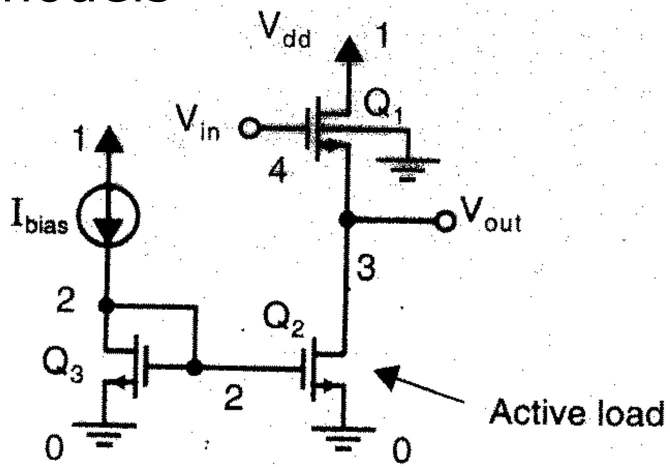

Fig. 3.43 Circuit for Example 3.3.

NETLIST:

vdd	1	0			dc 5
ibias	1	2			dc 100u
m3	2	2	0	0	nmos w=100u l=1.6u
m2	3	2	0	0	nmos w=100u l=1.6u
m1	1	4	3	0	nmos w=100u l=1.6u
vin	4	0			dc 2 ac 1

Source: Johns & Martin, Analog Integrated Circuit Design

Simulation – transistor model

Transistor models:
- BSIM3, BSIM4
- EKV
- MM9, MM11
- …

Challenges:
- How to model the transition between the different regions?
  - Capacitances
  - Output resistance
- Short channel effects
  - Mobility degradation
  - Velocity saturation
- Geometry dependent parameters
  - Mobility
- Temperature dependence

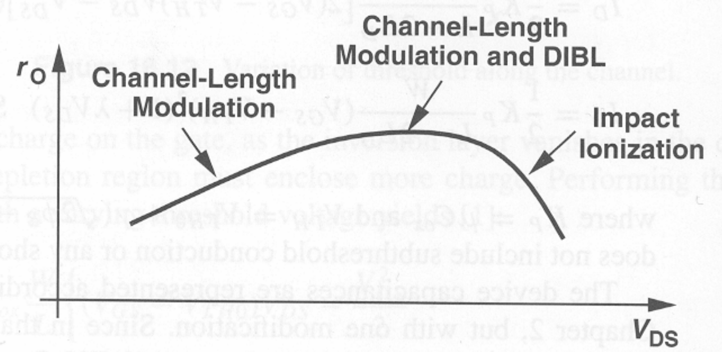

Figure 16.11 Overall variation of output resistance as a function of V_{DS}.

Source: B. Razavi, Design of Analog CMOS Integrated Circuits

BSIM- model

Example: threshold voltage

Long-channel, uniform doping:

$$V_{th} = VTH0 + \gamma(\sqrt{(\Phi s - V_{bs})} - \sqrt{\Phi s})$$

Non-uniform doping:

$$V_{th} = VTH0 + K1(\sqrt{(\Phi s - V_{bs})} - \sqrt{\Phi s}) - K2V_{bs}$$

BSIM4.6.2 MOSFET Model

-User's Manual

Wenwei (Morgan) Yang, Mohan V. Dunga, Xuemei (Jane) Xi, Jin He,
Weidong Liu, Kanyu, M. Cao, Xiaodong Jin, Jeff J. Ou, Mansun Chan,
Ali M. Niknejad, Chenming Hu

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BSIM - Summary

- The model is:
  - Physics based - some fitting parameters
  - Accurate
  - Scalable

  - > 100 parameters

BSIM:
http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

Simulation – process corners

- How do we take into account process variations?
  - Lot to lot
  - Wafer to wafer
  - Die to die

- These variations are translated to speed variations
  - Typical
  - Slow
  - Fast

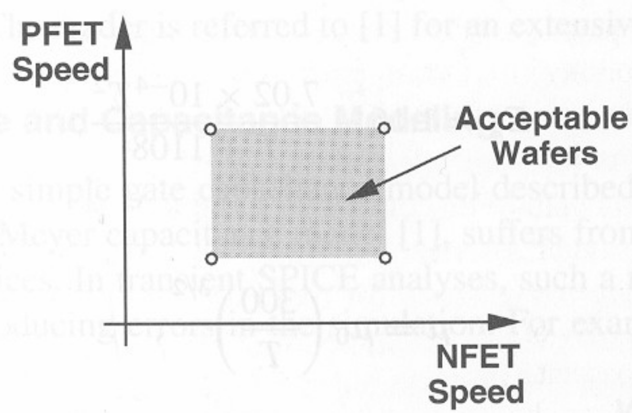


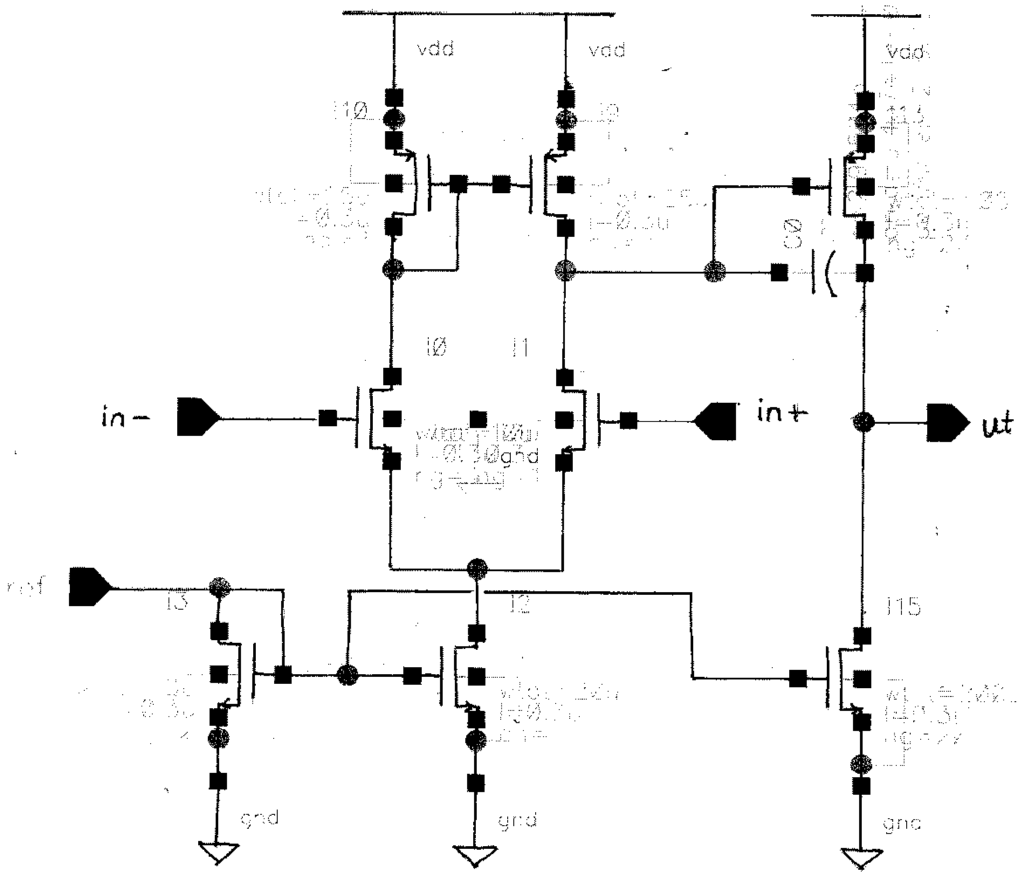
Figure 16.17 Process corners based on speed of NMOS and PMOS devices.

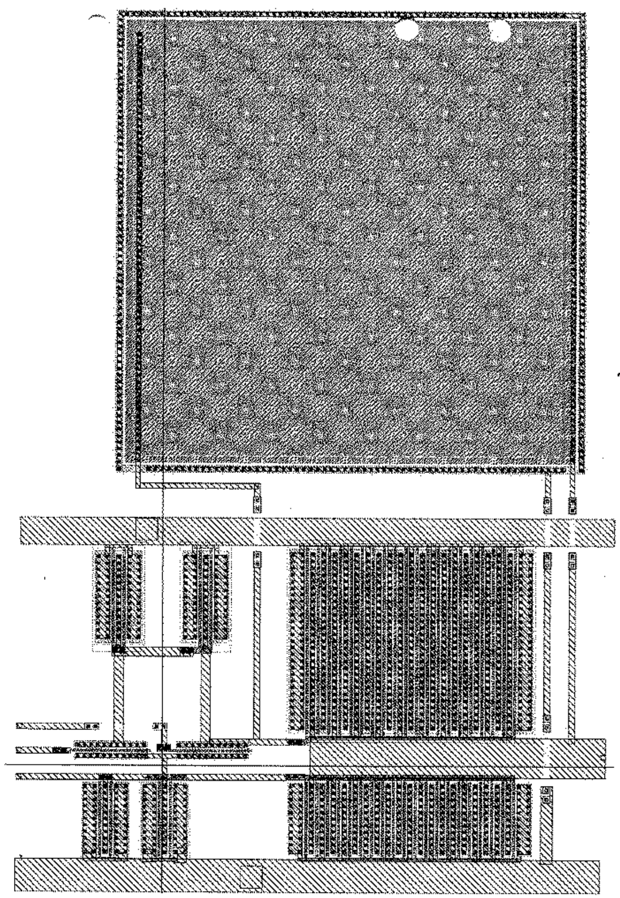
Source: B. Razavi, Design of Analog CMOS Integrated Circuits

Simulation - Example

Amplifier:

- 2-stage Opamp





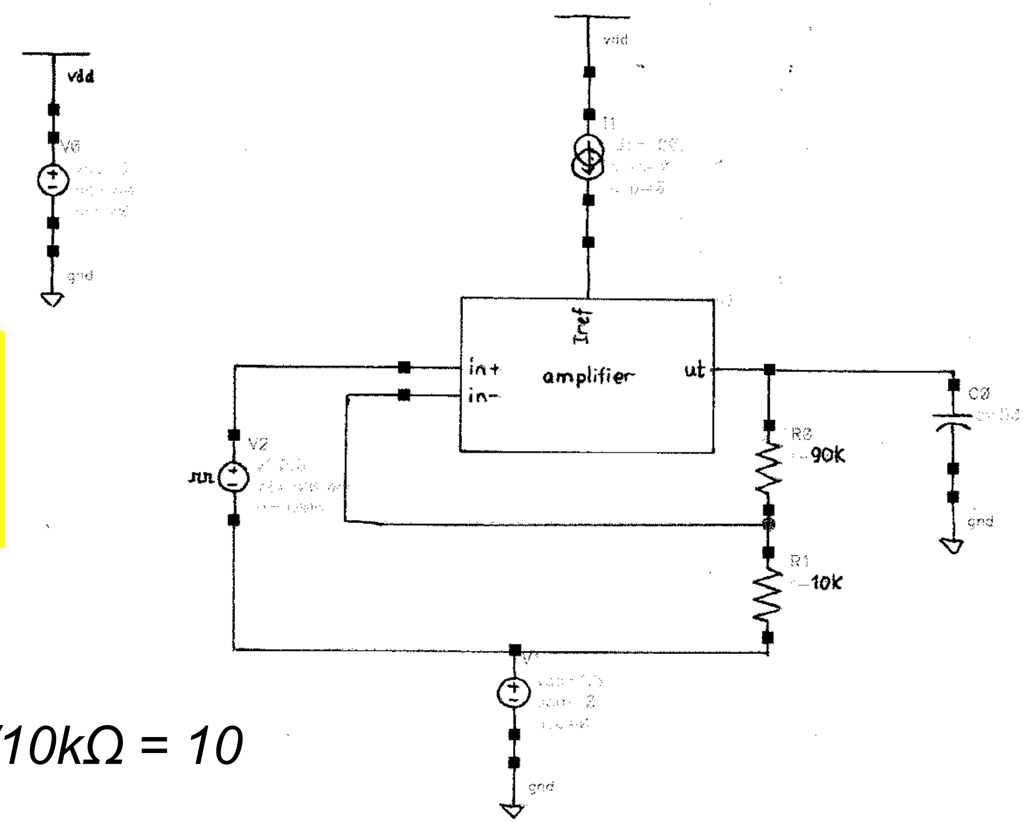
Simulation - Example

Simulations:

- DC, time domain, frequency domain, noise, RF, …

Example:

- Opamp in negative feedback configuration

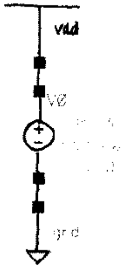


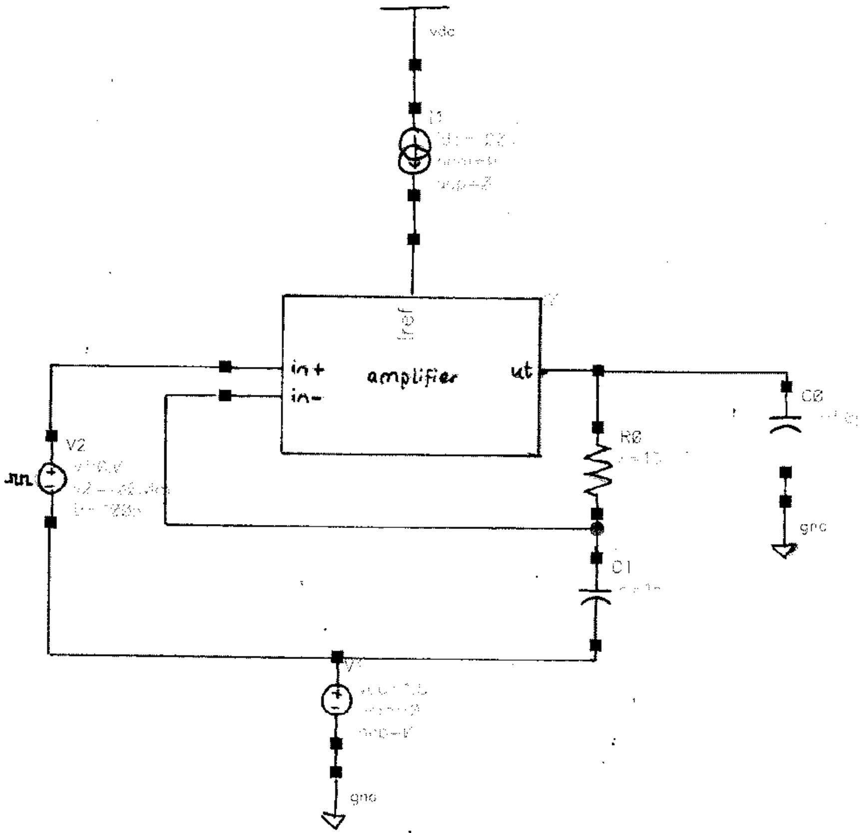
$$A_v = v_o/v_i = 1 + 90k\Omega/10k\Omega = 10$$

Simulation - Example

Non-inverting amplifier with differentiator

$$v_o/v_i\,(s) = 1 + R_1/Z_C$$
$$= 1 + sCR_1$$



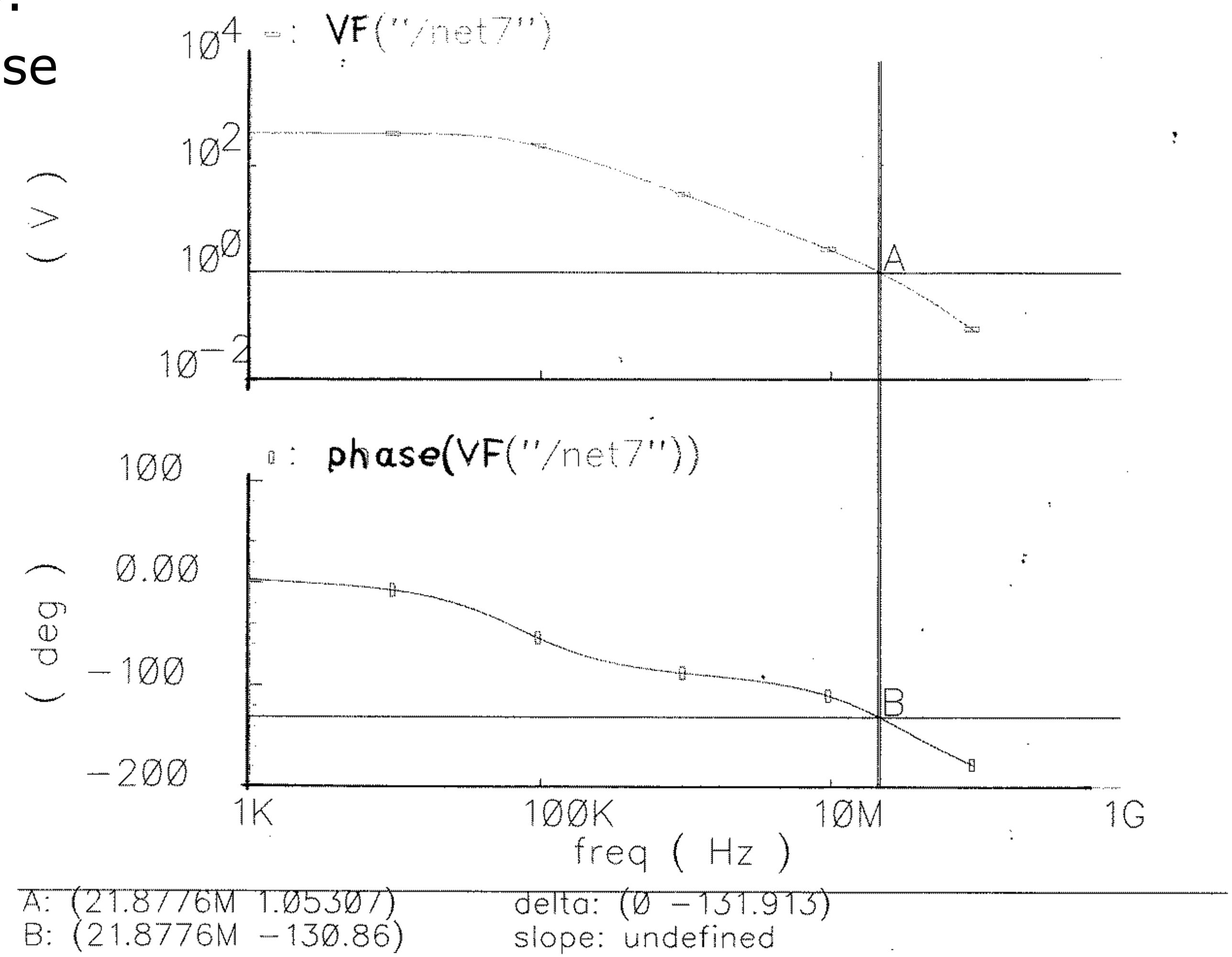


Simulation - Example

Open-loop opamp:

Frequency response

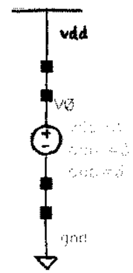
- Amplitude
- Phase

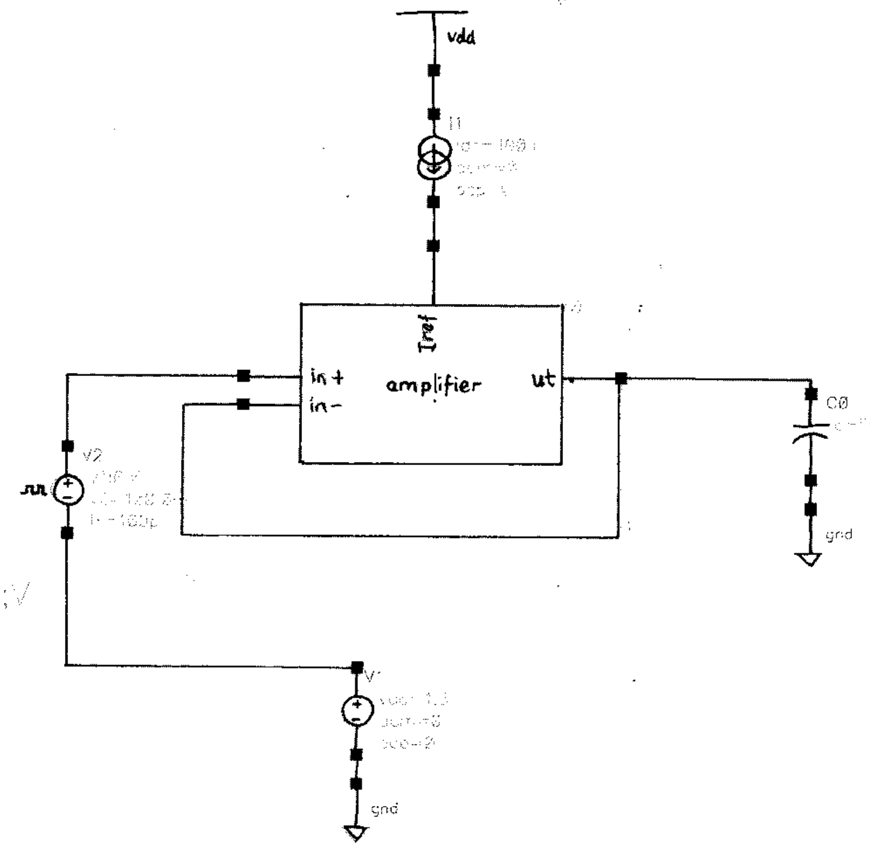


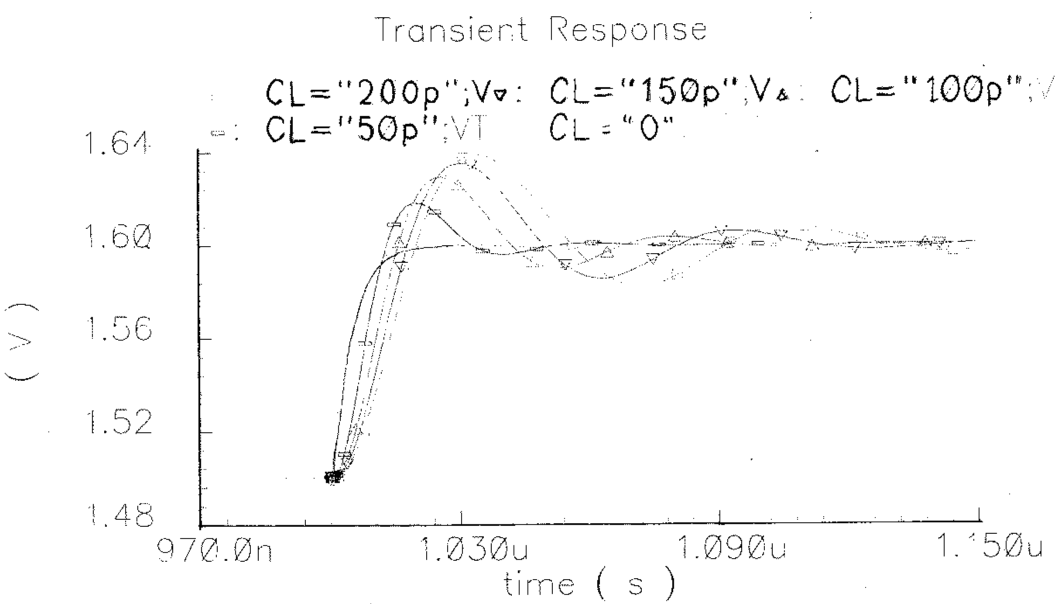
Simulation - Example

Amplifier in unity gain:

- Step response – time domain



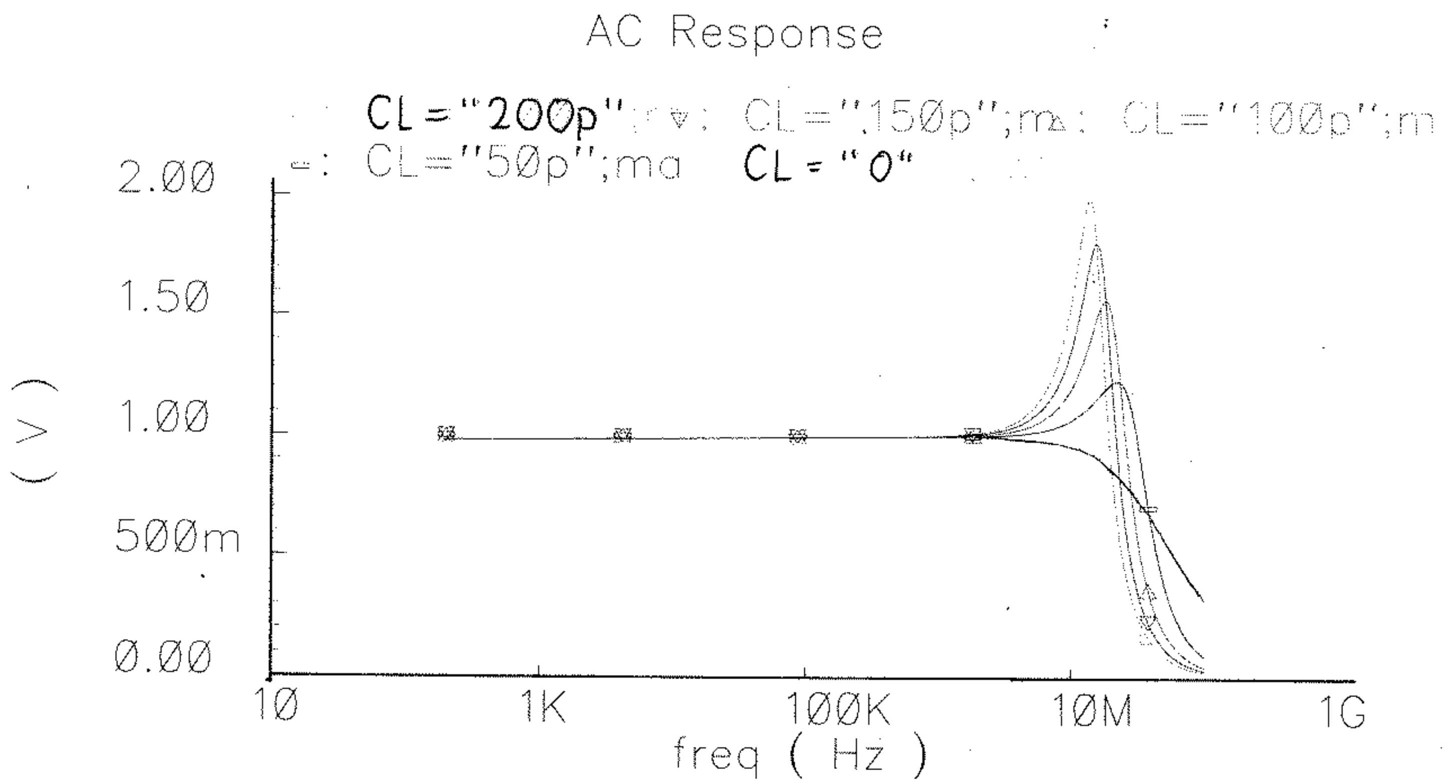




Simulation - Example

Amplifier in unity gain, AC simulation:

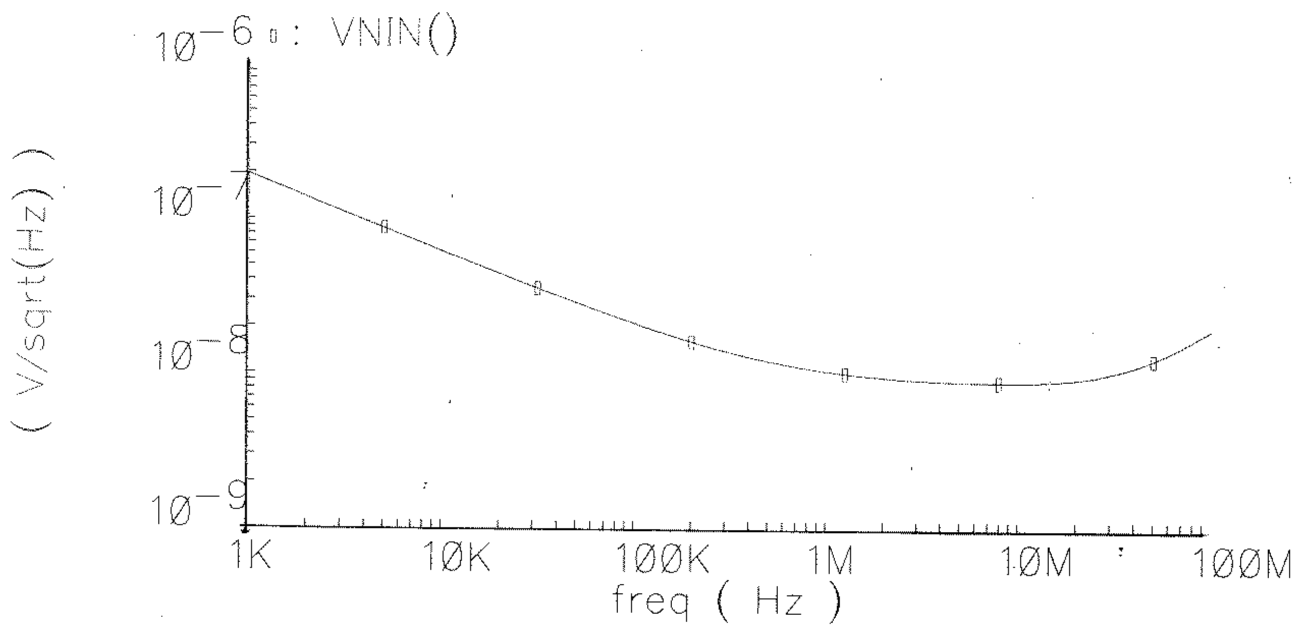
- Linearized circuit parameters!



Simulation - Example

Noise simulation:

- Noise vs frequency
- Referred to input/output



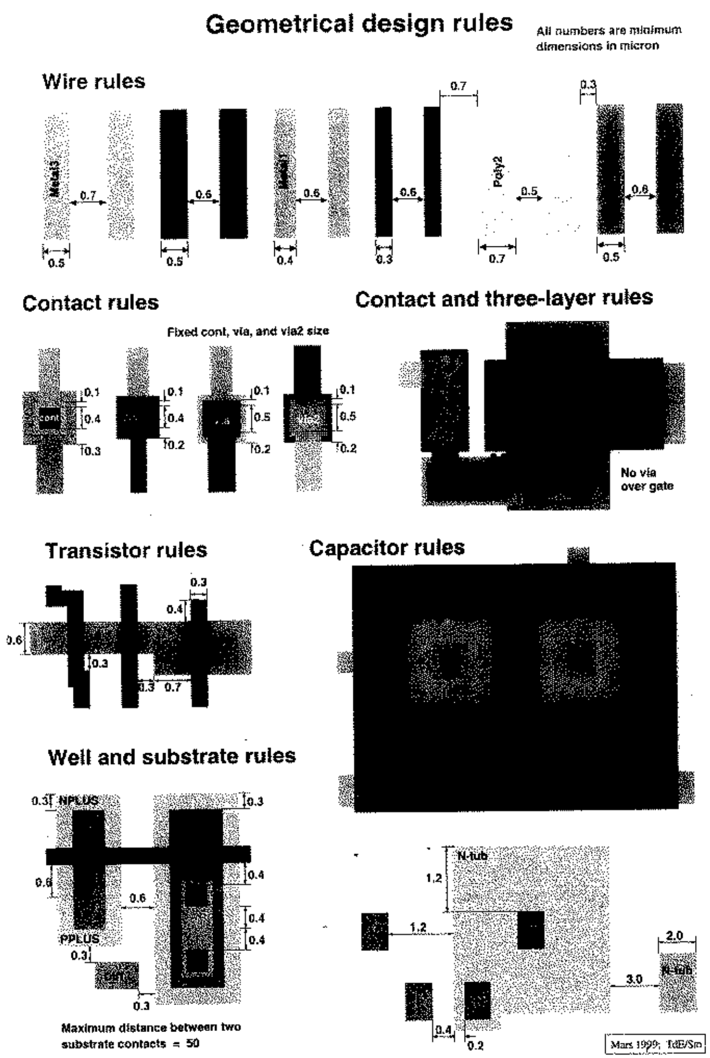
2 minute question!

Discuss in groups of 2 or 3 the following questions:

- What is the fundamental difference between transient and AC simulation?
- Which one is more time consuming?

Be prepared to give a short comment based on your group discussion…

Layout - Design rules



CAD tool:

- Design rule check
  E.g. Cadence Assura

Example of design rules for a 0.35um CMOS technology:

http://www.eit.lth.se/fileadmin/eit/courses/eti063/geometry035.pdf

(see also Course Material)

Layout - Comparing layout and schematic

LVS:

- Layout vs schematic
  - Compare netlists
  - Compare device sizes
  - Compare terminals
- CAD tool:
  - Assura
- Only after running a succesful LVS the parasitics can be extracted
  - Select *Assura > Run RCX* to do this
- Then, the extracted view can be used in post-layout simulations
  - Tool: schematic view *config*

```
@(#)$CDS: LVS version [illegible].4.3 02/28/2001 23:53 (cds230) $

Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

   Net-list summary for /home/klerk/hsd/ams2000new/LVS/layout/netlist
      count
         9                          nets
         6                          terminals
         26                         nmos4
         1                          cpoly
         24                         pmos4

   Net-list summary for /home/klerk/hsd/ams2000new/LVS/schematic/netlist
      count
         9                          nets
         6                          terminals
         5                          nmos4
         1                          cpoly
         3                          pmos4


   Terminal correspondence points
            1         Iref
            2         gnd!
            3         in+
            4         in-
            5         ut
            6         vdd!

The net-lists match.

                              layout   schematic
                              instances
        un-matched            0         0
        rewired               0         0
        size errors           0         0
        pruned                0         0
        active                51        9
        total                 51        9

                              nets
        un-matched            0         0
        merged                0         0
        pruned                0         0
        active                9         9
        total                 9         9

                              terminals
        un-matched            0         0
        matched but
        different type        0         0
        total                 6         6
```

Links

General information on Cadence & CADtools:

http://www.eit.lth.se/cadsys/cadence.html

(note that the lab manual precedes over the general information!)

Simulator used in this course: GoldenGate

http://www.eit.lth.se/cadsys/goldengate.html

Golden gate manuals can be found at
'/usr/local-eit/cad2/agilent/GoldenGate-4-2-0/doc/gg_help.html'
(Copy link to the browser on a computer in E:2435)

Extra - BSIM - manual

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