

Analog to Digital (ADC) and Digital to Analog (DAC) Converters

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Introduction:

Electric voltage and current signals are often referred to as analog signals. Analog signals must be converted to digital signals prior to input into computers. Analog to Digital Converters (ADCs) are used to convert analog signals to digital signals. Inversely, the computer output that is in digital form must sometimes be converted to an analog signal prior to input to an electronic or electrical device. Digital to Analog Converters (DACs) are used to perform this operation. In this paper we will examine important characteristics associated with ADC/ DAC converters. In addition, we will explain how to specify a converter to meet the requirements of a specific system.

We will also state and describe different types of ADC / DAC converters. Binary-weighted, and R- 2R Ladder type DAC circuits will be displayed and analyzed. Parallel Comparator or Flash, Dual Slope, and Successive Approximation type ADC circuits will be displayed and analyzed. We will explain extensively the advantage / disadvantage criteria associated with each type of ADC or DAC converters. Finally, two computer interfacing laboratory assignments will demonstrate the constructions of the R-2R Ladder type DAC, and Successive Approximation type ADC converters.

Digital to Analog Converter (DAC) Characteristic:

When we select a Digital to Analog Converter (DAC) chip for an application, we must consider three characteristic associated with a DAC. First, resolution or step size defines the smallest voltage or current change possible for the DAC output signal. For example, an 8-bit DAC that generates a maximum output voltage of 5 volts has a step size or resolution of $(5V / 2^8) = 19.5$ mV. Sometimes, the resolution is stated in the percentage value. For the 8-bit DAC, the percent resolution is $(1 / 2^8) \times 100 = 0.39\%$. Settling time is the time required for the DAC output to settle to 99.5% of its new value. Typical settling time for a commercial DAC is 300 nanoseconds. Accuracy is used to state the percentage of actual output of a DAC to expected output. Usually the accuracy is 50% of the step size. For the 5 V, 8-bit DAC the accuracy is 0.975 mV. This implies that the maximum output is guaranteed by the DAC manufacturer to be within 5.00975V and 4.99025V.

Digital to Analog Converter (DAC) types:

There are two methods of constructing a DAC; Binary Weighted type, and R-2R Ladder type. Figure 1 displays an 8-bit binary weighted type DAC circuit. The output voltage for a binary weighted DAC is found using the following equation.

$$V_{OUT} = (V_{REF}) * (R_F / R) * (D7 / 2^0 + D6 / 2^1 + + D1 / 2^6 + D0 / 2^7)$$

Note that the switches represent transistors that can be opened (i.e., operates in turned off, or open collector to emitter state), or closed (i.e., operates in turned on, or saturated state).

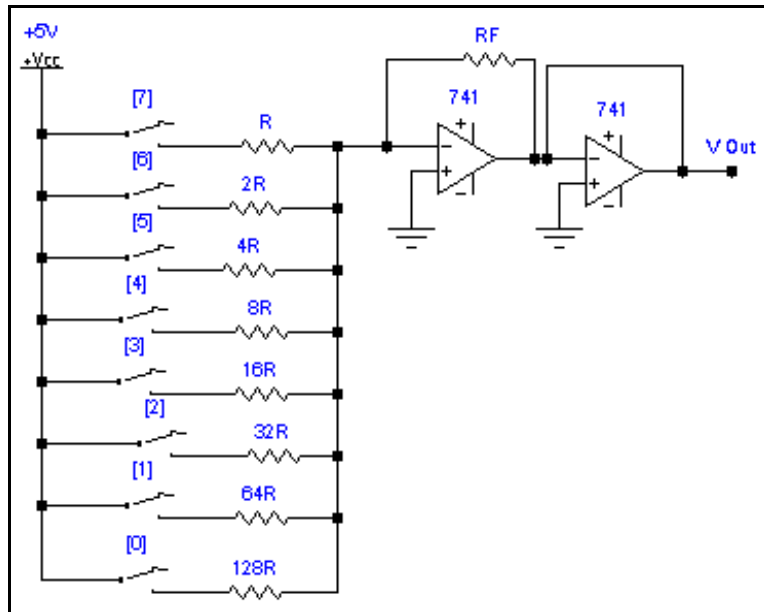


Figure 1. 8-bit, Binary Weighted Type DAC

The advantage of a binary weighted DAC circuit is due to its simplistic construction with fewer electronic components. However, the disadvantage is that as the number of input bits increases, the value of the current on the least significant bit (D0) branch will decrease. This reduction in current value will eventually be significant enough to distort the current signal in the branch that has the switch for the least significant bit. To solve this problem, most DACs are constructed using R-2R Ladder type circuits. Figure 2 displays an 8-bit R-2R Ladder type DAC circuit. In order to analyze the circuit, assume that all bits except one are connected to the ground. Then, equivalent resistance is calculated by realizing that two 2R resistors are in parallel, which will generate an equivalent value of R. Next, this equivalent resistor is in series with another R to produce an equivalent resistance of 2R. This process continues until the number of resistors in the circuit are reduced to a couple of 2R resistors.

Figure 3 displays the equivalent circuit when D7 is connected to +5V. Now we can find the Thevenin Equivalent Circuit of the section to the left of the Operational Amplifier (Op-Amp), and proceed to calculate the output voltage generated by the associated bit. The following equation represents the DAC output voltage for the R-2R Ladder type circuit.

$$V_{OUT} = (V_{REF}) * (R_F / 2R) * (D7 / 2^0 + D6 / 2^1 + + D1 / 2^6 + D0 / 2^7)$$

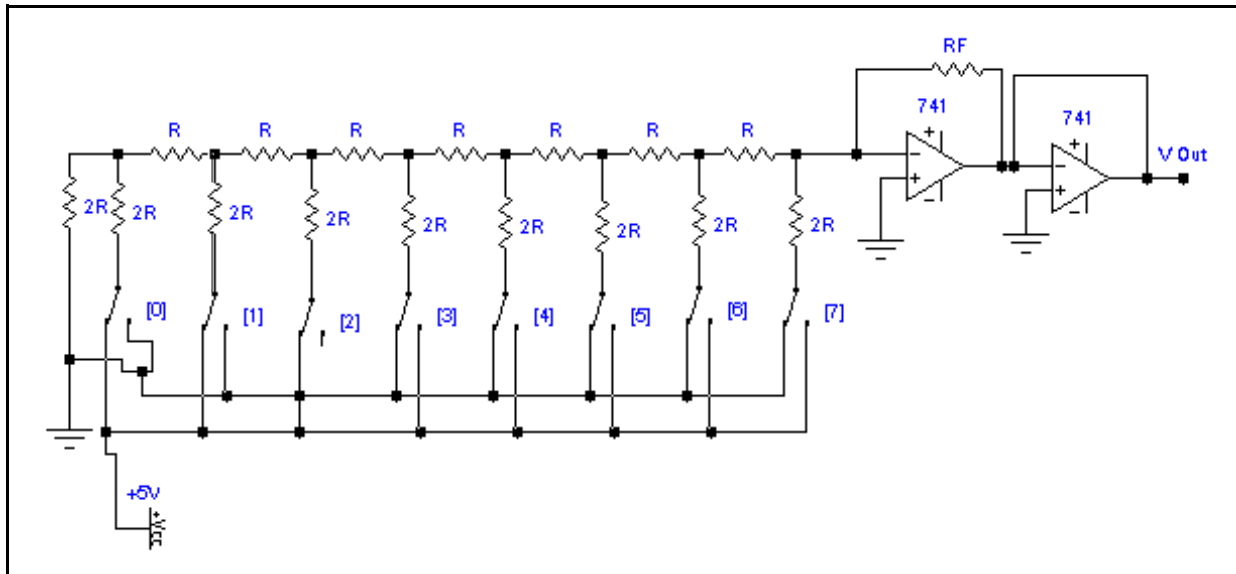


Figure 2. 8-bit, R-2R Type Digital to Analog Converter.

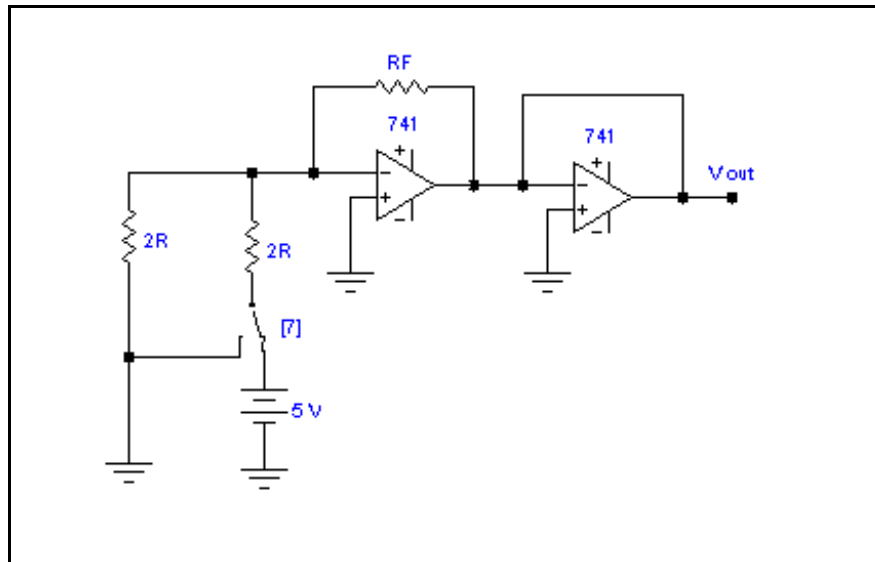


Figure 3. R-2R Equivalent Circuit when only bit seven (D7) is on.

Digital to Analog Converter (DAC) Lab Assignment:

Students use the electronic circuit simulation packages available [1,2] in the computer lab to analyze the binary weighted and R-2R Ladder type circuits. In addition, a lab assignment illustrates the construction of a R-2R Ladder type DAC, and the use of this circuit to generate waveforms. Figure 4 shows the wiring diagram of the DAC lab assignment. We have used a computer interface card to connect the DAC circuit to a personal computer. A complete description of the interface card, and its associated address decoder circuit are in a previously published paper [3]. The Y1 output of the 74LS138, three-to-eight decoder chip represents address 301Hex =769 Decimal.

Once the circuit is wired and connected to the computer and oscilloscope, the program listed in Appendix A is used to check the validity of the value of each DAC bit. Finally, the programs

listed in Appendix B are used to generate different types of waveforms. The MC1408 Digital to Analog converter chip manufactured by Motorola [4] is a typical 8-bit DAC chip. Figure 5 shows the wiring diagram of the MC1408 DAC chip[5].

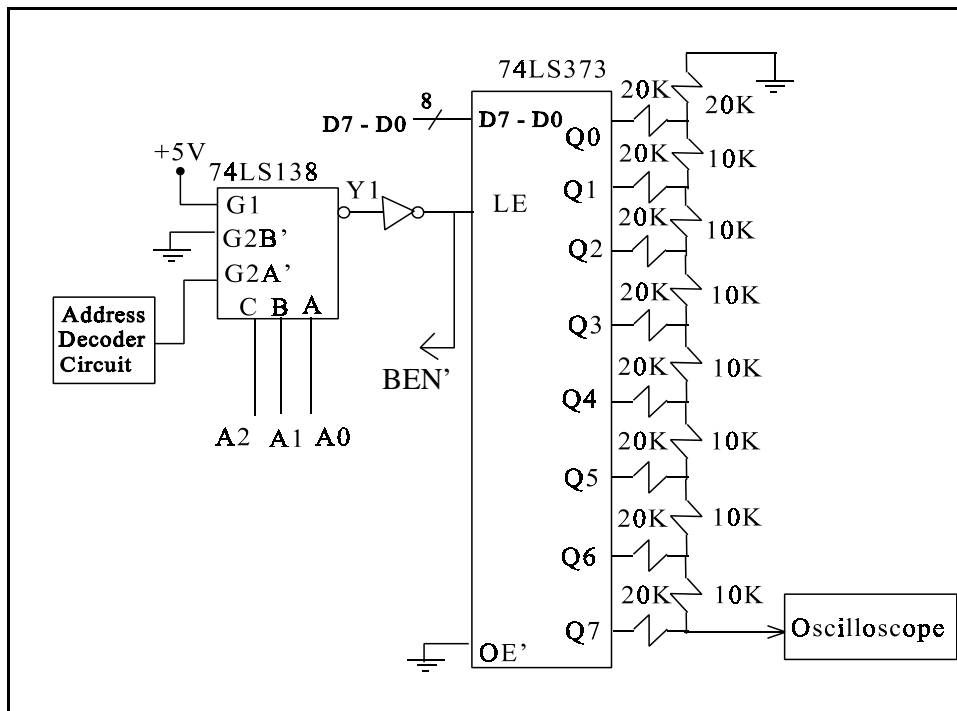


Figure 4. Wiring Diagram of R-2R Ladder Type DAC Lab Assignment

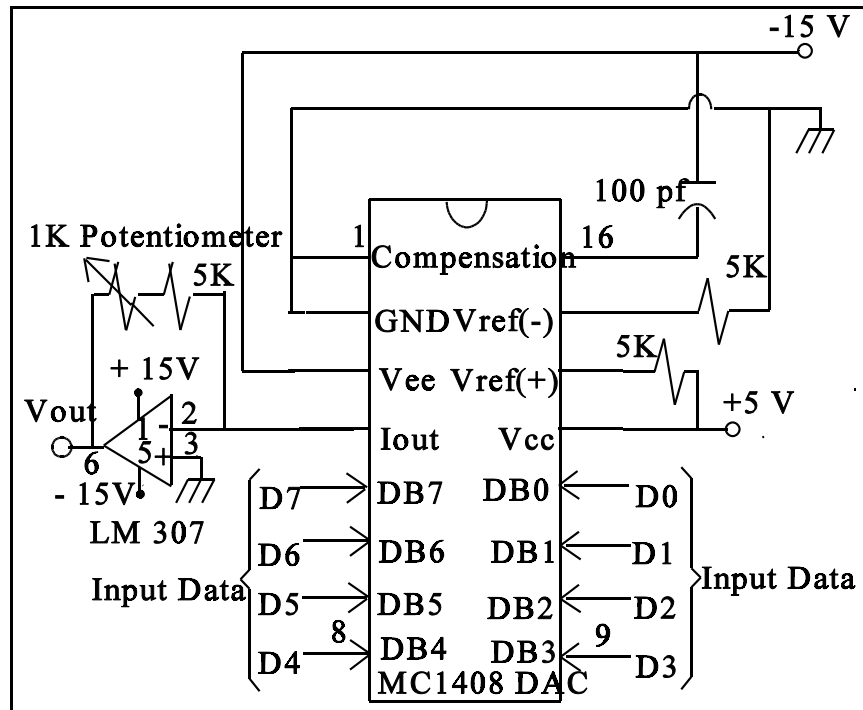


Figure 5. MC1408 Digital to Analog Converter (DAC)

Analog to Digital Converter (ADC):

When selecting an Analog to Digital converter (ADC) chip for an application, three characteristics must be considered. Similar to selecting a DAC, these characteristics are; number of bits, accuracy, and speed. There are three different methods used for constructing Analog to Digital converters. These ADC types are; Parallel Comparator or Flash type, Dual-Slope type, and Successive Approximation type.

Figure 6 displays a 3-bit, flash type ADC circuit. The voltage divider provides eight reference voltages on the negative poles of the operational amplifiers. The unknown input voltage is compared to each one of the reference voltages. If the input voltage is greater than any one of the reference voltages, the associated Op-Amp will be saturated to its positive supply voltage level. The eight-to-three encoder will generate an appropriate three bit binary word according to the inputs A0 through A7. For example, assume A4 is the only input to the encoder that is set. That would mean that the input voltage is 2.5V, and the output binary number will be 100.

The advantage of a Flash type ADC is its instantaneous speed. The Flash type ADC is expensive due to the large numbers of OP-Amp devices contained therein. For example, an 8-bit flash type ADC requires $2^8 - 1 = 255$ Op-Amps. Flash type ADCs are used in special applications such as systems used by the military or NASA.

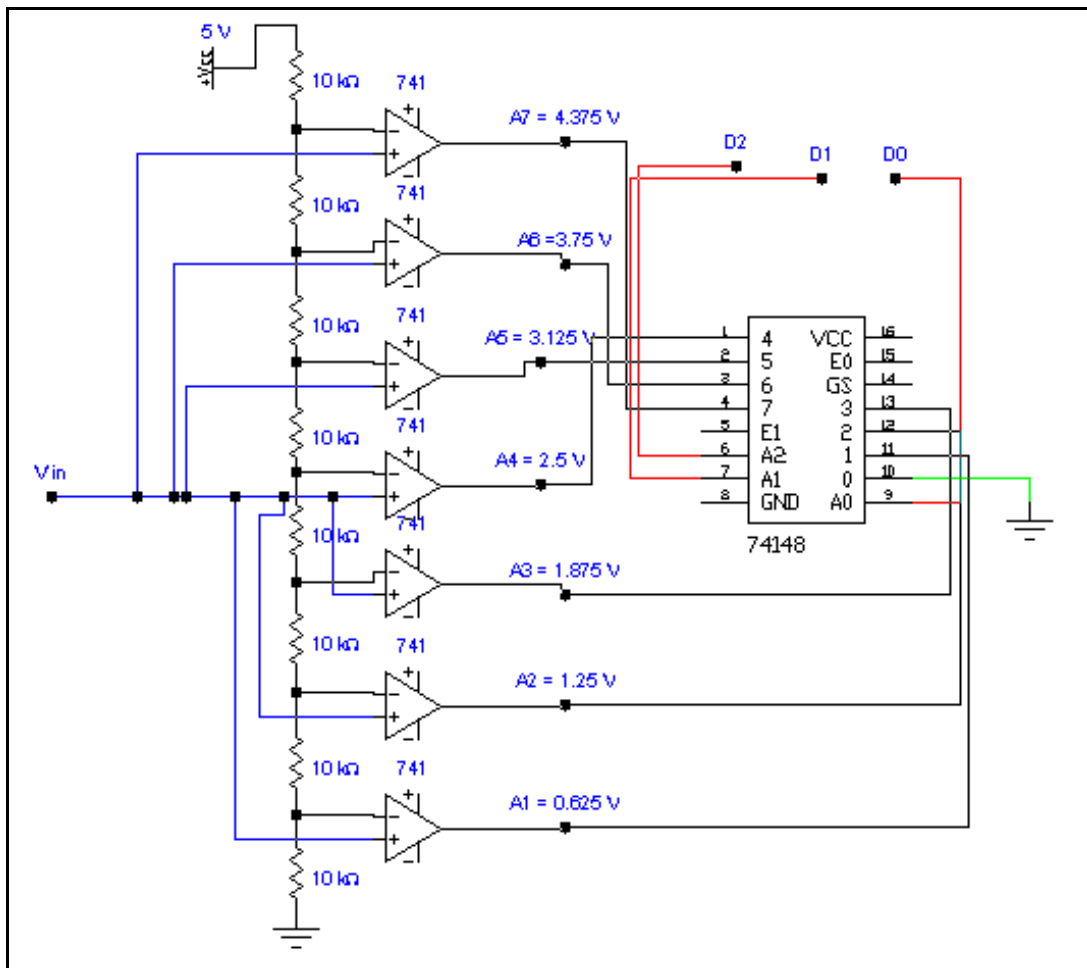


Figure 6. Three-bit, Flash Type Analog to Digital Converter Circuit

In the Dual Slope ADC type, a capacitor is connected to input voltage and allowed to charge up for a fixed amount of time. Then, the capacitor is connected to the ground and allowed to discharge. The time required for the capacitor to discharge is calibrated to reflect the value of the input voltage. Figure 7 illustrates the operation of the Dual Slope type ADC. These type of ADCs are very slow, and are usually found in electronic voltmeters.

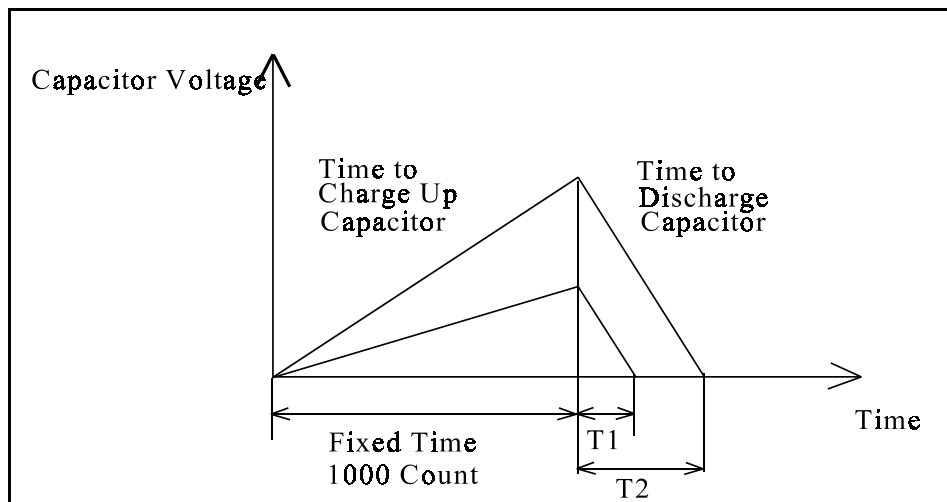


Figure 7. Operation of the Dual-Slope Type Analog to Digital Converter

Figure 8 displays a block diagram of a successive approximation ADC. In the successive approximation ADC, the output of a comparator is connected to the input of a special counter register called a Successive Approximation Register (SAR).

The OP-Amp comparator is used to compare the unknown input voltage to the output of a DAC. The successive binary numbers generated by the SAR are fed into the DAC. Upon receiving an active signal from the “Start Conversion” line, the SAR will turn its Most Significant Bit (MSB) on. If the output from the comparator is low, the bit will be turned off, otherwise the MSB will be kept on. Next, the second highest bit on the SAR is turned on, and the decision is made to keep the bit on, or turn it off. This process will continue until the Least Significant Bit (LSB) is checked. Then a signal from the “End Of Conversion” line will enable the octal latch in order to have the data released onto the data lines. If we connect the “End Of Conversion” line to the “Start Conversion” line as shown in Figure 8, the conversion will be continuous.

Figure 9 illustrates the operation of the successive approximation type ADC. Note that every conversion requires eight (8) clock pulses. Therefore, the successive approximation type ADC converts faster than the Dual Slope type ADC.

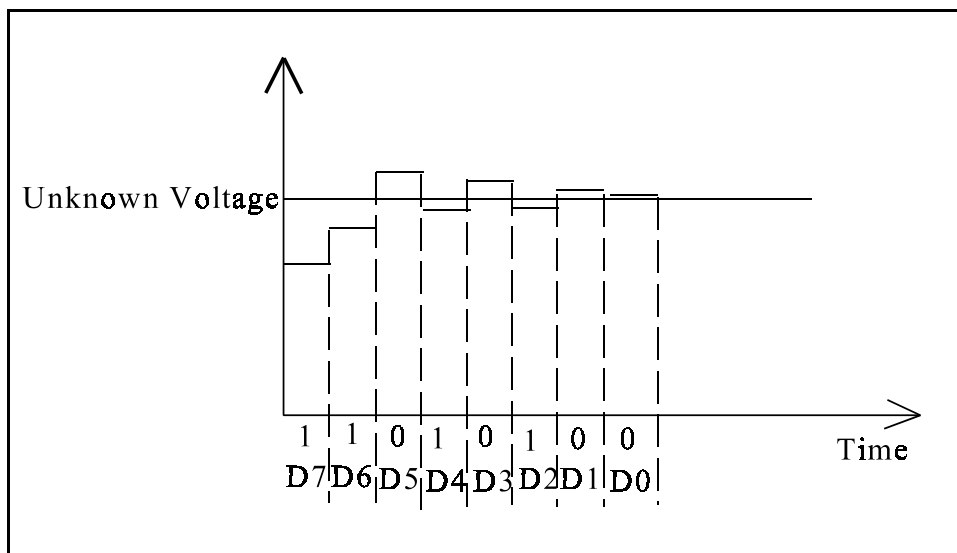


Figure 9. Operation of the Successive Approximation Type ADC.

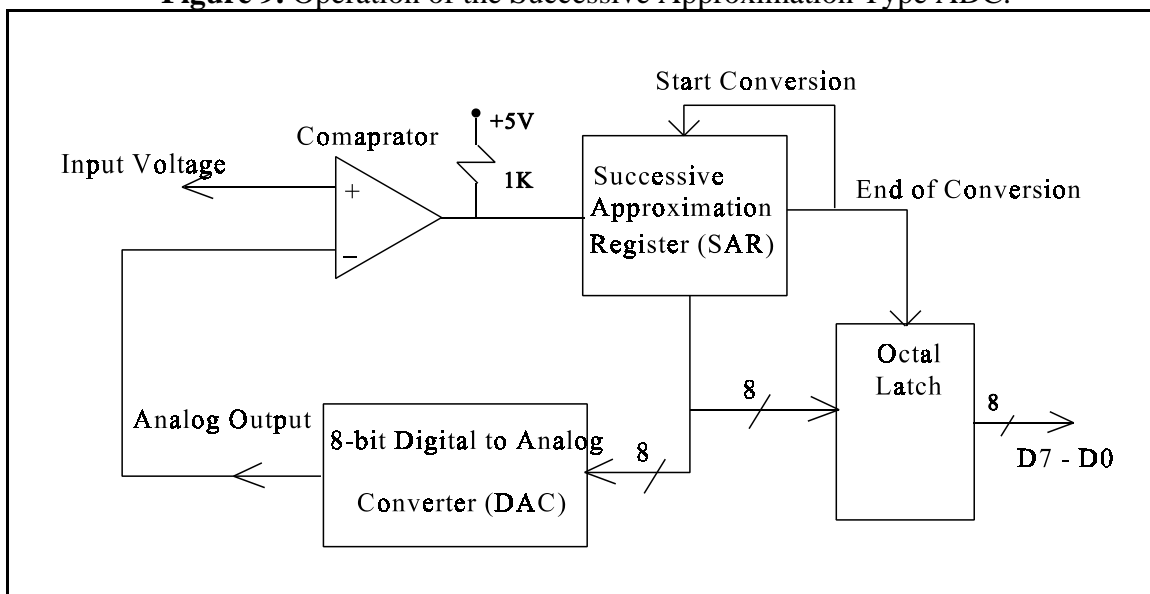


Figure 8. Block Diagram of the Successive Approximation Type ADC.

Most of the commercially available ADCs are the successive approximation type. Figure 10 displays a connection diagram of the 0804 ADC [5]. This chip is manufactured by the National Semiconductor Corporation [6]. This chip is an inexpensive, 8-bit, successive approximation type ADC.

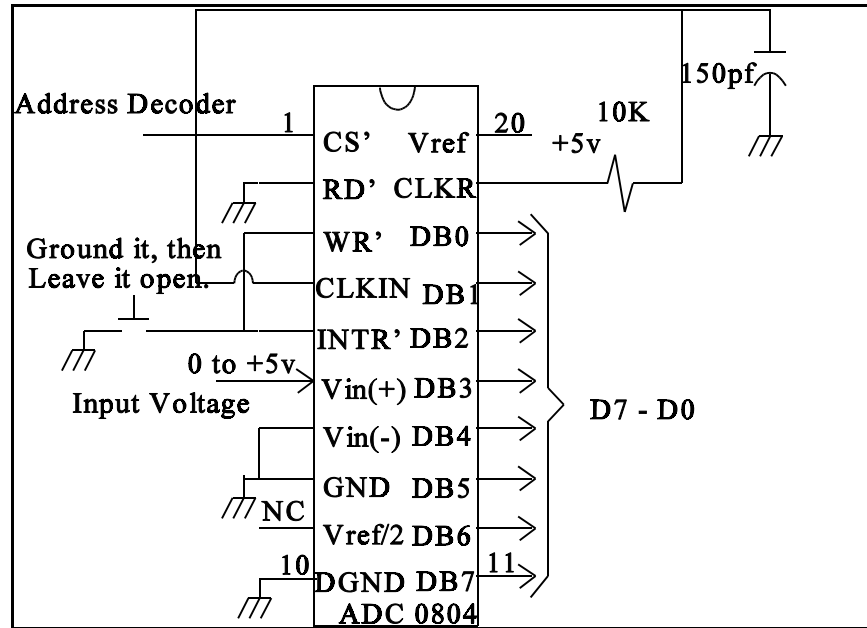


Figure 10. Connection Diagram of the ADC0804

Analog to Digital Converter (ADC) Lab Assignment:

Figure 11 displays the wiring diagram of an ADC Lab Assignment. The program for simulating the operation of a successive approximation type ADC is listed in appendix C.

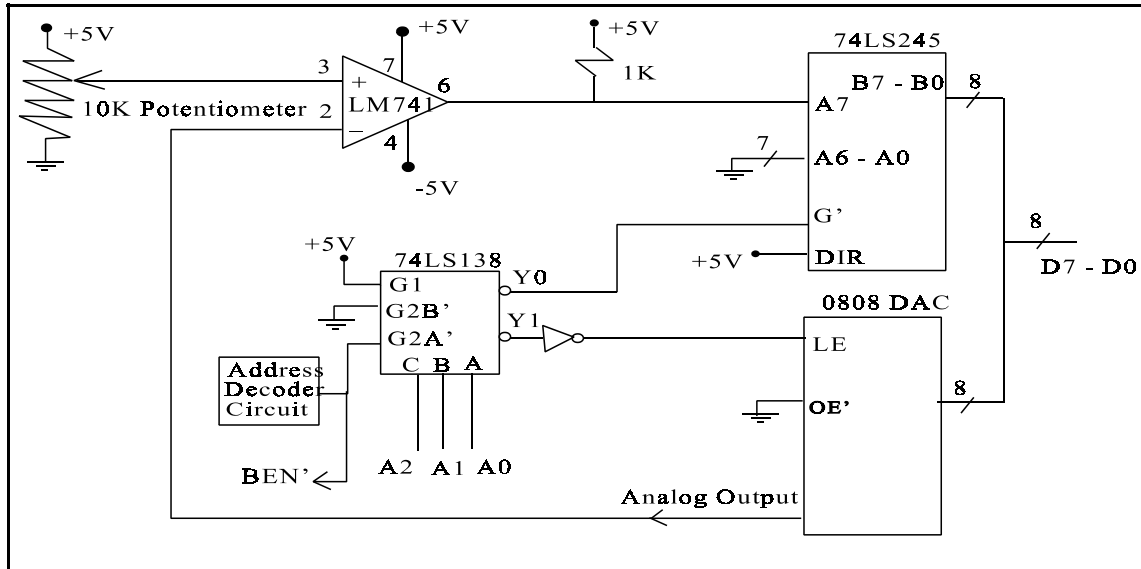


Figure 11. Successive Approximation Type ADC Lab Assignment.

Conclusion:

This paper presents an in-depth discussion of the construction, and use of Analog to Digital (DAC) and Digital to Analog (ADC) converters. These components are found in a majority of digital electronic instruments. Students in digital and microprocessor hardware classes are acquiring methods of constructing and utilizing ADCs and DACs. Hardware sections of the lab assignments are intended to familiarize students with the wiring connection of these devices in a circuit. Students are assigned programs to write. The purpose of these programs is to control the process of reading from / writing to the input / output ports.

Appendix A:

```

REM Check each bit.
10 INPUT D
20 OUT 769, D
30 FOR COUNT = 1 TO 100
40 PRINT D
50 NEXT COUNT
60 GOTO 10

```

Appendix B:

```

REM Increasing Ramp.
10 FOR I = 1 TO 255 STEP 5
15 OUT 769, I
20 FOR COUNT = 1 TO 10
40 NEXT COUNT
50 NEXT I

```

```
60 GOTO 10
```

```
REM Decreasing Ramp.
```

```
10 FOR I = 255 TO 1 STEP -5  
20 OUT 769, I  
30 FOR COUNT = 1 TO 10  
40 NEXT COUNT  
50 NEXT I  
60 GOTO 10
```

```
REM Sawtooth Waveform
```

```
10 FOR I = 1 TO 255 STEP 5  
20 OUT 769, I  
30 FOR COUNT = 1 TO 10  
40 NEXT COUNT  
45 NEXT I  
50 FOR I = 255 TO 1 STEP -5  
60 OUT 769, I  
70 FOR COUNT = 1 TO 10  
80 NEXT COUNT  
90 NEXT I  
110 GOTO 10
```

```
REM Pulse Waveform
```

```
10 FOR I = 1 TO 50  
20 OUT 769, 0  
30 NEXT I  
40 FOR I = 1 TO 50  
50 OUT 769, 255  
60 NEXT I  
70 GOTO 10
```

Appendix C:

```
10 CLS  
20 D = 128  
30 OUT 769, D  
40 L = INP(768)  
50 IF L = 128 THEN B7 = 128 ELSE B7 = 0  
55 D = B7 + 64  
60 OUT 769, D  
70 L = INP(768)  
80 IF L = 128 THEN B6 = 64 ELSE B6 = 0  
90 D = B7 + B6 + 32
```

```

100 OUT 769, D
110 L = INP(768)
120 IF L = 128 THEN B5 = 32 ELSE B5 = 0
130 D = B7 + B6 + B5 + 16
140 OUT 769, D
150 L = INP(768)
160 IF L = 128 THEN B4 = 16 ELSE B4 = 0
170 D = B7 + B6 + B5 + B4 + 8
180 OUT 769, D
190 L = INP(768)
200 IF L = 128 THEN B3 = 8 ELSE B3 = 0
210 D = B7 + B6 + B5 + B4 + B3 + 4
250 OUT 769, D
260 L = INP(768)
270 IF L = 128 THEN B2 = 4 ELSE B2 = 0
280 D = B7 + B6 + B5 + B4 + B3 + B2 + 2
290 OUT 769, D
300 L = INP(768)
310 IF L = 128 THEN B1 = 2 ELSE B1 = 0
320 D = B7 + B6 + B5 + B4 + B3 + B2 + B1 + 1
330 OUT 769, D
340 L = INP(768)
350 IF L = 128 THEN B0 = 1 ELSE B0 = 0
360 D = B7 + B6 + B5 + B4 + B3 + B2 + B1 + B0
370 PRINT D
380 SLEEP 1
390 GOTO 10

```

References:

1. PSpice and Circuit Analysis, MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718.
2. Electronics Workbench, Interactive Image Technologies LTD., 111 Peter Street, #801, Toronto, Ontario, Canada M5V 2H1.
3. "Computer Interface for Liquid Crystal Display (LCD)", 1997 American Society for Engineering Education (ASEE) Annual Conference Proceedings, Session #1532, Paper #6, June 1997.
4. Motorola Literature Distribution, P.O.Box 20912, Phoenix, AZ 85036.
5. "Design, Construction, and Analysis of a Micro Controller", COMPUTERS IN EDUCATION JOURNAL, published by the Computers in Education Journal Division of the American Society for Engineering Education (ASEE), Volume VI, Number 2, pp. 63-68, April-June, 1996 Journal.

6. National Semiconductor Corporation, 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, CA 95052-8090.

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