Analog-to-Digital Converter Design

From System Architecture to Transistor-level

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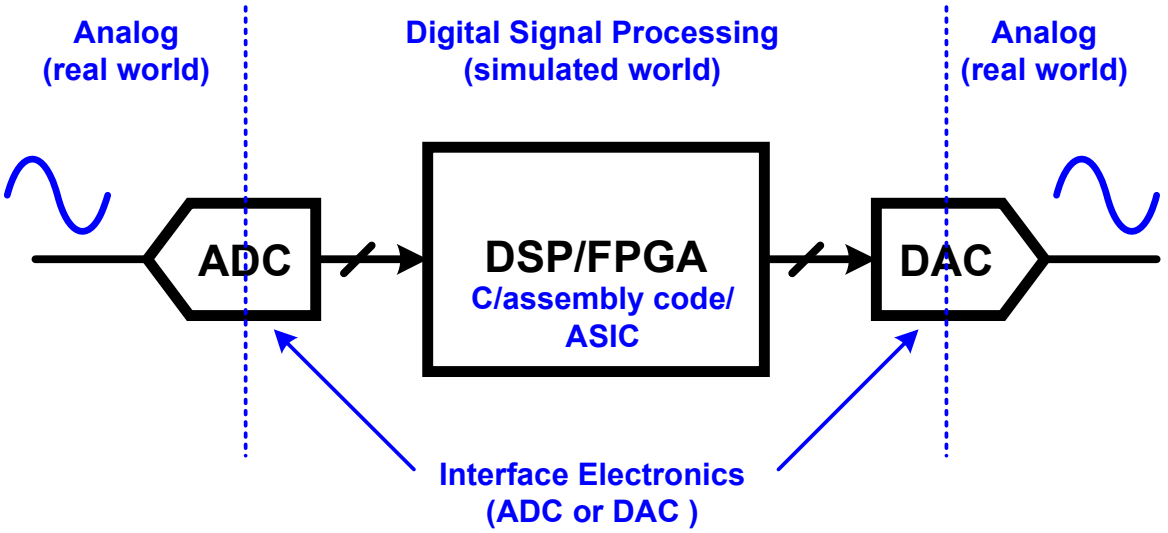
Outline

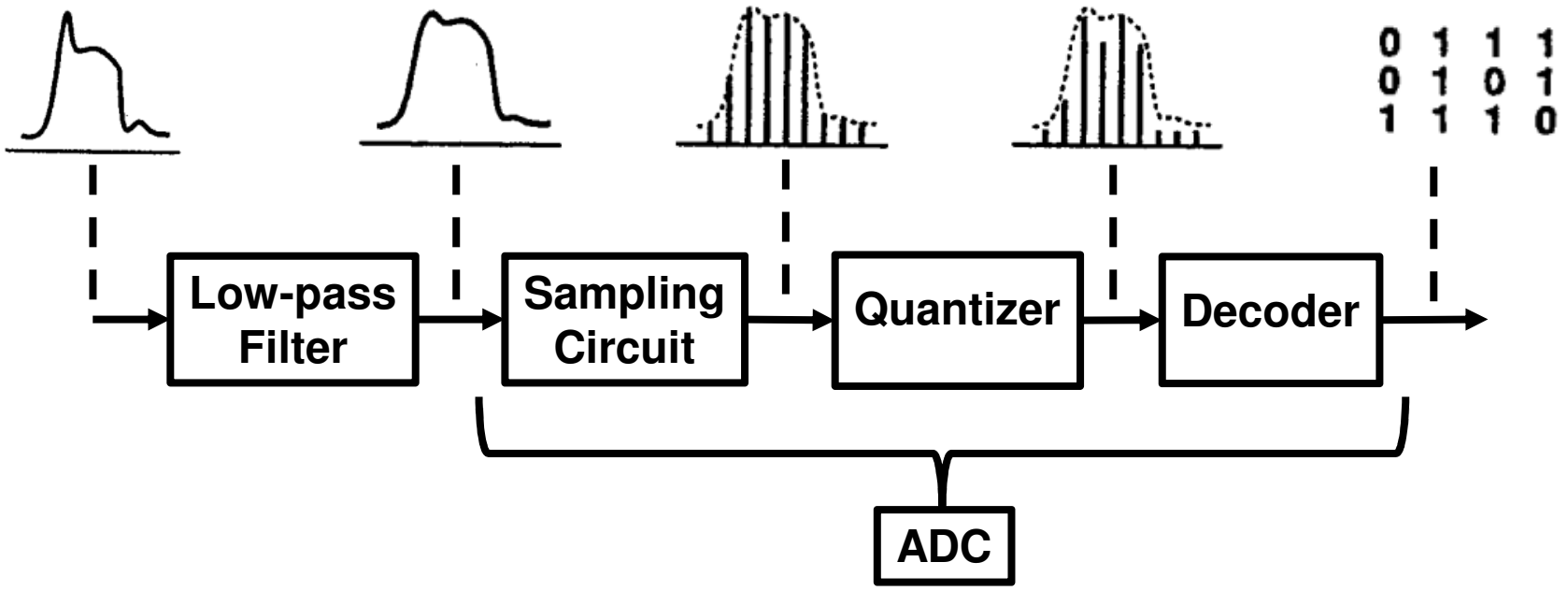
- Introduction to Data Converters
  - Sampling and Quantization
  - Oversampling to improve performance
- Overview of Pipelined ADCs
  - Switch-capacitor Circuits – Overview
  - Non-idealities
  - Thermal Noise Cancellation
- System-level Specs. to Circuit Details
  - Case Study of Pipelined ADC
- Impact of Scaling on Data Converter Design
- Why Calibration
- Basics of Digital Calibration Techniques – With Examples

Data Converters 101



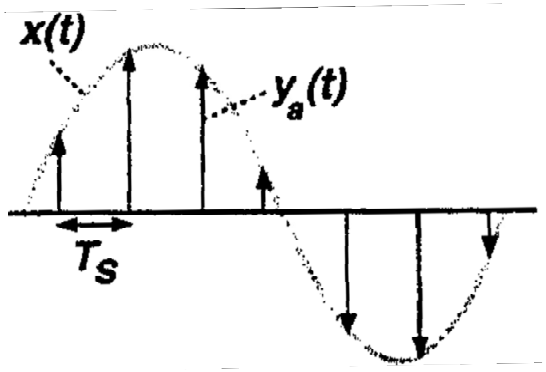
- **Real world: Continuous-time, continuous-amplitude signals**
- **Digital world: Discrete-time, discrete-amplitude signal representation**
- **Interface circuits: ADC and DACs**

Data Converters 101 (Contd.)

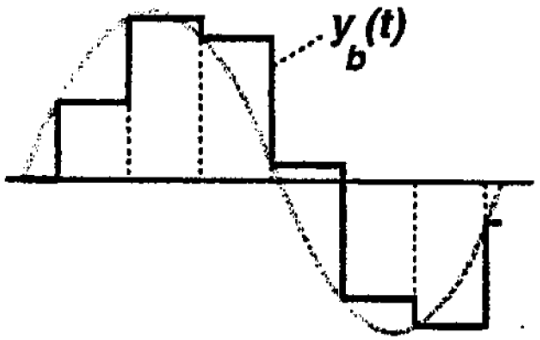


- **Low-pass filtering to avoid aliasing → Also called signal conditioning**
- **The process of sampling→quantization→decoding is an analog-to-digital converter (ADC)**

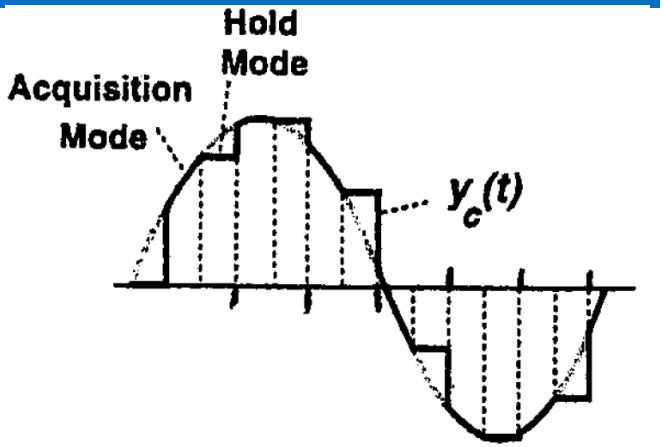
Sampling-Time Domain



Impulse Sampling



Zero-order Hold



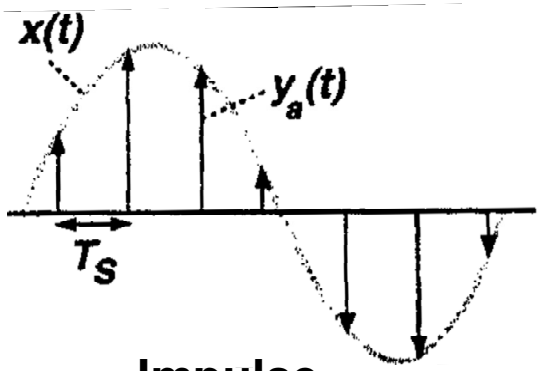
Track-and Hold

$$y_a(t) = x(t) \sum_{k=-\infty}^{k=+\infty} \delta(t - kT_S)$$

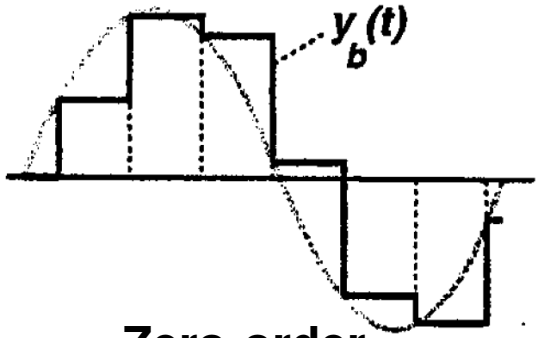
$$y_b(t) = x(t) \sum_{k=-\infty}^{k=+\infty} \delta(t - kT_S) * \prod\left(\frac{t}{T_s} - \frac{1}{2}\right)$$

$$y_c(t) = y_1(t) + y_2(t)$$

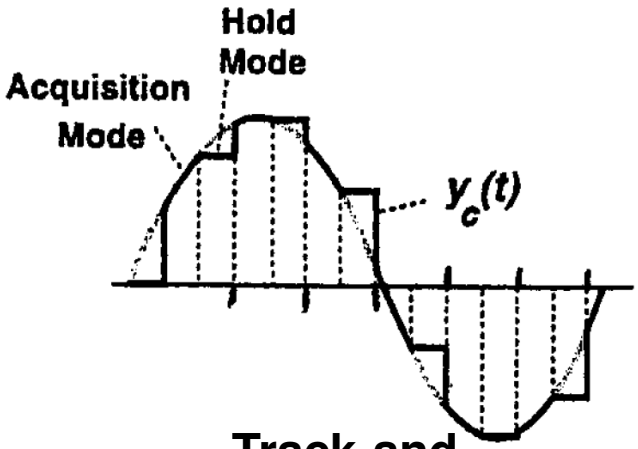
Sampling-Frequency Domain



Impulse Sampling



Zero-order Hold



Track-and Hold

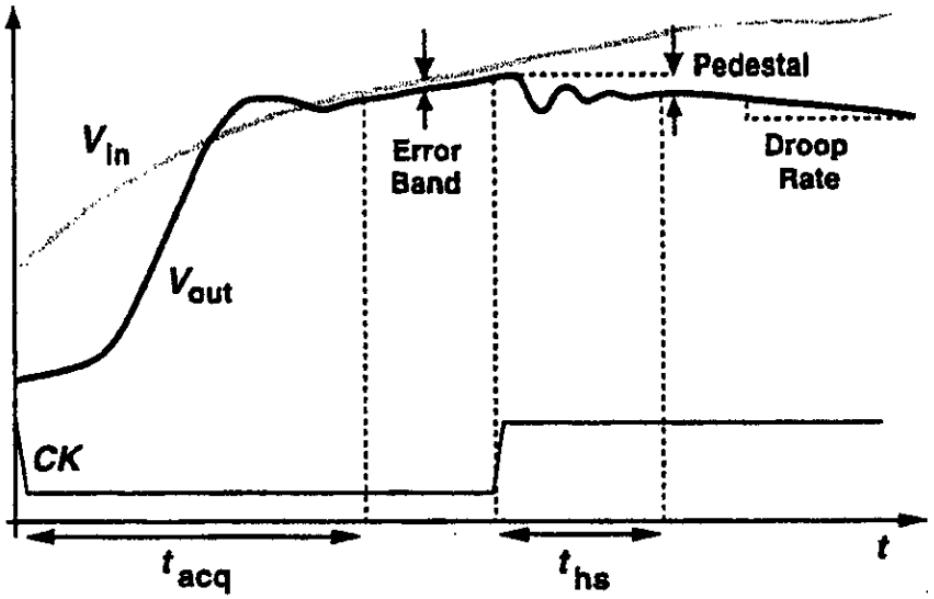
$$Y_a(f) = \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} X(f - \frac{n}{T_S})$$

$$Y_b(f) = e^{-j\pi f T_S} \frac{\sin \pi f T_S}{\pi f T_S} \sum_{n=-\infty}^{+\infty} X(f - \frac{n}{T_S})$$

$$Y_c(f) = \sum_{n=-\infty}^{+\infty} e^{-jn\pi/2} \frac{\sin(n\pi/2)}{n\pi} X(f - \frac{n}{T_S})$$

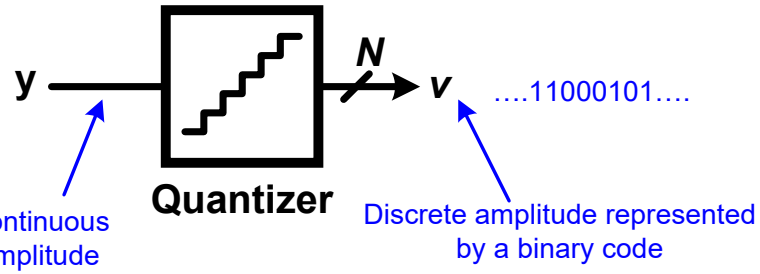
$$+ e^{-3j\pi f T_S/2} \frac{\sin(\pi f T_S/2)}{\pi f T_S} \sum_{n=-\infty}^{+\infty} X(f - \frac{n}{T_S})$$

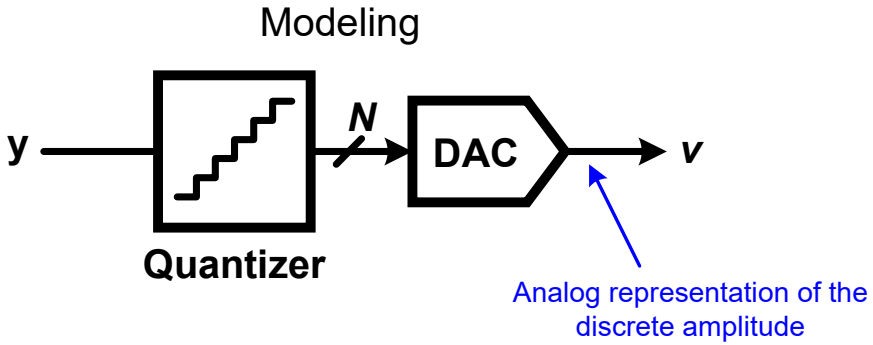
Various Non-Idealities in Sampling



- Acquisition-time
- Error band → defines accuracy of sampling
- Hold settling time
- Pedestal Error
- Droop rate
- Sampling clock uncertainty
  - Clock Jitter
- Non-linearity
- Thermal Noise

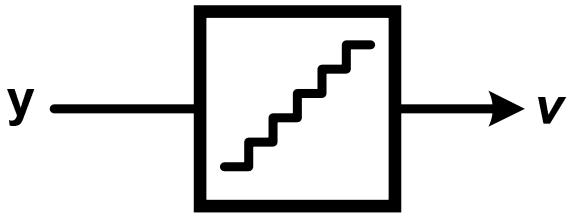
Quantization Basics

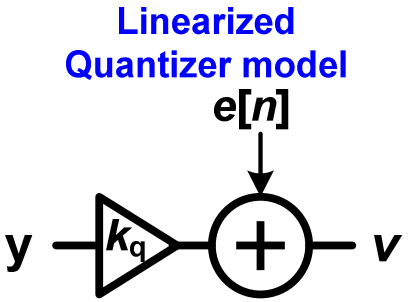




- **Quantization error/noise: e[n] = v[n]–y[n]**
- **Least significant bit (LSB): Δ**
- **Quantizer has non-linear input-output characteristics**
- **Exact analytical modeling is difficult**
  - **Use a simplified model**

Quantizer Modeling





- **Quantization noise modeling can be simplified with the assumptions**
  - **Input (y) stays within the no-overload input range**
  - **e[n] is uncorrelated with the input y**
  - **Spectrum of e[n] is white**
  - **Quantization noise is uniformly distributed**
- **Linearized quantizer model**
  - **Uniform Distribution of Noise**
- **Quantization noise power:** $\sigma_e^2 = \frac{\Delta^2}{12}$
- ***SQNR* = 6.02· *N* + 1.76**

Performance Metrics of ADC

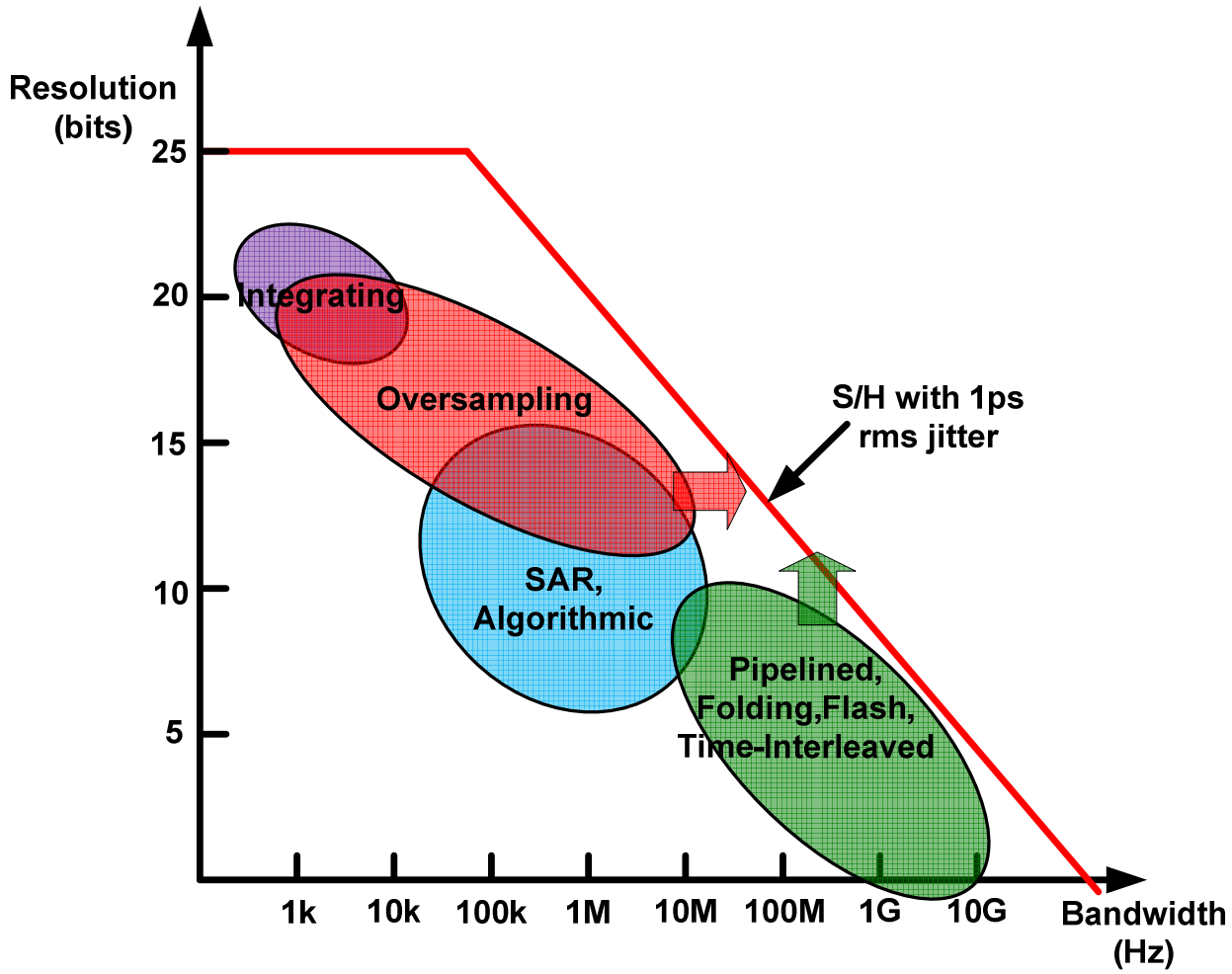
- **Static Performance Metric**
  - Offset error
  - Gain error
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)
  - Monotonicity

- **Dynamic Performance Metric**
  - Signal-to-Quantization Noise Ratio (SQNR)
  - Signal-to-Noise Ratio (SNR) ➔ quantization + thermal noise
  - Spurious Free Dynamic Range (SFDR)➔ For an N-bit quantizer

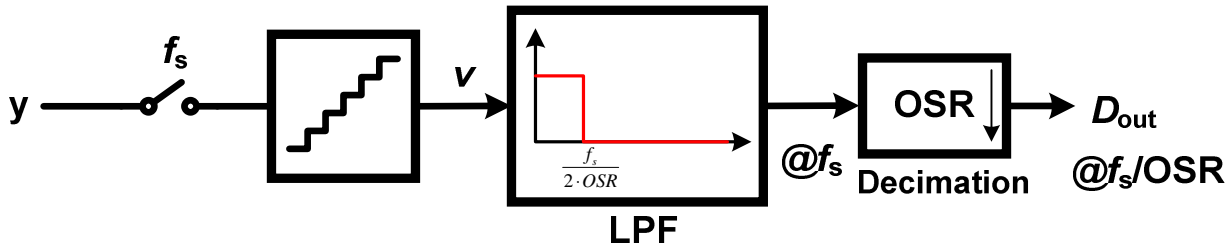
$$SFDR = 9.03N + 0.91 \ (dB) \text{ for } N < 4\text{-bits},$$
$$SFDR = 8.07N + 3.29 \ (dB) \text{ for } N > 4\text{-bits}.$$

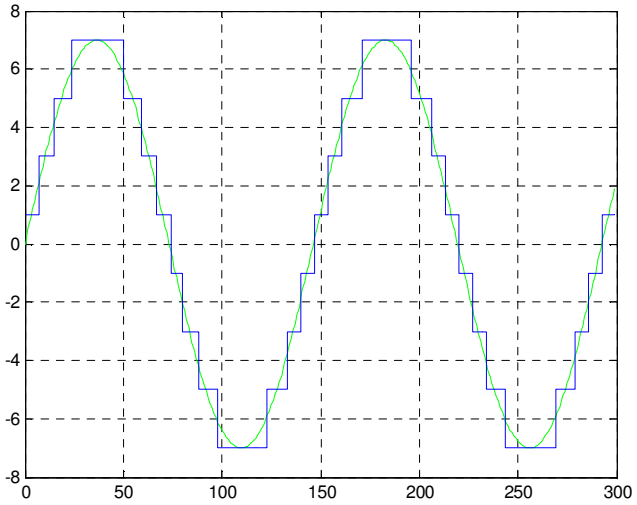
  - Signal-to-Noise + Distortion Ratio (SNDR)
  - Effective Number of Bits (ENOB)➔ (SNDR-1.76)/6.02
  - Total Harmonic Distortion (THD)
  - Figure-of-Merit (FoM) ➔ Power/($2f_{in,max}\ 2^{ENOB}$) Joules/conv-step

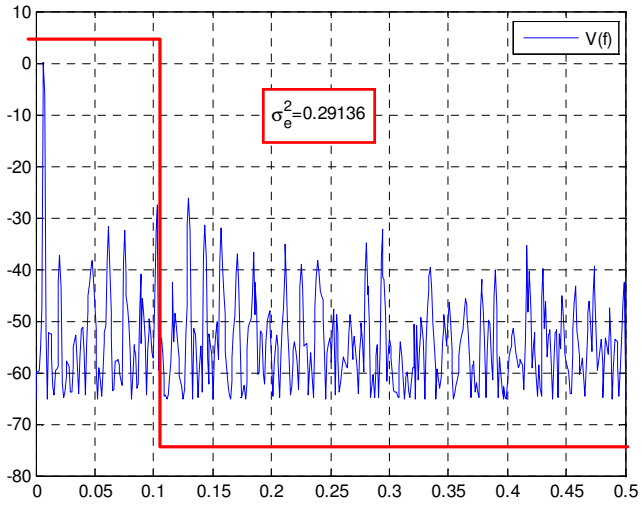
Analog to Digital Converter Architectures



Oversampling

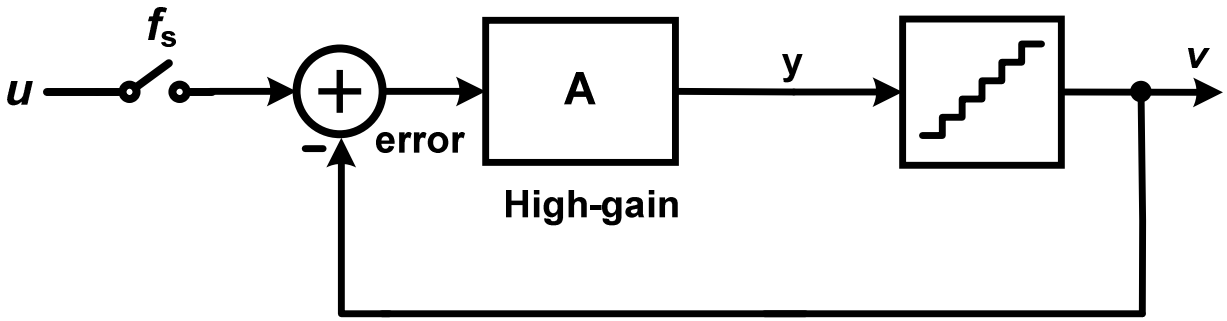






- Oversampling ratio (*OSR*)
- Conversion bandwidth: $f_B = f_s/2 \cdot OSR$
- $SQNR = 6.02 \cdot N + 1.76 + 10 \cdot \log_{10}(OSR)$
- 0.5 bits increase in resolution per doubling in OSR

Oversampling with Feedback

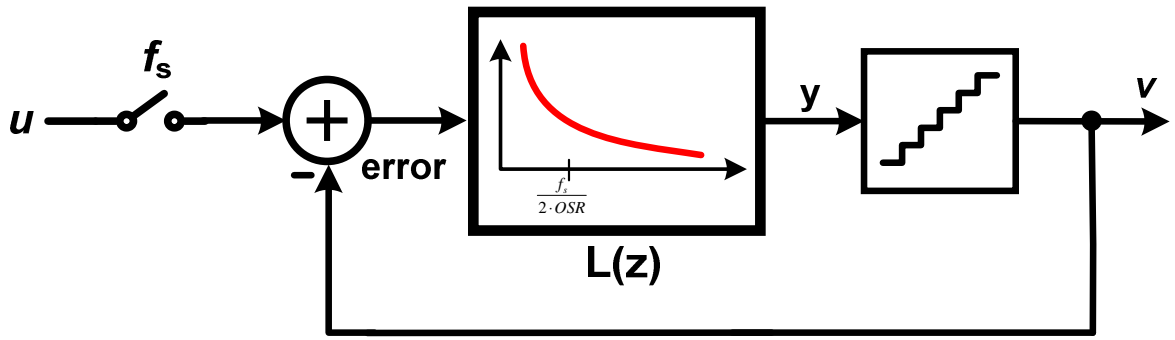


- Can we use feedback with high loop-gain ($A \cdot k_q$) to reduce the error e=|u-v| ?
- Since quantizer output can not be equal to the input

$$A \cdot k_q \to \infty \Rightarrow e = |u - v| \to \infty$$

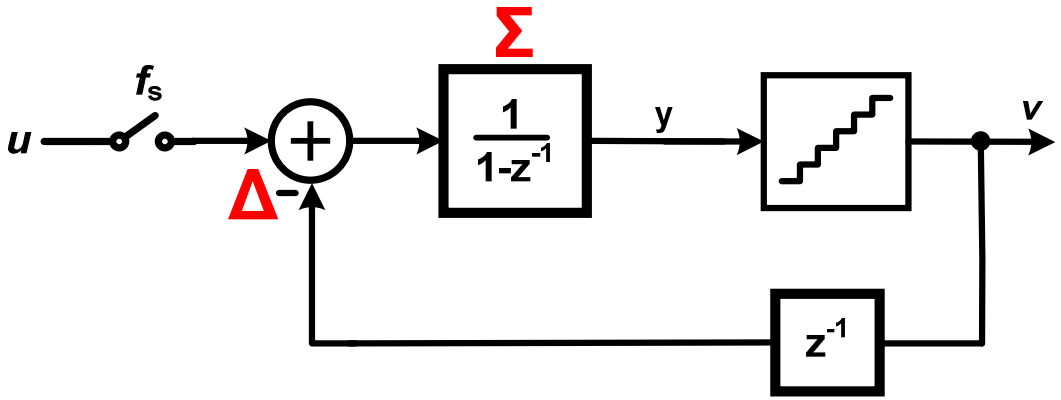
- The loop will be unstable as the error gets unbounded

Oversampling with Feedback



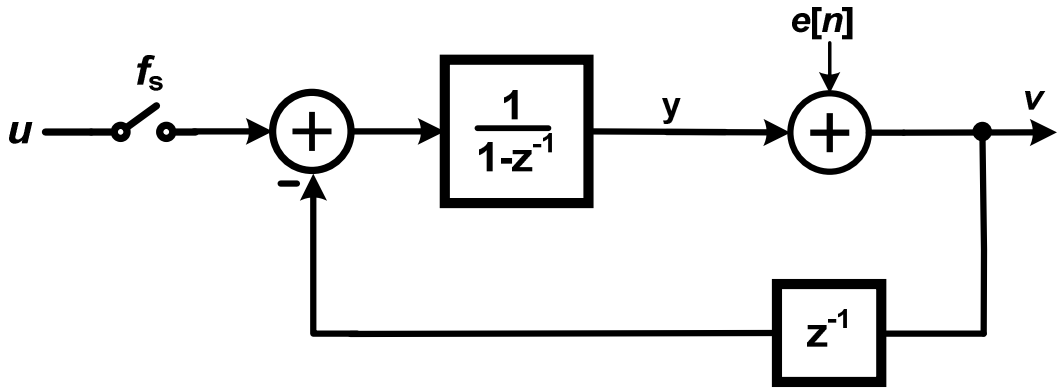
- Use large loop-gain in the signal band and small loop-gain at higher frequencies
- At low frequencies $e = |u - v| \rightarrow 0$
- At high frequencies, low loop-gain stabilizes the loop
- *L*(*z*) is the loop-filter
- This feedback arrangement is called a (noise) modulator

First-order Modulator



- **Differencing (Δ) followed by an accumulator (Σ)**
  - **ΔΣ modulator**
- **At low frequencies** $e = |u - v| \rightarrow 0$

First-order Noise Shaping



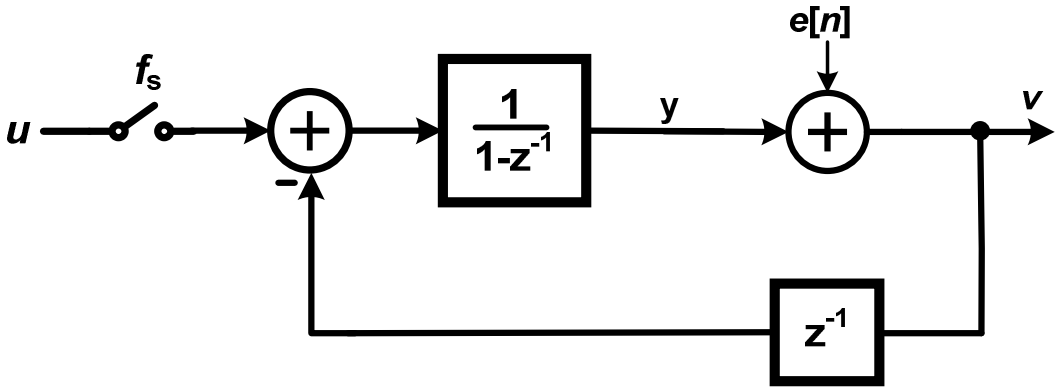
- **Linearized model for the modulator**

$$V(z) = \boxed{z^{-1}} U(z) + \boxed{\left(1 - z^{-1}\right)} E(z)$$

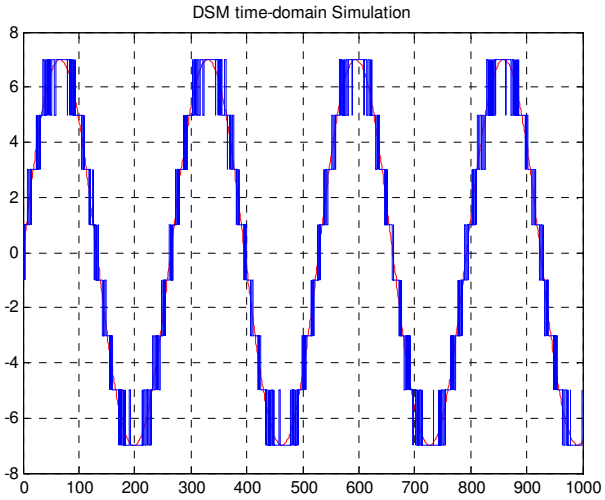
STF NTF

- **Noise transfer function (NTF)**
  - **$(1-z^{-1})$: first-order differentiator**
  - **High-pass shaping of quantization noise**
- **Signal transfer function (STF)**
  - **Unit delay**

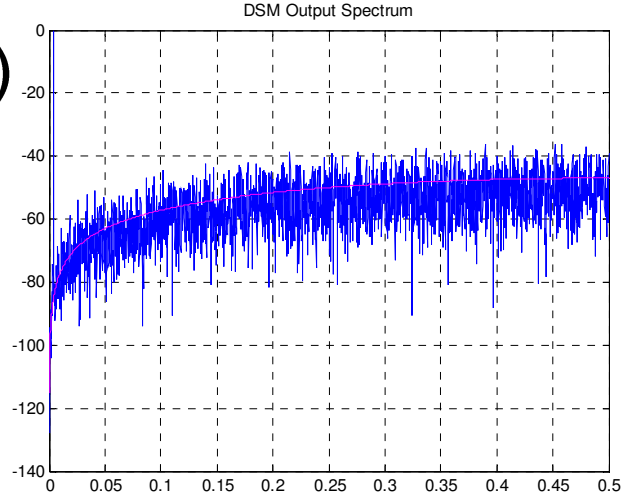
First-order ΔΣ Modulator



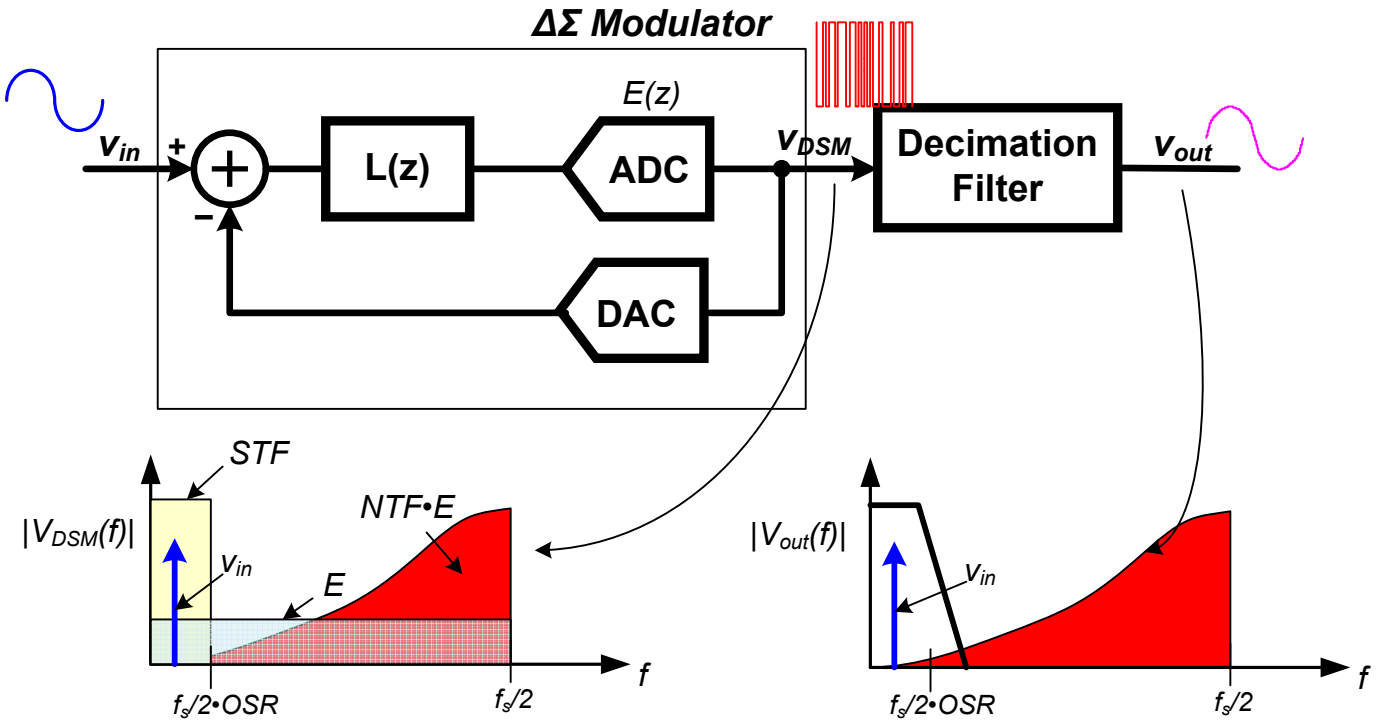
v[n]



$S_V(f)$

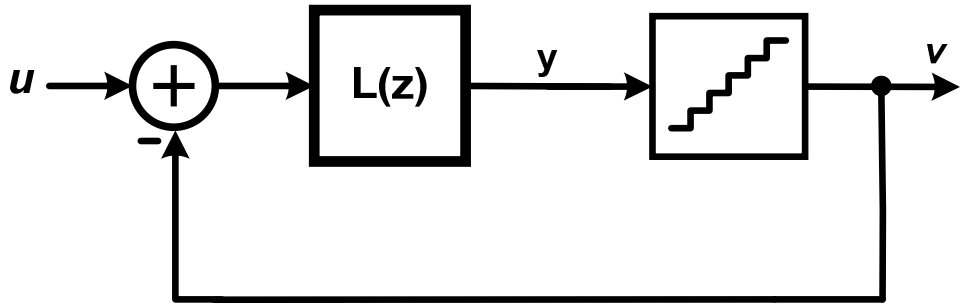


Delta-Sigma (ΔΣ) ADC



- **Use oversampling (f_s=2·*OSR*·*BW*) to shape the quantization noise out of the signal band**
- **Use low-resolution ADC and DAC to get much higher resolution**
- **Digitally filter out the out-of band shaped (modulated) noise**
- **Trades-off SQNR with oversampling ratio (OSR)**

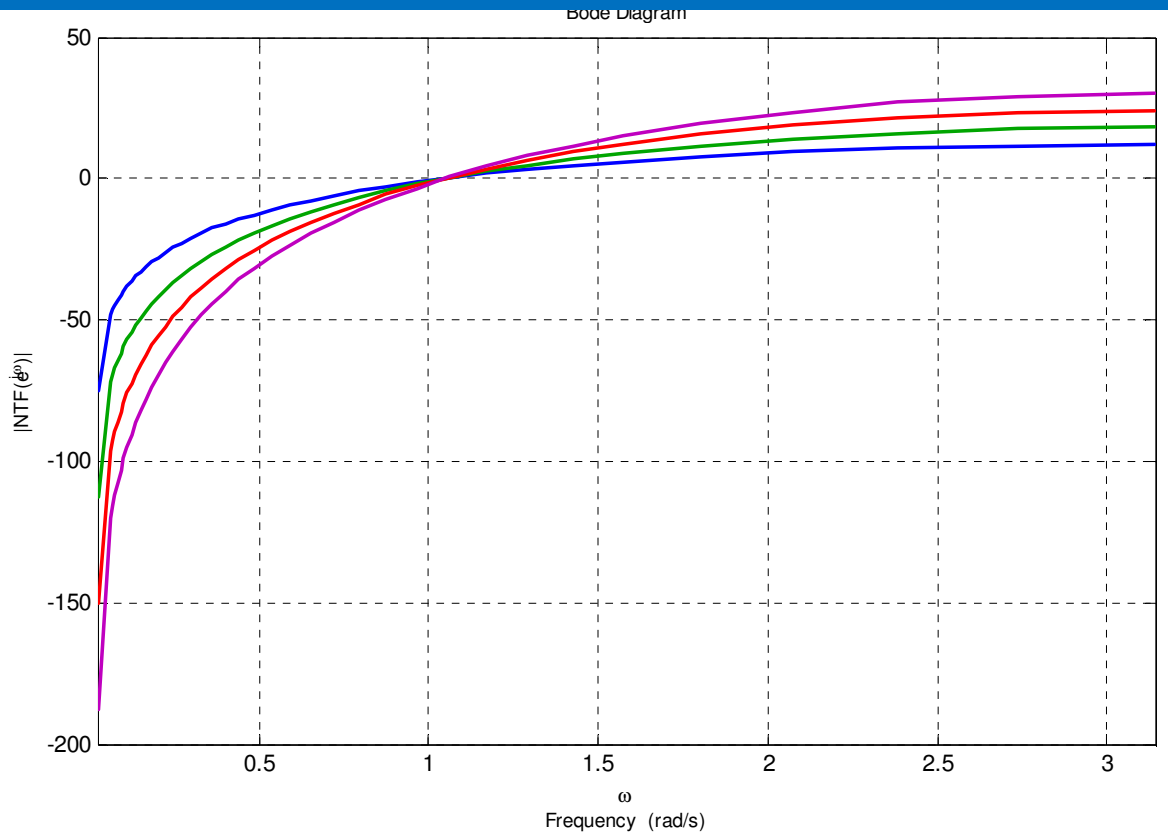
Higher-Order NTFs



$$V(z) = \underbrace{\frac{L(z)}{1+L(z)}}_{\text{STF}} U(z) + \underbrace{\frac{1}{1+L(z)}}_{\text{NTF}} E(z)$$

- **Higher order noise shaping**
  - **Reduced in-band noise, higher SQNR**
- **For *NTF*=(1-z^{-1})$^{-N}$, in-band noise (IBN):** $\frac{\Delta^2}{12} \cdot \frac{\pi^{2N}}{(2N+1)} \cdot OSR^{-(2N+1)}$
  - **Ideally (N+1/2) bits increase in resolution per doubling in OSR**

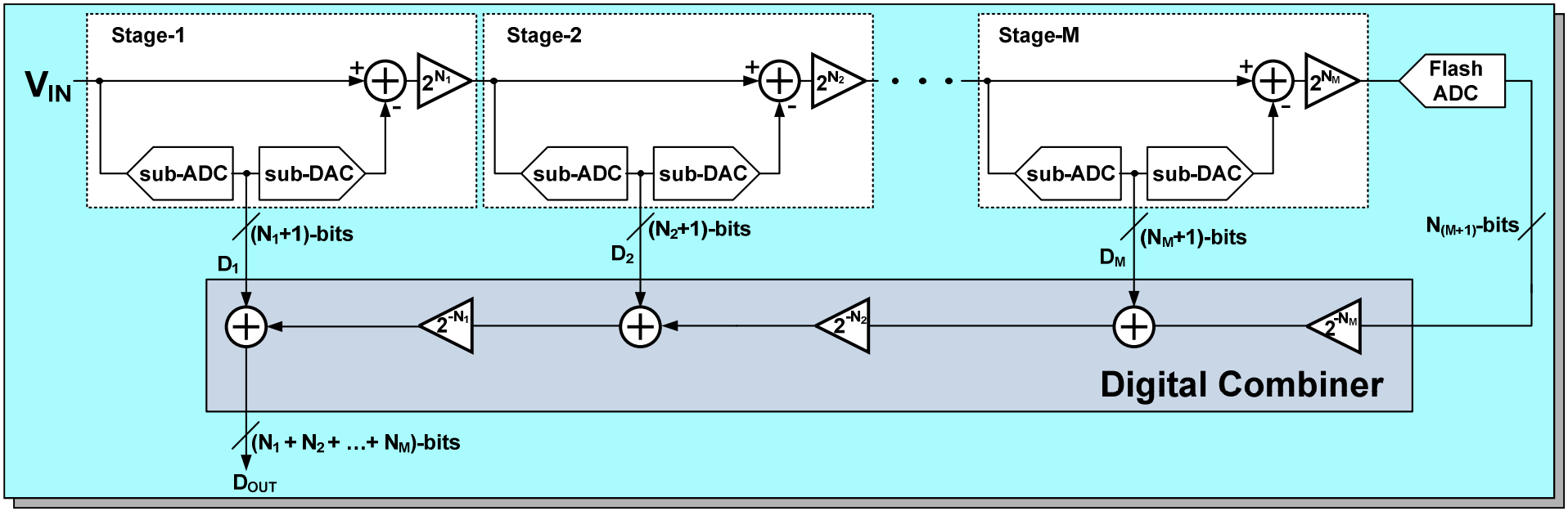
Higher-Order NTFs



- **NTF gain increases at high frequencies (around ω≈π)**
- **Can we go on increasing the order? The loop becomes unstable resulting in oscillation.**

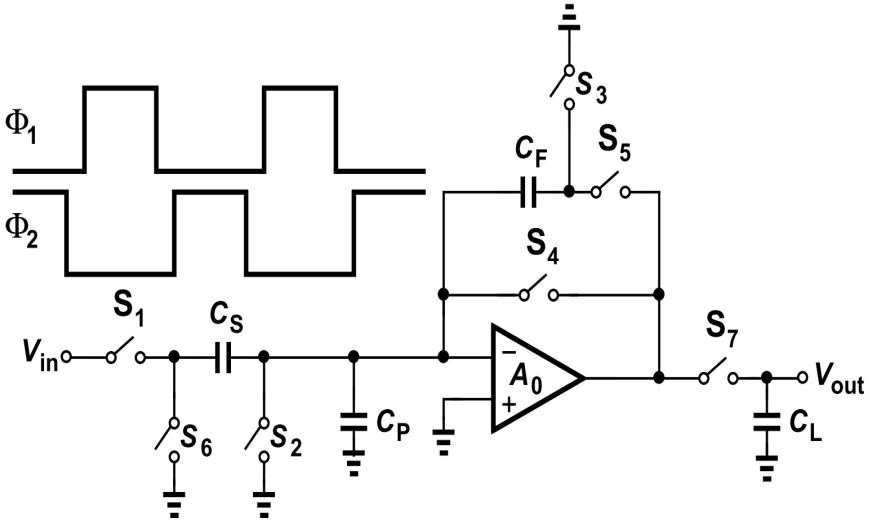
Pipelined ADC
- An Overview -

Generic Pipelined ADC



- Each stage resolves a small number of bits (i.e. N_1, N_2, …, N_M bits).
- The overall resolution of the ADC is $P = (N_1+N_2+\ldots+N_M+N_{M+1})$.
- Output of stage-i (called "residue" r_i) is digitized to $(P-\Sigma^{i}_{j=1} N_j)$-bits.
- The low resolution ADC digitizing r_i is called the backend of stage-i.

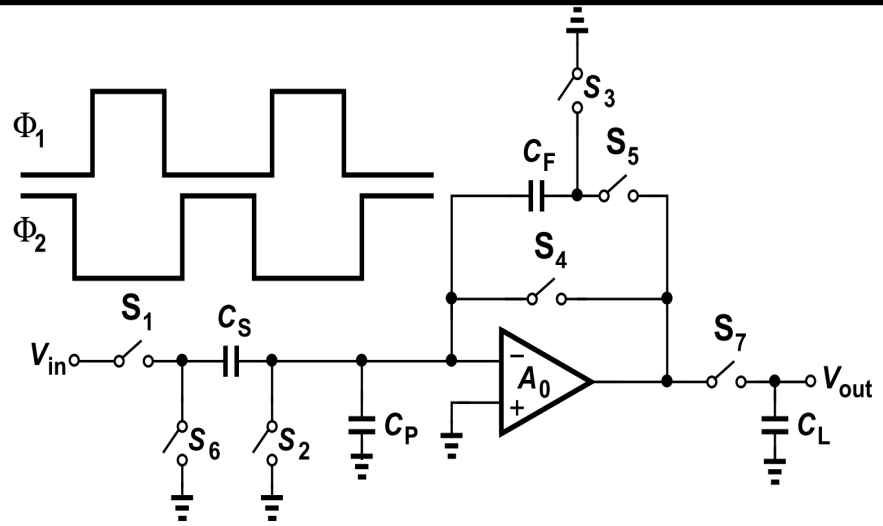
Switched-Capacitor (SC) Circuit – An Overview (1)

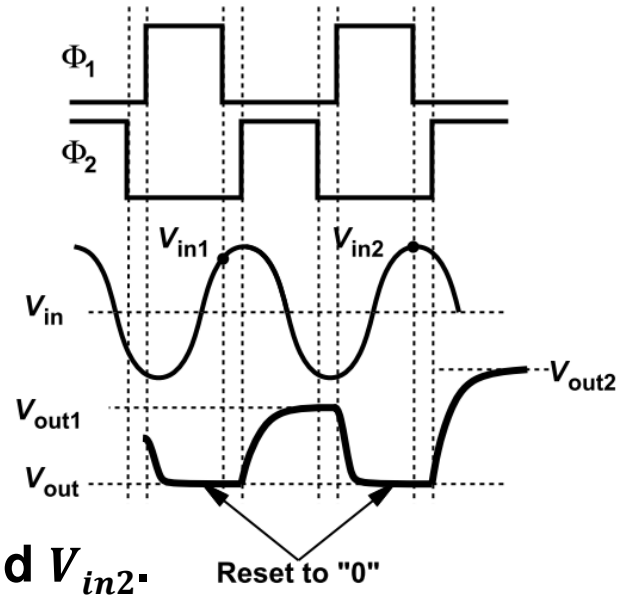


- **Key building blocks:**
  - **Switches**
  - **Capacitors**
  - **Op amp**
  - **Two-phase non-overlapping clock generator**

- **SC-Circuits function in charge domain.**
- **Sample/Reset phase ➔ Φ_1 is high ➔ Switches S_1 to S_4 are controlled by Φ_1, i.e. S_1 to S_4 close when Φ_1 is high.**
  - **It is called sample-phase as input signal is sampled.**
  - **It is also called reset-phase as op amp is reset (more later).**
- **Hold/Amplification phase➔ Φ_2 is high ➔ Switches S_5 to S_7 are controlled by Φ_2, i.e. S_5 to S_7 close when Φ_2 is high.**
  - **V_{out} is an amplified and held version of the sampled V_{in}.**

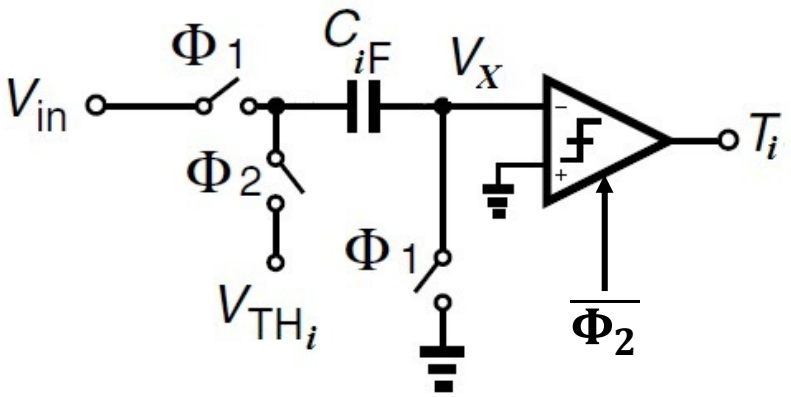
Switched-Capacitor (SC) Circuit – An Overview (2)

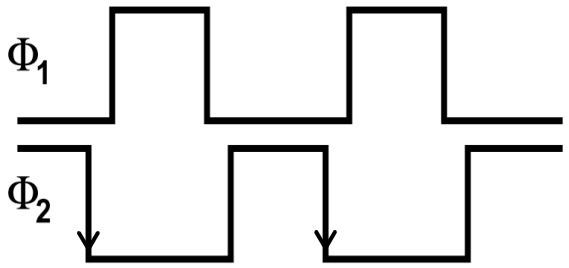




- Falling edge of Φ_1 samples the input, V_{in1} and V_{in2}.
- In Φ_2 the sampled values get amplified to give V_{out1} & V_{out2}, respectively.
- During Φ_1 the sampled charge is $Q_S = C_S V_{in}$.
- During Φ_2 the charge is $Q_H = C_F V_{out}$.
- Since charge is conserved, $Q_S = Q_H \Rightarrow V_{out} = \frac{C_S}{C_F} V_{in}$.
- The gain of the circuit is the ratio of the sampling capacitor (C_S) to feedback capacitor (C_F).

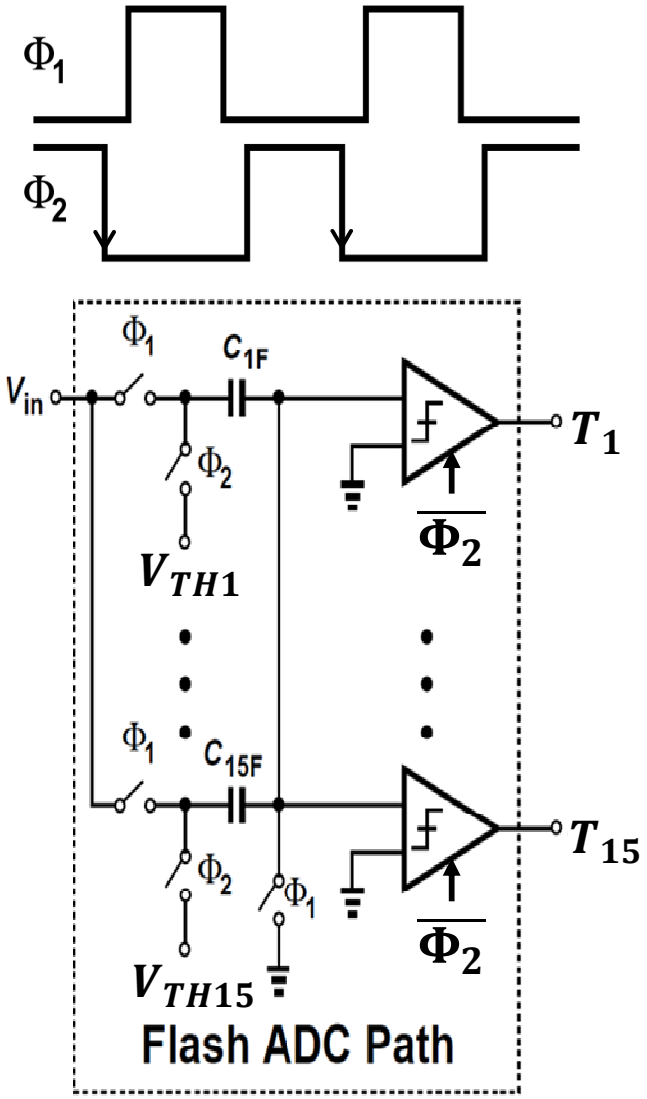
Switched-Capacitor Comparator





- During Φ_1 the sampled charge $Q_S = C_{iF}V_{in}$.
- Since charge is conserved the charge during Φ_2 is given by $Q_H = C_{iF}(V_{THi} - V_X)$ resulting in $V_X = V_{in} - V_{THi}$.
- When the comparator is clocked with the falling edge of Φ_2 it makes a decision based on whether $V_{in} > V_{THi}$ or $V_{in} < V_{THi}$.

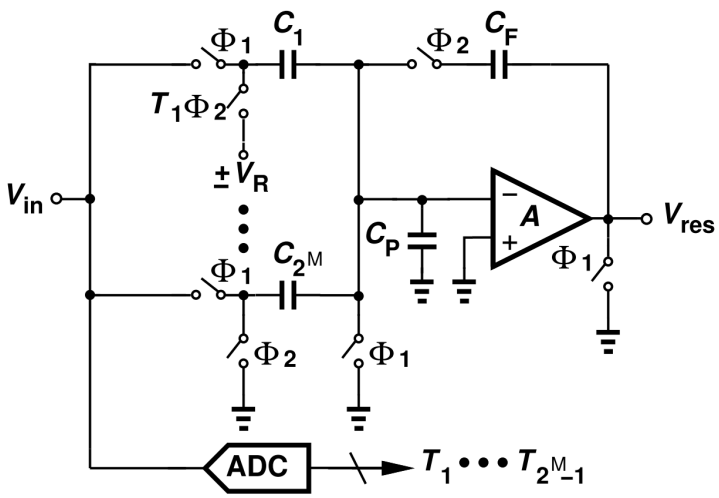
Switched-Capacitor 4-bit Flash

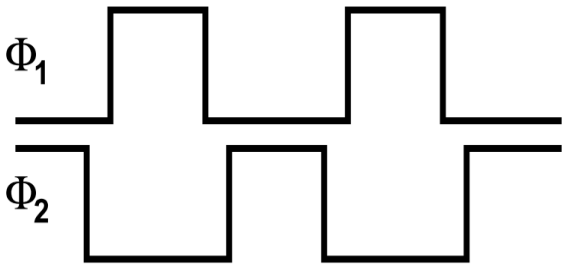


- A 4-bit flash incorporates 15 switched capacitor comparators.
- The threshold voltages V_{TH1} to V_{TH15} are generated by a resistor ladder comprising of 16 equal resistors.
- The outputs of the comparator give a 15-bit wide thermometer code which controls the DAC of the MDAC.
- The thermometer code is converted to 4-bit binary code using an on-chip look-up table, also called read-only-memory (ROM).

Note: A switched capacitor N-bit flash would incorporate 2^{N-1} switched capacitor comparators and a resistor ladder comprising 2^N resistors to generate the 2^{N-1} threshold voltages, V_{TH1} to $V_{TH2^{N-1}}$.

Switched-Capacitor MDAC (1)

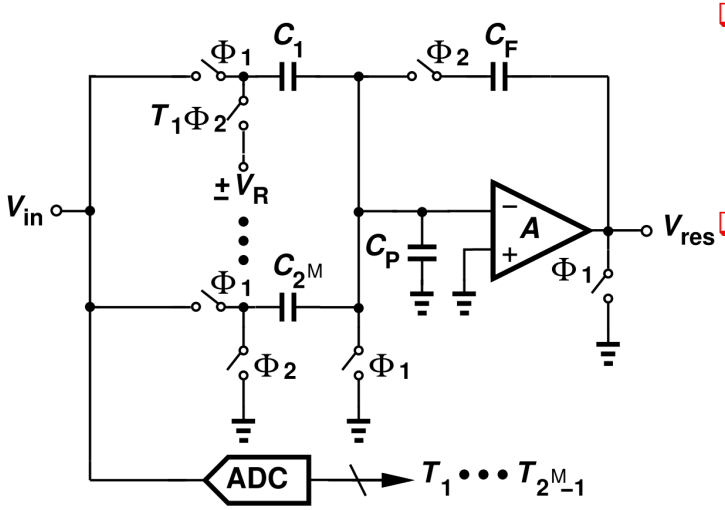


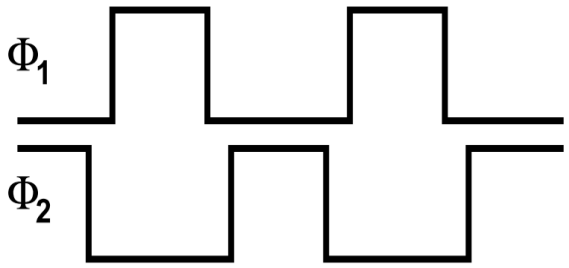


- An M-bit MDAC incorporates 2^M unit capacitors (C_i , i=1 to 2^M), feedback capacitor C_F, switches, and an op amp.
- This block does the following operations:
  - Φ_1 is high (Sample phase/Reset phase):
    - Sampling of input
  - Φ_2 is high (Amplification phase):
    - Digital-to-Analog Conversion (DAC)
    - Subtraction ➔ quantization noise generation
    - Amplification (Multiplying) ➔ scaling of the quantization noise to the full-scale for the later stages to digitize to relax the sensitivity requirements of the later stage circuits.

Note: A switched capacitor 4-bit flash would incorporate 2^4 unit capacitors.

Switched-Capacitor MDAC (2)





- During sample phase the sampled charge is,

$$Q_s = \sum_{i=1}^{2^M} C_i V_{in}$$

- During amplification phase the charge is given by,

$$Q_a = \sum_{i=1}^{2^M-1} T_i C_i V_R + C_F V_{res}$$

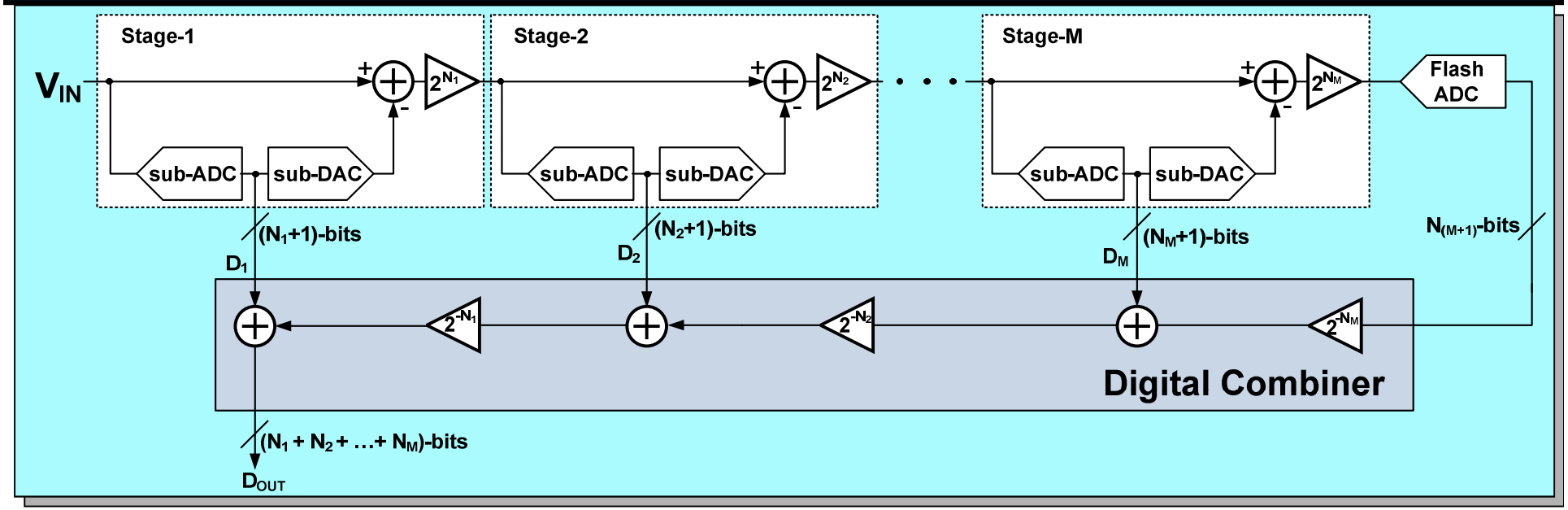
- By conservation of charge we get,

$$V_{res} = \frac{\sum_{i=1}^{2^M} C_i V_{in} - \sum_{i=1}^{2^M-1} B_i C_i V_R}{C_F}$$

where, B_i=1 if T_i=1 and B_i=–1 if T_i=0.

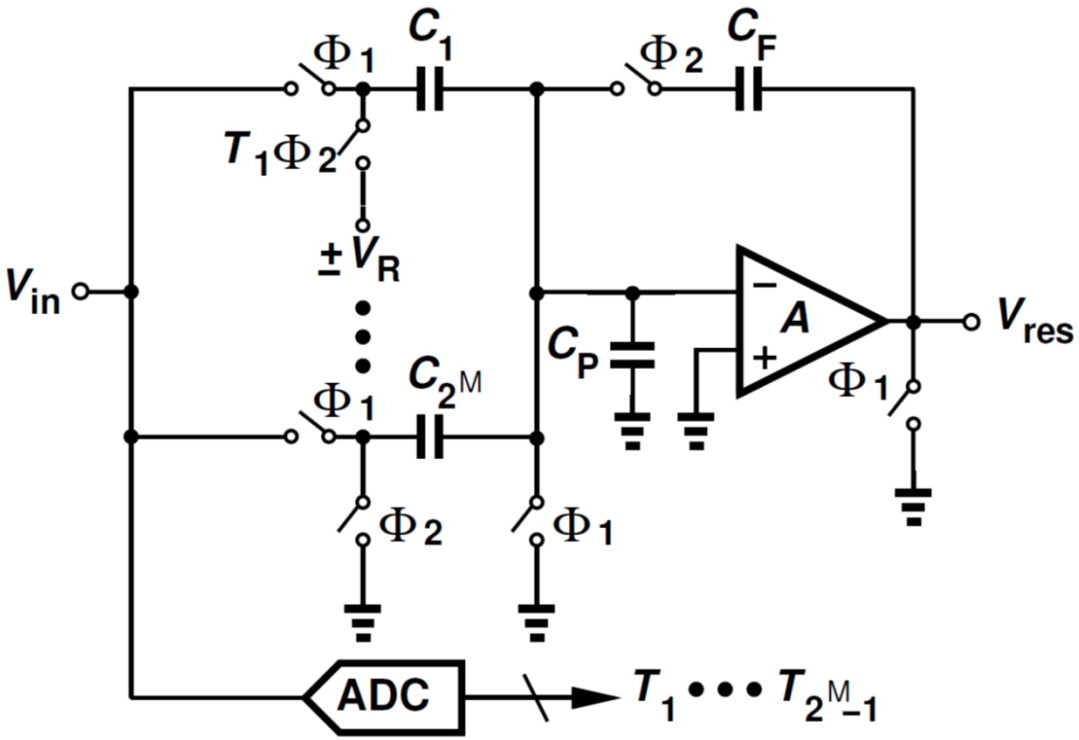
- If $C_F = C_i$ then gain $\approx 2^M$, if $C_F = 2C_i$ then gain $\approx 2^{M-1}$.

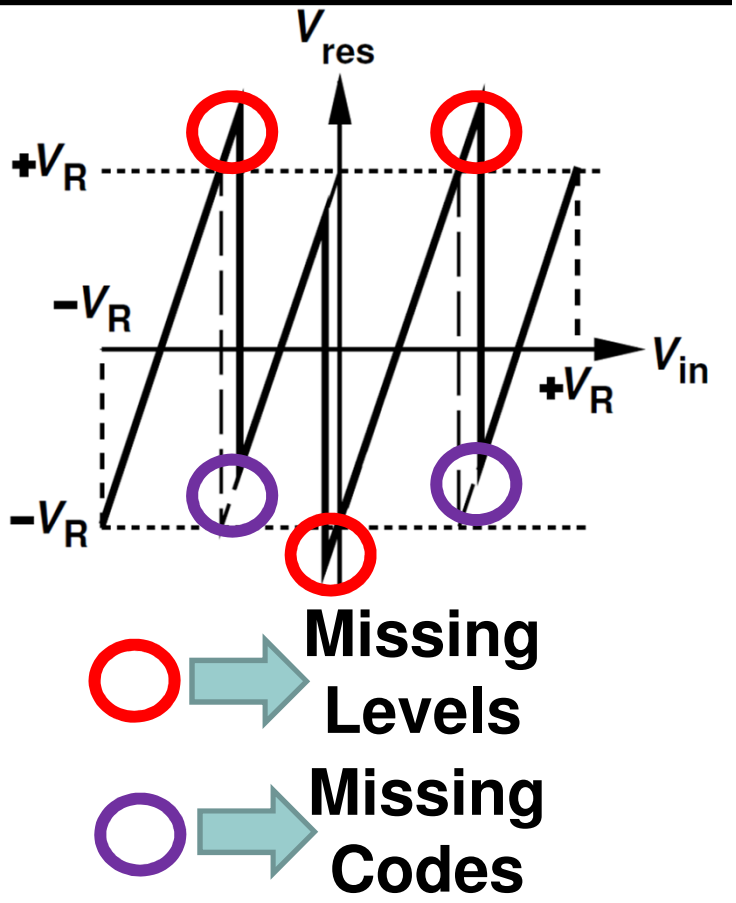
Sources of Errors in Pipelined ADC



▪ Comparator Offset	▪ Op Amp Nonlinearity
▪ Capacitor Mismatch	▪ Op Amp Offset
▪ Op Amp Gain	▪ Charge Injection Mismatch
▪ Op Amp Input Capacitance	▪ Op Amp and kT/C Noise

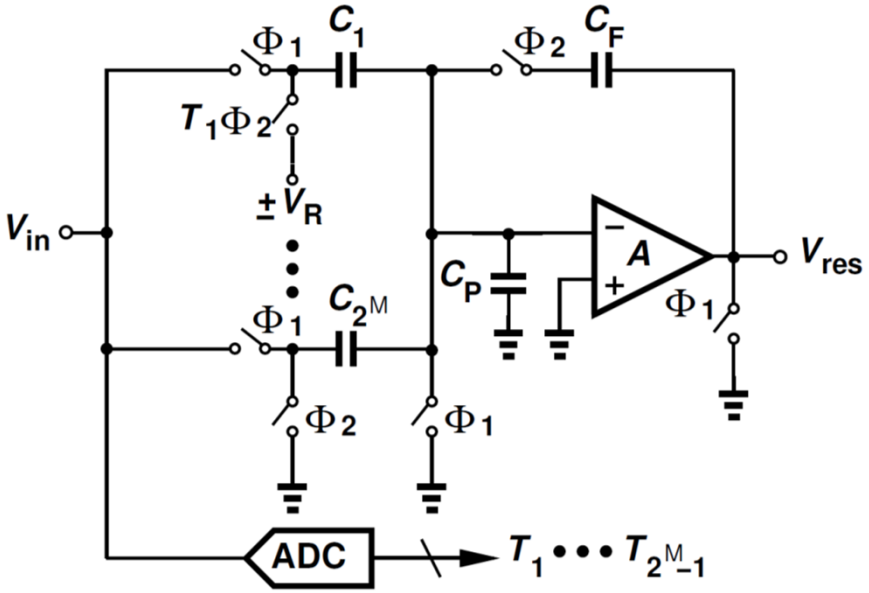
Comparator Offset

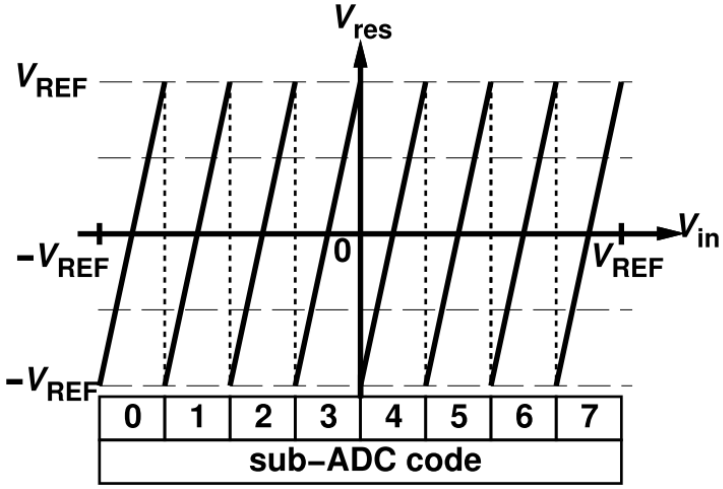




- **Comparator offset saturates the later stage.**
- **Redundancy can overcome this.**

Overcoming Comparator Offset (1)

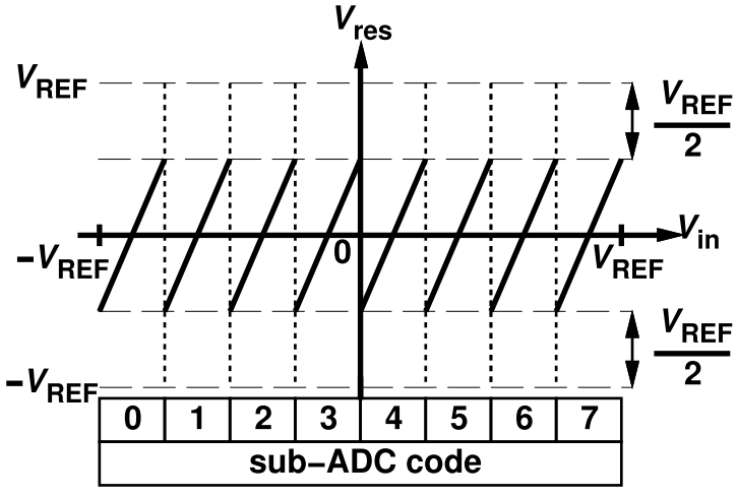




$C_F = C_i$, M=3 ➔ No redundancy

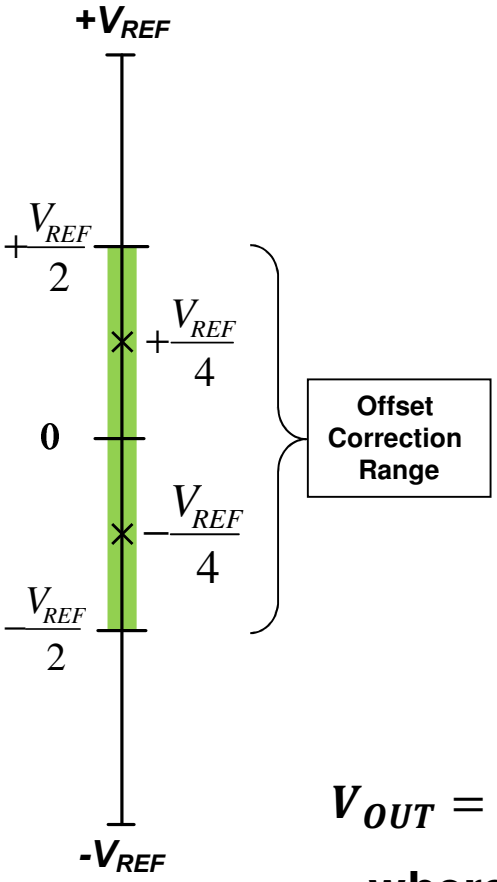
$$V_{res} = \frac{\sum_{i=1}^{2^M} C_i V_{in} - \sum_{i=1}^{2^M-1} B_i C_i V_R}{C_F}$$

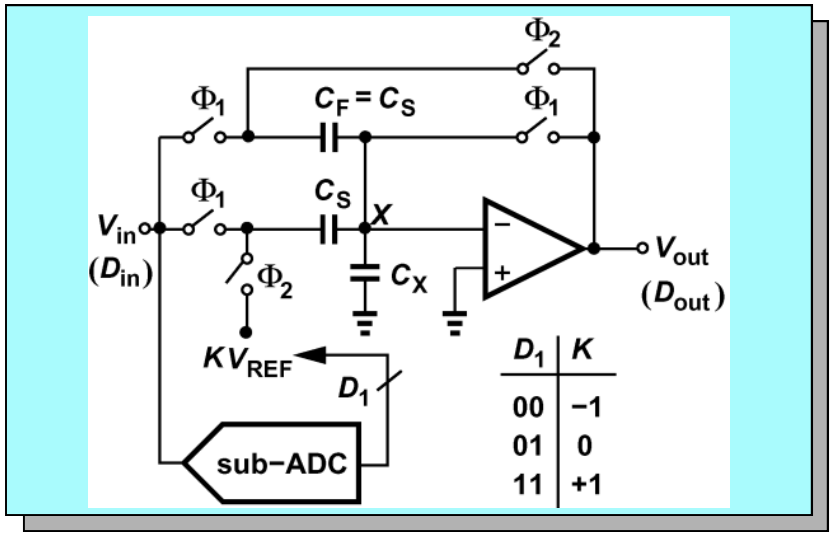
If $C_F = 2C_i$ then gain $\approx 2^{M-1}$ resulting in comparator offset tolerance of $\pm V_{REF}/2^M$.



$C_F = 2C_i$, M=3➔ Redundancy

Overcoming Comparator Offset (2) –1.5-bit Architecture–

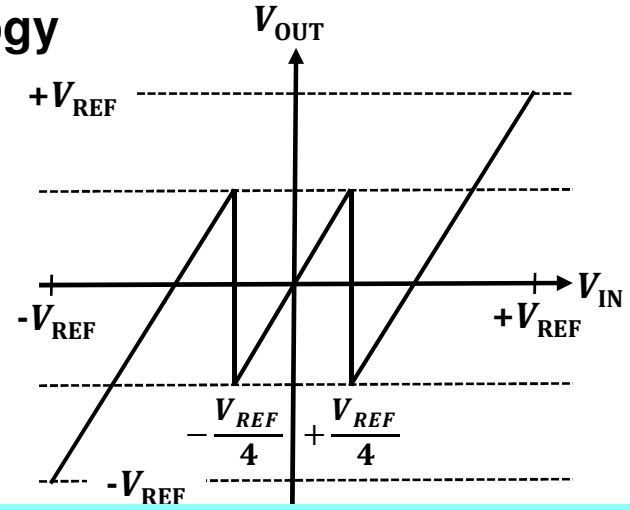




Flip-around Topology

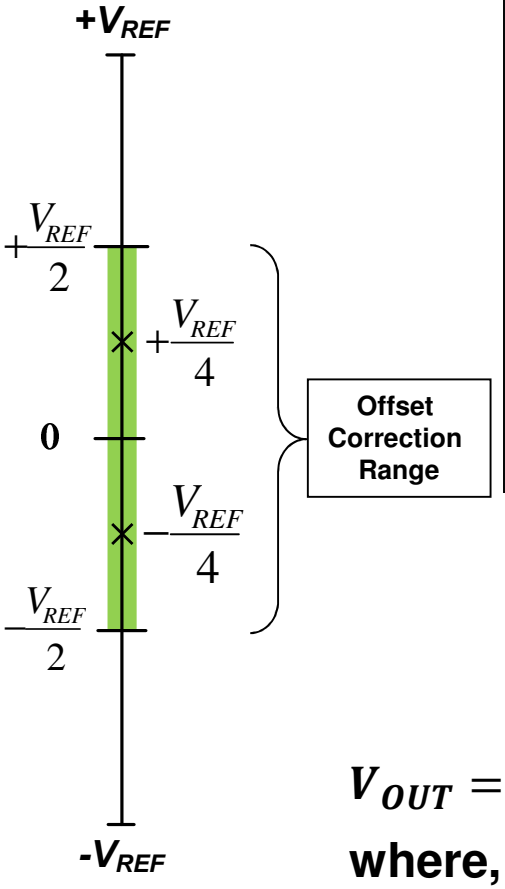
$$V_{OUT} = \frac{(C_S + C_F)V_{IN} - kC_SV_{REF}}{C_F}$$

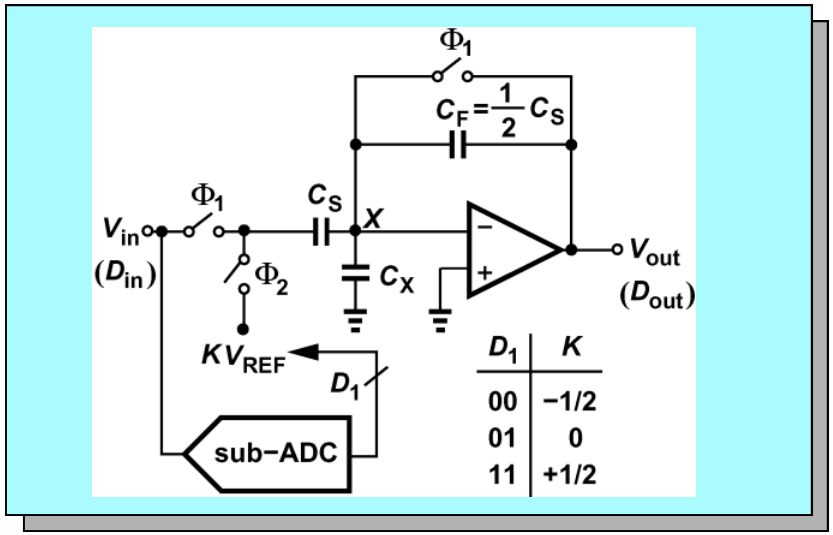
where, $k = \pm 1, 0$



Ref: S. Lewis et al, "A 10-b 20-MS/s Analog-to-Digital Converter," *IEEE JSSC.*, pp. 351-358, March 1992

Overcoming Comparator Offset (3)
–1.5-bit Architecture–

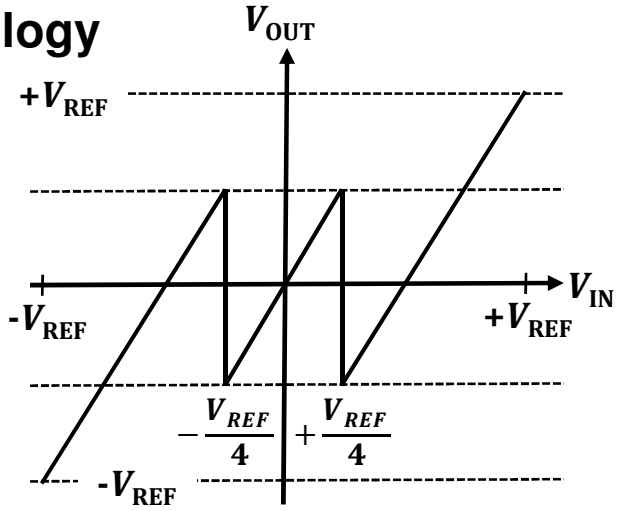




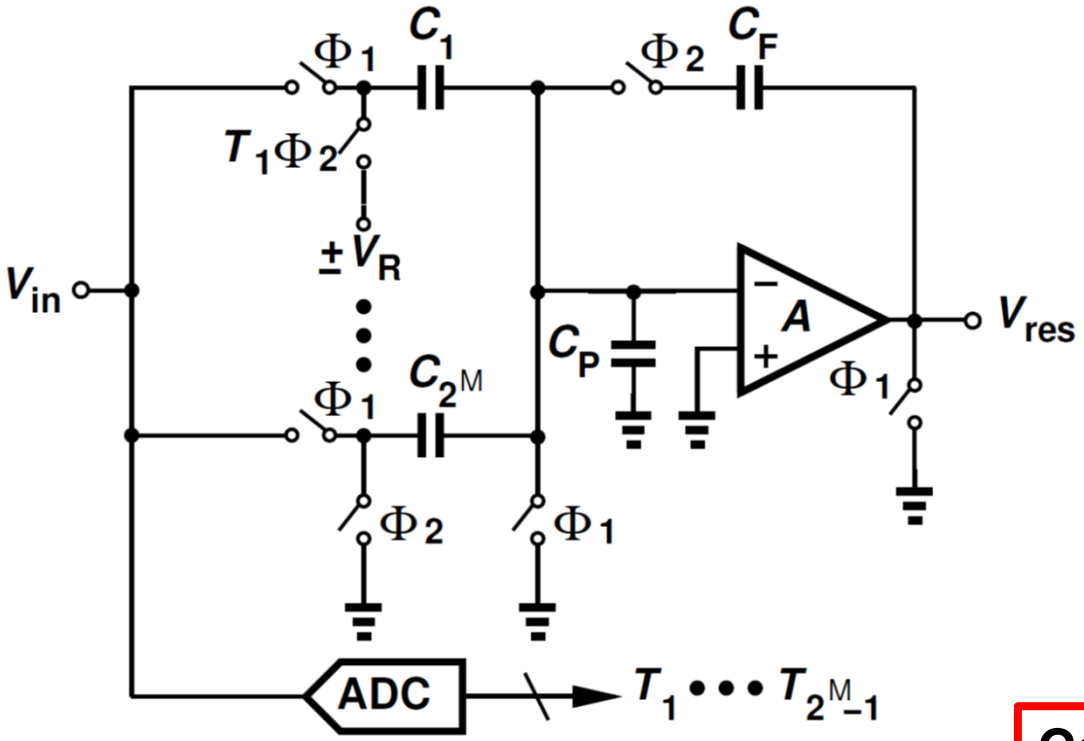
Non-Flip-around Topology

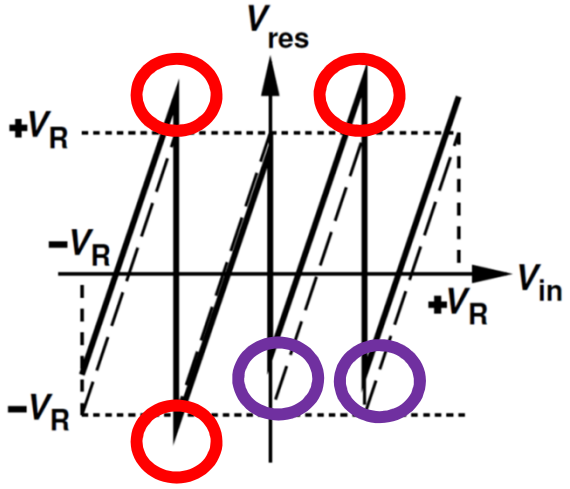
$$V_{OUT} = \frac{C_S}{C_F}(V_{in} - kV_{REF})$$

where, $k = \pm 1/2, 0$



Capacitor Mismatch





M=2, i.e., 2-bit stage

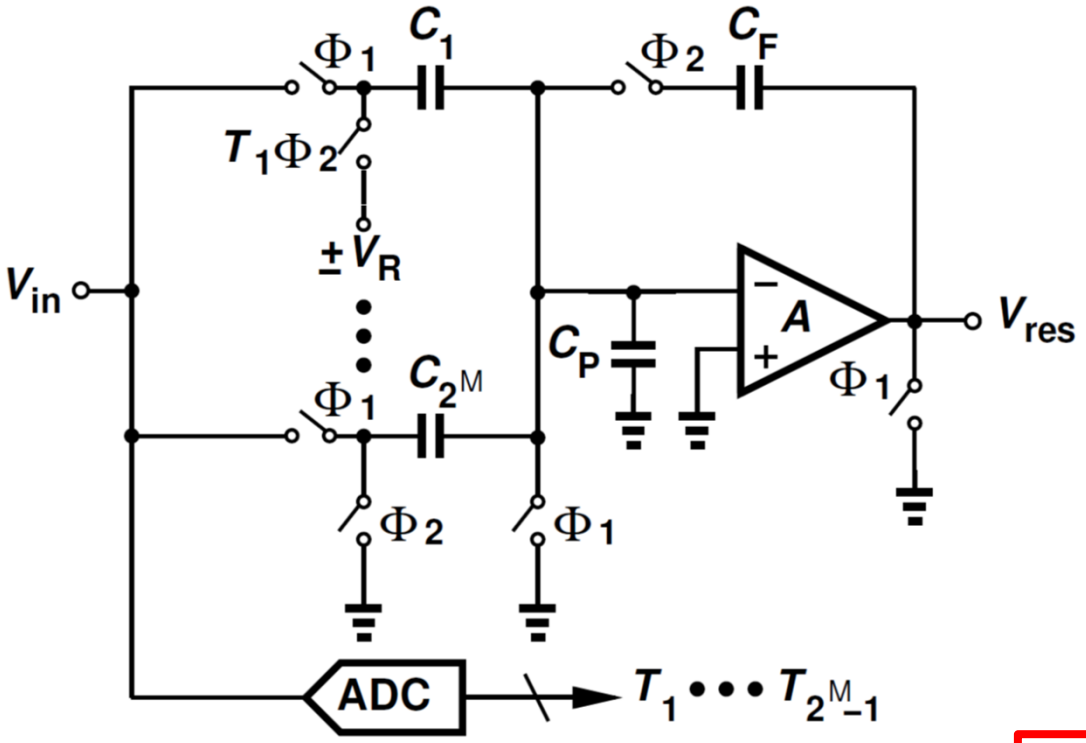
$$V_{res} = \frac{\sum_{i=1}^{2^M} C_i V_{in} - \sum_{i=1}^{(2^M-1)} B_i C_i V_{REF}}{C_F}$$

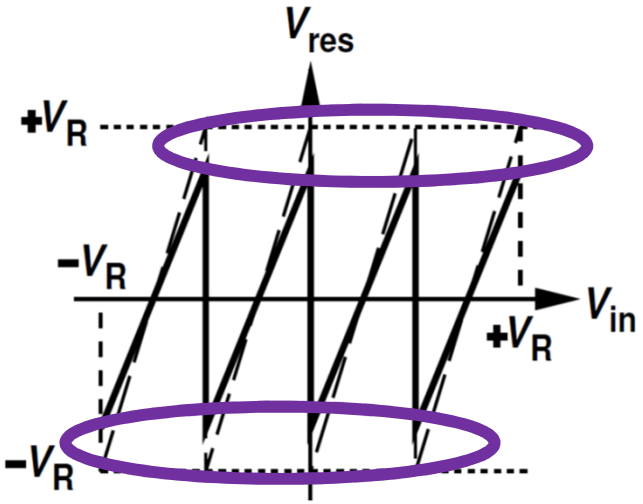
Capacitor mismatch

- Missing Levels
- Missing Codes

where, B_i=1 if T_i=1 and B_i=–1 if T_i=0

Finite Op amp Gain





M=2, i.e., 2-bit stage

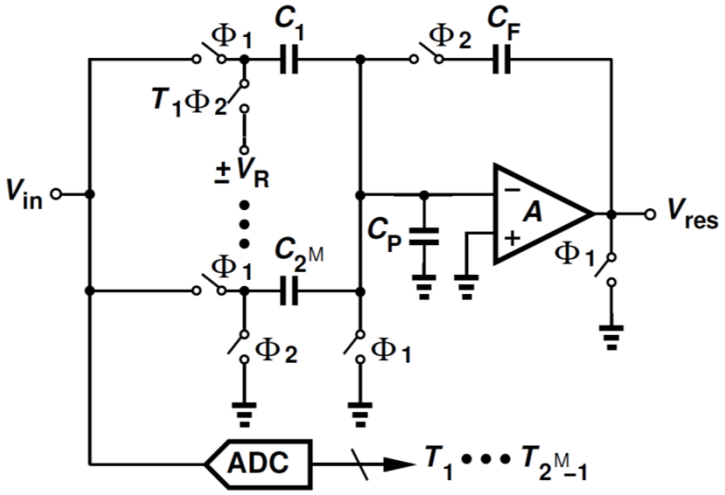
$$V_{res} = \frac{\sum_{i=1}^{2^M} C_i V_{in} + \sum_{i=1}^{(2^M-1)} B_i C_i V_{REF}}{C_F + \frac{\left(C_F + C_P + \sum_{i=1}^{2^M} C_i\right)}{A}}$$

Finite op amp gain → **Missing Codes**

where, B_i=1 if T_i=1 and B_i=–1 if T_i=0

and A=

Op amp Nonlinearity (1)



- **Weakly nonlinear op amp open-loop input-output characteristic can be given by a 3rd order polynomial,**

$$V_{OUT} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3$$

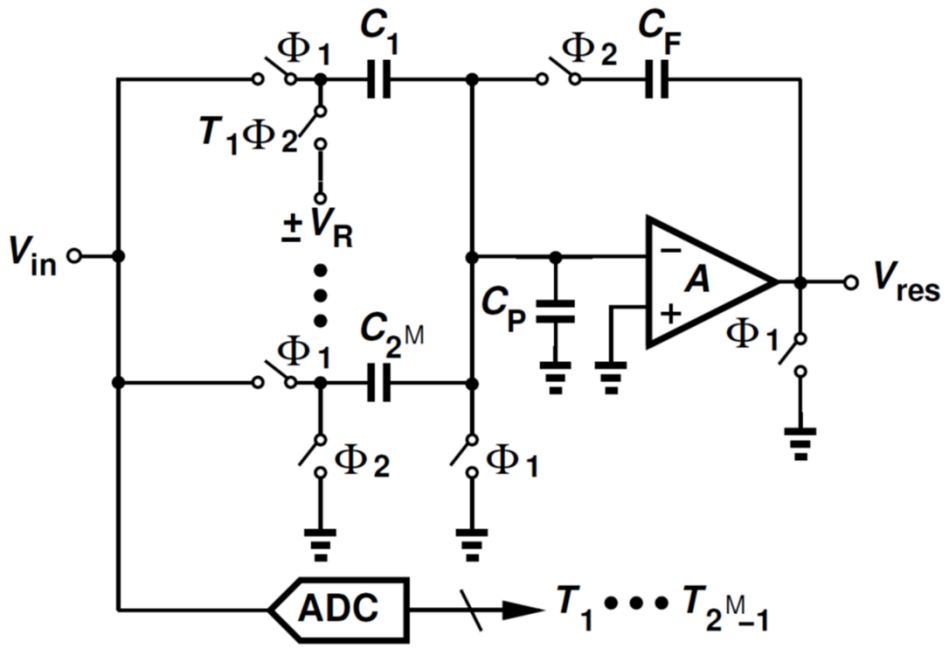
- **The inverse can be given by another polynomial**

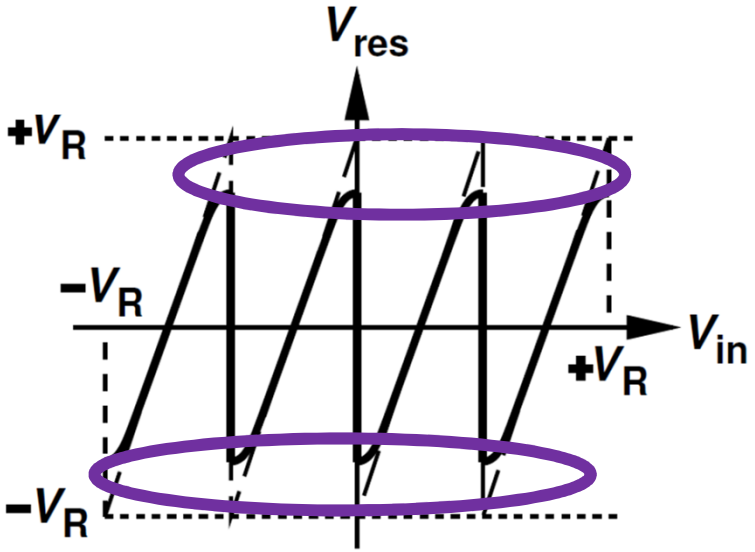
$$V_{in} = \beta_1 V_{out} + \beta_2 V_{out}^2 + \beta_3 V_{out}^3$$

where, $\beta_1 = \frac{1}{\alpha_1}$, $\beta_2 = \frac{-\alpha_2}{\alpha_1^3}$, **and** $\beta_3 = \frac{2\alpha_2^2}{\alpha^5} - \frac{\alpha_3}{\alpha_1^4}$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Op amp Nonlinearity (2)





M=2, i.e. 2-bit stage

Missing Codes

- **The input-output characteristic of the MDAC can be obtained by solving the following non-linear equation:**
  - $\sum_{i=1}^{2^M} C_i V_{in} = \sum_{i=1}^{(2^M-1)} C_i V_{REF} + C_F V_{res} - \left(\beta_1 V_{out} + \beta_2 V_{out}^2 + \beta_3 V_{out}^3\right)\left(C_F + C_P + \sum_{i=1}^{2^M} C_i\right)$

Thermal Noise Consideration (1)

- Signal-to-noise ratio of an ADC is given by,

$$SNR = 10log_{10}\left(\frac{P_{sig}}{(Q_N+N_T)}\right)$$

where,

  - P_{sig} = signal power = $\frac{V_{p-p}^2}{8}$ (for input $V_{in} = \frac{V_{p-p}}{2}sin(2\pi ft)$)
  - $Q_N = \frac{\Delta^2}{12}$,
  - N_T = Input referred thermal noise power of the ADC
  - $\Delta = \frac{V_{p-p}}{2^N}$, where N = ADC resolution.

- SNR of Semiconductor ADCs are limited by thermal noise of:
  - Switches
  - Op amps
- Switch thermal noise can be minimized by using large capacitors. The thermal noise of the switches is given by "kT/C", where $k = 1.38 \times 10^{-23}$, T =Temperature in K, and C is the sampling capacitor.
- Op amp thermal noise can be minimized by burning more current.

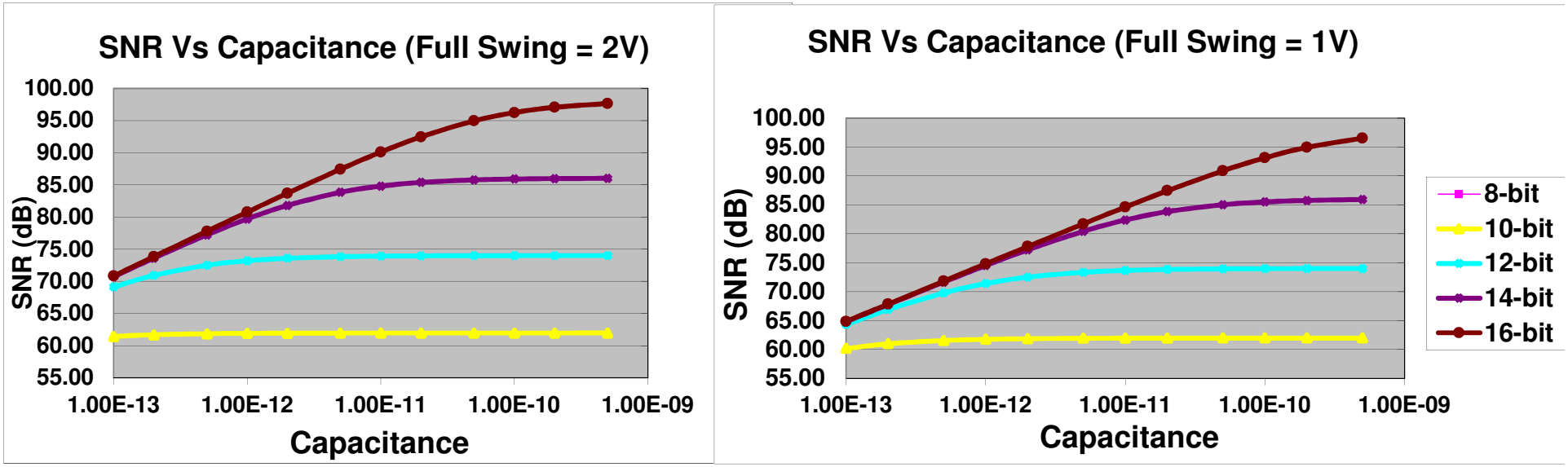
Thermal Noise Consideration (2)

- It is costly in terms of power, area, and speed to make input thermal noise smaller than quantization noise for ADC resolution, $N > 10$–bits.
- For example: If full-scale ADC input is 1 V, then for a 11-bit ADC the quantization noise power is given by:
- $Q_N = \frac{V_{LSB}^2}{12} = \frac{1}{12}\left(\frac{1}{2^{10}}\right)^2 = (141\mu V_{rms})^2$
- If thermal noise voltage power (N_T) is same as quantization noise power then the SNR takes a 3 dB hit.
- If SNR has to take < 1 dB hit then the $N_T \leq \frac{Q_N}{10}$.
- Size of the capacitor required to achieve this for 11 –bit system is $2\ pF$.
- For a 12-bit system the capacitor required would be $8\ pF$ (a large value).
- For a 16-bit system the capacitor size would be $2\ nF$ (almost physically unrealizable on chip).

Thermal Noise Consideration (3)

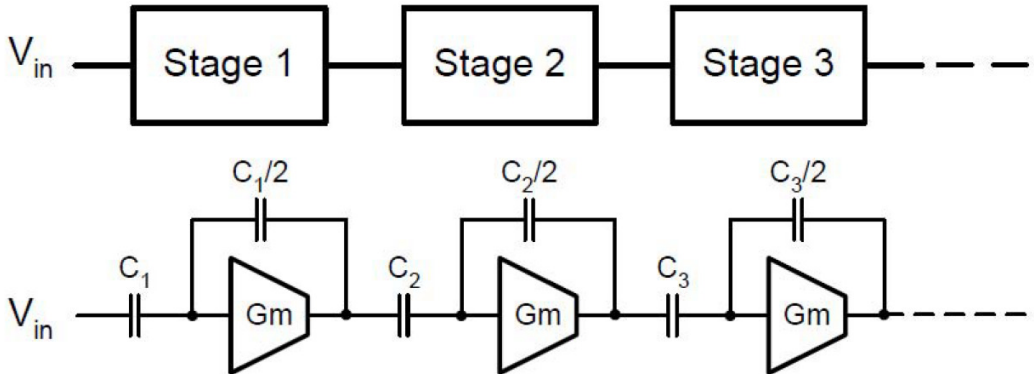
- **Ignoring other noise sources if thermal noise is only modeled by kT/C then the SNR if given by:**

$$SNR = 10log_{10}\left(\frac{P_{sig}}{\left(Q_N+\frac{kT}{C}\right)}\right)$$



Distribution of Thermal Noise

- Each stage contributes to the thermal noise.
- How do we distribute the thermal noise so that the overall input-referred thermal noise is minimized to maximize the SNR?
- Lets consider a pipelined ADC built using 1-bit stages (MDAC gain = 2)



- Considering only kT/C sampled noise the total input referred noise power:

$$N_T \propto kT\left[\frac{1}{C_1}+\frac{1}{G_1^2C_2}+\frac{1}{G_1^2G_2^2C_3}+\cdots+\frac{1}{G_1^2\cdots G_{N-1}^2C_N}\right]$$

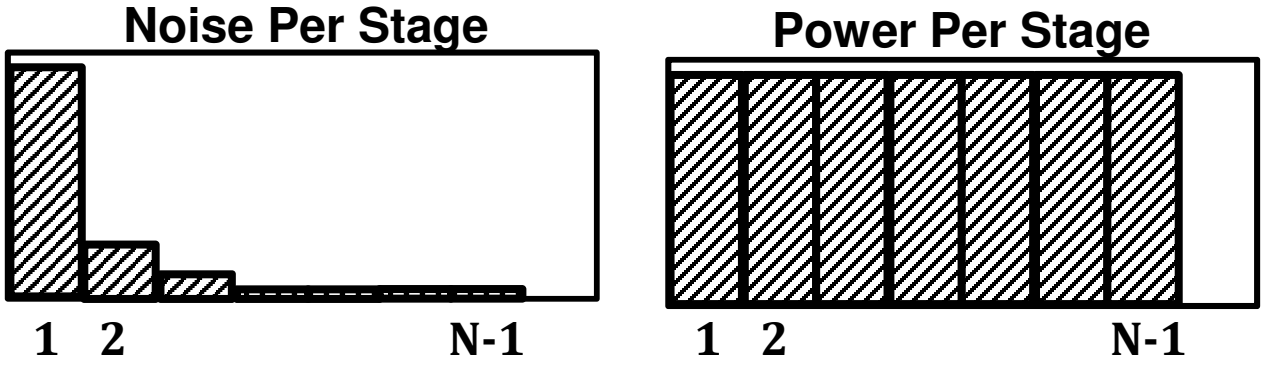
Stage Scaling for Optimal Noise (1)

$$N_T \propto kT\left[\frac{1}{C_1}+\frac{1}{G_1^2C_2}+\frac{1}{G_1^2G_2^2C_3}+\cdots+\frac{1}{G_1^2\cdots G_{N-1}^2C_N}\right]$$

- If $C_1 = C_2 = \cdots CN$ then backend stages contribute very little noise
  - Wasteful as power $\propto G_m \propto C$
- How about scaling by 2^M where M is the resolution of each stage.
  - Same amount of noise from each stage.
  - Power can be reduced.

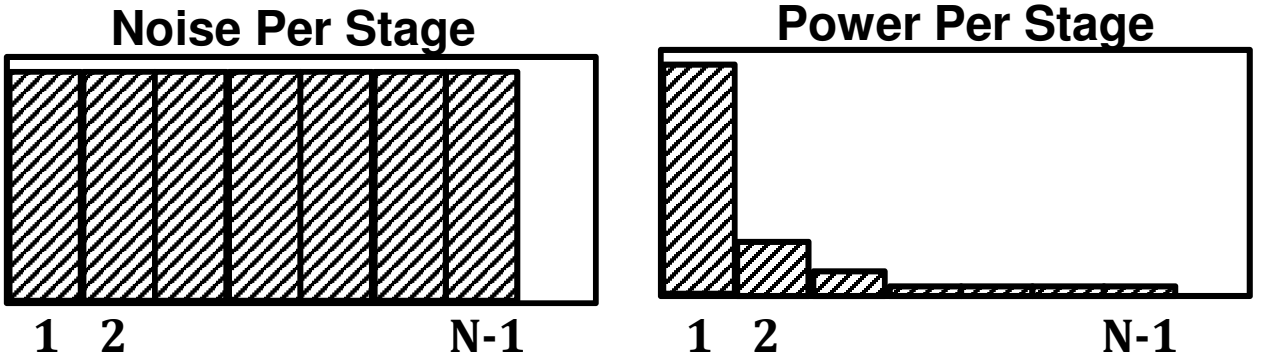
Stage Scaling for Optimal Noise (2)

Extreme Case - 1 : All Stages Consume the Same Power



Extreme Case - 2 : All Stages Contribute the Same Noise

[Cline 1995]



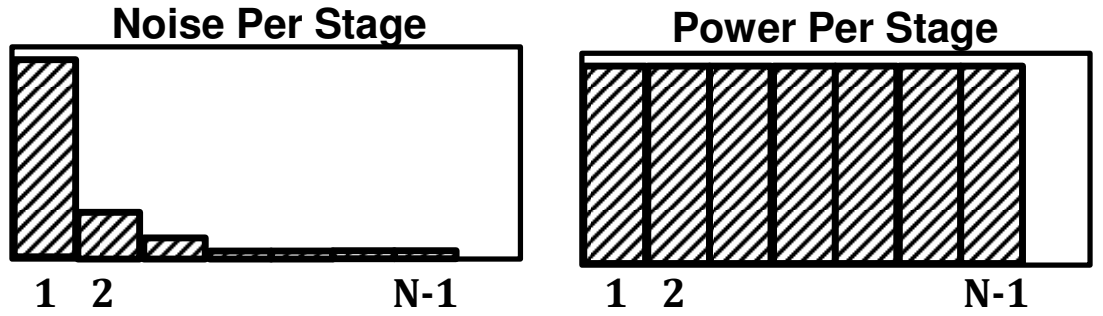
$$N_T \propto kT\left[\frac{1}{C_1}+\frac{1}{G_1^2C_2}+\frac{1}{G_1^2G_2^2C_3}+\cdots+\frac{1}{G_1^2\cdots G_{N-1}^2C_N}\right]$$

- Optimum capacitor scaling lies approximately midway between these two extremes.

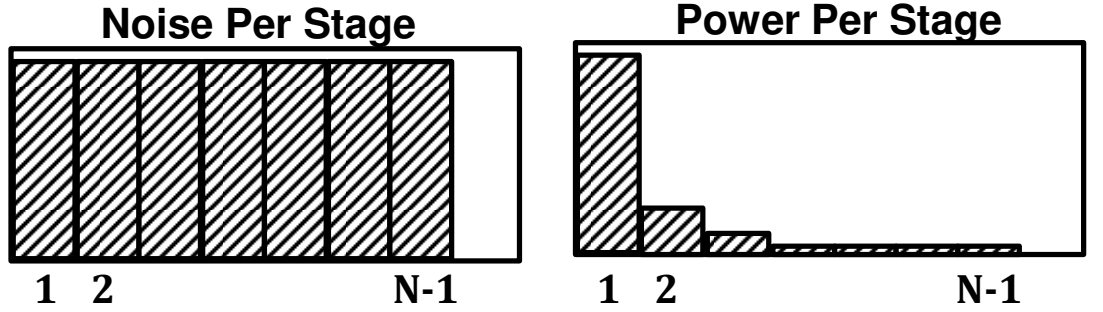
Stage Scaling for Optimal Noise (3)

Extreme Case - 1 : All Stages Consume the Same Power

[Cline 1995]

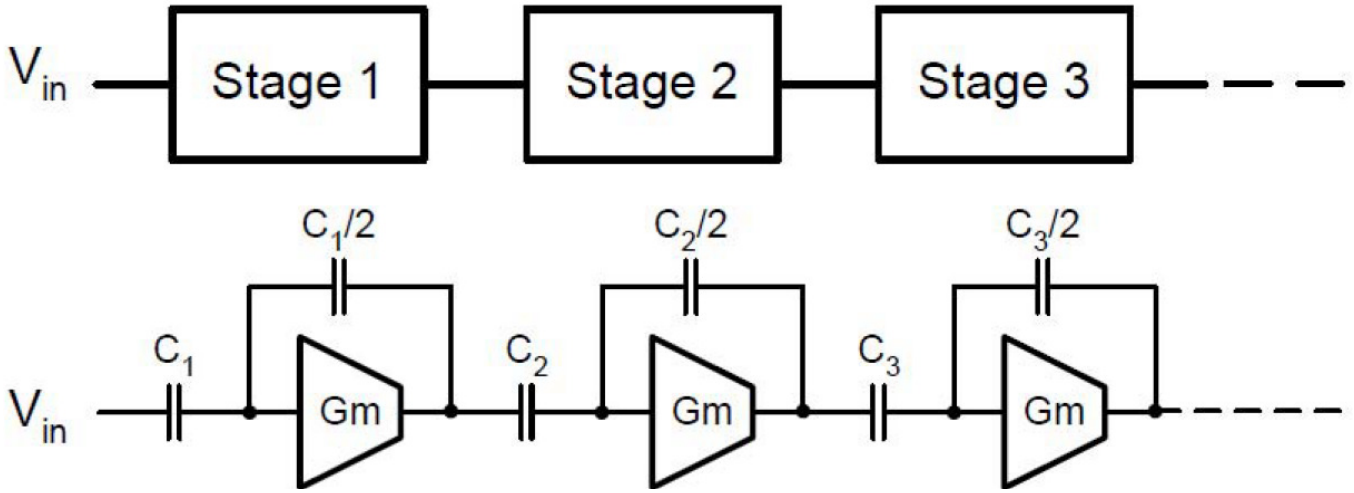


Extreme Case - 2 : All Stages Contribute the Same Noise



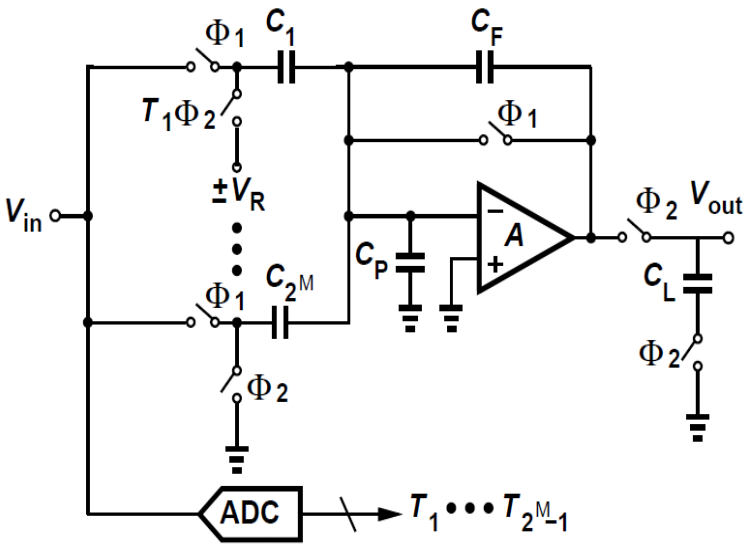
- As mentioned earlier optimal scaling is between the two extremes
- Capacitor scaling factor 2^{MX} where M is the stage resolution.
  - x=1 → scaling exactly by the stage gain.

Stage Scaling for Optimal Noise (4)



- Start by assuming capacitors are scaled precisely by stage gain
  - For 1-bit stages, capacitors can be scaled by factor of 2
  - For 2-bit stages, capacitors can be scaled by a factor of 2^2.
- Refine using the first pass circuit simulations by either using:
  - MATLAB
  - Excel

Noise Sources in Pipelined ADC



Switch Capacitor Implementation of a Pipelined Stage

- The output voltage of a pipelined stage is given by

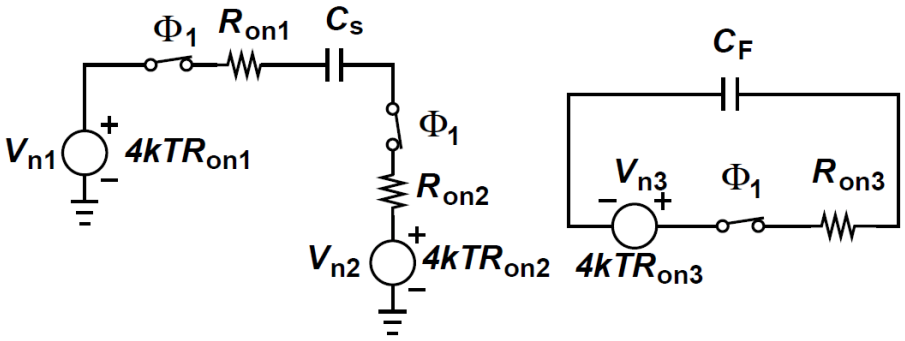
$$V_{OUT} = \frac{\sum_{i=1}^{2^M} C_i V_{IN} + \sum_{i=1}^{2^M-1} T_i C_i V_R}{C_F} + \sqrt{\overline{V_{n,tot}^2}}$$

- where $\overline{V_{n,tot}^2}$ is the MS value of the thermal noise of the stage.

$$\overline{V_{n,tot}^2} = \overline{V_{n,sp}^2} + \overline{V_{n,ap}^2}$$

- where, $\overline{V_{n,sp}^2}$ and $\overline{V_{n,ap}^2}$ are the MS value of the sample-phase noise and amplification-phase noise, respectively.

Sample-phase Noise



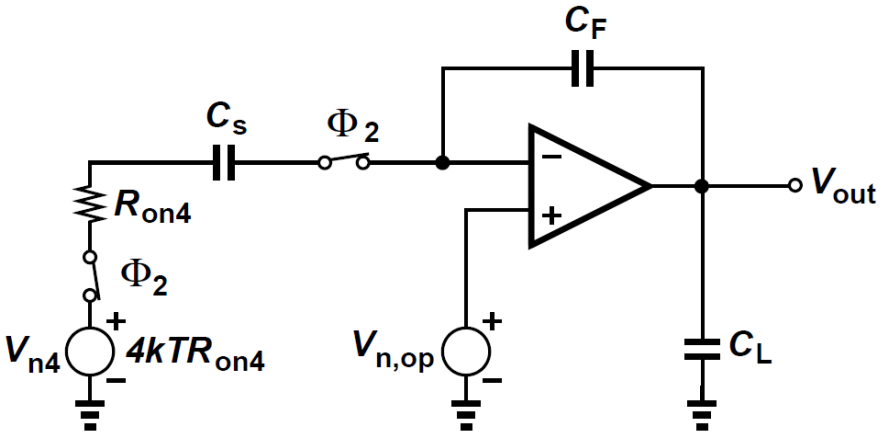
Noise equivalent model in sample phase

- The thermal noise of switch resistances R_{on1} and R_{on2} have single-sided PSD of $4kTR_{on1}$ and $4kTR_{on2}$ respectively.
- These are filtered by the RC network having a time-constant, $\tau = (R_{on1} + R_{on2})C_S$.
- The thermal noise of R_{on3} is filtered by the RC network with time-constant, $\tau = R_{on3}C_F$.
- The MS value of the noise charge sampled on C_S and C_F are kTC_S and kTC_F , respectively.

- This sampled charge is transferred to the output during the amplification phase producing a noise voltage at the output that has a MS value given by:

$$\overline{V_{n,sp}^2} = \frac{kTC_S + kTC_F}{C_F^2}$$

Amplification-phase Noise



Noise equivalent model in amplification phase

- Amplification-phase noise has the switch thermal noise and op amp thermal noise
- MS value of amplification noise is

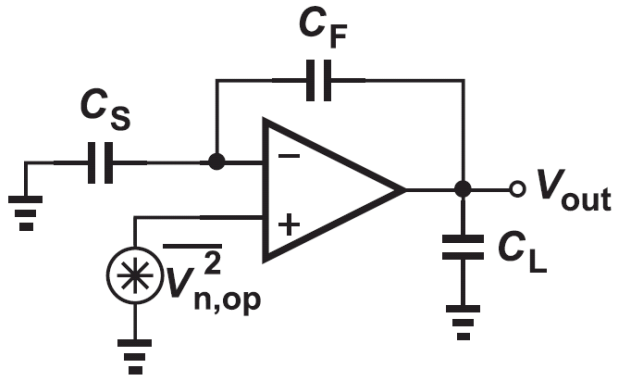
$$\overline{V_{n,ap}^2} = \overline{V_{n,ap,sw}^2} + \overline{V_{n,ap,op}^2}$$

- where, $\overline{V_{n,ap,sw}^2} = \frac{kT}{C_S}\left(\frac{C_S}{C_F}\right)^2$ and $\overline{V_{n,ap,op}^2}$ is the op amp noise.

- Thus, the MS value of the total noise at the output of the MDAC is $\overline{V_{n,tot}^2} = \frac{kTC_S + kTC_F}{C_F^2} + \frac{kT}{C_S}\left(\frac{C_S}{C_F}\right)^2 + \overline{V_{n,ap,op}^2}$
- The input-referred noise of the MDAC is $\overline{V_{n,inp-ref}^2} = \frac{\overline{V_{n,tot}^2}}{G}$ where $G = \frac{C_S}{C_F}$, if op amp gain is ∞.

Sampling Cap	Load Cap	Switch noise	Op amp noise
4 pF	800 fF	508.9 μV	1.01 mV

Op amp Noise



Op amp with capacitive negative feedback.

- The MS value of the output noise
  - single-stage op amp is

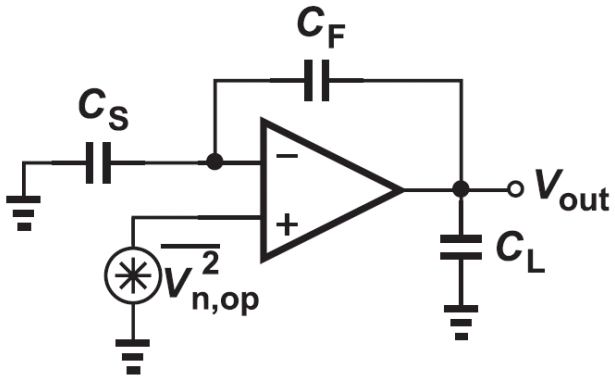
$$\overline{V_{n,ap,op}^2} = \frac{2kT\gamma}{\beta C_{eff}}$$

  - two-stage op amp is given by

$$\overline{V_{n,ap,op}^2} = \frac{2kT\gamma}{\beta C_c}$$

- The MS value of the output noise for both the single-stage and two-stage op amps is independent of the op amp transconductance.
- The output noise can be minimized by increasing
  - The effective load capacitance C_{eff} for a single stage op amp
  - The compensation capacitor C_c for a two-stage op amp
- However, if the op amp power is not increased, increasing C_c reduces the bandwidth of the closed loop amplifier

Op amp Noise (Cont.)



Op amp with capacitive negative feedback.

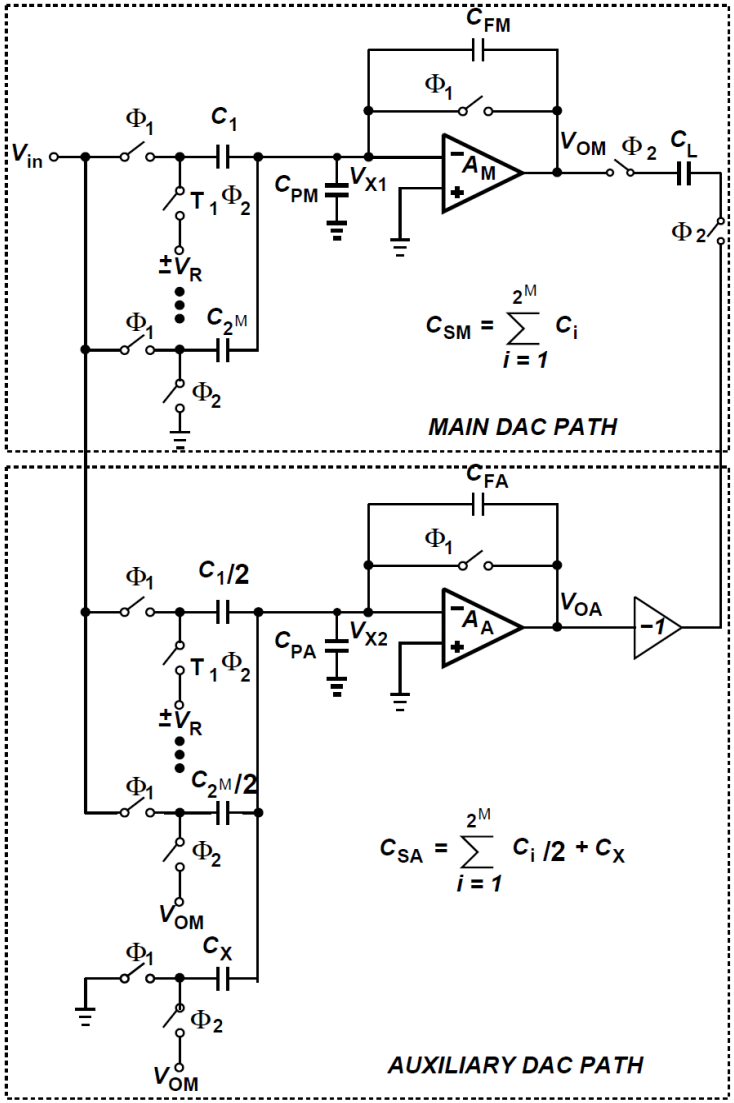
- For a two-stage op amp to have more than 60◦ phase margin for a given C_{eff}, power, and bandwidth, $C_c < C_{eff}/2$
- The transconductance of the second stage should be at least 5 to 8 times more than the transconductance of the first stage*.

- Thus, a two-stage op amp is more noisy than a single-stage op amp for a given C_{eff}, power, and bandwidth.
- Although a single-stage op amp is less noisy for a given load, power, and bandwidth, it has limited headroom and has limited applications.

* W. Sansen, *Analog Design Essentials. New York, NY, USA: Springer* Verlag, 2006, p. 165.

Thermal Noise Cancelling Technique

- Noise cancellation is a two-step process,
  - Faithful reproduction of the thermal noise
  - Application of the reproduced thermal noise to the bottom-plate of C_L
- An auxiliary path, which uses a single-stage op amp less noisy than a two-stage op amp, faithfully reproduces the noise and removes the signal component.
- Auxiliary path capacitors are scaled by a factor of 2 w.r.t. main path capacitors to facilitate this.
- Perfect noise cancellation occurs if both the circuits are ideal.



Bibhudatta Sahoo

Input-Output Characteristic of Auxiliary DAC

- During sampling phase,

$$Q_{s,a} = 8CV_{IN}$$

- During hold phase,

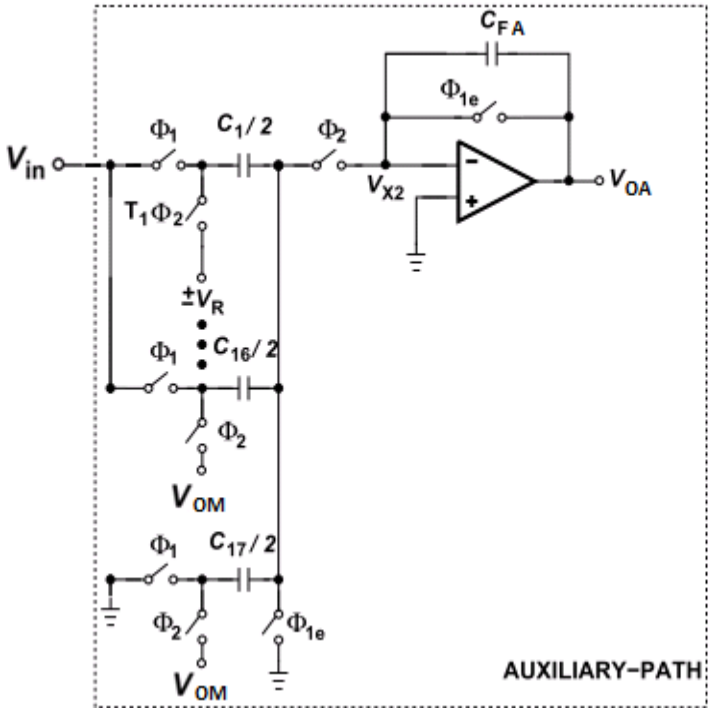
$$Q_{h,a} = \sum_{i=1}^{15} T_i V_R C/2 + V_{OM} C + V_{OA} C_{FA}$$

- By charge conservation and substituting the value of output of main MDAC V_{OM}, Auxiliary path output is

$$V_{OA} = \frac{8CV_{IN} - \sum_{i=1}^{15} T_i V_R C/2 - V_{OM} C}{C_{FA}}$$

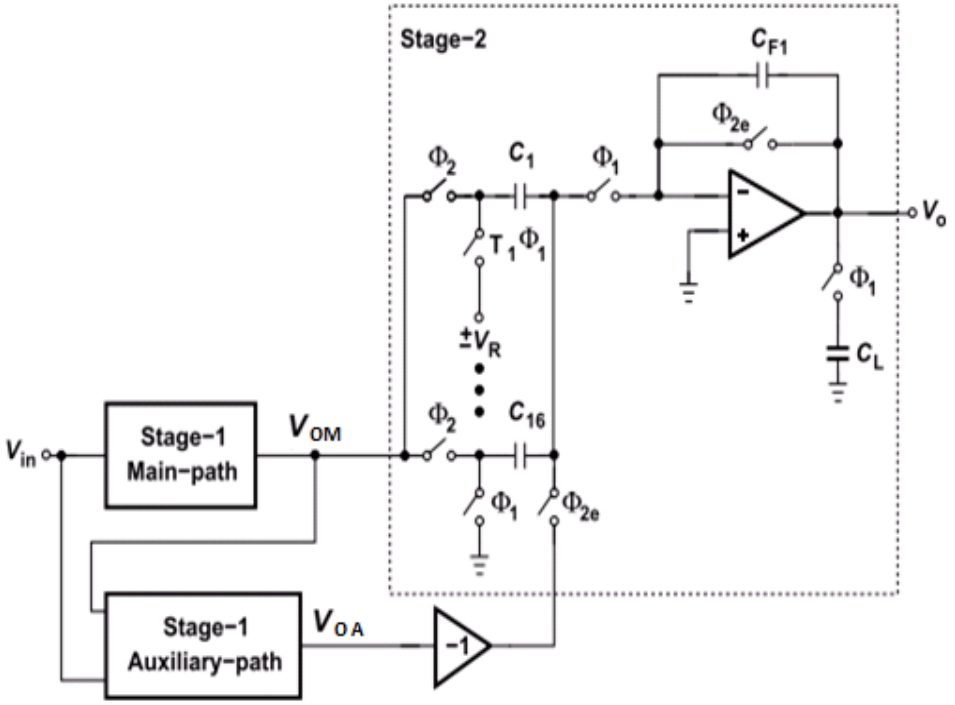
- If $C_{FM} = 2C$ and $C_{FA} = C$ then,

$$V_{OA} = -\sqrt{\overline{V_{n,tot}^2}}$$



Overall Noise Cancellation Technique

- The output of the auxiliary-path is inverted and connected to the top-plate of Stage-2 sampling capacitor which is C_L of 1st-stage.
- Top-plate and bottom-plate of C_1 samples the noise of the main path resulting in noise cancellation.
- In differential implementation inversion is realized by swapping the differential output of the auxiliary-path.
- Thus, the sampled noise as well as the op amp noise of main-path is cancelled ➔ auxiliary path sampled and op amp noise is present ☹.



$$C_1+C_2+C_3+\ldots\ldots+C_{16}=C_L$$

Effect Of Non-Idealities

- Perfect noise cancellation does not happen in the presence of non-idealities such as:
  - Finite op amp gain
  - Input parasitic capacitance of the op amp
  - Op amp offset
- Both main-path MDAC and auxiliary-path DAC contribute to these non-idealities.
- Since the swing at the output of the auxiliary-path op amp is just the thermal noise which is very small, a high-speed single stage moderate gain op amp is used.

Effect of Auxiliary Path Noise

- **The auxiliary path also has both sample-phase and amplification-phase noise whose MS values can be defined as:**

$$\overline{V_{m,sp,a}^2} = \frac{kTC_{SA} + kTC_{FA}}{C_{FA}^2}, \quad and \quad \overline{V_{n,ap,a}^2} = \frac{kTC_{SA}}{C_{FA}^2} + \frac{2kT\gamma}{\beta C_{eff}}.$$

- **Auxiliary-path op amp, being a single-stage op amp, can be designed to be of high-speed and have low noise.**
- **Table summarizing the noise of the main-path and auxiliary-path for a prototype 4-bit noise-cancelling MDAC designed in IBM 32-nm SOI process that operates from 1.5 V supply at 400 MHz sample-rate and provides a signal swing of ±750 mV in the main-path.**

	Sampling Cap	Load Cap	Switch noise	Op amp noise
Main-path	4 pF	0.8 pF	508.9 μV	1.01 mV
Auxiliary-path	2 pF	0.8 pF	752.7 μV	356 μV

Effect of Auxiliary Path Op amp Gain and Bandwidth

- If all other parameters are ideal and only the auxiliary path op amp gain is finite, then the auxiliary path output is

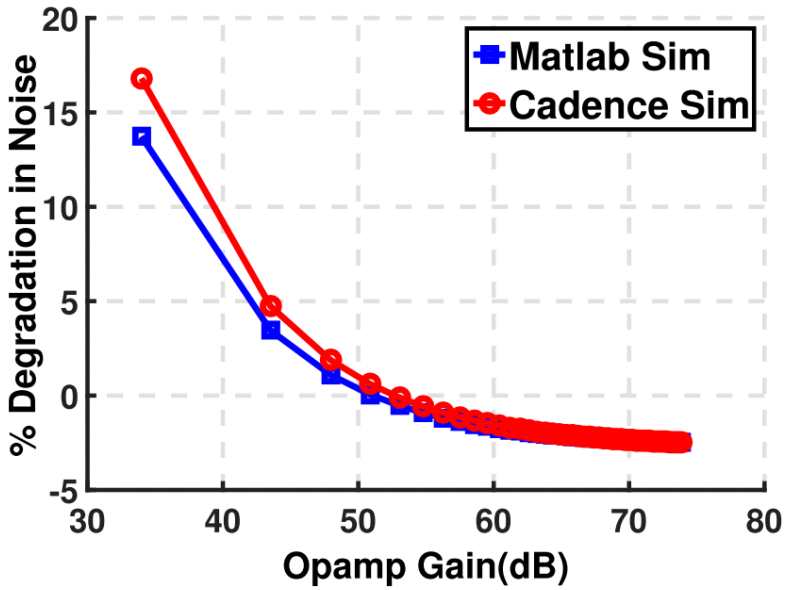
$$V_{OA} = \frac{C}{C_{FA} + \frac{\sum_{i=1}^{17} C_i / 2 + C_{FA} + C_{PA}}{A_A}} \cdot \left[\left(\frac{1}{2} - \frac{C}{C_{FM}} \right) \left(V_{in} 2^M - \sum_{i=1}^{2^M - 1} T_i V_R \right) - \sqrt{\overline{V_{n,tot}^2}} \right]$$

$$\Rightarrow V_{OA} = \gamma \sqrt{\overline{V_{n,tot}^2}} \quad where \quad \gamma = 1/(1 + (\sum_{i=1}^{17} C_i / 2 + C_{FA} + C_{PA}) / A_A C_{FA}))$$

- Finite gain and bandwidth of the auxiliary path affects only the noise term and a **fraction** of the total main-path noise is cancelled.

Effect of Auxiliary Path Op amp Gain and Bandwidth (Cont.)

- Proposed architecture uses a single stage telescopic op amp with open-loop gain, A_{aux} = *40 dB* ➔ 7% degradation .
- Due to finite bandwidth the auxiliary-path output does not settle to the value of $\sqrt{\overline{V_{n,tot}^2}}$ and thus manifests as gain error too and hence only a fraction of the total main-path noise is cancelled
- In the proposed design the auxiliary-path op amp was designed to have a bandwidth such that there is < 0.1% degradation in the noise cancellation



Percentage degradation in the amount of noise cancellation as a function of auxiliary path op amp gain

Effect of Capacitor Mismatch

- With capacitor mismatch, the generalized noise cancelling equation becomes

$$V_{OA} = \frac{V_{in}\sum_{i=1}^{2^M}\left(\frac{(C_i+\Delta C_i)}{2} - (C_i+\Delta C_i)\frac{C}{C_{FM}}\right) - V_R\left(\sum_{i=1}^{2^M-1}\left[T_i\frac{(C_i+\Delta C_i)}{2} + T_i(C_i+\Delta C_i)\frac{C}{C_{FM}}\right]\right) - \sqrt{V^2_{n,tot,M}}C}{C_{FA}}$$

- The capacitor mismatch error can be calibrated out using various techniques.
- The fractional mismatch in the $\sqrt{V^2_{n,tot}}$ term is going to be a small value which hardly affects the overall noise cancellation performance and hence can be ignored.

Simulation Results

- The effectiveness of the proposed noise cancelling technique was validated in simulation by building 12-bit, 14-bit, and 16-bit pipelined ADCs in IBM 32-nm SOI process.
- The ADCs were designed for a sample-rate of 400 MHz.
- The following table summarizes the resolution of the various stages used in the ADCs.

	Resolution				
	Stage-1	Stage-2	Stage-3	Stage-4	Stage-5
16-bit	4	4	4	4	4
14-bit	4	4	4	4	2
12-bit	4	4	4	3	-

- All the stages have a redundancy of 1-bit except for the last stage.

C. Ravi, D. James, V. Sarma, B. Sahoo, and A. Inamdar, "Thermal Noise Canceling Pipelined ADC", accepted to *IEEE ISCAS, Baltimore, USA,* 2017.

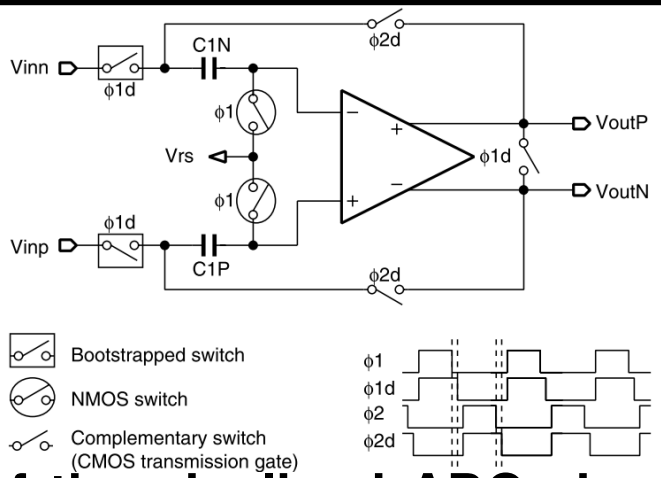
Case-Study

	Stage-1 Sample-phase Noise	Amplification-phase Input Referred Noise(μV)					Total Input Referred Noise(μV)	SNR (dB)
		Stage-1	Stage-2	Stage-3	Stage-4	Stage-5		
	$\sqrt{\frac{2kT}{C_s}}$	$\sqrt{V_{n,1}^2}$	$\sqrt{V_{n,2}^2}$	$\sqrt{V_{n,3}^2}$	$\sqrt{V_{n,4}^2}$	$\sqrt{V_{n,5}^2}$	$\sqrt{\sum \overline{V_{n,i}^2} + \frac{2kT}{C_s}}$	
16-bit ADC								
		$C_s = 4\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$		
No Cancellation	45.49	128	24.2	3.02	0.38	0.04	138.02	71.68
Stage-1 Noise Cancellation	62.42	55.97	24.2	3.02	0.38	0.04	87.32	75.64
Stage-1 and 2 Noise Cancellation	62.42	55.97	14.18	3.02	0.38	0.04	85.08	75.86
14-bit ADC								
		$C_s = 4\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$	$C_s = 0.2\,pF$		
No Cancellation	45.49	128	24.2	3.02	0.38	0.05	138.02	71.53
Stage-1 Noise Cancellation	62.42	55.97	24.2	3.02	0.38	0.05	87.32	75.29
Stage-1 and 2 Noise Cancellation	62.42	55.97	14.18	3.02	0.38	0.05	85.09	75.49
12-bit ADC								
		$C_s = 4\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$	$C_s = 0.8\,pF$			
No Cancellation	45.49	128	24.2	3.02	0.38		138.02	69.69
Stage-1 Noise Cancellation	62.42	55.97	24.2	3.02	0.38		87.32	71.75
Stage-1 and 2 Noise Cancellation	62.42	55.97	14.18	3.02	0.38		85.09	71.84

$\overline{V_{n,i}^2} = \frac{\overline{V_{n,tot,i}^2}}{\prod_{k=1}^{i} G_k^2}$, $C_s = C_{SM}$ for rows corresponding to no cancellation and $C_s = C_{SA}$ for rows corresponding to noise cancellation.

$V_{in,p-p} = 1.5$ V

Front End Sample-and-Hold Amplifier (SHA)



[Ishii 2005]

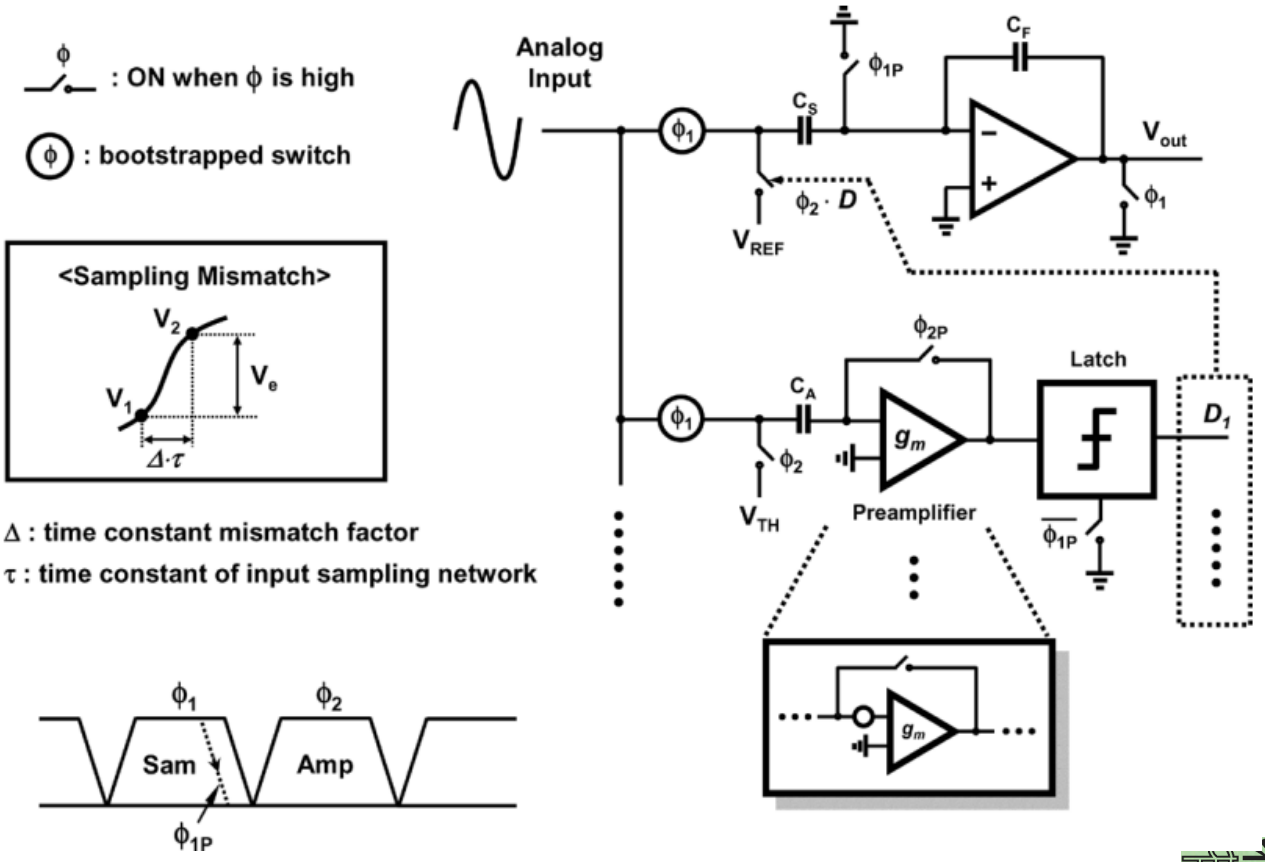
- The first stage of the pipelined ADC should ideally be preceded by a SHA
  - MDAC and sub-ADC of the pipelined stage see the same input voltage.
- Since the SHA has a gain of 1 the total input referred noise increases:

$$N_T \propto kT\left[\frac{1}{C_{1N,1P}}+\frac{1}{C_1}+\frac{1}{G_1^2C_2}+\frac{1}{G_1^2G_2^2C_3}+\cdots+\frac{1}{G_1^2\cdots G_{N-1}^2C_N}\right]$$

- SHA can burn up to 1/3 of total ADC power

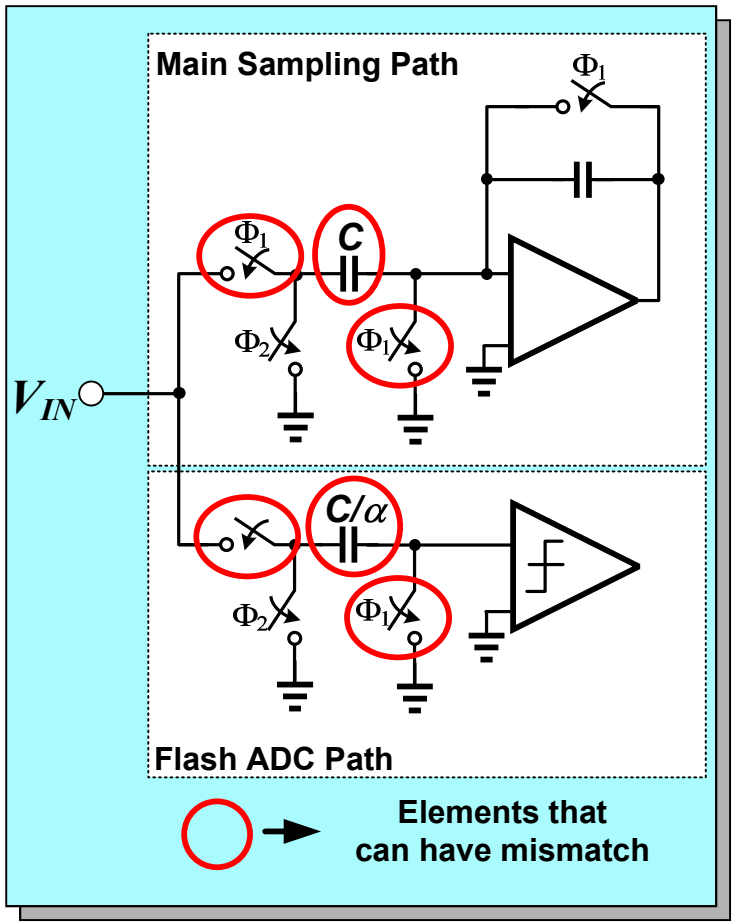
SHA-less Front-end

- Removing the front-end SHA reduces the power consumption.
- Leads to timing mismatch between the signal sampled in the MDAC and Flash.



[Chang 2004]

SHA-less Architecture (2)

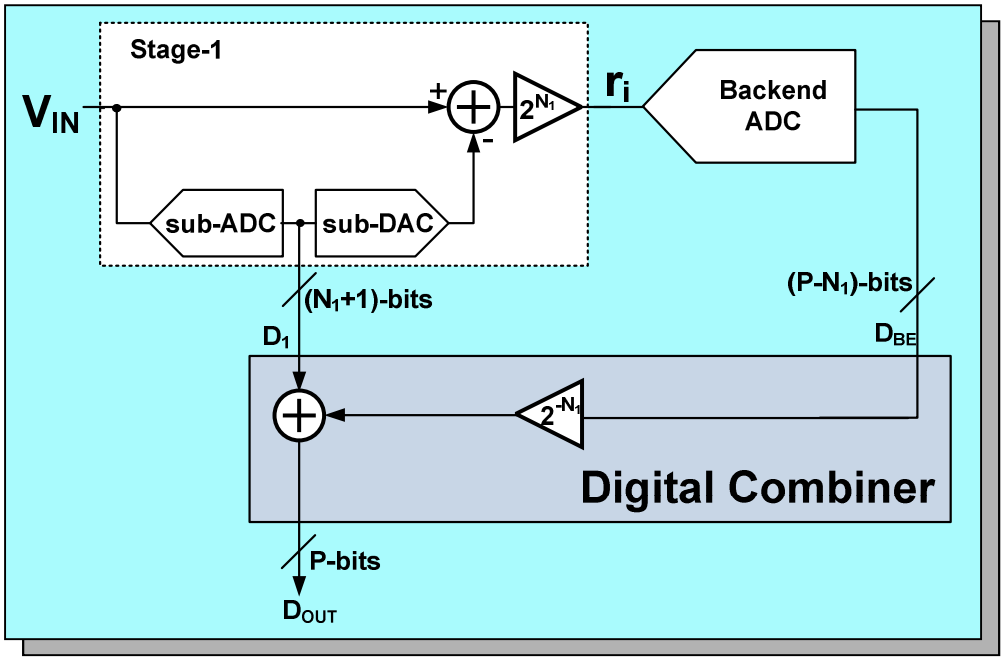


[Mehr 2000]

- Any mismatch between the "main sampling path" and "flash ADC path" results in different voltages being sampled on "C" and "C/α".
- The mismatch can be translated to time-constant mismatch (τ).
- For a signal of amplitude "A" and frequency "f_{in}" the difference in voltage sampled on "C" and "C/α" is:
  - $\Delta V = 2\pi f_{in} A\tau$
- Match the flash and MDAC paths.

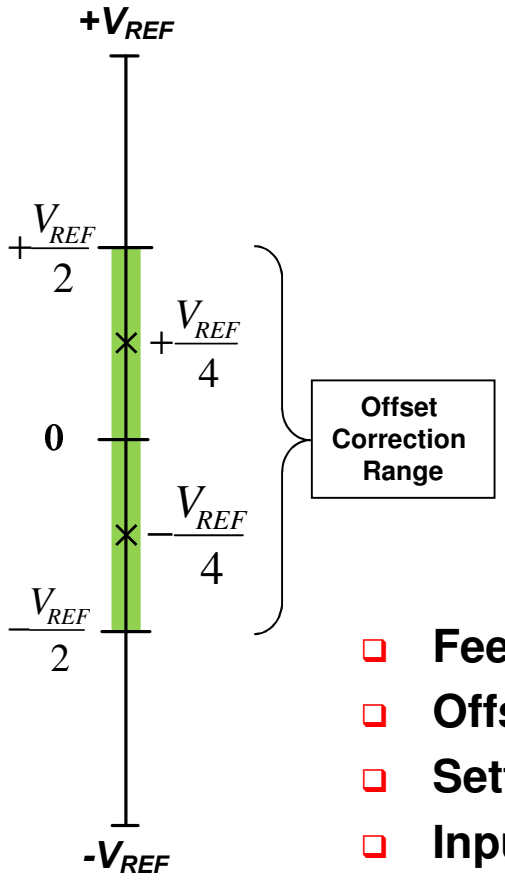
Pipeline ADC
- Area, Power, Speed, Resolution Optimization-
System Specifications to Circuit

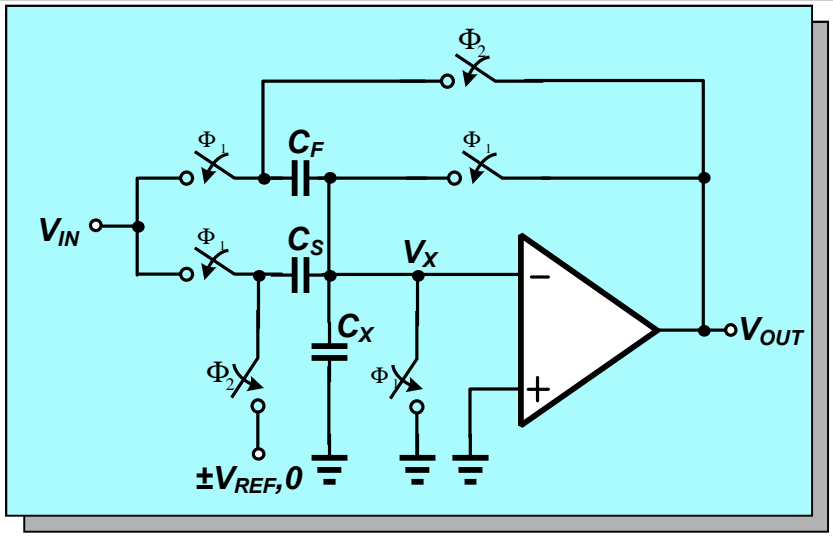
Pipeline ADC – Area, Power, Speed, Resolution Trade-off



- For a given ADC resolution, the number of stages and number of bits resolved in each stage determines:
  - power consumption
  - area

1.5-bit Stage

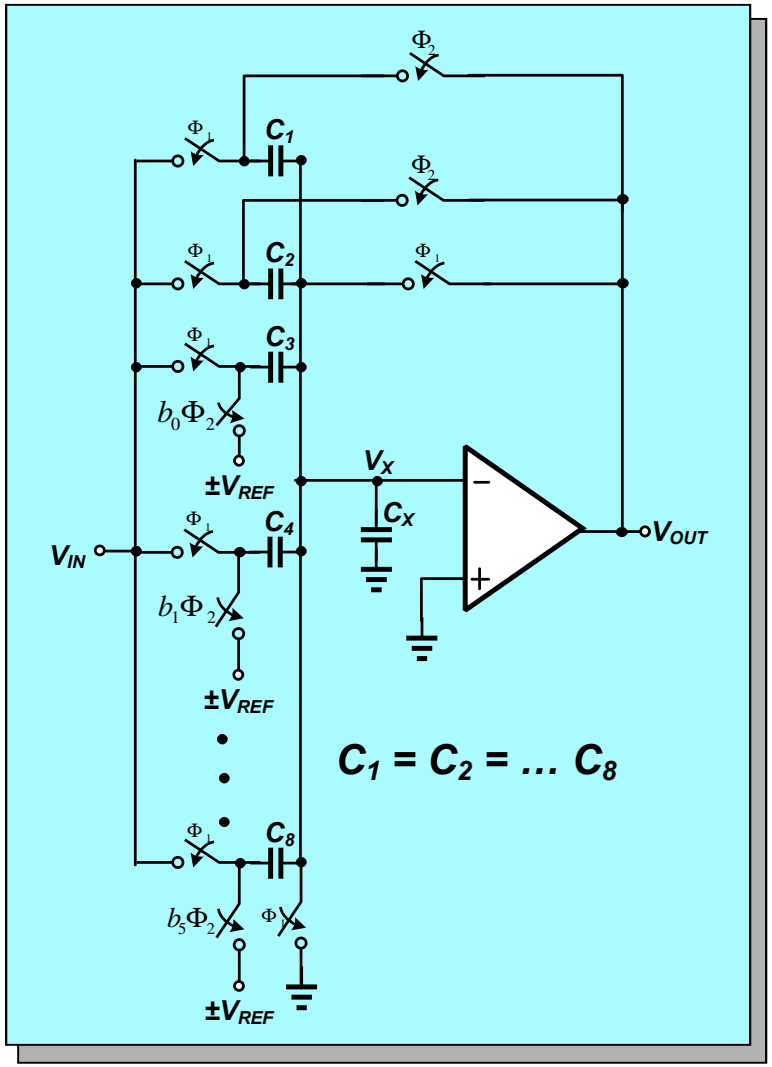


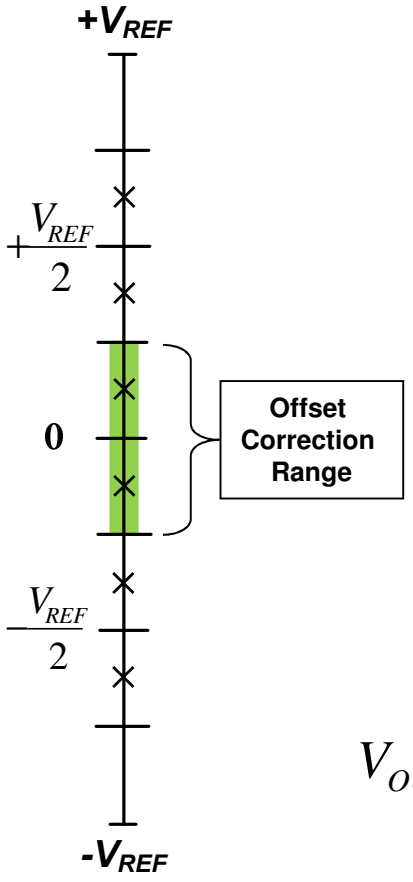


$$V_{OUT} = \frac{(C_S + C_F)V_{IN} - kC_S V_{REF}}{C_F - \left(\frac{kC_S + C_X + C_F}{A}\right)}$$

- Feedback factor = ½.
- Offset correction range = $\pm V_{REF}/4$ (i.e. ±150 mV for V_{REF}=0.6V).
- Settling Requirement on the op amp reduced by 1-bit.
- Input referred noise = ½ of output noise.

2.5-bit Stage

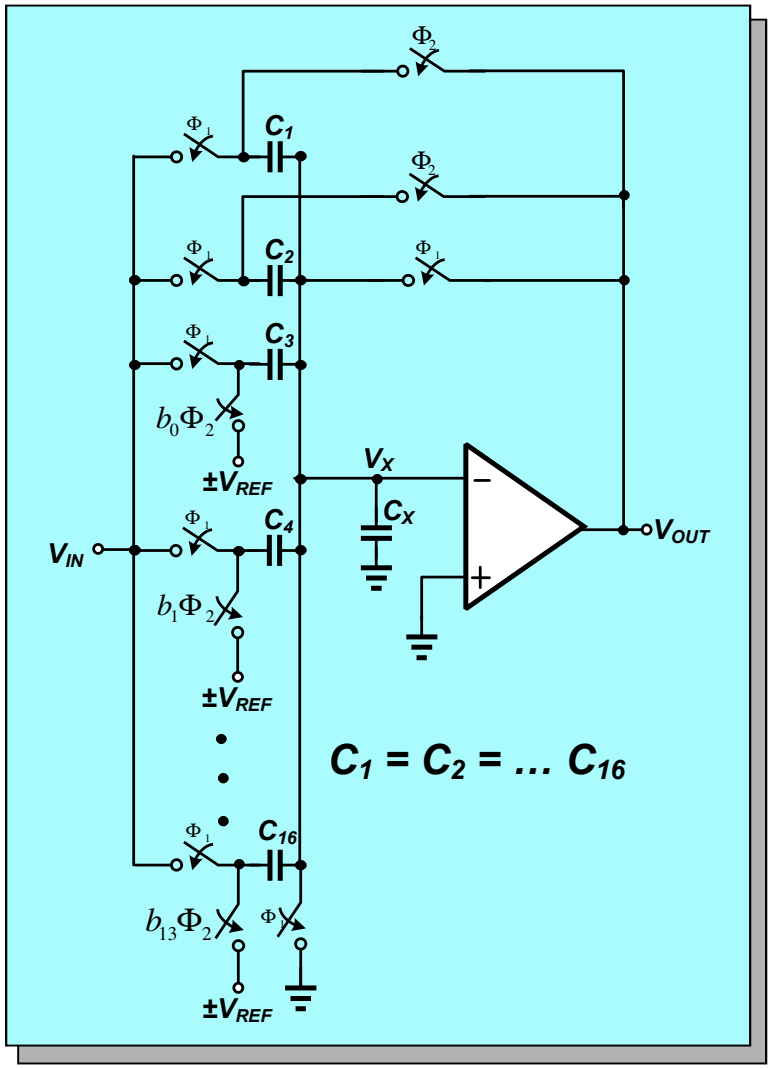


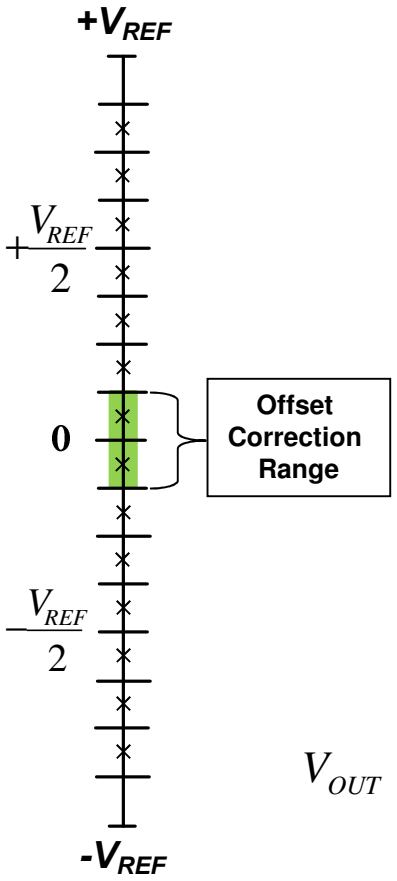


- Feedback factor =1/4.
- Offset correction range = $\pm V_{REF}/8$ (i.e. ±75 mV for V_{REF}=0.6V).
- Settling Requirement on the op amp reduced by 2-bits.
- Input referred noise is ¼ of output noise.
- Input-Output transfer function is:

$$V_{OUT} = \frac{\sum_{i=1}^{8} C_i V_{IN} - \sum_{i=0}^{5} C_{i+3} b_i V_{REF}}{C_1 + C_2 + \frac{C_1 + C_2 + C_X}{A}}$$

3.5-bit Stage





- Feedback factor = 1/8.
- Offset correction range = $\pm V_{REF}/16$ (i.e. ±37.5 mV for V_{REF}=0.6V).
- Settling Requirement on the op amp reduced by 3-bits.
- Input referred noise is 1/8 of output noise.
- Input-Output transfer function is:

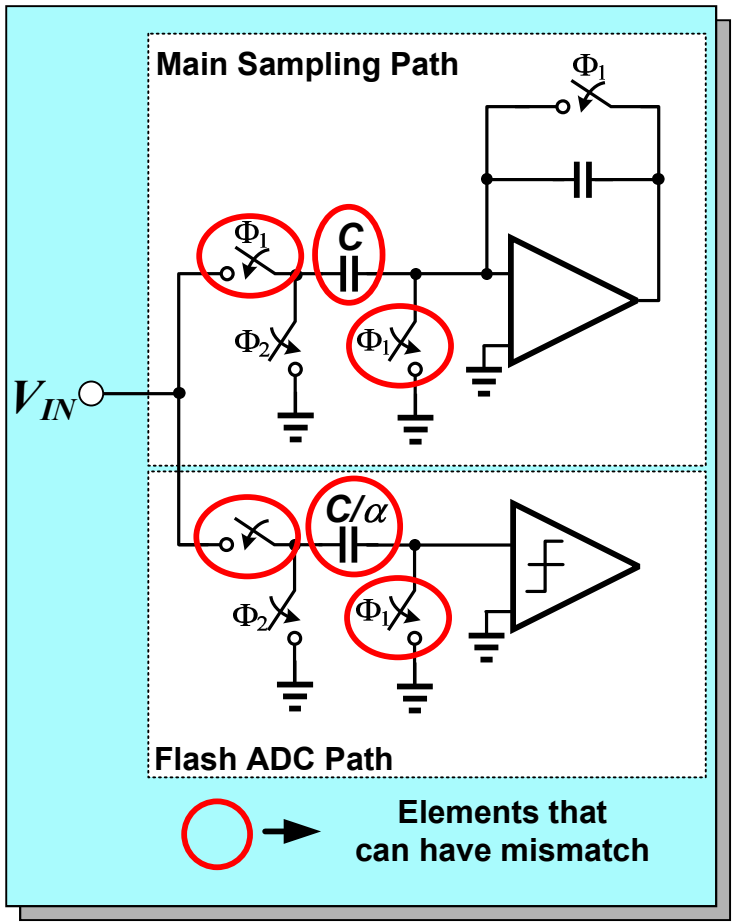
$$V_{OUT} = \frac{\sum_{i=1}^{16} C_i V_{IN} - \sum_{i=0}^{13} C_{i+3} b_i V_{REF}}{C_1 + C_2 + \frac{C_1 + C_2 + C_X}{A}}$$

Architecture Summary

Summary of ADC Stage Architectures				
	1.5-bit Stage	*2.5-bit Stage*	*3.5-bit Stage*	*Parameter effected*
Feedback Factor	$1/2$	$1/4$	$1/8$	*Speed and Power*
Offset Correction Range	$\pm V_{REF}/4$	$\pm V_{REF}/8$	$\pm V_{REF}/16$	*Linearity of ADC*
Reduction in Settling Requirement	1-bit	2-bits	*3-bits*	*Speed and Power*
Noise Scaling	$1/2$	$1/4$	$1/8$	*SNR, Power, & Area*
Reduction in Capacitor Matching Requirement	*1-bit*	*2-bits*	*3-bits*	*Power and Area*

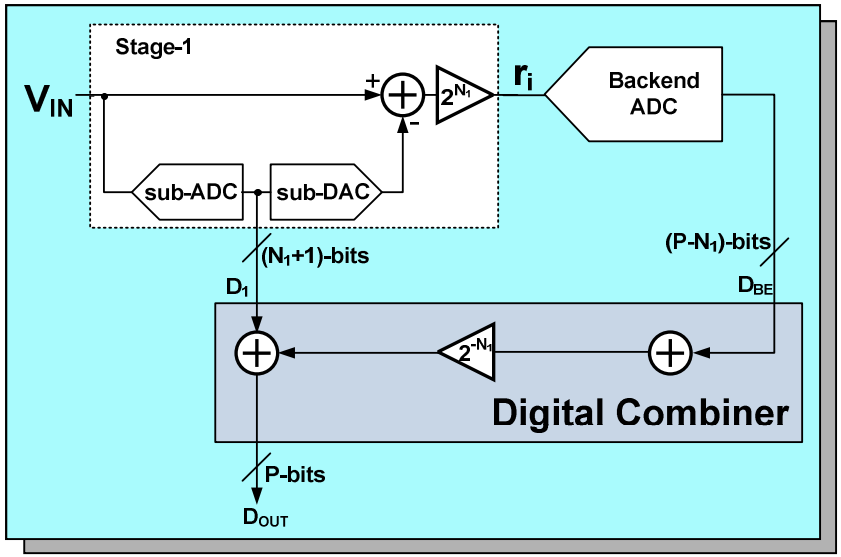
- **For resolutions more than 10-bits it is better to resolve more bits in the first stage:**
  - **relaxing op amp settling.**
  - **capacitor matching.**
  - **reducing capacitance ➔ input referred noise is reduced.**
  - **DOES NOT relax the op amp open loop DC gain requirement (more later).**

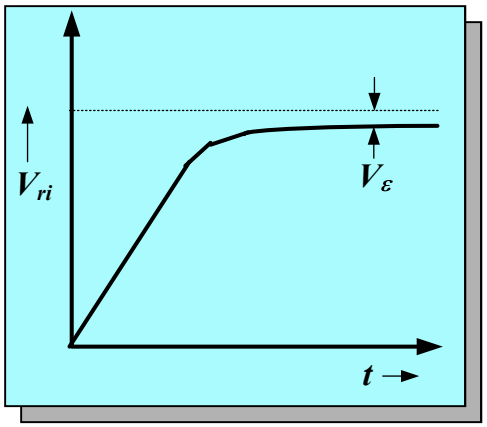
Why not resolve more bits in 1st Stage?



- Any mismatch between the "main sampling path" and "flash ADC path" results in different voltages being sampled on "C" and "C/α".
- The mismatch can be translated to time-constant mismatch (τ).
- The difference in voltage should be within the offset correction range of the Flash ADC.
- Resolving more bits in the 1st stage reduces the offset-correction range and hence could result in missing codes.
- Offset correction range should include:
  - Comparator offsets in the flash.
  - Time constant mismatch (τ).
- For a signal of amplitude "A" and frequency "f_{in}" the difference in voltage sampled on "C" and "C/α" is:
  - $\Delta V = 2\pi f_{in} A \tau$

DC Gain Requirement of op amp in each stage





- Residue voltage V_{ri} has to settle to $LSB/2$ of the backend-ADC.
- Gain error:

$$\frac{V_\varepsilon}{V_{ideal}} = \frac{1}{1+\beta A_{DC}} < \frac{1}{2^{(P-N_1+1)}}$$

- Resolution reduces but the feedback factor also reduces by the same amount $\Rightarrow$ DC gain is defined by the resolution of the ADC and not the resolution of the backend ADC that follows.
- The above holds true for the op amps in the later stages of the pipeline.

Architecture Optimization (1)

- **Some expressions used for architecture optimization i.e. number of pipeline stages and number of bits/stage:**
  - **Settling time for *N*-bit accuracy:**

$$t_{settle} = (N+1) \bullet \tau \bullet \ln(2)$$

  - **Two stage op amp poles and unity gain bandwidths:**

$$\omega_{p1} = \frac{1}{R_1 g_{m2} R_2 C_C},\ \omega_{p2} = \frac{g_{m2}}{C_L},\ \omega_u = \frac{g_{m1}}{C_C},\ \text{and}\ \omega_{p2} \approx 5 \bullet \omega_u$$

  - **Variance of input referred sampled noise:**

$$\sigma_{IN}^2 = 2 \bullet \left[\frac{kT}{C_1} + \sum_{i=2}^{N} \frac{kT}{C_i} \frac{1}{G_{i-1}^2} \right] + \sigma_{op}^2 + \sigma_{ref}^2 + \sigma_{jitter}^2$$

    where, C_i = sampling caps in each stage, and G_i = gain of each stage.
  - **2nd stage of the op amp is a common source stage. For maximum output swing at the highest speed typical gain in the 2nd stage is ≈ 10.**
  - **Overdrive voltage to maximize swing is chosen to be around V_{OV}=*150 mV* and hence current in each branch in the two stages are $I_{D1} = g_{m1} \bullet V_{OV}/2$ and $I_{D2} = g_{m2} \bullet V_{OV}/2$.**

Architecture Optimization (2)

- **Signal swing = ±*750 mV* for *1.5 V* supply**
- **Resolution = *12-bits* (determines quantization noise)**
- f_{MAX_IN} = ***100 MHz***
- f_S = ***200 MHz***
- $t_{slewing}$ = ***0.5 ns***
- $t_{non\_overlap}$ = ***0.2 ns***
- $t_{settling}$ = ***1.8 ns***
- **Noise Budget:**
  - **Quantization Noise**
  - **Sampled Thermal Noise**
  - **Op amp Noise**
  - **Reference Noise**
  - **Jitter Noise**
  - **Input signal buffer Noise**

Architecture Optimization (3) Jitter Specification

- The variance of jitter voltage is given by:

$$\sigma_{jitter} = \sqrt{2}\,\pi\, t_j\, f_{in} A$$

where, t_j = variance of jitter.

f_{in}= frequency of the input signal.

A = amplitude of the input signal.

- For maximum input frequency of 100 MHz and jitter limited SNR of 80 dB the required rms jitter is $700\ fs$.

Architecture Optimization (4)
Noise Budget

Noise Budget	
LSB (Δ)	$\frac{V_{p-p}}{2^{12}} = \frac{1.5}{2^{12}} = 366\ \mu V$
Reference Noise	90 µV
Op Amp Noise	120 µV
Sampled Noise (kT/C)	64 µV (2 pF)
Jitter Noise $(\sqrt{2}\pi t_j f_{in} V_{p-p}/2)$	66 µV (200 *fs* RMS jitter)
Overall SNR	67.8 dB (in 100 MHz band)

Architecture Optimization (5)

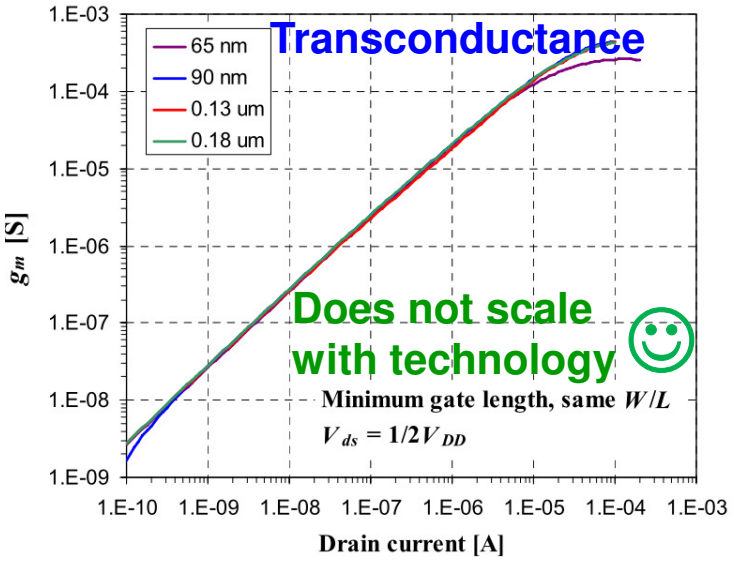
Sl. No.	*Architecture*	*Sampling Capacitor (pF)*	*Capacitance switching to Reference (pF)*	*Power (mW)*
1	9, 1.5-bit stages, 3-bit flash	3.0	4.0	138
2	4, 2.5-bit stages, 4-bit flash	1.5	2.5	120
3	3, 3.5-bit stages, 3-bit flash	1.0	2.0	140
4	2.5-bit 1st stage, 6, 1.5-bit stages, and 4-bit flash	2.0	2.5	77
5	3.5-bit 1st stage, 5, 1.5-bit stages, and 4-bit flash	1.0	1.5	50

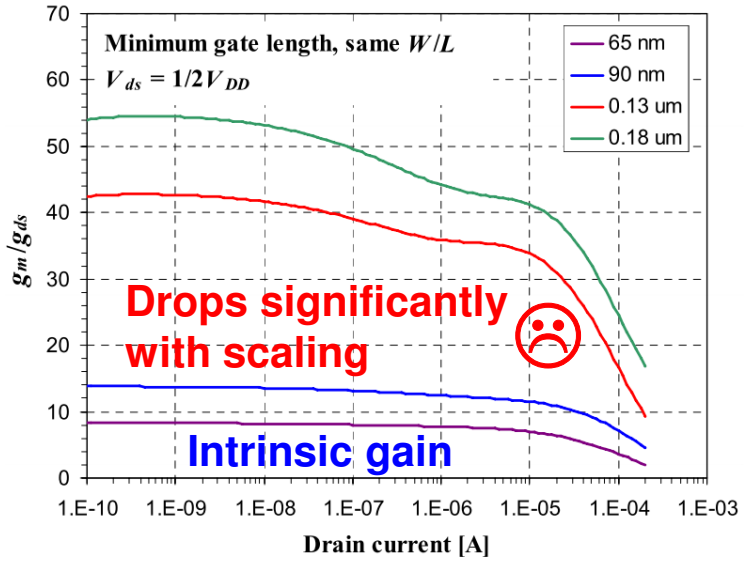
- Optimization based on the following:
  - $V_{in(p-p)(diff)}$=1.5 V
  - Quantization noise is at 12-bit level.
  - Thermal noise limited to 66 dB in 100MHz band.

- **Architecture 5 is optimal.**

Scaling Trend
- Impact On Data Converter Design -

Transconductance and Intrinsic Gain





Courtesy : http://www.eecg.toronto.edu/cider/presentations/ytterdal.pdf

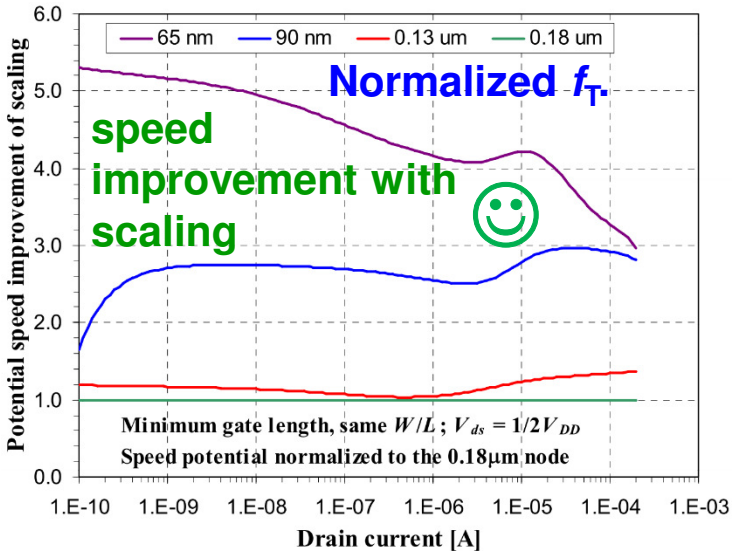
- Transconductance is for all practical purposes independent of technology node.
- For velocity saturated channel:

$$I_d = WC_{ox}V_{eff}v_s$$

$$\Rightarrow g_m = WC_{ox}v_s$$

- With constant field scaling if W gets scaled down by a factor "k" then C_{ox} gets scaled up by a factor of "k" ➔ g_m stays constant.
- Intrinsic gain reduces as technology scales down ➔ the maximum intrinsic gain in 65-nm < 20% of the maximum intrinsic gain in 180-nm

Potential Speed Improvement

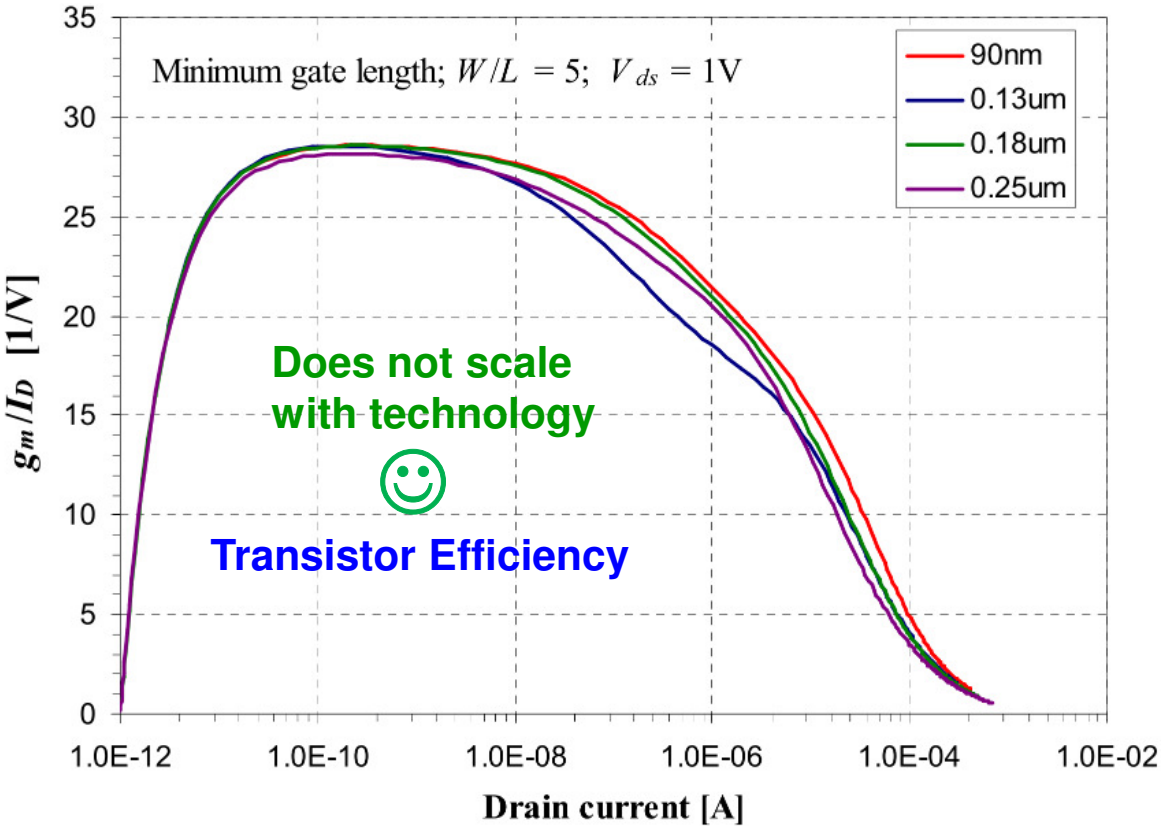


$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{db})}$$

- By scaling down potential speed improvement can be obtained.
- Almost 5 times speed improvement is obtained in 65-nm process over 180-nm process.

Courtesy : http://www.eecg.toronto.edu/cider/presentations/ytterdal.pdf

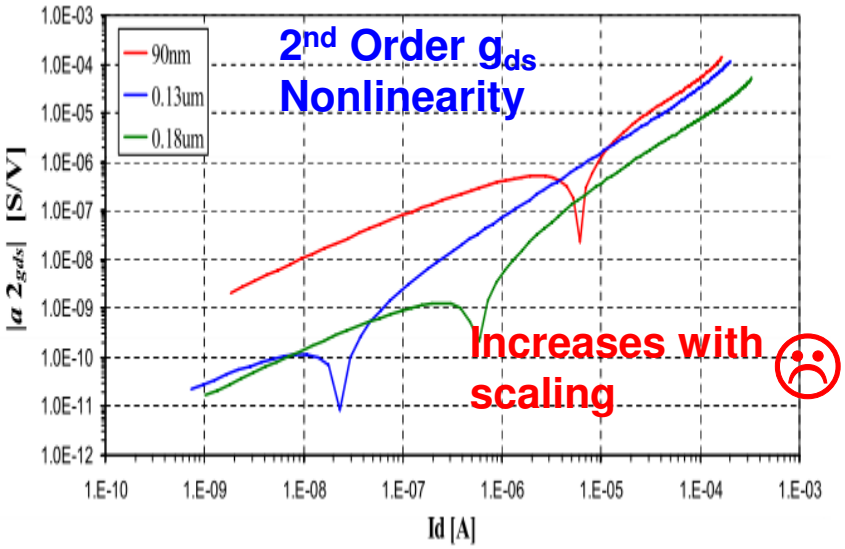
Transistor Efficiency

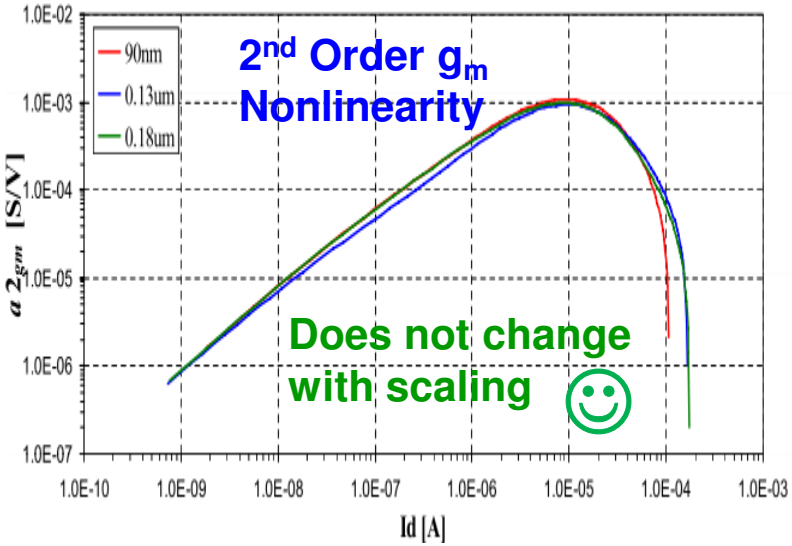


Courtesy : http://www.eecg.toronto.edu/cider/presentations/ytterdal.pdf

- **Maximum efficiency is nearly independent of technology.**

Transistor Linearity



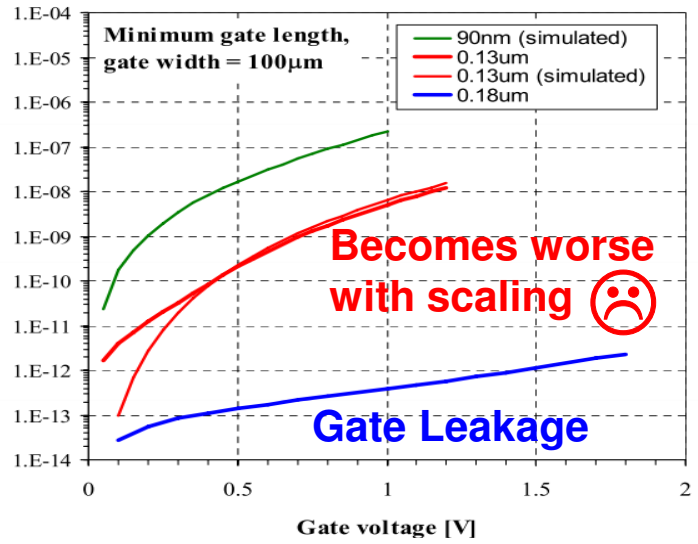


Courtesy : http://www.eecg.toronto.edu/cider/presentations/ytterdal.pdf

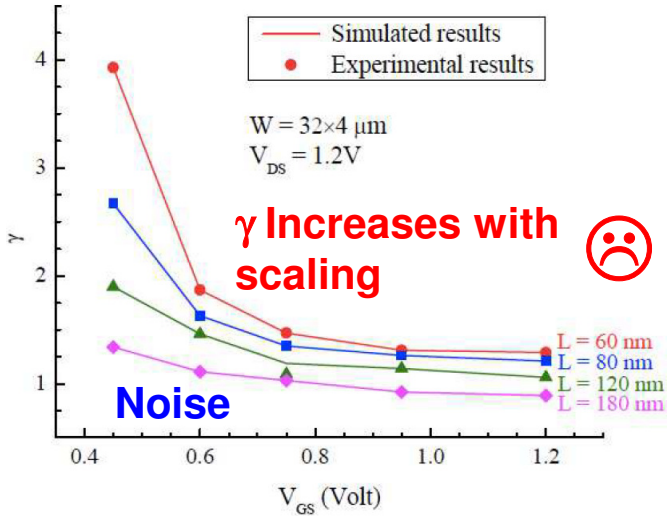
- Increased g_{ds} nonlinearity makes design of linear op amp a challenge in scaled down CMOS.

Gate Leakage and Noise

Courtesy : http://www.eecg.toronto.edu/cider/presentations/ytterdal.pdf

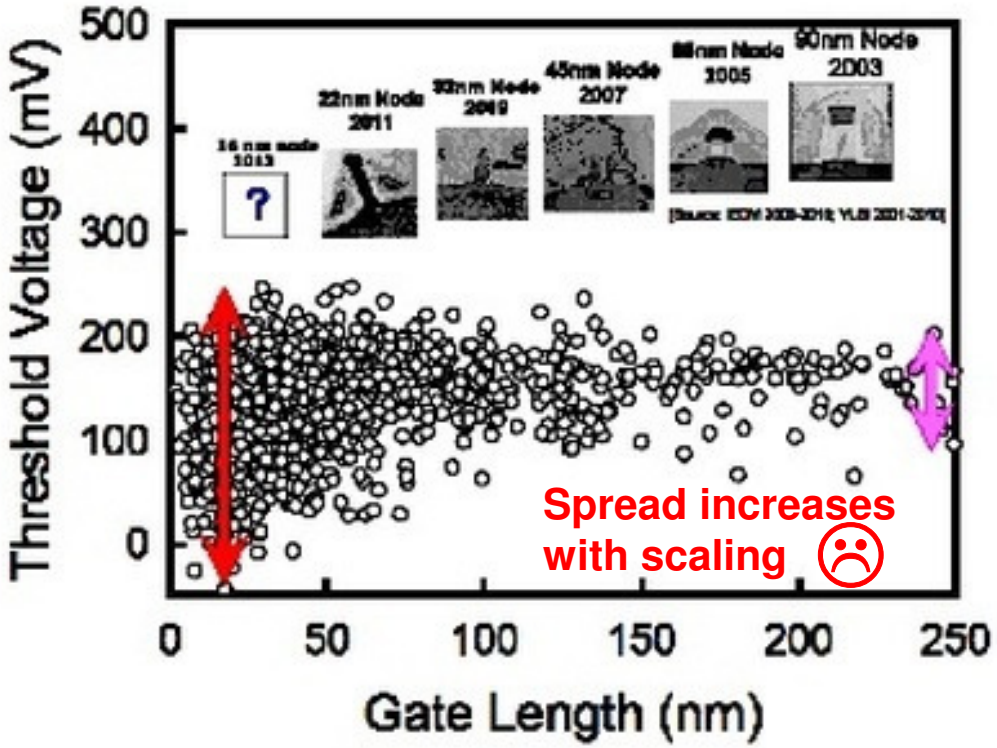


- Gate leakage current dominated by tunneling current.
- Designing highly linear sample-and-hold becomes very challenging as the held value may leak out.



- Noise factor γ increases with reduced channel length.
- Reduces the SNR of the data converters.

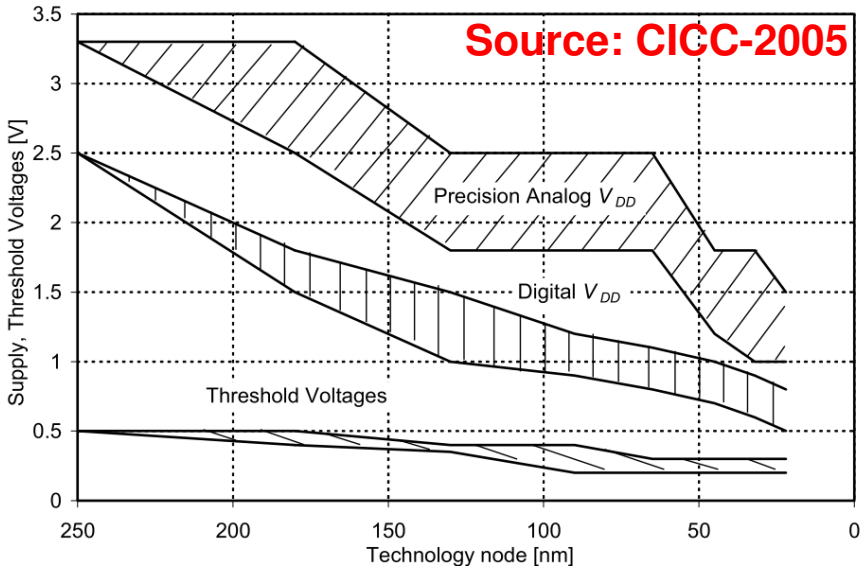
Transistor Performance Trend with Scaling (III)



Courtesy of Prof. Yiming Li, National Chiao Tung University, Taiwan

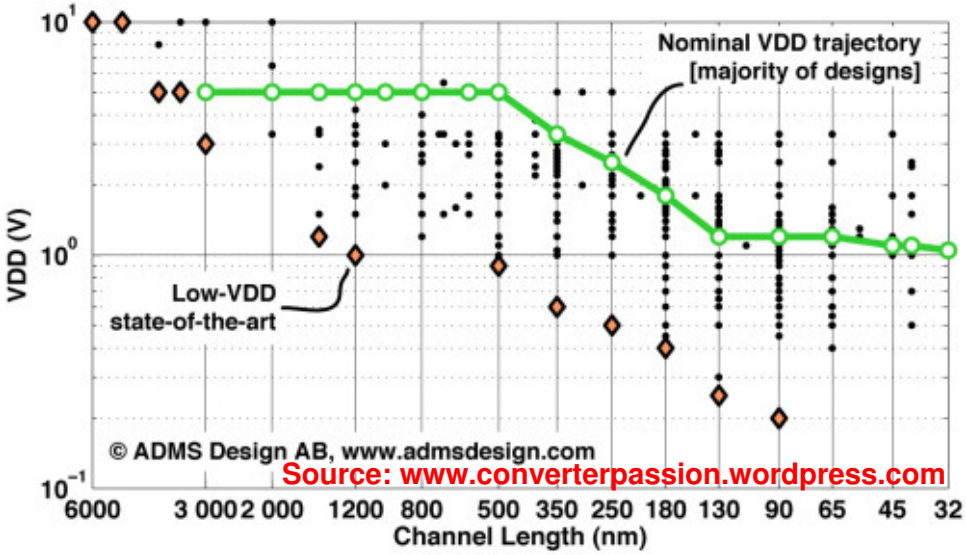
- **Increased spread makes the design of op amps and other precision circuits very challenging.**

Supply Voltage Scaling (I)

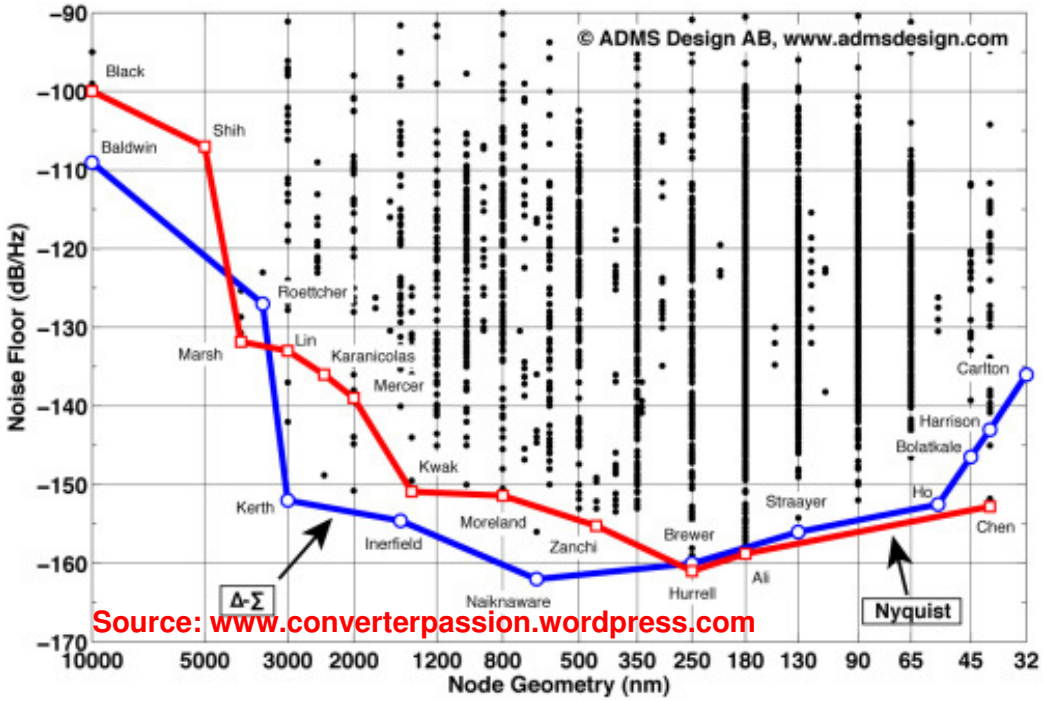


- Supply voltage scaling more aggressive compared to threshold voltage scaling
  - To minimize leakage
- Digital V_{DD} scaling more than Analog V_{DD} scaling.

- Majority of ADC designs have V_{DD} > 1 V.
- However, some ADCs have used V_{DD}'s which are commensurate with digital V_{DD} ➔ especially VCO based architectures.

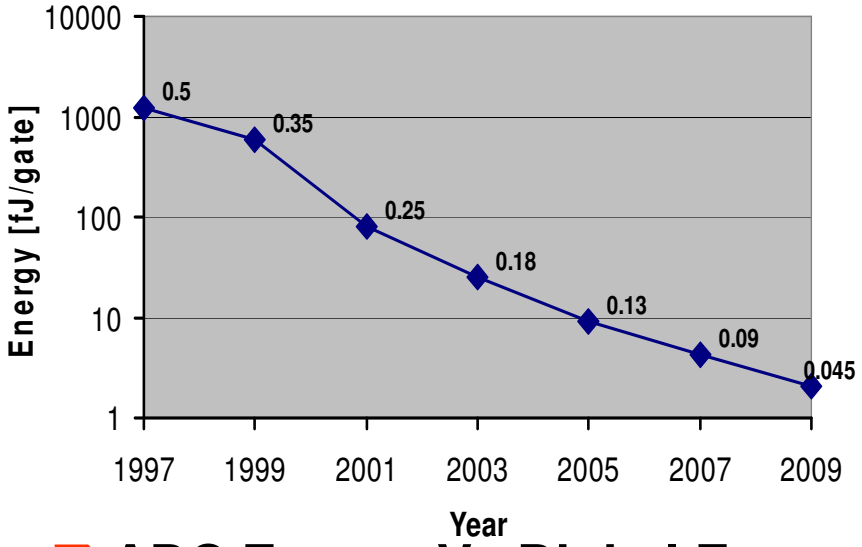


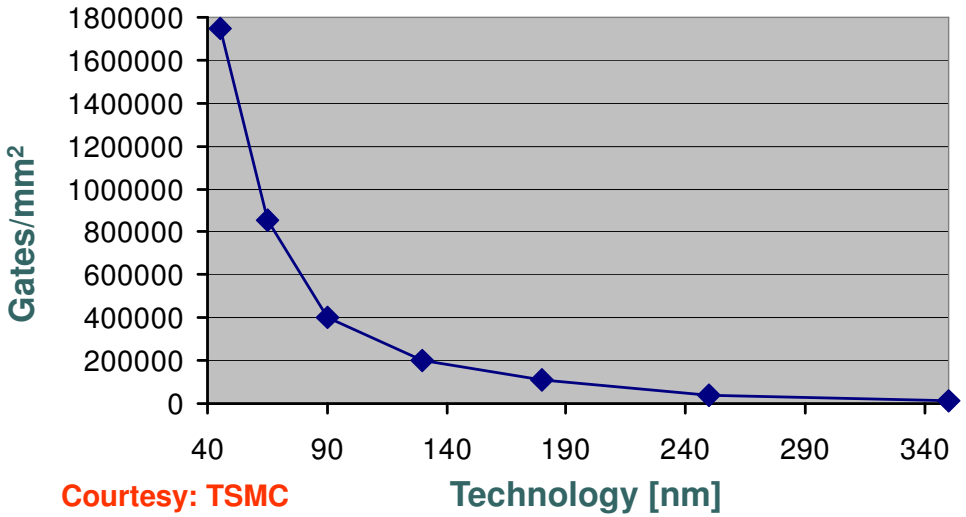
Supply Voltage Scaling (II)



- Scaling of supply voltage ➔ reduction in signal swing ➔ reduction in SNR.
- Achieving an SNR of "x" dB in 10 kHz band is not as attractive as achieving the same in 1 GHz band
- Relative noise floor = $-(SNR + 10 \bullet \log_{10}(BW))$

Digital Circuit Trends





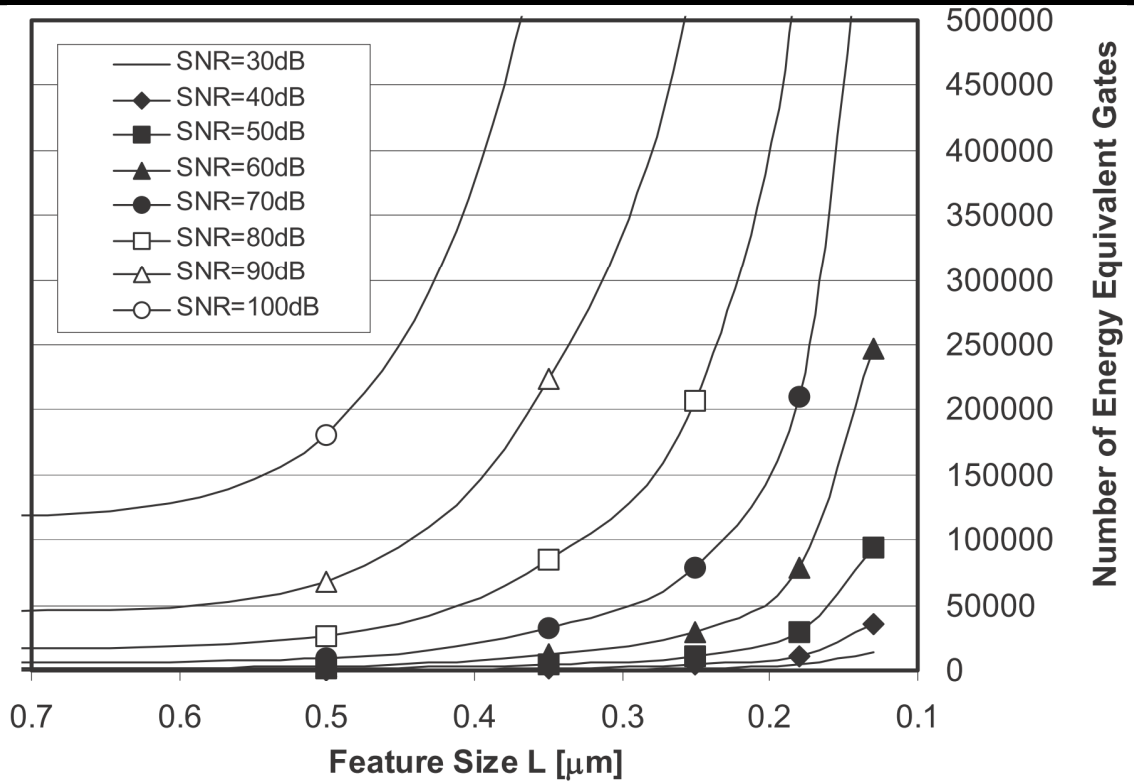
Courtesy: TSMC

- **ADC Energy Vs Digital Energy**
  Example
  - Standard digital gates (NAND2) in 0.13mm CMOS consume about 6nW/Gate/MHz
    - Energy/Gate = 6fJ
  - State-of-the-art 10-bit ADC consumes 1mW/MSample/sec
    - Energy/Conversion = 1nJ
  - Energy equivalent number of gates
    - 1nJ/6fJ= 166,666

Source: http://www.hotchips.org/wp-content/uploads/hc_archives/hc17/3_Tue/HC17.S5/HC17.S5T3.pdf
"Digitally Assisted Analog Design", Boris Murmann.

Bibhudatta Sahoo

ADC/Digital Logic Energy Trends



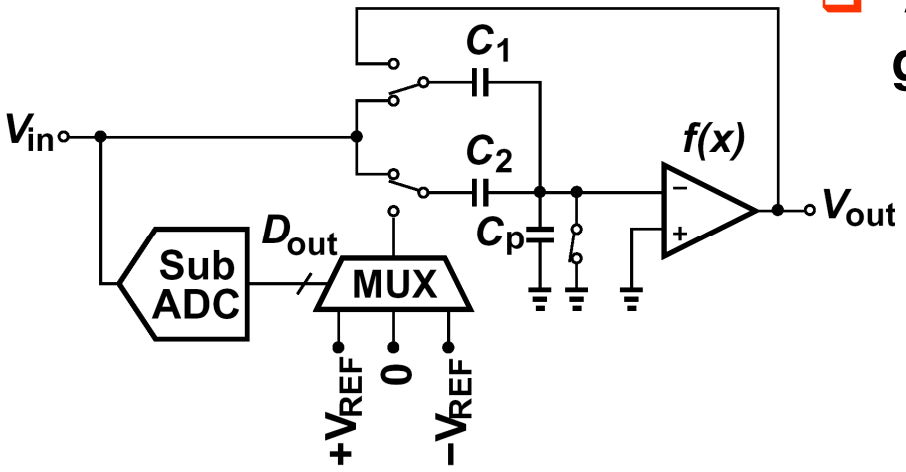
- For SNRs < 50 dB additional digital processing is expensive.
- For SNRs > 50 dB using few tens of thousands of gates has hardly any impact on overall energy.

Source: http://www.hotchips.org/wp-content/uploads/hc_archives/hc17/3_Tue/HC17.S5/HC17.S5T3.pdf
"Digitally Assisted Analog Design", Boris Murmann.

Calibration : A Necessity

Why Calibrate?

Basic Pipeline Stage



$$A_1 = \frac{3\left(1-2^{-(N+1)}\right)}{2^{-(N+1)}}$$

- As technology scales it is difficult to get:
  - get high op amp gain to
    1. remove gain error
    2. suppress nonlinearity
  - low op amp offset.
  - capacitor matching to remove DAC nonlinearity.
- For example, op amp gain in a 12-bit system should exceed 12000 ≈ 81 dB.

Current ADC Design Trends

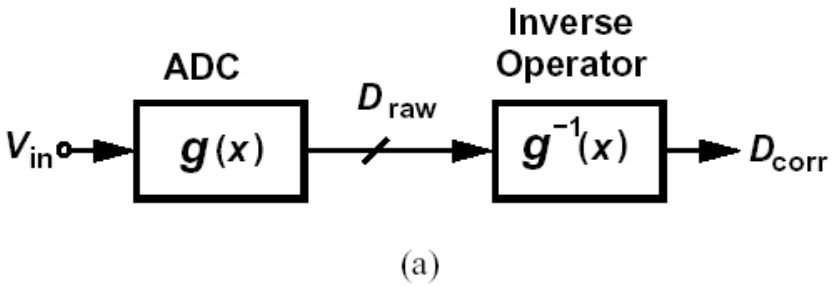
- **Choose capacitors to satisfy kT/C noise, not matching.**
- **Choose op amp with high swing**

  → kT/C noise relaxed

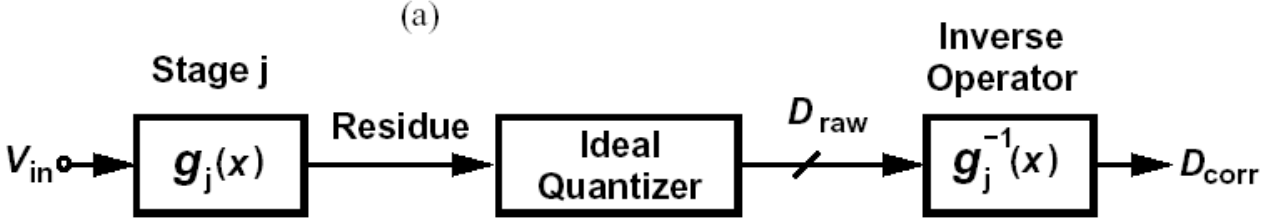
  → power consumption reduced.

  → Relaxes op amp linearity requirement
- **Choose best trade-off between speed, power, and noise of op amp regardless of its gain.**
- **Digitally correct for everything!**

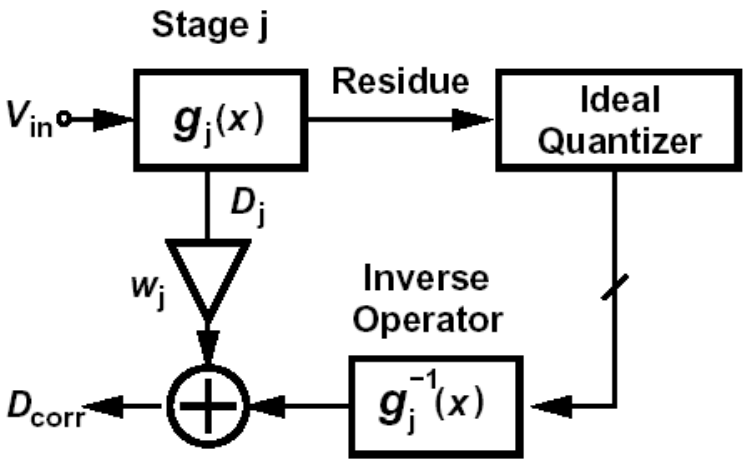
How to Calibrate?



(a)



(b)

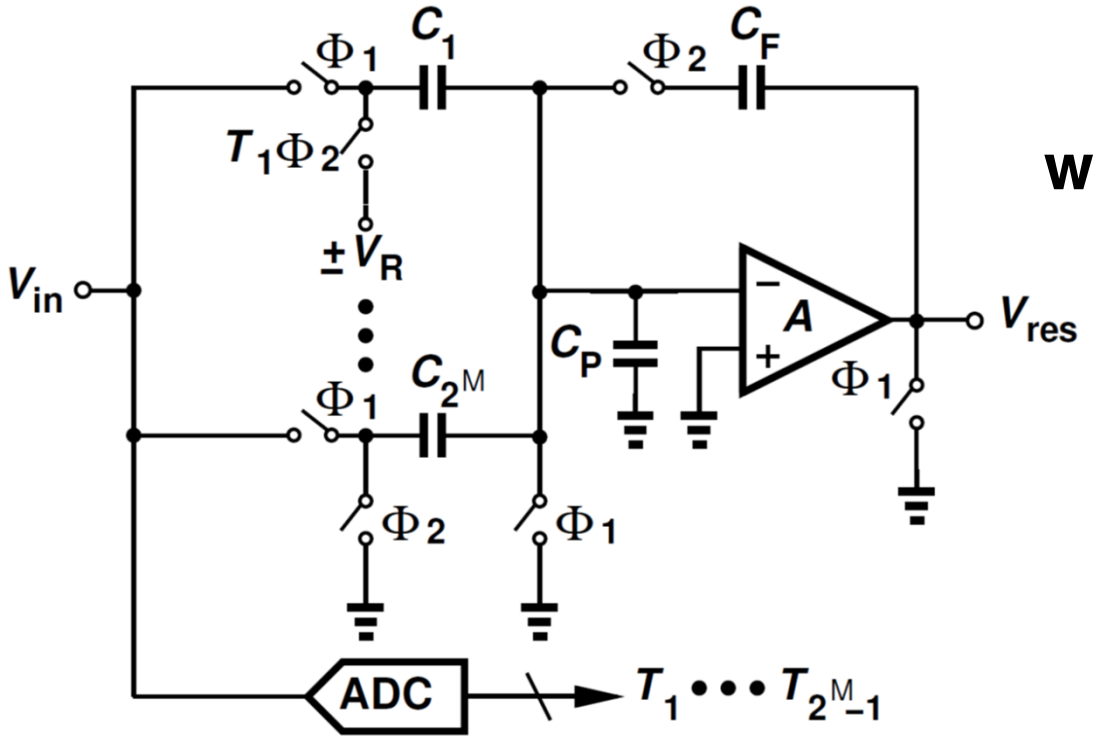


(c)

- **Inverse Operator estimation can be done in:**
  - **Background**
  - **Foreground**

Capacitor Mismatch Calibration

Comparator Forcing Based Calibration



$$V_{res} = \alpha V_{in} + \beta_j V_R$$

where,

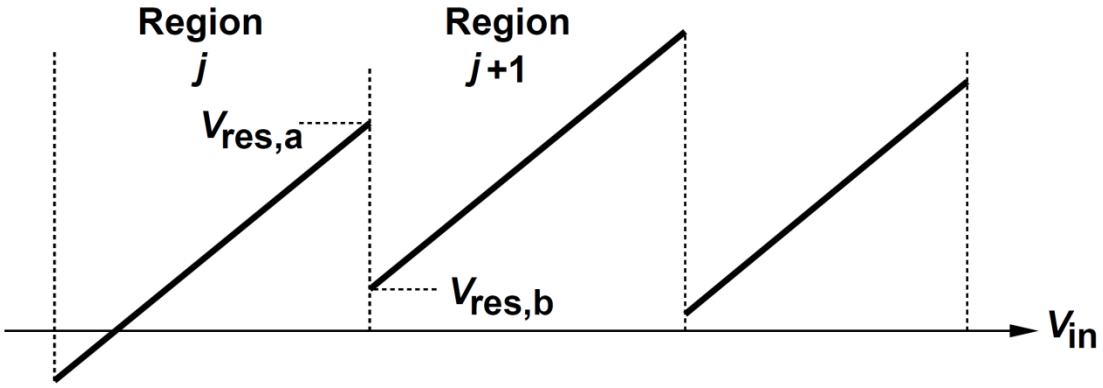
$$\alpha = \frac{\sum_{i=1}^{2^M} C_i}{C_{eq}},$$

$$\beta_j = \frac{\sum_{i=1}^{2^M-1} T_i C_i V_R}{C_{eq}}$$

and $$C_{eq} = C_F + \frac{1}{A}\left(C_F + \sum_{i=1}^{2^M} C_i + C_P\right)$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 48, pp. 1442-1452, Jan. 2013.

Computation of β_j (I)



$$V_{res,b} - V_{res,a} = (\beta_j - \beta_{j+1})V_{REF}$$

$$\downarrow \qquad \downarrow$$

$$D_{j,b} - D_{j,a} = \beta_j - \beta_{j+1}$$

In other words,

$$D_{1,b} - D_{1,a} = \beta_1 - \beta_2$$

$$D_{2,b} - D_{2,a} = \beta_2 - \beta_3$$

$$\vdots$$

$$D_{15,b} - D_{15,a} = \beta_{15} - \beta_{16}$$

Computation of β_j (II)

$$
\begin{aligned}
D_{1,b} - D_{1,a} &= \beta_1 - \beta_2 \\
D_{2,b} - D_{2,a} &= \beta_2 - \beta_3 \\
&\vdots \\
D_{15,b} - D_{15,a} &= \beta_{15} + \beta_1
\end{aligned}
$$

$$
\begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_{15} \end{bmatrix} = \begin{bmatrix} D_{1,b} - D_{1,a} \\ D_{2,b} - D_{2,a} \\ \vdots \\ D_{15,b} - D_{15,a} \end{bmatrix}
$$

In other words,

$$
\Longrightarrow \begin{bmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_{15} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 & \cdots & 1 \\ -1 & 1 & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & \cdots & 1 \end{bmatrix} \begin{bmatrix} D_{1,b} - D_{1,a} \\ D_{2,b} - D_{2,a} \\ \vdots \\ D_{15,b} - D_{15,a} \end{bmatrix}
$$

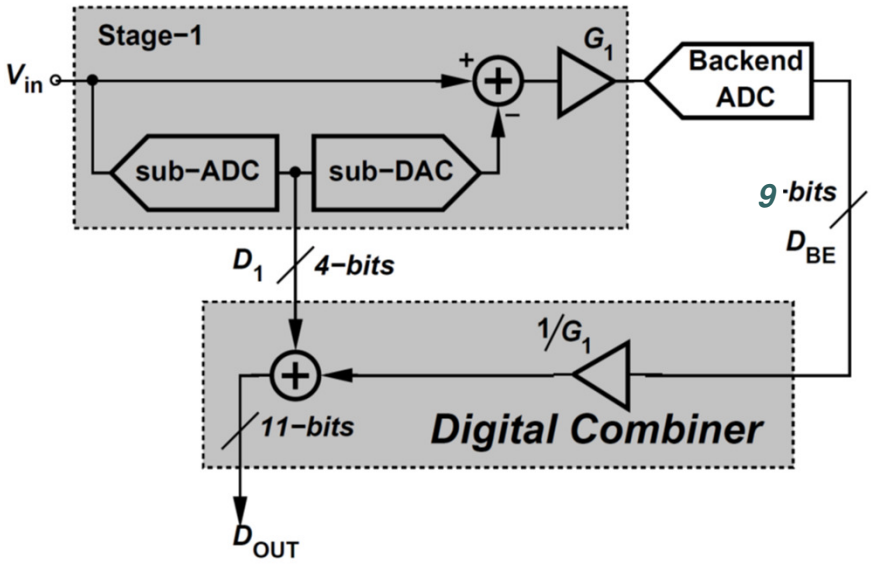
β_j's can be calculated using adders and right shifts.

B. Sahoo and B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC", IEEE Journal of Solid-State Circuits, vol. 48, pp. 1442-1452, Jun. 2013.

A. Karanicolas, et. al., "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC, ", IEEE Journal of Solid-State Circuits, vol. 28, pp. 1207-1215, Dec. 1993.

Capacitor Mismatch Calibration (1)

- **The input output characteristic of a 4-bit stage is:**



$$V_{OUT} = \frac{\sum_{m=1}^{16} C_m V_{IN} - \sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}$$

$$\Rightarrow V_{OUT} = \alpha V_{IN} - \frac{\sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}$$

$$\Rightarrow V_{OUT} = \alpha V_{IN} - \beta_j V_R ,$$

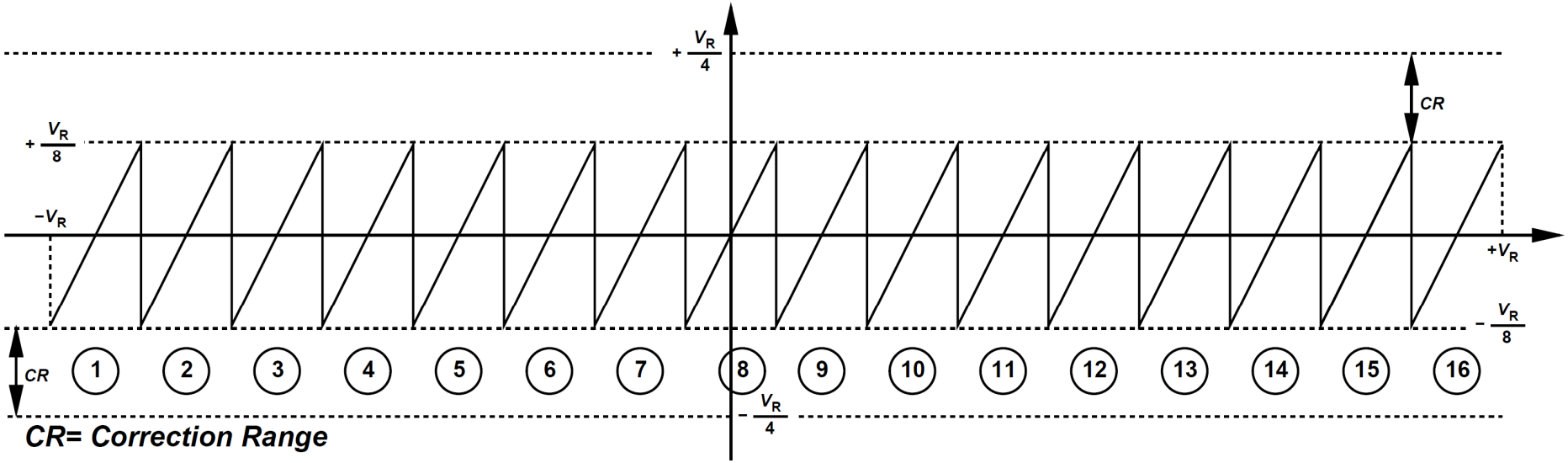
$$\text{where } \beta_j = \frac{\sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}} \text{ and } \alpha = \frac{\sum_{i=1}^{16} C_m}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}.$$

- **Dividing both sides by V_R we get,**

$$D_{BE} = \alpha D_{IN} - \beta_j$$

$$\Rightarrow D_{IN} = \frac{D_{BE}}{\alpha} + \frac{\beta_j}{\alpha}$$

Capacitor Mismatch Calibration (2)



$$\text{Region 1}: D_{BE} = \alpha D_{IN} + \frac{(C_1 + C_2 + \bullet\bullet\bullet + C_{15})}{C_F - \dfrac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \beta_1$$

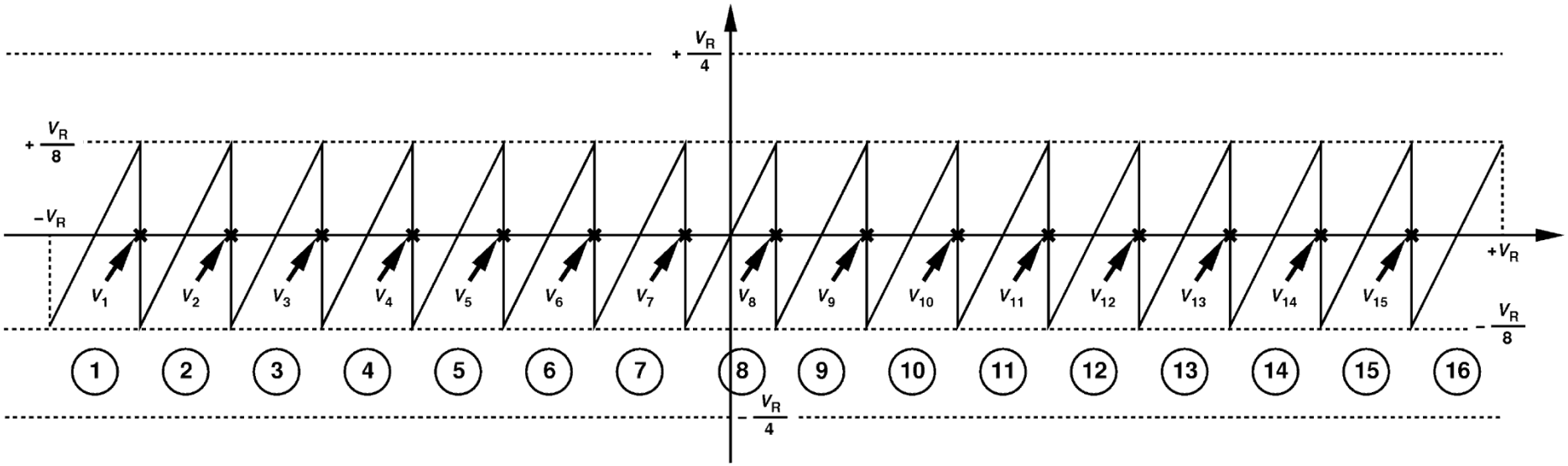
$$\text{Region 2}: D_{BE} = \alpha D_{IN} - \frac{[C_1 - (C_2 + \bullet\bullet\bullet + C_{15})]}{C_F - \dfrac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \beta_2$$

$$\text{Region 3}: D_{BE} = \alpha D_{IN} - \frac{[C_1 + C_2 - (C_3 + \bullet\bullet\bullet + C_{15})]}{C_F - \dfrac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \beta_3$$

$$\text{Region 15}: D_{BE} = \alpha D_{IN} - \frac{[C_1 + C_2 + \bullet\bullet\bullet + C_{14} - C_{15}]}{C_F - \dfrac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \beta_{15}$$

$$\text{Region 16}: D_{BE} = \alpha D_{IN} - \frac{(C_1 + C_2 + \bullet\bullet\bullet + C_{15})}{C_F - \dfrac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} + \beta_1$$

Capacitor Mismatch Calibration (3)



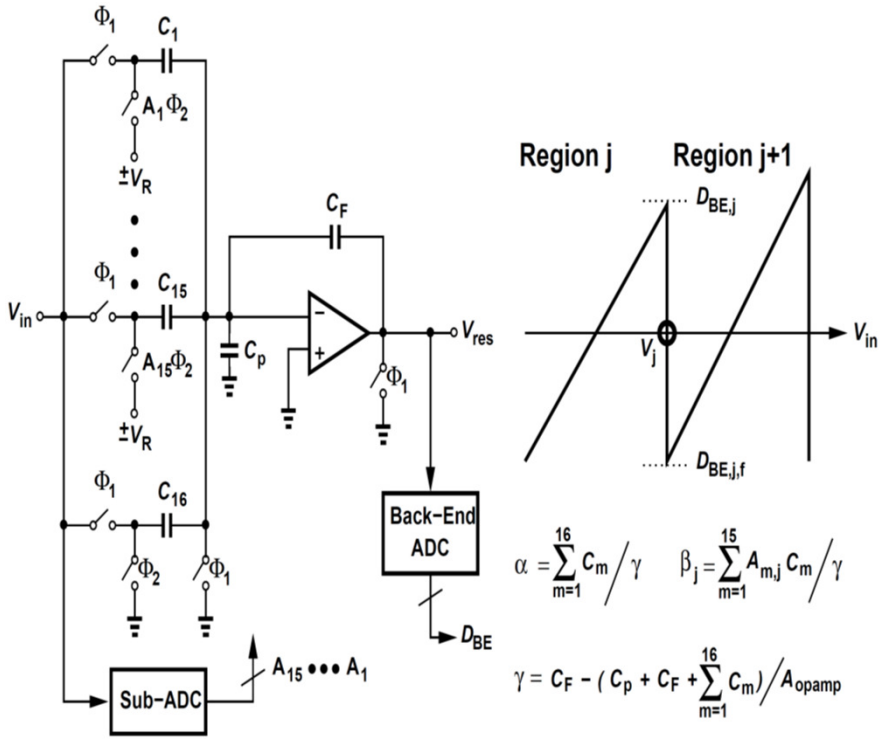
- The digital output goes from 0 to 15 when the input changes from $-V_R$ to $+V_R$.

- Apply V_j close to the comparator threshold and force the flash ADC output so that the residue is once in region j and then in region (j+1).

- The redundancy/offset correction range in the architecture prevents the ADC from clipping.

- The backend ADC gives two different codes for the same input voltage.

Capacitor Mismatch Calibration (4)



- Applying V_j to the ADC in region j we get,

$$D_j = \frac{D_{BE,j}}{\alpha} + \frac{\beta_j}{\alpha}$$

- Similarly applying V_j and forcing the ADC to be in region (j+1) we get,

$$D_{j,f} = \frac{D_{BE,j,f}}{\alpha} + \frac{\beta_{j+1}}{\alpha}$$

- Since, same voltage is applied we can equate both of them:

$$D_{BE,j,f} - D_{BE,j} = \beta_j - \beta_{j+1}$$

which is not dependent on gain error.

- Repeat the above steps for *j=1 to 15*.

Capacitor Mismatch Calibration (5)

- **Thus we end up with:**

$$
\begin{aligned}
D_{BE,1,f} - D_{BE,1} &= \beta_1 - \beta_2 \\
D_{BE,2,f} - D_{BE,2} &= \beta_2 - \beta_3 \\
D_{BE,3,f} - D_{BE,3} &= \beta_3 - \beta_4 \\
D_{BE,4,f} - D_{BE,4} &= \beta_4 - \beta_5 \\
D_{BE,5,f} - D_{BE,5} &= \beta_5 - \beta_6 \\
D_{BE,6,f} - D_{BE,6} &= \beta_6 - \beta_7 \\
D_{BE,7,f} - D_{BE,7} &= \beta_7 - \beta_8 \\
D_{BE,8,f} - D_{BE,8} &= \beta_8 - \beta_9 \\
D_{BE,9,f} - D_{BE,9} &= \beta_9 - \beta_{10} \\
D_{BE,10,f} - D_{BE,10} &= \beta_{10} - \beta_{11} \\
D_{BE,11,f} - D_{BE,11} &= \beta_{11} - \beta_{12} \\
D_{BE,12,f} - D_{BE,12} &= \beta_{12} + \beta_{13} \\
D_{BE,13,f} - D_{BE,13} &= \beta_{13} - \beta_{14} \\
D_{BE,14,f} - D_{BE,14} &= \beta_{14} - \beta_{15} \\
D_{BE,15,f} - D_{BE,15} &= \beta_{15} + \beta_1
\end{aligned}
\quad \Rightarrow \quad
\begin{bmatrix}
1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \\ \beta_4 \\ \beta_5 \\ \beta_6 \\ \beta_7 \\ \beta_8 \\ \beta_9 \\ \beta_{10} \\ \beta_{11} \\ \beta_{12} \\ \beta_{13} \\ \beta_{14} \\ \beta_{15} \end{bmatrix}
=
\begin{bmatrix}
D_{BE,1,f} - D_{BE,1} \\
D_{BE,2,f} - D_{BE,2} \\
D_{BE,3,f} - D_{BE,3} \\
D_{BE,4,f} - D_{BE,4} \\
D_{BE,5,f} - D_{BE,5} \\
D_{BE,6,f} - D_{BE,6} \\
D_{BE,7,f} - D_{BE,7} \\
D_{BE,8,f} - D_{BE,8} \\
D_{BE,9,f} - D_{BE,9} \\
D_{BE,10,f} - D_{BE,10} \\
D_{BE,11,f} - D_{BE,11} \\
D_{BE,12,f} - D_{BE,12} \\
D_{BE,13,f} - D_{BE,13} \\
D_{BE,14,f} - D_{BE,14} \\
D_{BE,15,f} - D_{BE,15}
\end{bmatrix}
$$

- **Solving for β_j is straight forward and does not require multiplication.**

Capacitor Mismatch Calibration (6)

- Thus β_j can be obtained as follows without the need of multipliers:

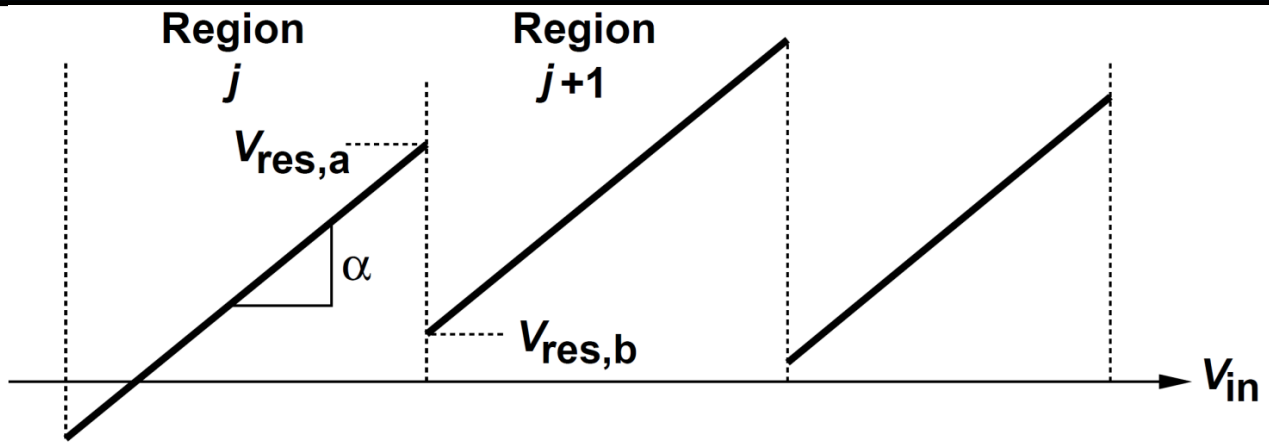
$$\begin{bmatrix}\beta_1\\ \beta_2\\ \beta_3\\ \beta_4\\ \beta_5\\ \beta_6\\ \beta_7\\ \beta_8\\ \beta_9\\ \beta_{10}\\ \beta_{11}\\ \beta_{12}\\ \beta_{13}\\ \beta_{14}\\ \beta_{15}\end{bmatrix} = \frac{1}{2}\begin{bmatrix}1&1&1&1&1&1&1&1&1&1&1&1&1&1&1\\ -1&1&1&1&1&1&1&1&1&1&1&1&1&1&1\\ -1&-1&1&1&1&1&1&1&1&1&1&1&1&1&1\\ -1&-1&-1&1&1&1&1&1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&1&1&1&1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&1&1&1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&1&1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&-1&1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&1&1\\ -1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&-1&1\end{bmatrix}\begin{bmatrix}D_{BE,1,f}-D_{BE,1}\\ D_{BE,2,f}-D_{BE,2}\\ D_{BE,3,f}-D_{BE,3}\\ D_{BE,4,f}-D_{BE,4}\\ D_{BE,5,f}-D_{BE,5}\\ D_{BE,6,f}-D_{BE,6}\\ D_{BE,7,f}-D_{BE,7}\\ D_{BE,8,f}-D_{BE,8}\\ D_{BE,9,f}-D_{BE,9}\\ D_{BE,10,f}-D_{BE,10}\\ D_{BE,11,f}-D_{BE,11}\\ D_{BE,12,f}-D_{BE,12}\\ D_{BE,13,f}-D_{BE,13}\\ D_{BE,14,f}-D_{BE,14}\\ D_{BE,15,f}-D_{BE,15}\end{bmatrix}$$

- Combining the bits with appropriate β_j:
  - Flash ADC output tells us which region the analog voltage is in.
  - The above information can be used appropriately combine the bits.

Gain Calibration for Multi-bit MDAC

Computation of α

$$\alpha = \frac{C_1 + \cdots + C_{16}}{C_{eq}}$$



- Need to obtain C_1/C_{eq}, C_2/C_{eq},…, C_{16}/C_{eq}.
- Fortunately $\beta_{j+1} - \beta_j = \frac{C_1 + \cdots + C_{j+1}}{C_{eq}} - \frac{C_1 + \cdots + C_j}{C_{eq}}$

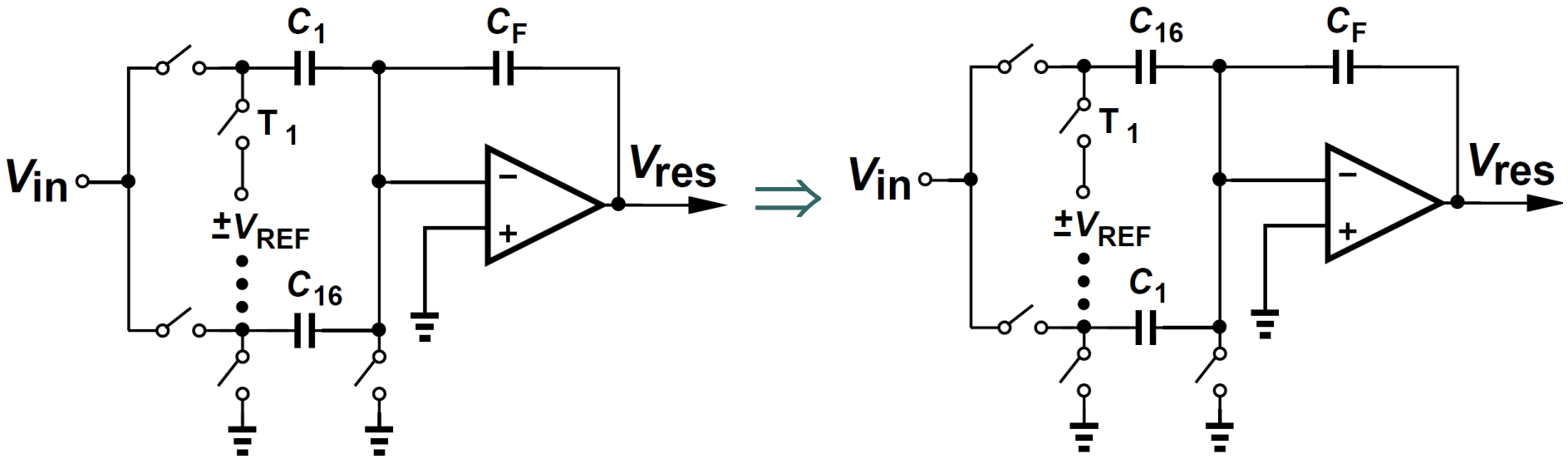
$$= \frac{C_{j+1}}{C_{eq}}$$

- We already have these values from previous measurements

$$D_{1,b} - D_{1,a} = \beta_1 - \beta_2$$
$$D_{2,b} - D_{2,a} = \beta_2 - \beta_3$$
$$\vdots$$
$$D_{15,b} - D_{15,a} = \beta_{15} + \beta_1$$

Computation of C_{16}/C_{eq}

- **Swap C_1 and C_{16}:**

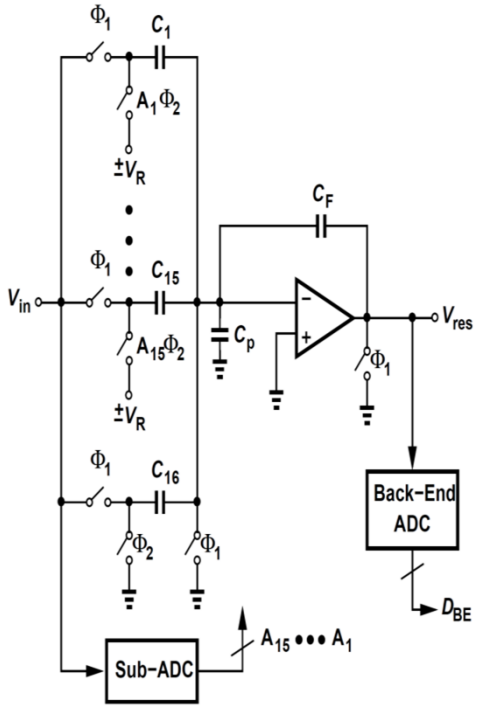


$$\Rightarrow \beta_{16} = \frac{C_2 + \cdots + C_{16}}{C_{eq}} \Rightarrow \frac{C_{16}}{C_{eq}} = \beta_{16} - \beta_{15}$$

- **Thus, $\alpha = \frac{C_1 + \cdots + C_{16}}{C_{eq}}$ is obtained.**

Gain Error Calibration (1)

- We can obtain a similar set of measurements by connecting C_{16} to $\pm V_R$ (controlled by A_1) and C_1 to V_{CM}.
- Instead of β_1 to β_{15} we can define η_1 to η_{15} as shown on the side.
- Similarly we can solve for η_1 to η_{15} by matrix inversion.



$$\text{Region 1}: D_{BE} = \alpha D_{IN} + \frac{(C_{16} + C_2 + \bullet\bullet\bullet + C_{15})}{C_F - \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \eta_1$$

$$\text{Region 2}: D_{BE} = \alpha D_{IN} - \frac{[C_{16} - (C_2 + \bullet\bullet\bullet + C_{15})]}{C_F + \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \eta_2$$

$$\text{Region 3}: D_{BE} = \alpha D_{IN} - \frac{[C_{16} + C_2 - (C_3 + \bullet\bullet\bullet + C_{15})]}{C_F + \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \eta_3$$

$$\vdots$$

$$\text{Region 15}: D_{BE} = \alpha D_{IN} - \frac{[C_{16} + C_2 + C_3 + \bullet\bullet\bullet - C_{15}]}{C_F + \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} - \eta_{15}$$

$$\text{Region 16}: D_{BE} = \alpha D_{IN} - \frac{(C_{16} + C_2 + C_3 + \bullet\bullet\bullet + C_{15})}{C_F + \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}} = \alpha D_{IN} + \eta_1$$

Gain Error Calibration (2)

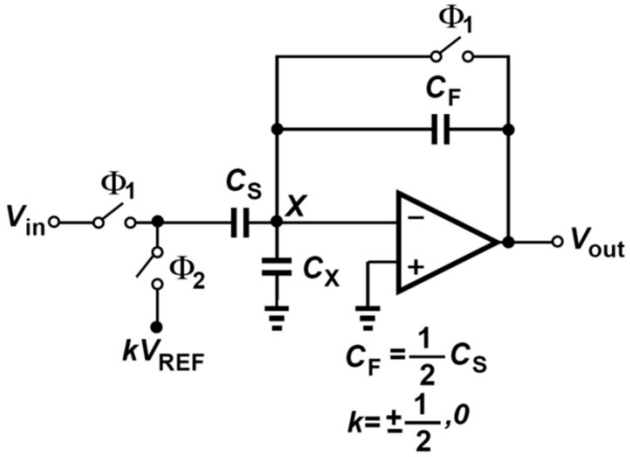
- We can rewrite β_1 to β_{15} in terms C_1 to C_{16} as shown below:

$$\frac{1}{\left(C_F - \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}\right)} \begin{bmatrix} -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \\ C_7 \\ C_8 \\ C_9 \\ C_{10} \\ C_{11} \\ C_{12} \\ C_{13} \\ C_{14} \\ C_{15} \end{bmatrix} = \begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \\ \beta_4 \\ \beta_5 \\ \beta_6 \\ \beta_7 \\ \beta_8 \\ \beta_9 \\ \beta_{10} \\ \beta_{11} \\ \beta_{12} \\ \beta_{13} \\ \beta_{14} \\ \beta_{15} \end{bmatrix}$$

- Similarly, we can rewrite η_1 to η_{15} in terms C_2 to C_{16}.
- Solving the two matrices we can obtain $C_i/(C_F\text{-}C_X)$ where, $C_X = \frac{C_F + C_P + \sum_{i=1}^{16} C_i}{A}$ for i=1 to 16.
- Gain error, $\alpha = \sum_{i=1}^{16} \frac{C_i}{C_F - C_X}$

Gain Error Calibration – 1.5 bit stages

- Backend stages ➔ need gain error calibration.
- Perturbation based calibration [1]:
  - Applying V_{IN} we get D_0 and D_{BE0}.
  - Applying $(V_{IN} + \Delta)$ we get D_1 and D_{BE1}.
  - Applying Δ we get D_0 and $D_{BE\Delta}$.
- V_{IN} and $(V_{IN} + \Delta)$ should produce different codes.



- Thus, gain error γ is obtained as follows:

$$(V_{IN} + \Delta) - V_{IN} - \Delta = 0$$

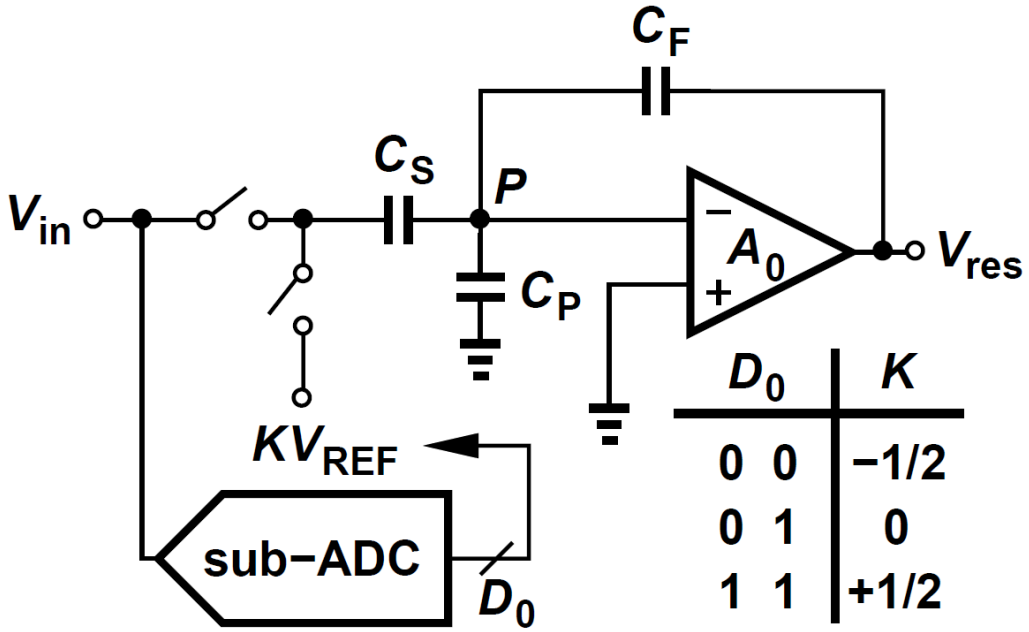
$$\Rightarrow D_1 + \gamma D_{BE1} - D_0 - \gamma D_{BE0} - D_0 - \gamma D_{BE\Delta} = 0$$

$$\Rightarrow \gamma = \frac{D_1}{D_{BE0} + D_{BE\Delta} - D_{BE1}}$$

[1] B. Sahoo and B. Razavi, "A 12-Bit 200-MHz CMOS ADC," IEEE Journal of Solid-State Circuits, vol. 44, pp. 2366-2380, Sept. 2009

Gain Calibration for 1.5-bit Non-flip-around MDAC

1.5-Bit Stages

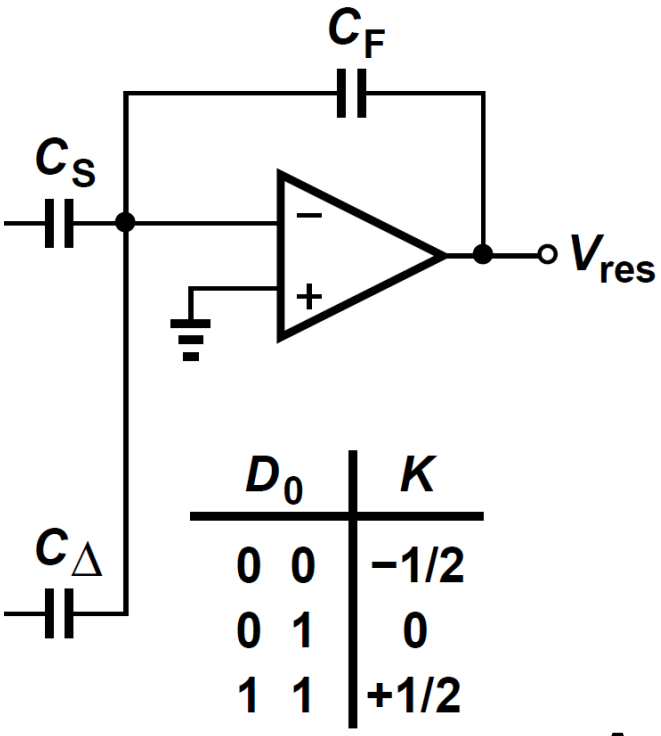


$$V_{res} = \frac{C_S}{C_F + \frac{C_S+C_F+C_P}{A_0}}(V_{in} - KV_{REF}) \Rightarrow D_{in} = K + \frac{1}{\alpha}D_{BE}$$

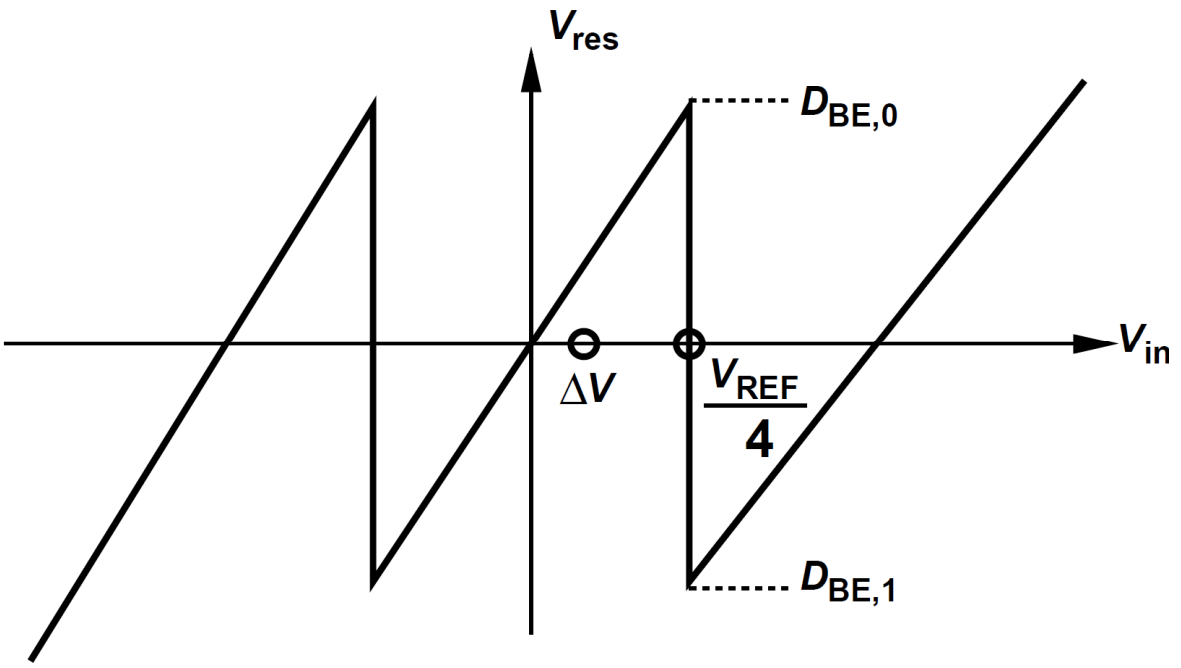
where, $\alpha = \dfrac{C_S}{C_F + \frac{C_S+C_F+C_P}{A_0}}$ is the gain.

- C_S and C_F cannot be swapped to obtain gain as it would lead to over-range.

Calibration Algorithm* (1.5-Bit Stages)



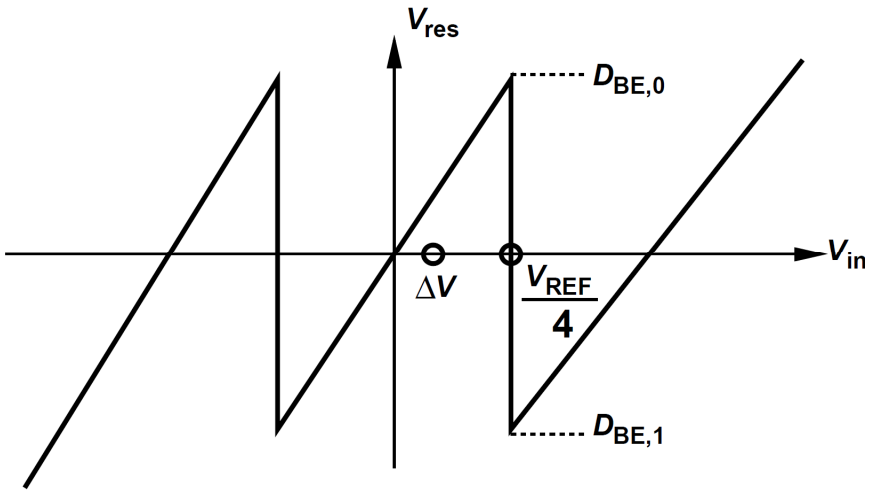
D_0	K
0 0	−1/2
0 1	0
1 1	+1/2



- Apply $\Delta V \approx 10$ mV
- Apply $V_{REF}/4$
- Apply $V_{REF}/4+\Delta V$

* B. Sahoo and B. Razavi, *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2366-2380, Sept. 2009

1.5-Bit Stages - Computing Inverse Gain (1/α)



- **Apply ΔV**

$$D_a = D_{sub,a} + \frac{1}{\alpha} D_{BE,a}$$

- **Apply V_{REF}/4, force comparator output to be "0"**

$$D_b = D_{sub,b} + \frac{1}{\alpha} D_{BE,b}$$

- **Apply (V_{REF}/4+ΔV), force comparator output to be "1"**

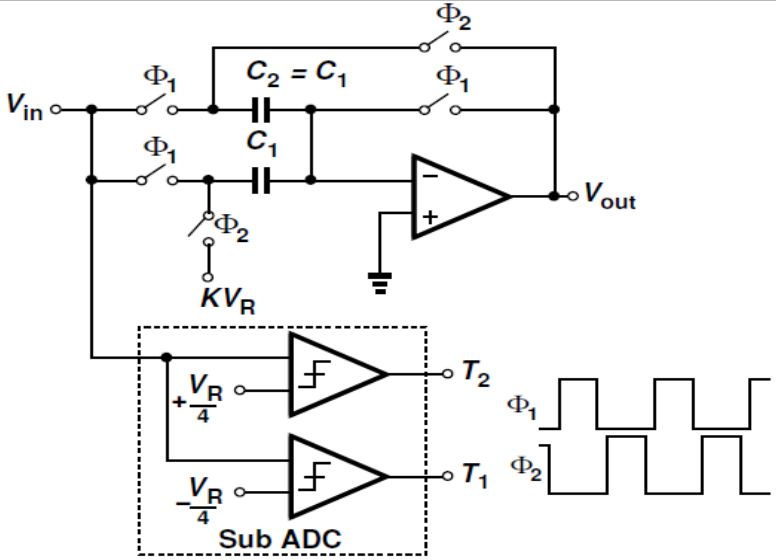
$$D_c = D_{sub,c} + \frac{1}{\alpha} D_{BE,c}$$

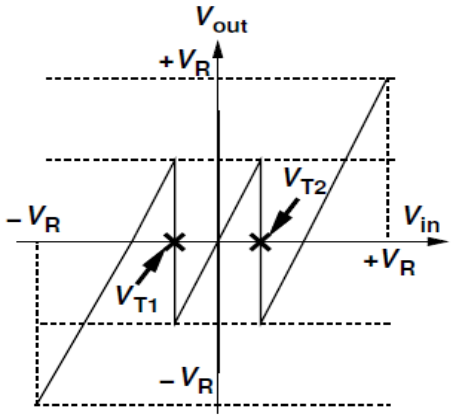
Inverse Gain : $\frac{1}{\alpha} = \frac{D_{sub,c}}{D_{BE,a} + D_{BE,b} - D_{BE,c}}$

- **Obtained using Newton-Raphson iterative method instead of division.**

Gain Calibration for 1.5-bit Flip-around, 2.5-bit, etc. MDAC

Gain Calibration for 1.5-bit Flip-around MDAC (1)





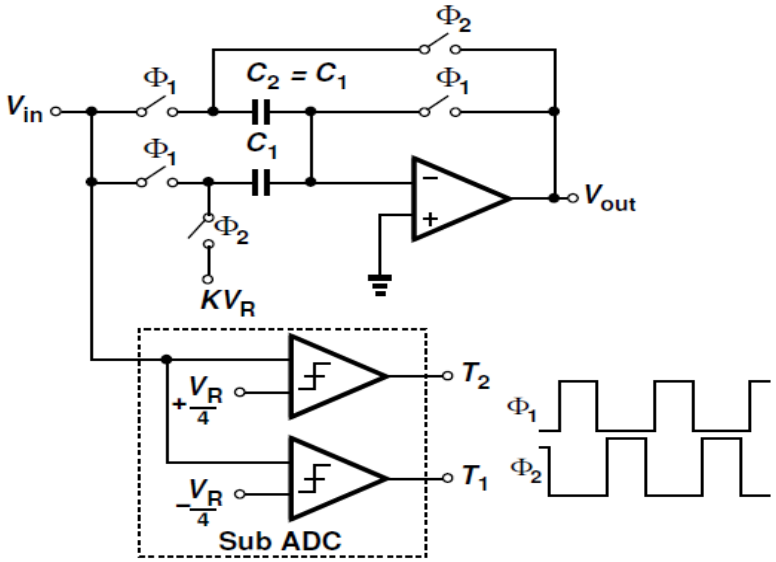
$$V_{out} = \frac{C_1+C_2}{C_2+\frac{C_1+C_2+C_P}{A}} V_{in} - \frac{C_1}{C_2+\frac{C_1+C_2+C_P}{A}} KV_R, \text{ where } K = \pm 1, 0$$

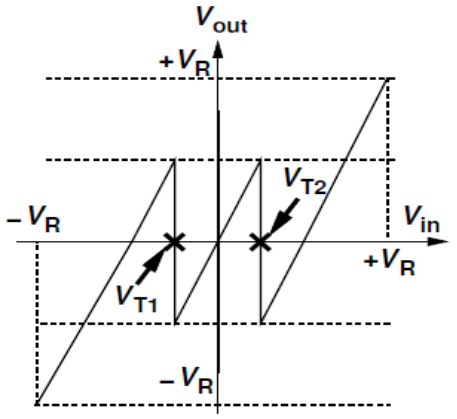
$$\Rightarrow V_{out} = \alpha V_{in} - K\beta V_R, \text{ where } \alpha = \frac{C_1+C_2}{C_2+\frac{C_1+C_2+C_P}{A}}, \text{ and } \beta = \frac{C_1}{C_2+\frac{C_1+C_2+C_P}{A}}$$

- β can be solved by applying V_{T1} or V_{T2} and forcing the corresponding comparator to "1" or "0".
- Unlike, an N-bit architecture as mentioned earlier we cannot swap the capacitors here to solve for α.
- Swapping capacitors changes the denominator $C_2 + \frac{C_1+C_2+C_P}{A}$ to $C_1 + \frac{C_1+C_2+C_P}{A}$

* C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015

Gain Calibration for 1.5-bit Flip-around MDAC (2)





$$V_{out} = \frac{C_1+C_2}{C_2+\frac{C_1+C_2+C_P}{A}} V_{in} - \frac{C_1}{C_2+\frac{C_1+C_2+C_P}{A}} KV_R, \text{ where } K = \pm 1, 0$$

$$\Rightarrow V_{out} = \alpha V_{in} - K\beta V_R, \text{ where } \alpha = \frac{C_1+C_2}{C_2+\frac{C_1+C_2+C_P}{A}}, \text{ and } \beta = \frac{C_1}{C_2+\frac{C_1+C_2+C_P}{A}}$$

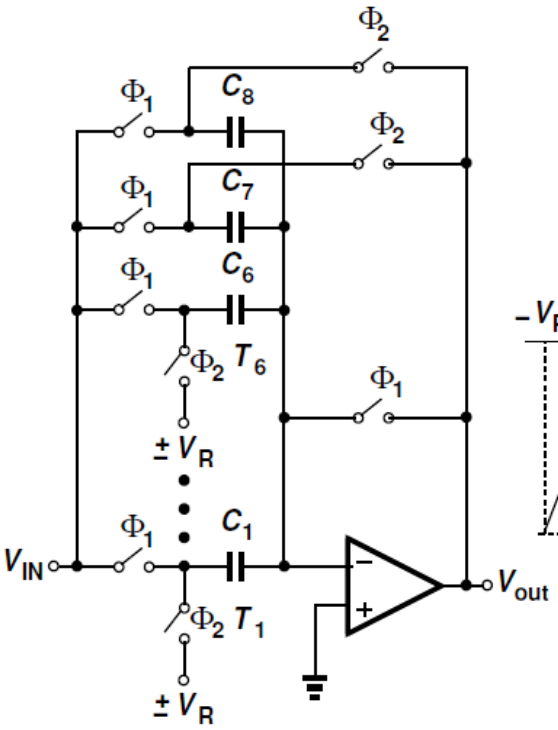
- Applying V_R the back-end ADC output can be given as:

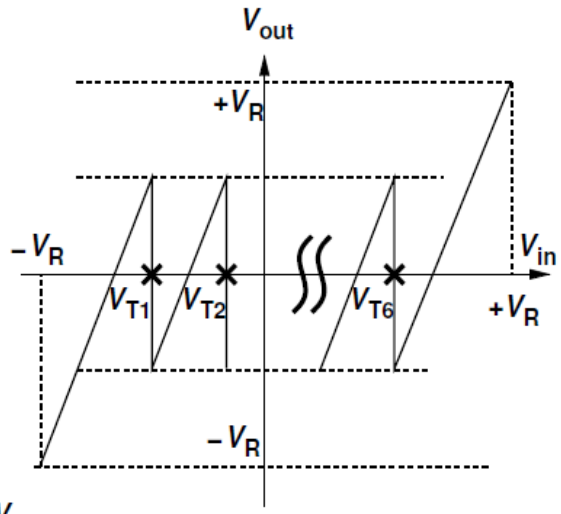
$$V_{out} = \alpha V_R - \beta V_R \Rightarrow V_{out} = \frac{C_2}{C_2 + \frac{C_1 + C_2 + C_P}{A}} V_R \Rightarrow D_{BE} = \frac{C_2}{C_2 + \frac{C_1 + C_2 + C_P}{A}}$$

- The β obtained using the comparator forcing algorithm can be added to the above D_{BE} measurement to obtain α

* C. Ravi, V. Sarma, and B. Sahoo,“ IEEE NEWCAS, June 2015

Gain Calibration for 2.5-bit Flip-around MDAC





$$V_{out} = \frac{\sum_{i=1}^{8} C_i V_{in}}{C_7 + C_8 + \frac{\sum_{i=1}^{8} C_i + C_P}{A}} - \frac{\sum_{i=1}^{6} T_i C_i}{C_7 + C_8 + \frac{\sum_{i=1}^{8} C_i + C_P}{A}} V_R$$

$$\Longrightarrow V_{out} = \alpha V_{in} - \beta_i V_R$$

- Comparator forcing based calibration technique is used to obtain β_1 to β_6.
- Just as in 1.5-bit flip-around topology swapping capacitor changes the denominator and hence cannot be used to solve for the gain α.
- Applying the full-scale input to the MDAC and digitizing the output using the backend we obtain,

$$D_{BE} = \frac{C_7 + C_8}{C_7 + C_8 + \frac{\sum_{i=1}^{8} C_i + C_P}{A}}$$

- Now, $\beta_6 = \frac{\sum_{i=1}^{6} C_i}{C_7 + C_8 + \frac{\sum_{i=1}^{8} C_i + C_P}{A}}$.
- $\alpha = D_{BE} + \beta_6$
- Can be extended to 3.5-bit.

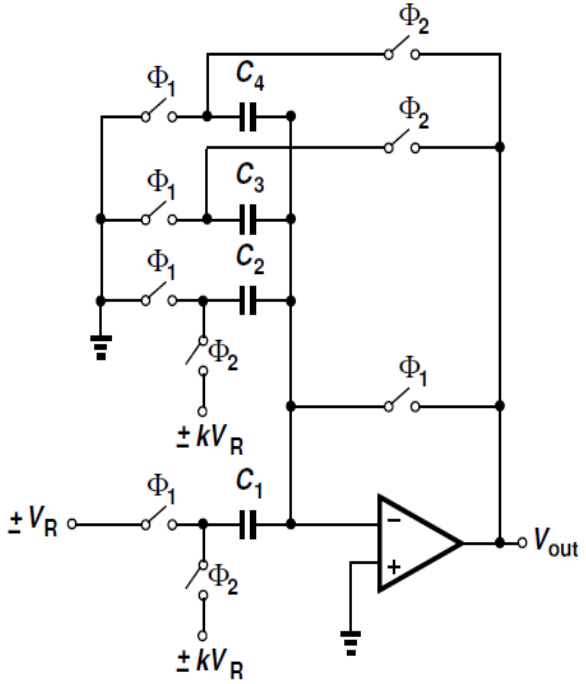
* C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015

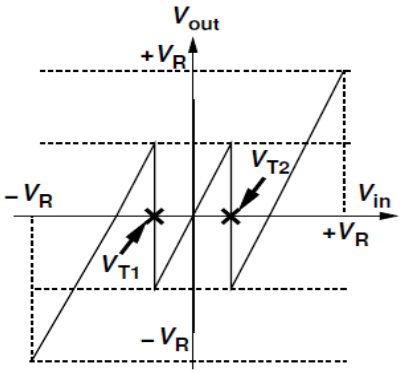
Calibration at Full-Speed

- **Speed of existing calibration methods are limited by**
  - **Circuitry which applies the calibration inputs**
- **Calibration at low speed doesn't capture the error in residue**
  - **Due to insufficient settling of the op amp at high frequency**
  - **Incorrect gain estimation**
- **In order to facilitate calibration at full-speed the calibration voltages have to be generated using capacitors switching to $\pm V_R$.**
- **This eliminates the resistor ladder to generate the calibration voltages.**

*** C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015**

Calibration Signal Generation for 1.5-bit Stage (1)

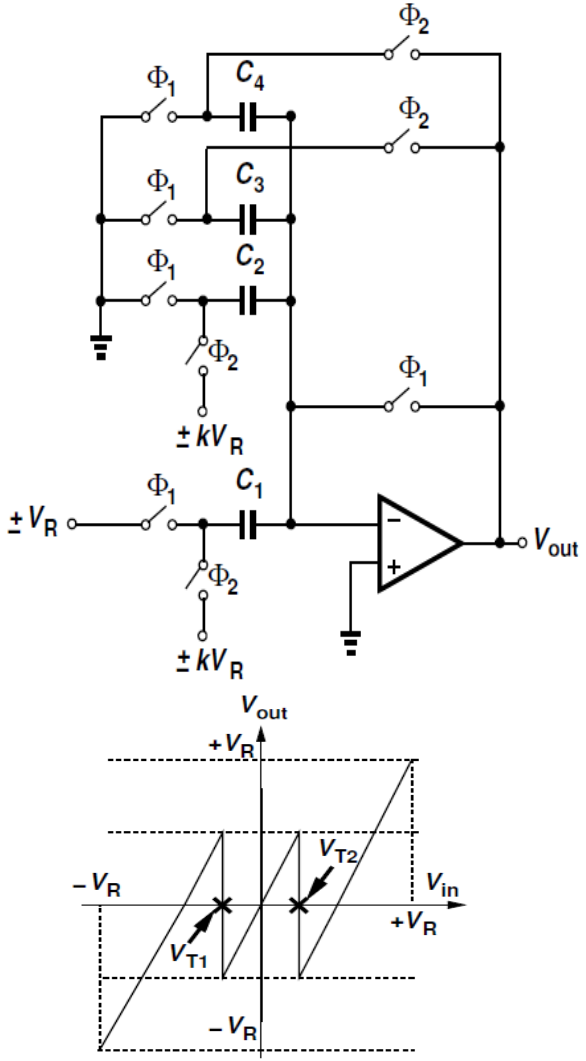




- **Split the sampling capacitor and the feedback capacitor into two equal unit capacitors**
- **During normal operation**
  - **Sampling phase: Input is sampled onto all the capacitors**
  - **Amplification phase: 2 capacitors are flipped around**
  - **Remaining two capacitors switch to KV_R**

*** C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015**

Calibration Signal Generation for 1.5-bit Stage (2)



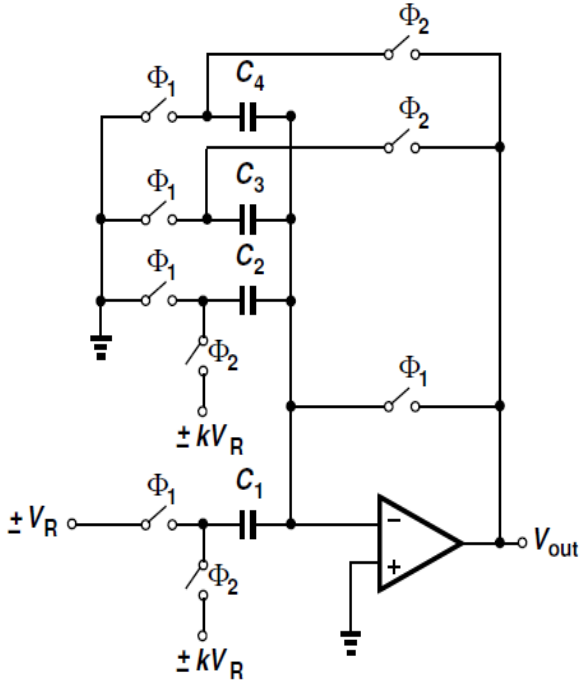
- During Calibration,
  - Sampling phase: $-V_R$ sampled onto one sampling capacitors
  - Remaining capacitors connected to ground for applying $V_{T1} = -V_R/4$.
  - Amplification phase: Two capacitors connected to KV_R
  - Two capacitors flipped around
- Resulting residue voltage is

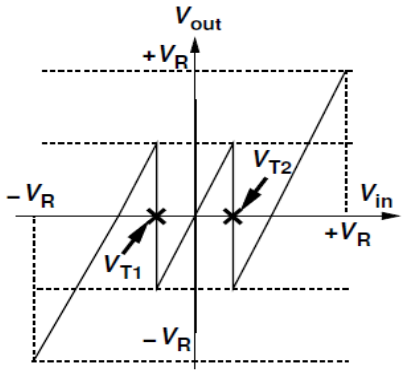
$$V_{out} = \frac{-V_R C_1 + KV_R(C_1 + C_2)}{C_3 + C_4 + \frac{C_1 + C_2 + C_3 + C_4}{A}}$$

- This residue is same as if $V_{IN} = -V_R/4$ is applied

* C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015

Calibration Signal Generation for 1.5-bit Stage (3)

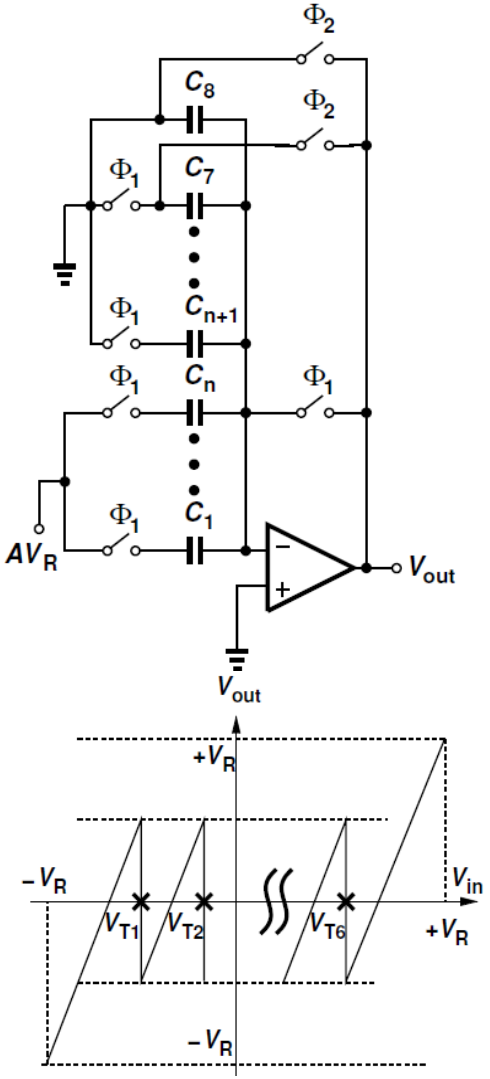




- **Similarly, we can mimic the generation of $V_{T2} = V_R/4$ by**
  - **Applying V_R to one sampling capacitor**
  - **Remaining connected to ground**

*** C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015**

Calibration Signal Generation for 2.5-bit Stage



- Calibration voltages for 2.5-bit stage architecture
  - $\pm 5V_R/8, \pm 3V_R/8$, and $\pm V_R/8$
  - Represented as $nAV_R/8$, where, $A = -1$ for V_{T1} to V_{T3}, $A = 1$ for V_{T4} to V_{T6}, and $n = 5, 3, 1$
- To apply V_{T1}, $A = -1$ and $n = 5$
- Resulting residue is

$$V_{out} = \frac{\sum_{i=1}^{5} C_i\,(-V_R) - \sum_{i=1}^{6} C_i\,V_R}{C_7 + C_8 + \frac{\sum_{i=1}^{8} C_i}{A}}$$

- Equivalent to applying $V_{T1} = -5V_R/8$
- Similar technique applied to 3.5-bit stage

* C. Ravi, V. Sarma, and B. Sahoo," IEEE NEWCAS, June 2015

Foreground Vs Background

- **Capacitor mismatch does not change with supply voltage and temperature**

  ➔ Power up foreground calibration is sufficient.

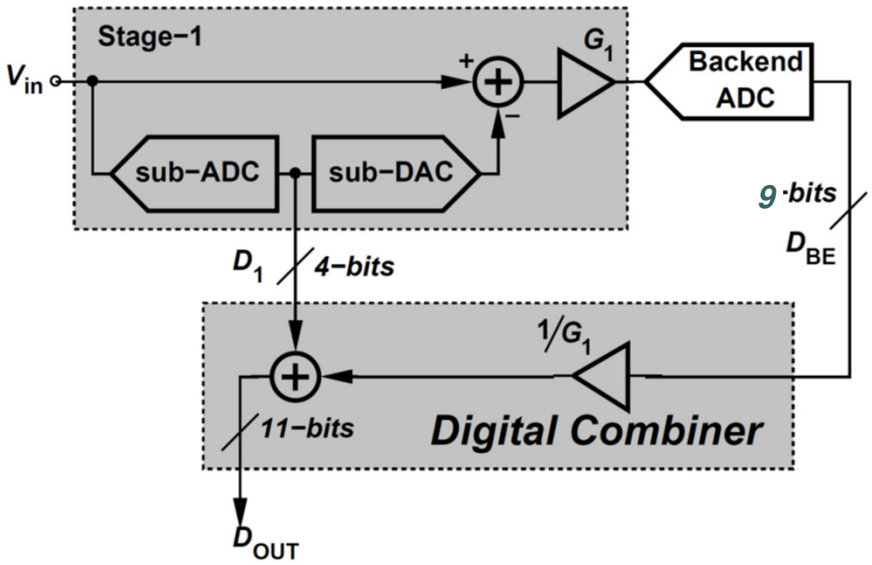
- **Op amp gain changes with supply voltage and temperature**

  ➔ Background calibration is a necessity.

Background Gain Calibration for Multi-bit, 1.5-bit, 2.5-bit, etc. MDACs

Pipeline Stage I/O Characteristic

- The input output characteristic of a 4-bit stage is:



$$V_{OUT} = \frac{\sum_{m=1}^{16} C_m V_{IN} - \sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}$$

$$\Rightarrow V_{OUT} = \alpha V_{IN} - \frac{\sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}$$

$$\Rightarrow V_{OUT} = \alpha V_{IN} - \beta_j V_R ,$$

$$\text{where } \beta_j = \frac{\sum_{m=1}^{15} C_m A_{m,j} V_R}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}} \text{ and } \alpha = \frac{\sum_{i=1}^{16} C_m}{C_F - \frac{C_F + C_P + \sum_{m=1}^{16} C_m}{A}}.$$

- Dividing both sides by V_R we get,

$$D_{BE} = \alpha D_{IN} - \beta_j$$

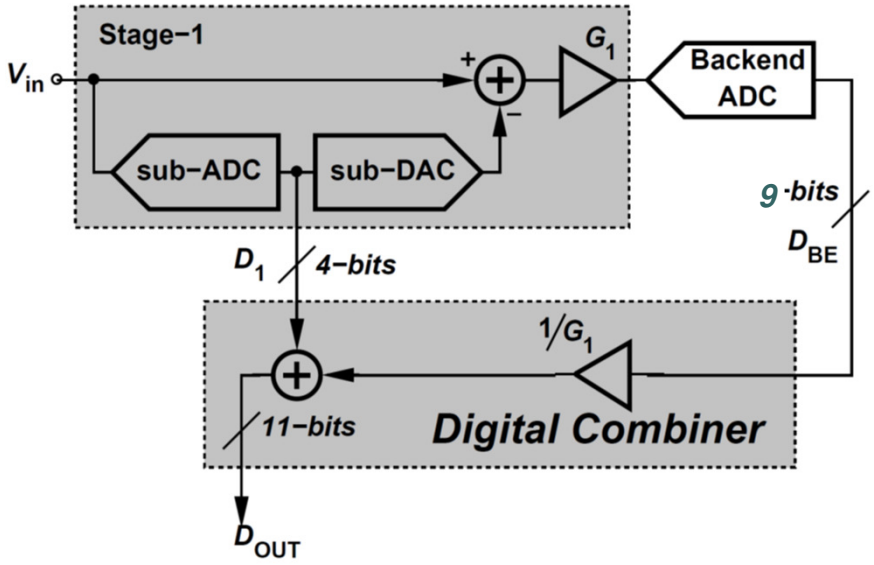
$$\Rightarrow D_{IN} = \frac{D_{BE}}{\alpha} + \gamma_j$$

where,

- γ_j is the capacitor mismatch ➔ independent of op amp gain
- α is the gain (G_1)➔ function of op amp gain.

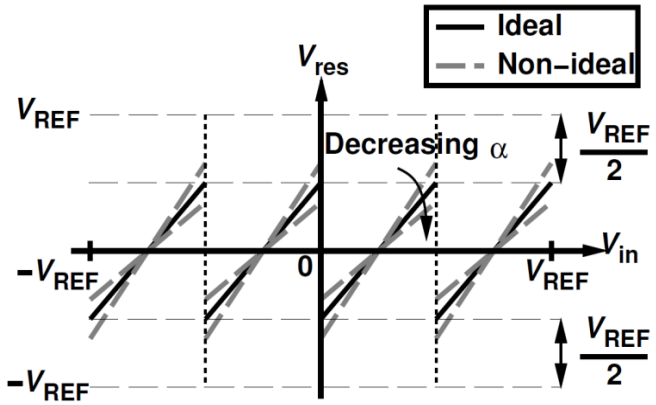
Proposed Calibration Algorithm

- **Initially estimate the gain (α=G_1) and the capacitor mismatch (γ_j) in the foreground using the calibration technique in [ϒ].**
- **Then estimate the inter-stage gain α, in the background.**

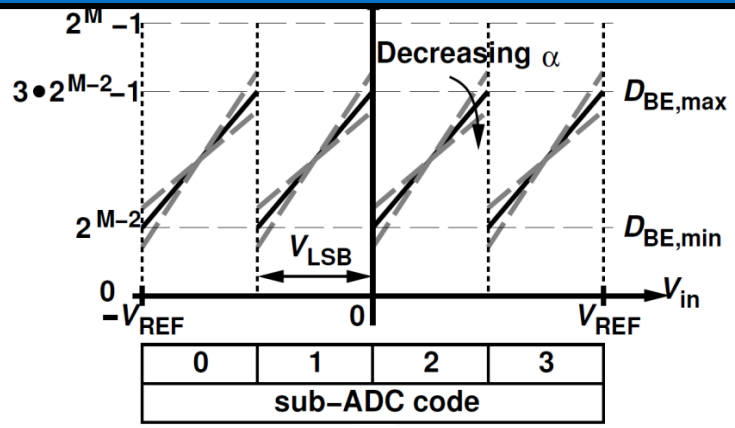


[ϒ] B. Sahoo, and B. Razavi, "A 10-bit 1-GHz 33-mW CMOS ADC," *IEEE JSSC*, June 2013.

Pipelined Stage Residue Characteristic with MDAC Gain Variation



2-bit MDAC residue characteristics
V_{res} Vs V_{in} with Gain variation



2-bit MDAC residue characteristics
D_{BE} Vs V_{in} with Gain variation

- MDAC gain (α) changes ➔ slope of the residue characteristic changes.
- Residue quantized by an ideal M-bit back-end to give a digital estimate, D_{BE},

$$D_{BE,\,min} = 2^{M-2} \text{ and } D_{BE,\,max} = 3\times2^{M-2} - 1$$

- Ideally $\alpha = D_{BE,\,max}/V_{LSB}/2$.
- Parameter drift changes $D_{BE,\,min}$ and $D_{BE,\,max}$.

Calibration Algorithm

- Estimate the MDAC gain, α in the foreground mode using technique in [Υ].
- Estimate $D_{BE,max1}$ in the background mode, immediately after the foreground calibration is done. Thus, $\alpha = D_{BE,max1}/V_{LSB}/2$.
- Calibration engine keeps on estimating $D_{BE,max}$. If the gain drifts a new back-end maximum, $D_{BE,max2}$ is obtained, resulting in $\alpha_{new} = D_{BE,max2}/V_{LSB}/2$.
- Thus,

$$\frac{\alpha_{new}}{\alpha} = \frac{D_{\max 2}}{D_{\max 1}} \Rightarrow \alpha_{new} = \alpha \frac{D_{\max 2}}{D_{\max 1}}$$

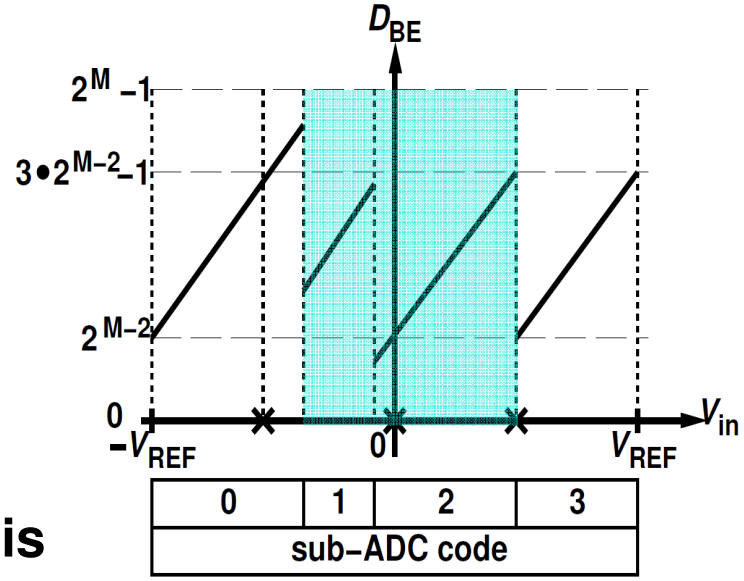
[Υ] B. Sahoo, and B. Razavi, "A 10-bit 1-GHz 33-mW CMOS ADC," *IEEE JSSC*, June 2013.

Effect of Non-Idealities

- **The estimation of $D_{BE,\,MAX}$ can be corrupted due to the following non-idealities:**
  - **Comparator Offset**
  - **Capacitor mismatch**
  - **Thermal Noise**

Effect of Comparator Offset

- With comparator offset maximum back-end code changes from region to region, but slope in each region is the same.
- Maximum in any one region gives the accurate estimate of inter-stage gain
- The region should be such that the calibration can work even with lower signal swing
- For 2-bit MDAC, characteristic corresponding to output code of 1 or 2 is chosen

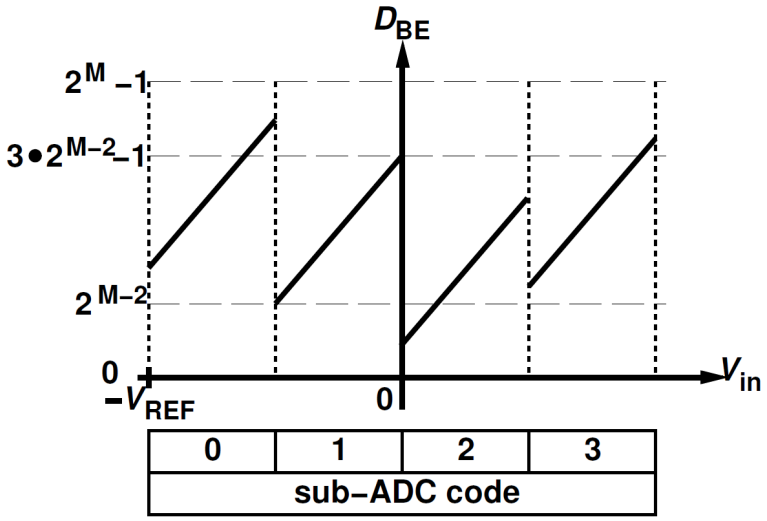


- For 3-bit and 4-bit MDACs calibration would work for 1/4th and 1/8th of the signal swing.

Proposed calibration would thus require a minimum swing that is either 12 dB or 18 dB below full scale.

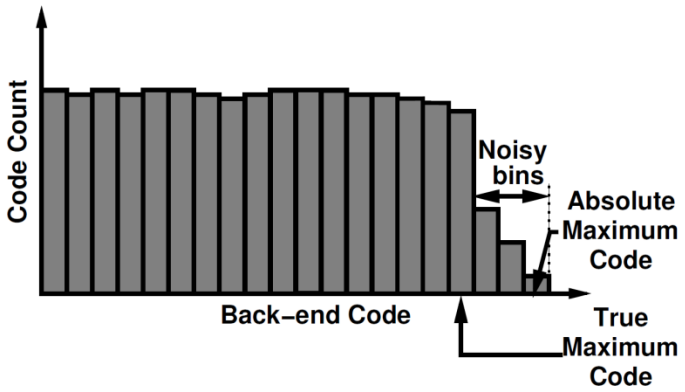
Effect of Capacitor Mismatch

- Capacitor mismatch changes the residue/back-end characteristic.
- Although the slope is the same in each region the maximum in each region is different.
- Calibration obtains the maximum back-end code for a particular region



Effect of Thermal Noise

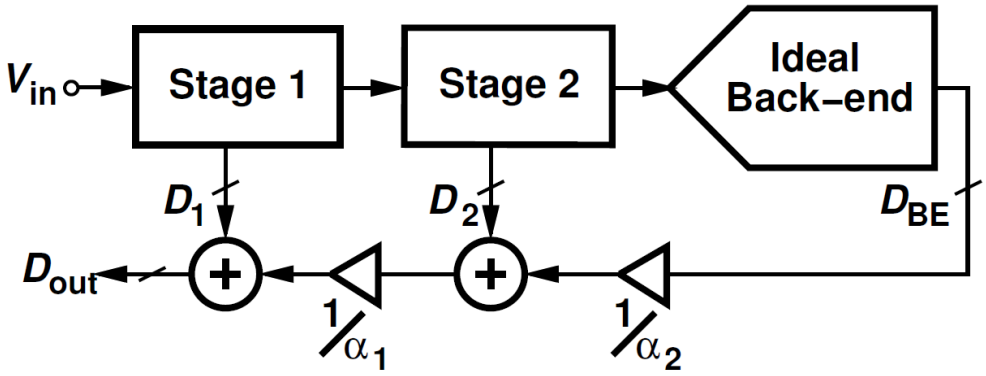
- Thermal noise corrupts the measurement of $D_{BE,max}$.
- Histogram of the back-end code estimates the true maximum code and eliminates the absolute maximum code.



- For a noisy bin to have the same height as that of a noiseless bin, the thermal noise should have a variance, σ_{NTH} > 10 LSB ➔ SNR degradation of approx. 30 dB.

➔ Noisy bins cannot be of the same height as noiseless bins

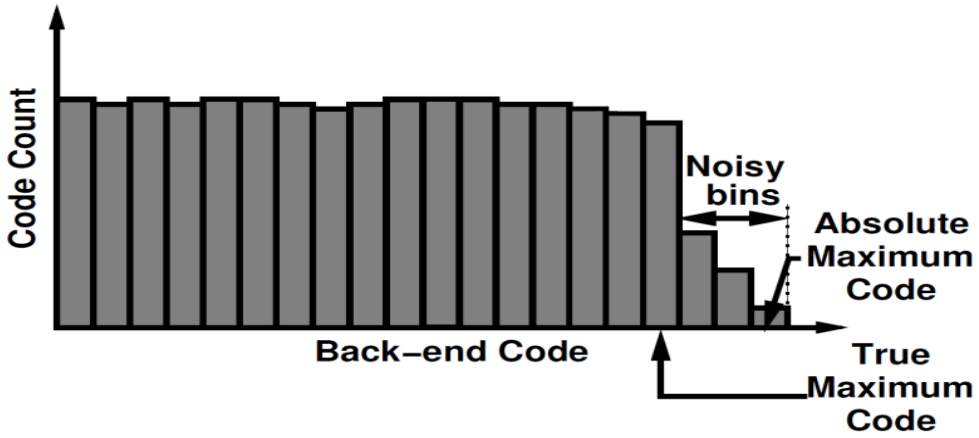
Multi-stage Gain Calibration



- Algorithm first calibrates the 2nd stage that has an ideal back-end
- Consider the 2nd stage onwards as an ideal back-end and calibrate the 1st stage
- Calibration starts from the later stages and moves to the 1st stage

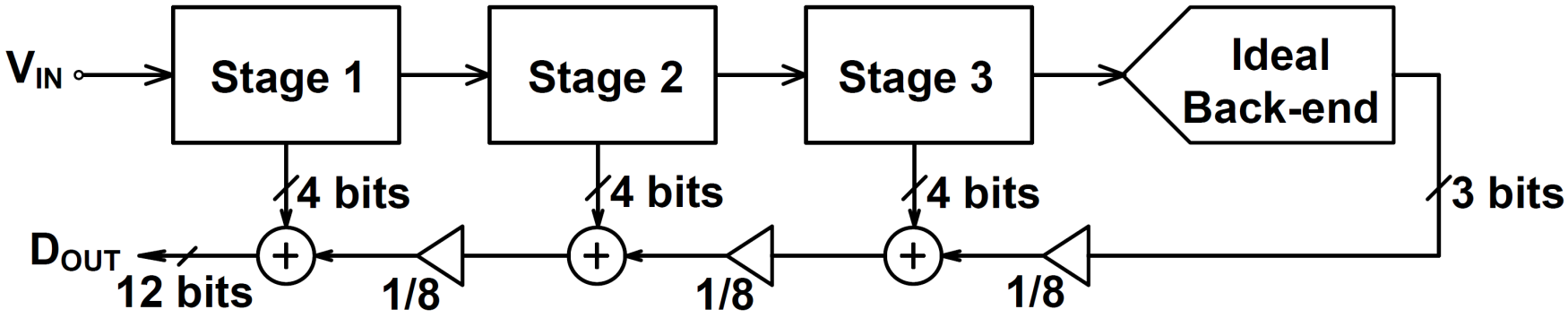
Digital Hardware Complexity

- Histogram requires counters and finding the maximum requires comparators.
- For M-bit back-end, do we need 2^M comparators and counters! **No ☺**



- Foreground calibration gives an initial estimate of $D_{BE,max}$ and noise corrupts this by maximum of ±10 to ±20 back-end codes
- Hence maximum of 40 digital comparators and counters used
- Division operation is realized using Newton-Raphson technique, which requires a multiplier and adder

Simulation Setup



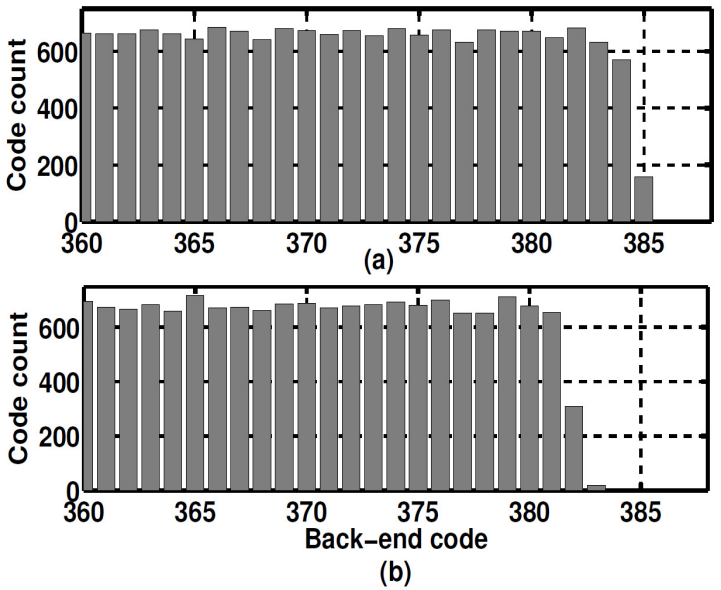
- Proposed calibration technique applied to the first 2 stages with the remaining two stages acting as an ideal back-end.
- Circuit noise has been added to each stage of the pipeline to limit the effective number of bits (ENOB) to 11.3 bits.

SIMULATION PARAMETERS

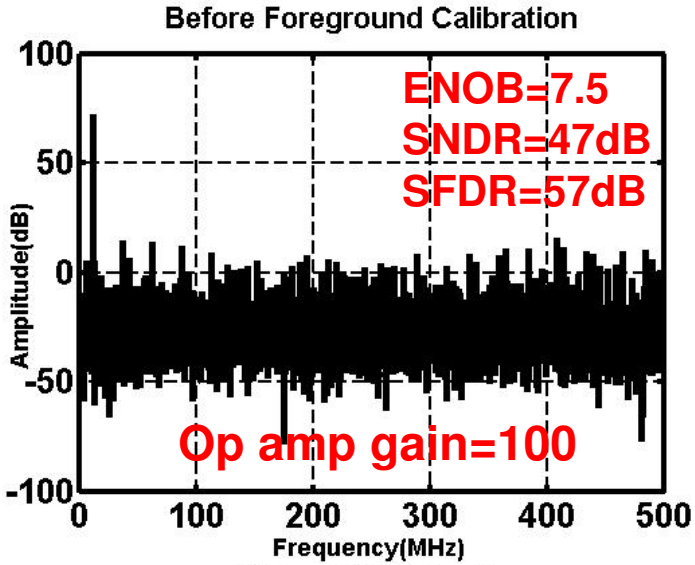
Stage No	Op amp gain	3σ—Comparator Offset	3σ—Capacitor Mismatch
1	$100 \pm 20\%$	15 mV	3%
2	$100 \pm 20\%$	15 mV	3%

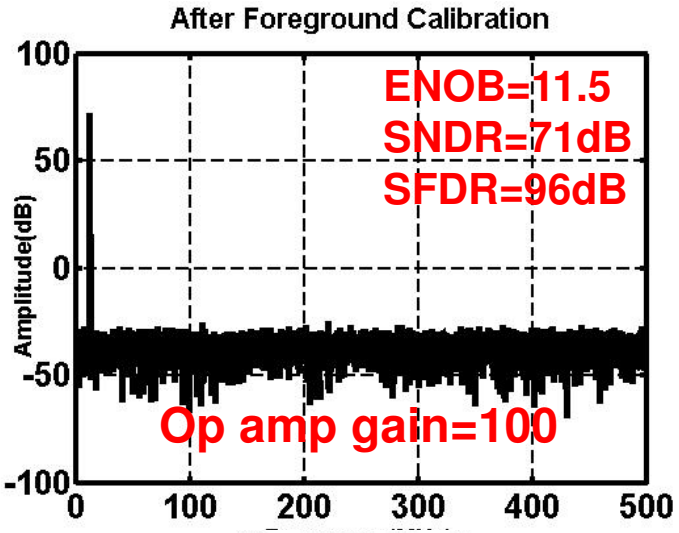
Simulation Results (1)

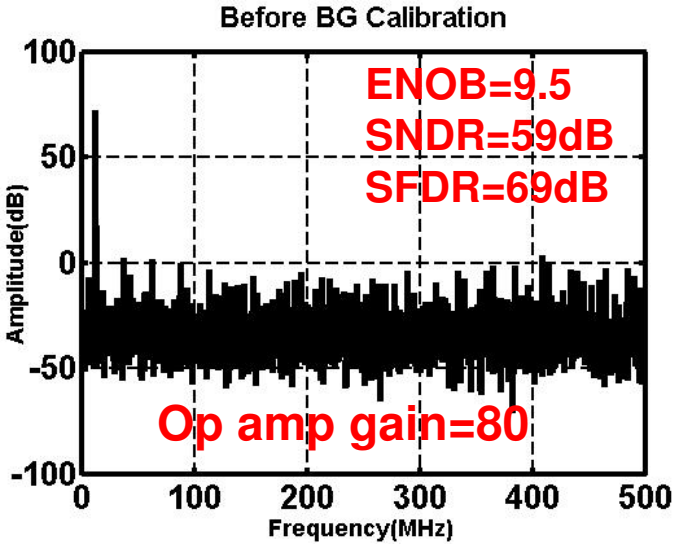
- Fig (a) shows the histogram of the output of stage-1 simulated with an op amp gain of 100 i.e., 40 dB and an ideal 9 bit back-end
- Fig (b) shows the histogram with stage-1 op amp gain changed to 80 i.e., 20 % reduction in gain.
- Used sine wave as an input signal for this.
- For *ramp and random* Inputs similar histograms can be obtained.

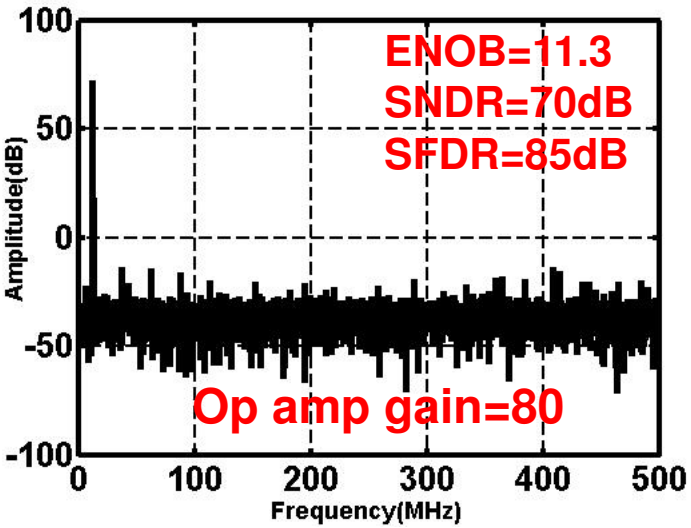


Simulation Results (2)









Op amp Nonlinearity Calibration

Op Amp Modeling

- **Nonlinear op amp input-output characteristic,**

$$V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3$$

- **Inverse given by,**

$$V_{in} = \sum_{i=0}^{\infty} \beta_i V_{out}^i$$

$$\Rightarrow V_{in} = \sum_{i=0}^{\infty} \beta_i \left(\alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3\right)$$

- **For a weakly nonlinear system we have,**

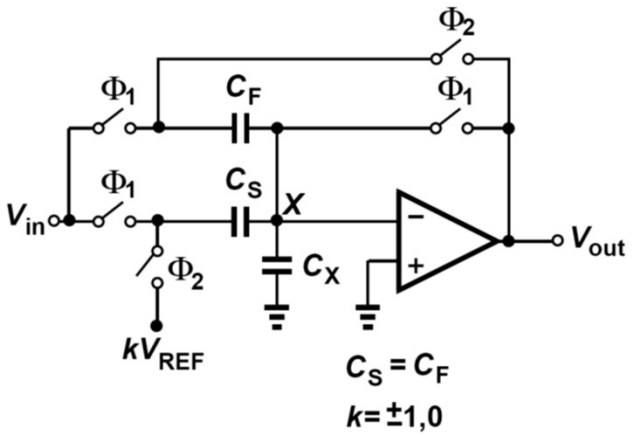
$$V_{in} = \beta_1 V_{out} + \beta_2 V_{out}^2 + \beta_3 V_{out}^3$$

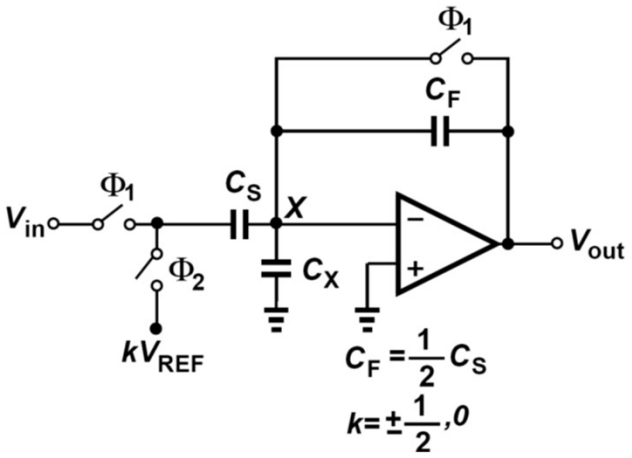
where,

$$\beta_1 = \frac{1}{\alpha_1}, \beta_2 = \frac{-\alpha_2}{\alpha_1^3}, \beta_3 = \frac{2\alpha_2^2}{\alpha_1^5} - \frac{\alpha_3}{\alpha_1^4}$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

MDAC for 1.5-b/stage (1)





$$V_{out} = \frac{1+\frac{C_S}{C_F}}{1+\frac{1}{A}\left(1+\frac{C_S}{C_F}+\frac{C_X}{C_F}\right)}V_{in} + \frac{\frac{C_S}{C_F}}{1+\frac{1}{A}\left(1+\frac{C_S}{C_F}+\frac{C_X}{C_F}\right)}kV_{REF}$$

$$V_{out} = \frac{\frac{C_S}{C_F}}{1+\frac{1}{A}\left(1+\frac{C_S+C_X}{C_F}\right)}(V_{in} - kV_{REF})$$

- **Conservation of charge gives:**

$$C_S V_{in} = (kV_{REF} - V_X)C_S + V_X C_X + (V_{out} - V_X)C_F$$

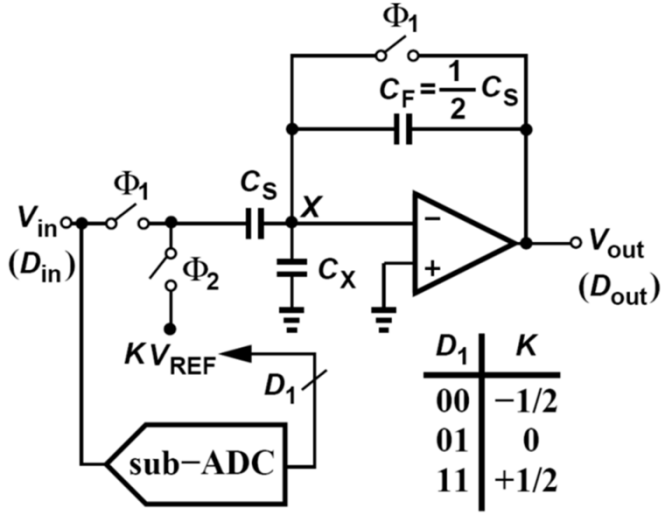
$$V_{in} = kV_{REF} + \left[\frac{C_F}{C_S} + \beta_1\gamma\right]V_{out} + \beta_2\gamma V_{out}^2 + \beta_3\gamma V_{out}^3$$

where,

$$\gamma = \frac{C_X + C_F}{C_S} - 1$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

MDAC for 1.5-b/stage (2)



- **Defining $D_{in} \equiv V_{in}/V_{REF}$ and $D_{out} \equiv V_{out}/V_{REF}$ the input-output characteristic is given by,**

$$D_{in} = D_1 + \eta_1 D_{out} + \eta_2 D_{out}^2 + \eta_3 D_{out}^3$$

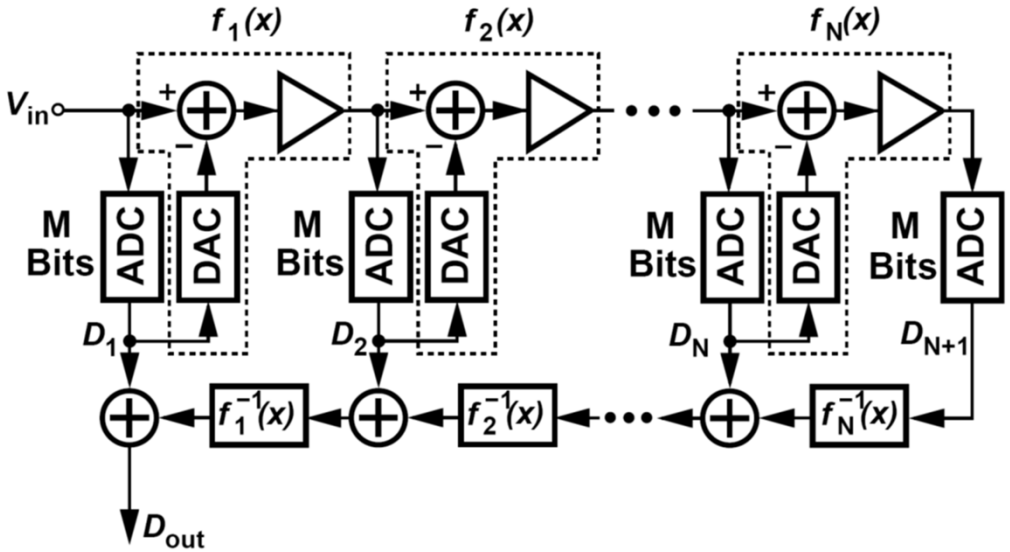
where,

$$\eta_1 = \frac{C_F}{C_S} + \gamma\beta_1, \eta_2 = \gamma\beta_2, \eta_3 = \gamma\beta_3$$

- **Calibration thus estimates the coefficients of D_{out}.**

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Pipelined ADC Modeling (1)



- **Recursive implementation of the pipelined ADC,**

$$D_{out} = D_{in,1}$$

$$D_{in,1} = D_1 + \eta_{1,1} D_{out,1} + \eta_{2,1} D_{out,1}^2 + \eta_{3,1} D_{out,1}^3$$

$$D_{in,2} = D_2 + \eta_{1,2} D_{out,2} + \eta_{2,2} D_{out,2}^2 + \eta_{3,2} D_{out,2}^3$$

$$\bullet$$

$$\bullet$$

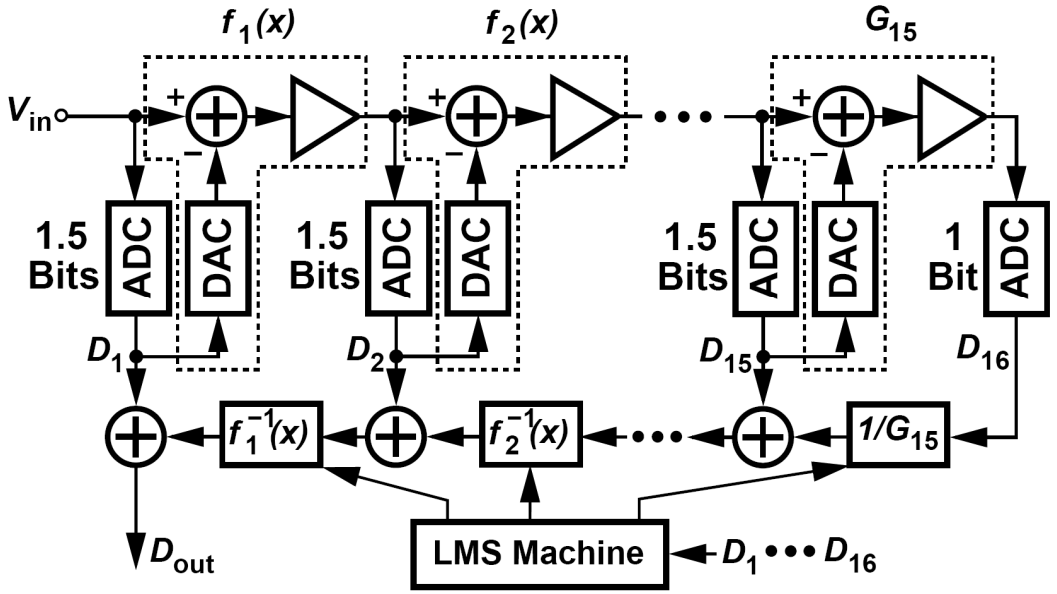
$$\bullet$$

$$D_{in,N} = D_N + \eta_{1,N} D_{out,N} + \eta_{2,N} D_{out,N}^2 + \eta_{3,N} D_{out,N}^3$$

$$D_{in,N+1} = D_{N+1} + \eta_{1,N+1} D_{out,N+1} + \eta_{2,N+1} D_{out,N+1}^2 + \eta_{3,N+1} D_{out,N+1}^3$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Pipelined ADC Modeling (2)



- **Recursive relation can be written as,**

$$D_{out} = D_{in,1}$$

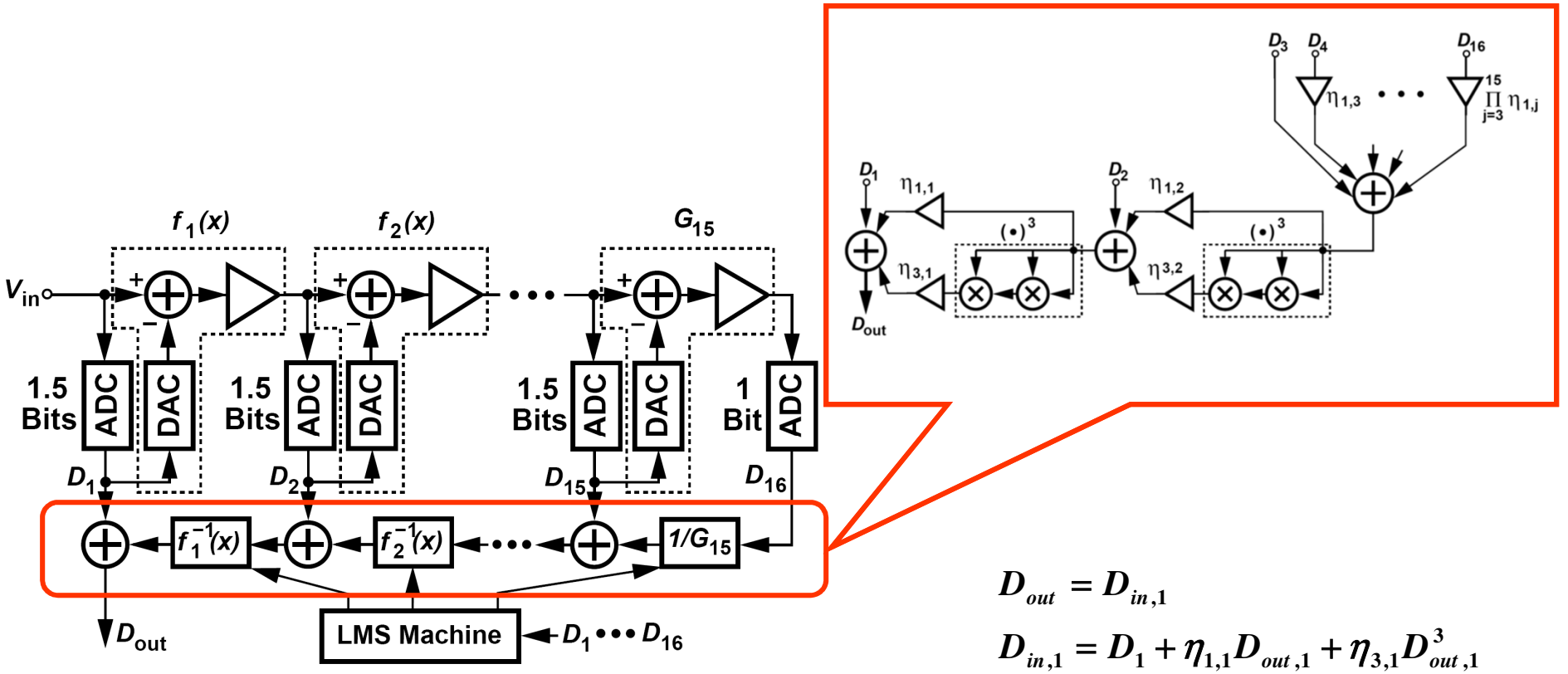
$$D_{in,1} = D_1 + \eta_{1,1} D_{out,1} + \eta_{3,1} D_{out,1}^3$$

$$D_{in,2} = D_2 + \eta_{1,2} D_{out,2} + \eta_{3,2} D_{out,2}^3$$

$$D_{in,3} = D_3 + \sum_{i=3}^{15} \Pi_{j=3}^{i} \eta_{1,j} D_{i+1}$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

FIR Filter Implementation



- $D_{in,3}$ does not need multipliers.

$$D_{out} = D_{in,1}$$

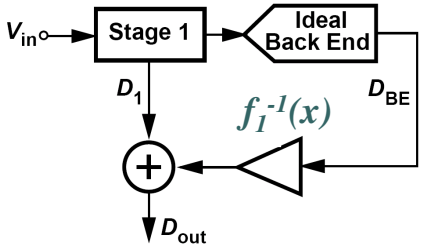
$$D_{in,1} = D_1 + \eta_{1,1} D_{out,1} + \eta_{3,1} D_{out,1}^3$$

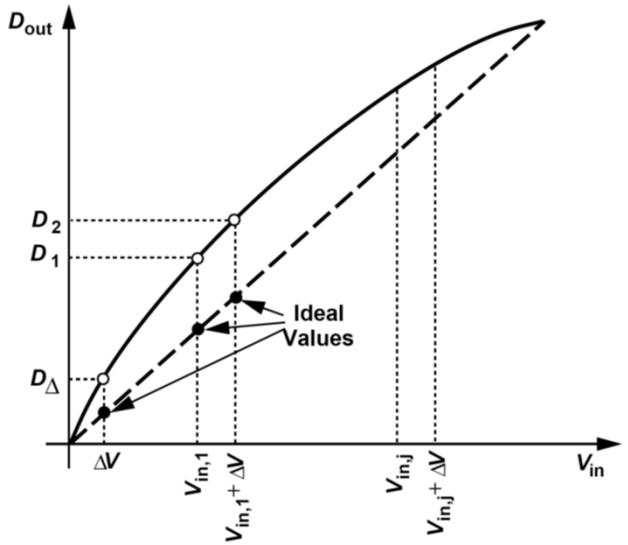
$$D_{in,2} = D_2 + \eta_{1,2} D_{out,2} + \eta_{3,2} D_{out,2}^3$$

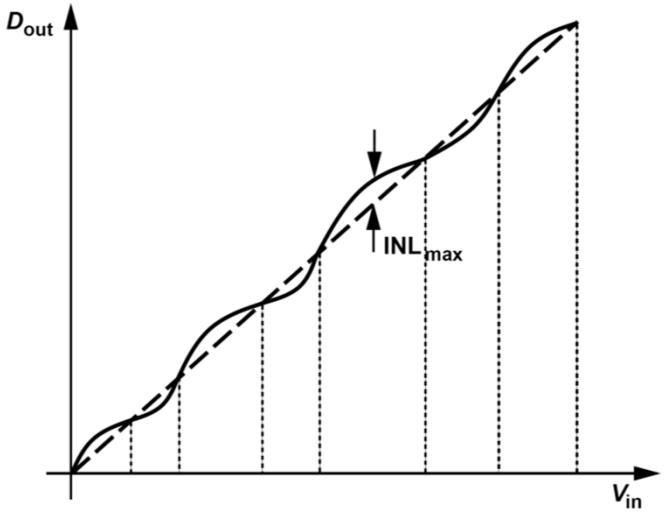
$$D_{in,3} = D_3 + \sum_{i=3}^{15} \Pi_{j=3}^{i} \eta_{1,j} D_{i+1}$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Calibration Concept (1)







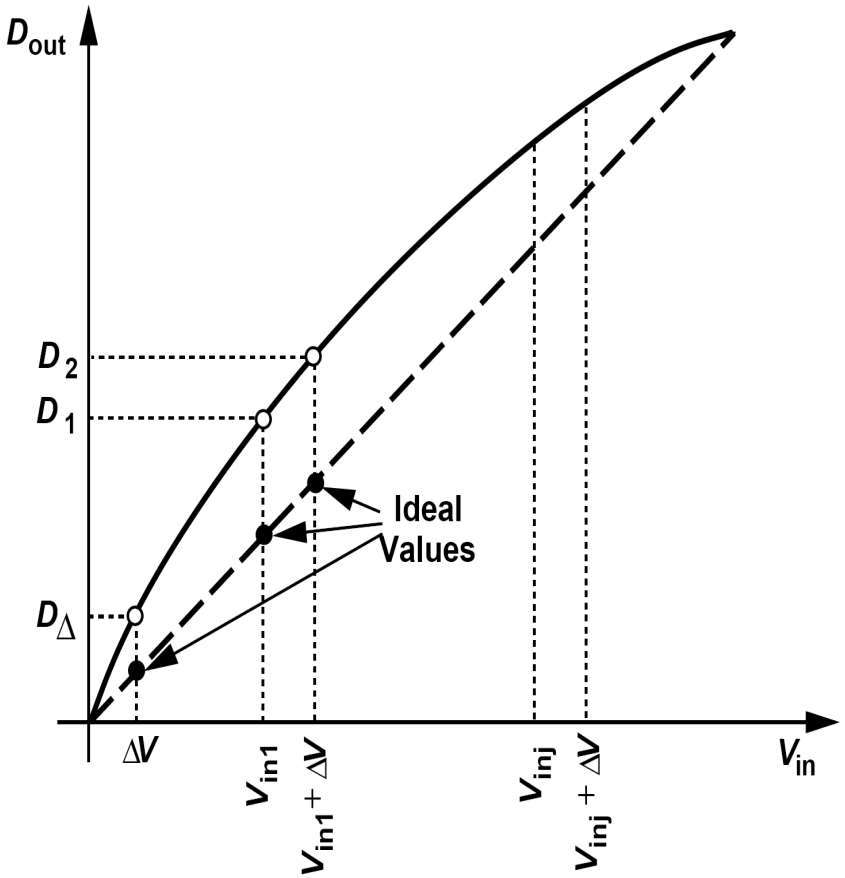
- V_{in1} → $D_1 = D_{1,1} + f_1^{-1}(D_{BE1})$
- $V_{in1} + \Delta V$ → $D_2 = D_{1,1,\Delta} + f_1^{-1}(D_{BE2})$
- ΔV → $D_\Delta = D_{1,\Delta} + f_1^{-1}(D_{BE\Delta})$
- **Cost function →** $\varepsilon = (D_\Delta - (D_1 - D_2))^2$
- **Repeat above measurement for various values of $V_{in,j}$.**

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Calibration Concept (2)

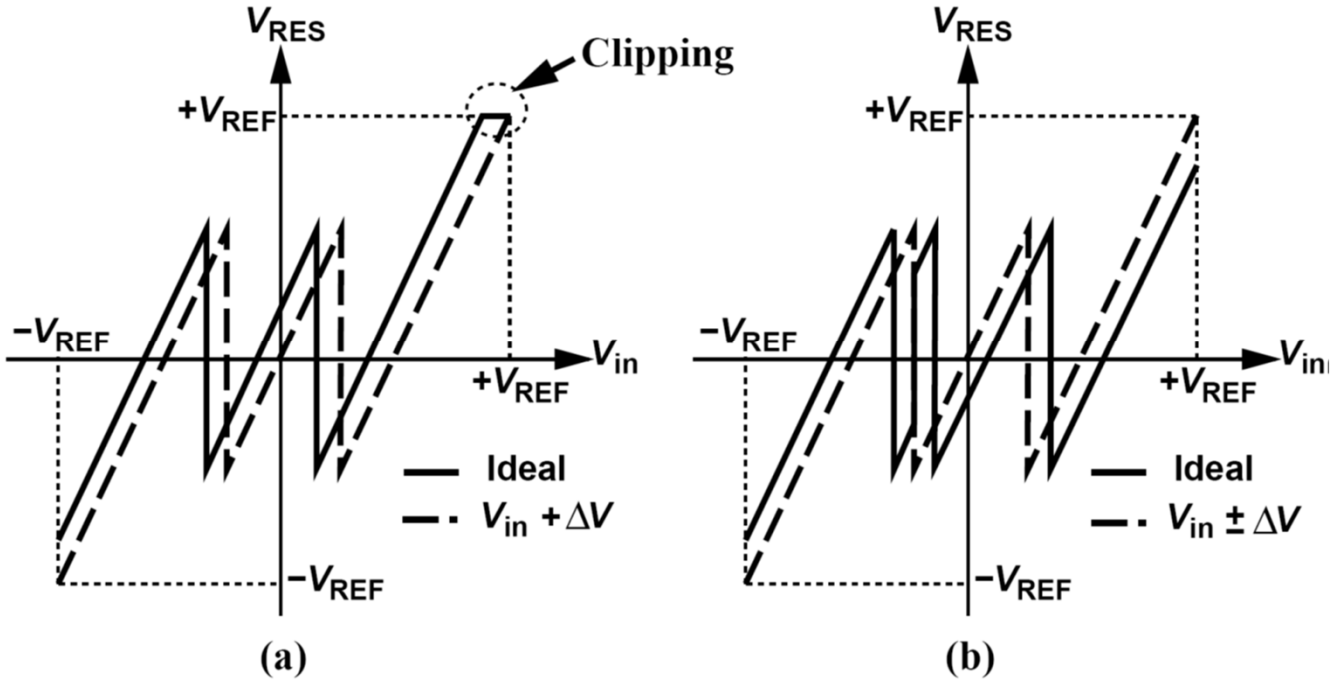
- **Perturbation voltage ΔV:**
  - **need not be known accurately.**
  - **must remain constant when V_{in} is swept to cover the entire range.**
- **$V_{in,j}$ values need not be equally spaced.**
- **Offset voltage incorporated in cost function:**

$$\varepsilon = (D_\Delta - D_{OS} - (D_1 - D_2))^2$$



B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Calibration Concept (3)

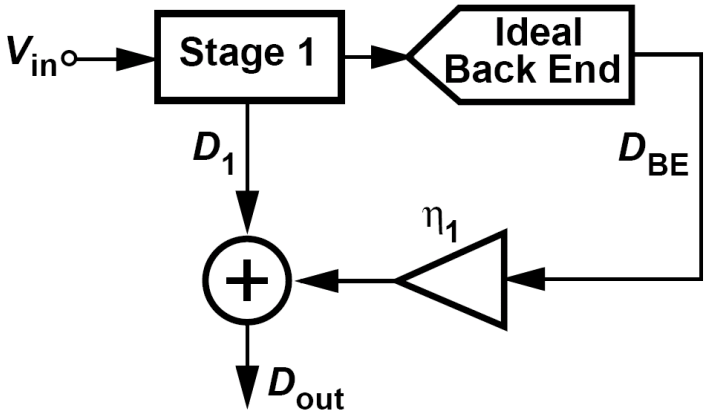


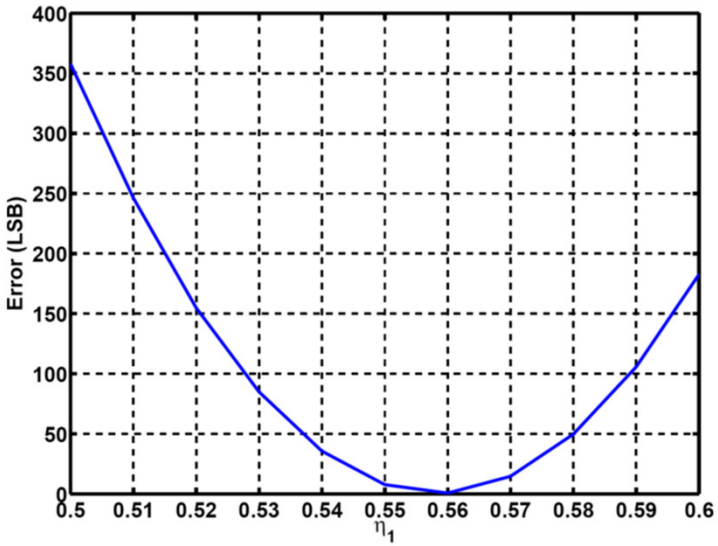
- **Addition or subtraction of perturbation voltage ΔV at all input levels causes residue overflow.**

- **ΔV is subtracted for $V_{in} > -V_{REF}/4$ and is added otherwise.**

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Properties of Cost Function (1)





Mean Square Error

- The output computed for $V_{in,j}$, $V_{in,j}+\Delta V$ and ΔV is given by,

$$D_{out,j} = D_{1,j} + \eta_1 D_{BE,j}$$

$$D_{out,j,\Delta} = D_{1,j,\Delta} + \eta_1 D_{BE,j,\Delta}$$

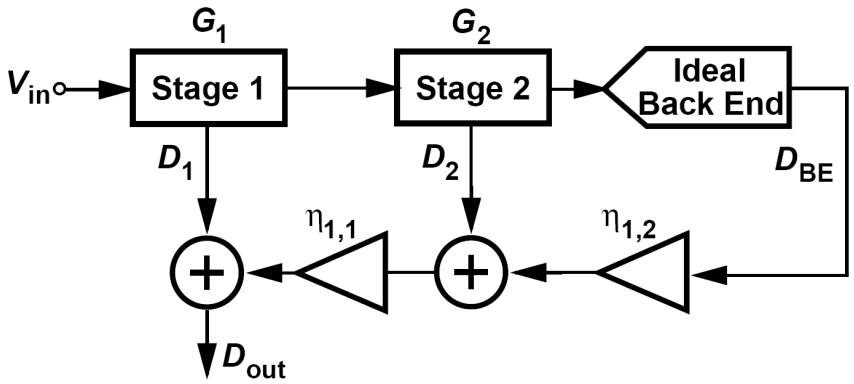
$$D_{out,\Delta} = D_{1,\Delta} + \eta_1 D_{BE,\Delta}$$

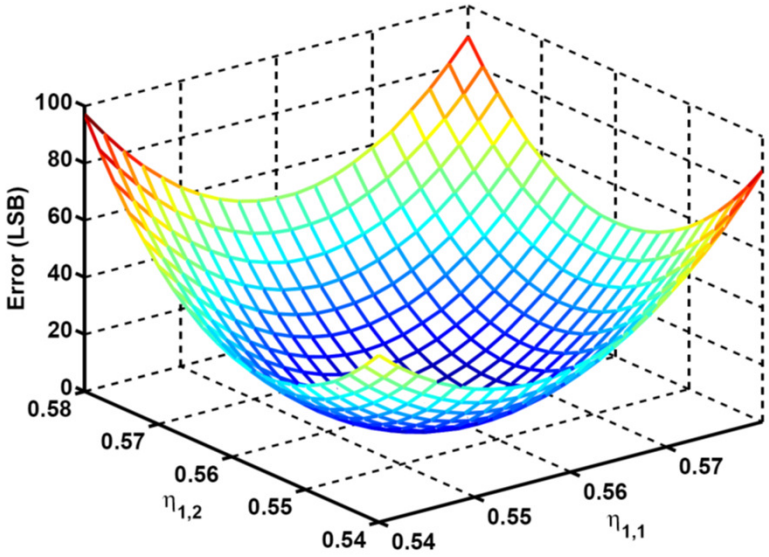
B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

- Mean squared error is given as,

$$\epsilon^2_{MSE} = \frac{1}{128}\sum_{j=1}^{128}[|D_{out,j} - D_{out,j,\Delta}| - D_{out,\Delta}]^2$$

Properties of Cost Function (2)



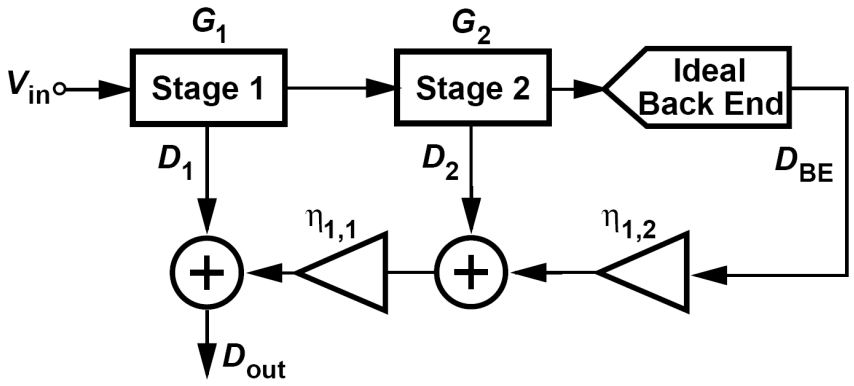


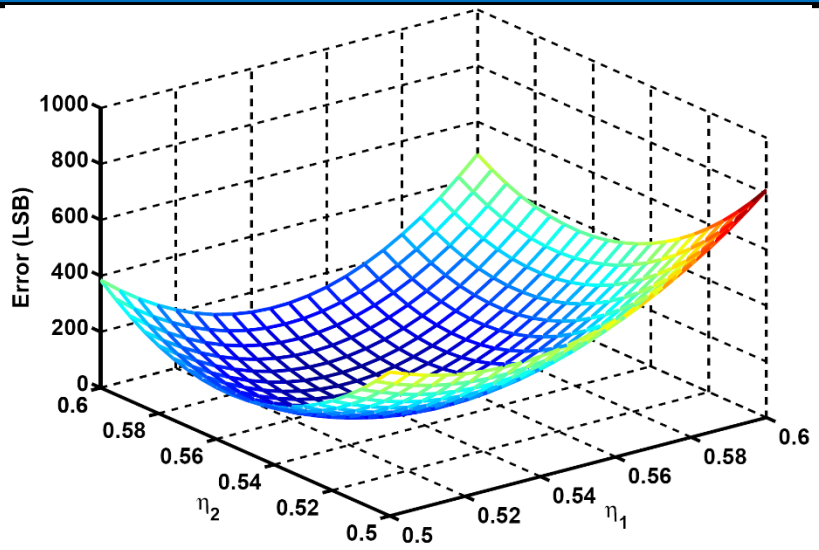
- **The output computed for $V_{in,j}$, $V_{in,j}+\Delta V$ and ΔV is given by,**

$$D_{out,j} = D_{1,j} + \eta_1\left(D_{2,j} + \eta_2 D_{BE,j}\right)$$
$$D_{out,j,\Delta} = D_{1,j,\Delta} + \eta_1\left(D_{2,j,\Delta} + \eta_2 D_{BE,j,\Delta}\right)$$
$$D_{out,\Delta} = D_{1,\Delta} + \eta_1\left(D_{2,\Delta} + \eta_2 D_{BE,\Delta}\right)$$

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Properties of Cost Function (3)





- Capacitor mismatch leads to asymmetric MSE curve.
- A minimum still exists.
- Can be extended to *N* stages having both gain error and nonlinearity with the overall ε_{MSE} still displaying a minimum.

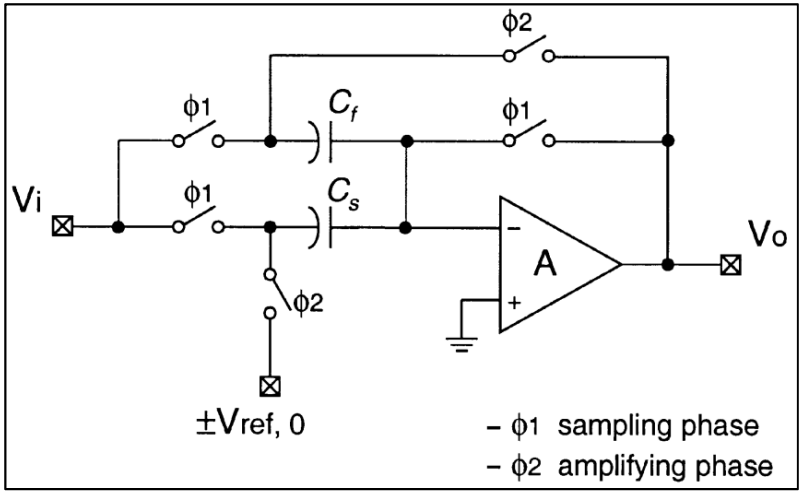
B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

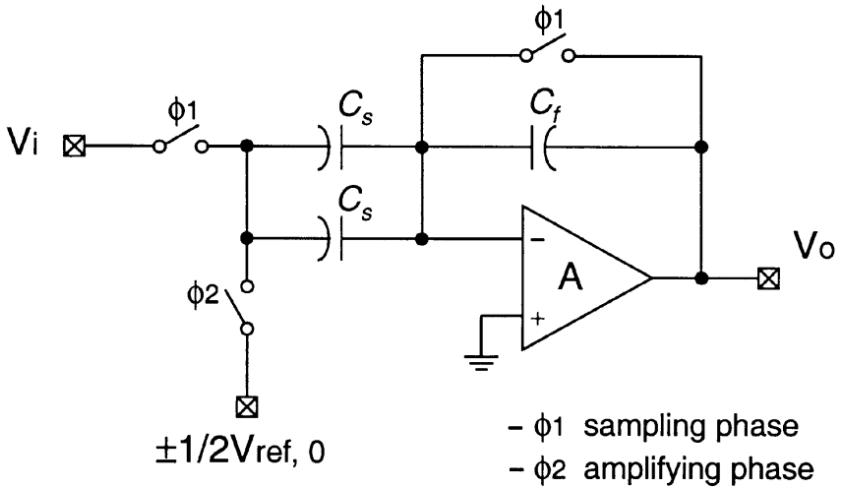
Blind LMS Algorithm

- **Initial estimate of the gain error and the nonlinear coefficient provided to the LMS engine.**
- **Digital bits corresponding to $V_{in,j}$ and $V_{in,j} + \Delta V$ stored in a memory to be retrieved by LMS engine.**
- **Calibration signals $V_{in,j}$ and $V_{in,j} + \Delta V$ applied at full clock rate**
  - **Corrects for incomplete settling components in the MDAC.**
- **LMS machine runs at slow rate ($f_s/16$) .**

B. Sahoo and B. Razavi, IEEE JSSC, vol. 44, pp. 2366-2380, Jan. 2009.

Radix Based Calibration (1)





$$V_O = \frac{1}{1+\frac{C_S+C_F}{AC_F}}\left(\frac{C_S+C_F}{C_F}V_i - \frac{C_S}{C_F}DV_{ref}\right)$$

$$\rightarrow V_O = (1+\delta)(2+\alpha)\left\{V_i - \frac{(1+\beta)}{(2+\alpha)}DV_{ref}\right\}$$

where, $(1+\delta) = \frac{1}{1+\frac{C_S+C_F}{AC_F}}$, $(2+\alpha) = \frac{C_S+C_F}{C_F}$,

and $(1+\beta) = \frac{C_S}{C_F}$

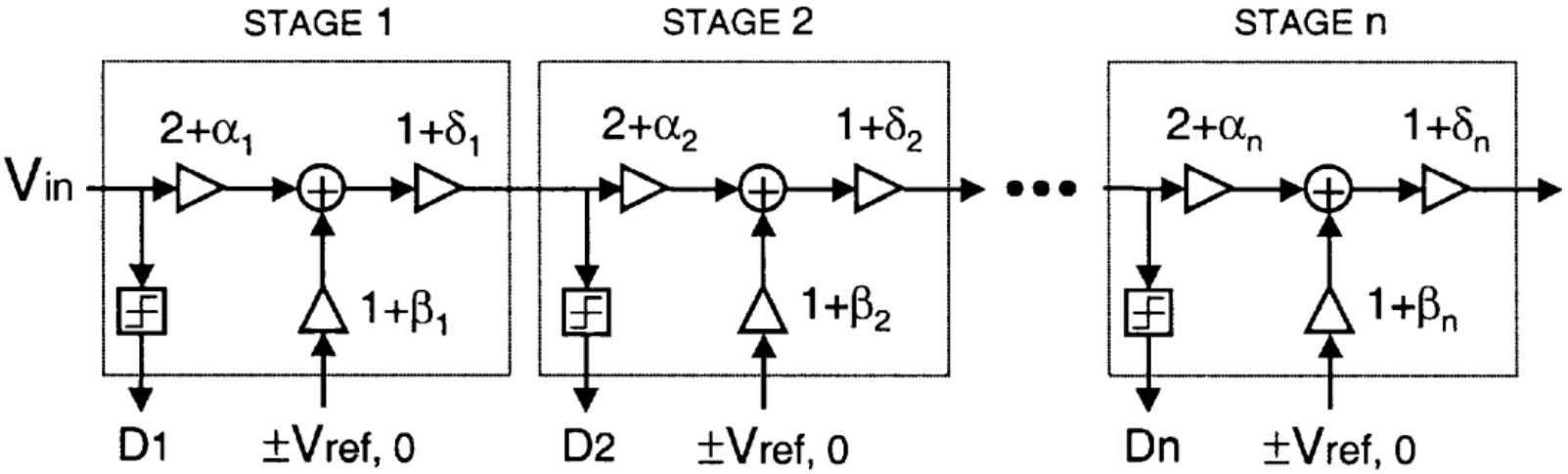
$$V_O = \frac{2C_S}{C_F}\frac{1}{1+\frac{2C_S+C_F}{AC_F}}\left(V_i - \frac{1}{2}DV_{ref}\right)$$

$$\rightarrow V_O = (1+\delta)(2+\alpha)\{V_i - DV_{ref}\}$$

where, $(1+\delta) = \frac{1}{1+\frac{C_S+C_F}{A}}$ and $(2+\alpha) = \frac{C_S+C_F}{C_F}$,

J. Li and Un-Ku Moon, IEEE TCAS-I, vol. 50, pp. 531-538, Sept. 2003.

Radix Based Calibration (2)



Representation of the pipelined ADC with each stage using 1.5-bit non-flip around topology.

- **The digital output can be represented as:**

$$D_O = D_n + D_n(ra) + D_n(ra)^2 + \cdots + D_1(ra)^{n-1}$$

where, $ra = (1+\delta)(2+\alpha)$ **and reference voltage of each stage is scaled.**

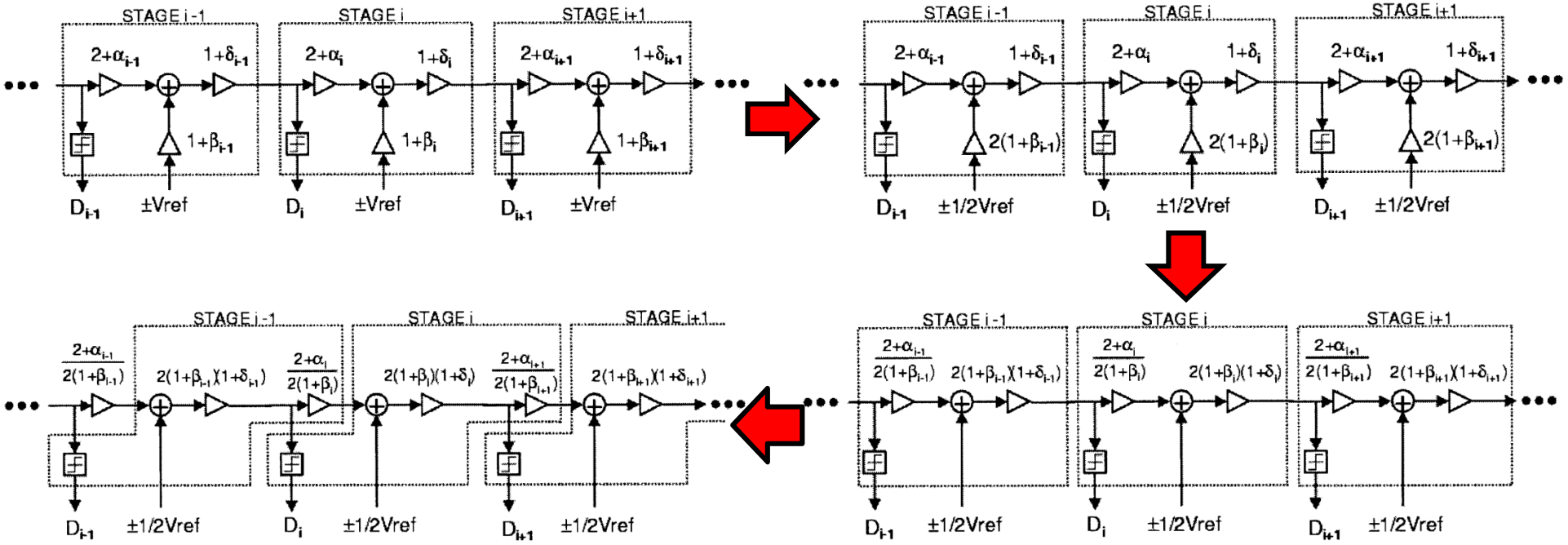
- **Since the reference is scaled for each stage this is not attractive.**
- **However if each stage uses a non-flip-around topology then,**

$$D_O = D_n + D_n(ra) + D_n(ra)^2 + \cdots + D_1(ra)^{n-1}$$

where, $ra = (1+\delta)(2+\alpha)$ **and reference voltage of each stage is not scaled.**

J. Li and Un-Ku Moon, IEEE TCAS-I, vol. 50, pp. 531-538, Sept. 2003.

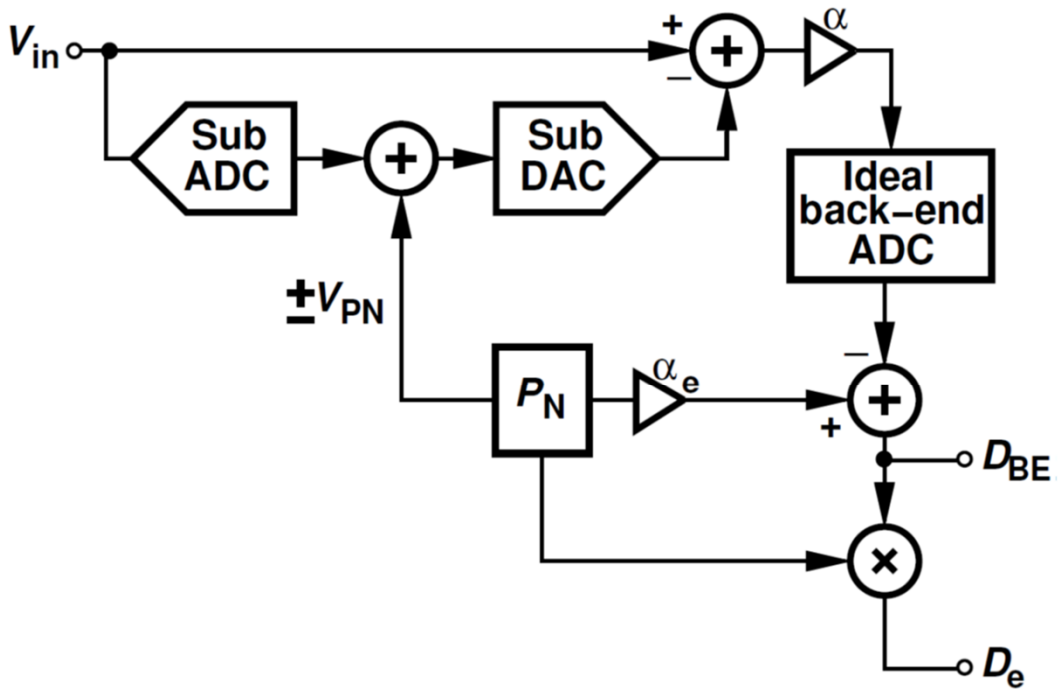
Radix Based Calibration (3)



- The new radix is . $ra = (1+\beta_i)(1+\delta_i)\frac{(2+\alpha_{i+1})}{(1+\beta_{i+1})}$.
- The reference voltage is not scaled from stage-to-stage.

J. Li and Un-Ku Moon, IEEE TCAS-I, vol. 50, pp. 531-538, Sept. 2003.

Radix Based Calibration (4)



$$D_{BE} = P_N \cdot \alpha_e - D_{res} - P_N \cdot \alpha$$
$$\Rightarrow D_e = \alpha_e - \alpha - P_N \otimes D_{res}$$
$$\Rightarrow \alpha = \alpha_e - D_e$$

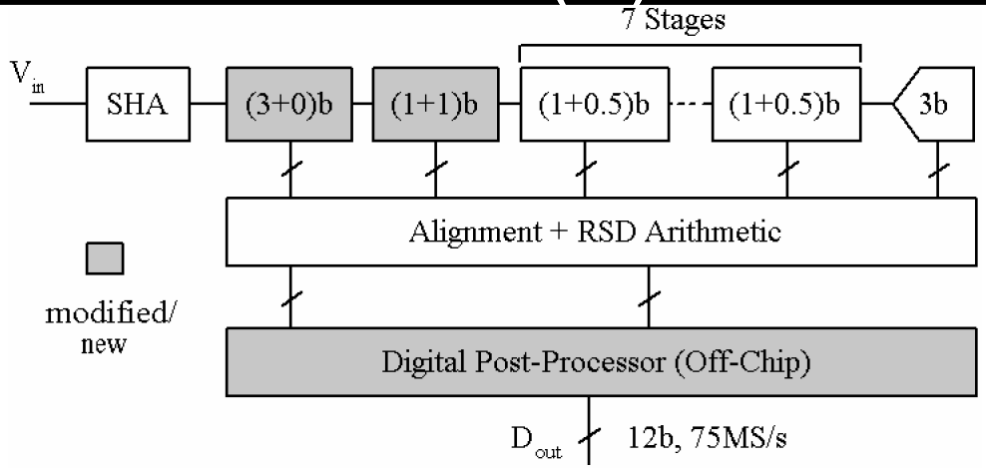
J. Li and Un-Ku Moon, IEEE TCAS-I, vol. 50, pp. 531-538, Sept. 2003.

Radix Based Calibration (5)

- **Large convergence time as D_{BE} has to be correlated for a long time to guarantee that $P_N \otimes D_{res}$ vanishes.**
- **Generation of precise analog voltage $\pm V_{PN}$ whose digital value is PN.**
- **Reduction in dynamic range of the ADC due to injection of pseudorandom voltage $\pm V_{PN}$.**

J. Li and Un-Ku Moon, IEEE TCAS-I, vol. 50, pp. 531-538, Sept. 2003.

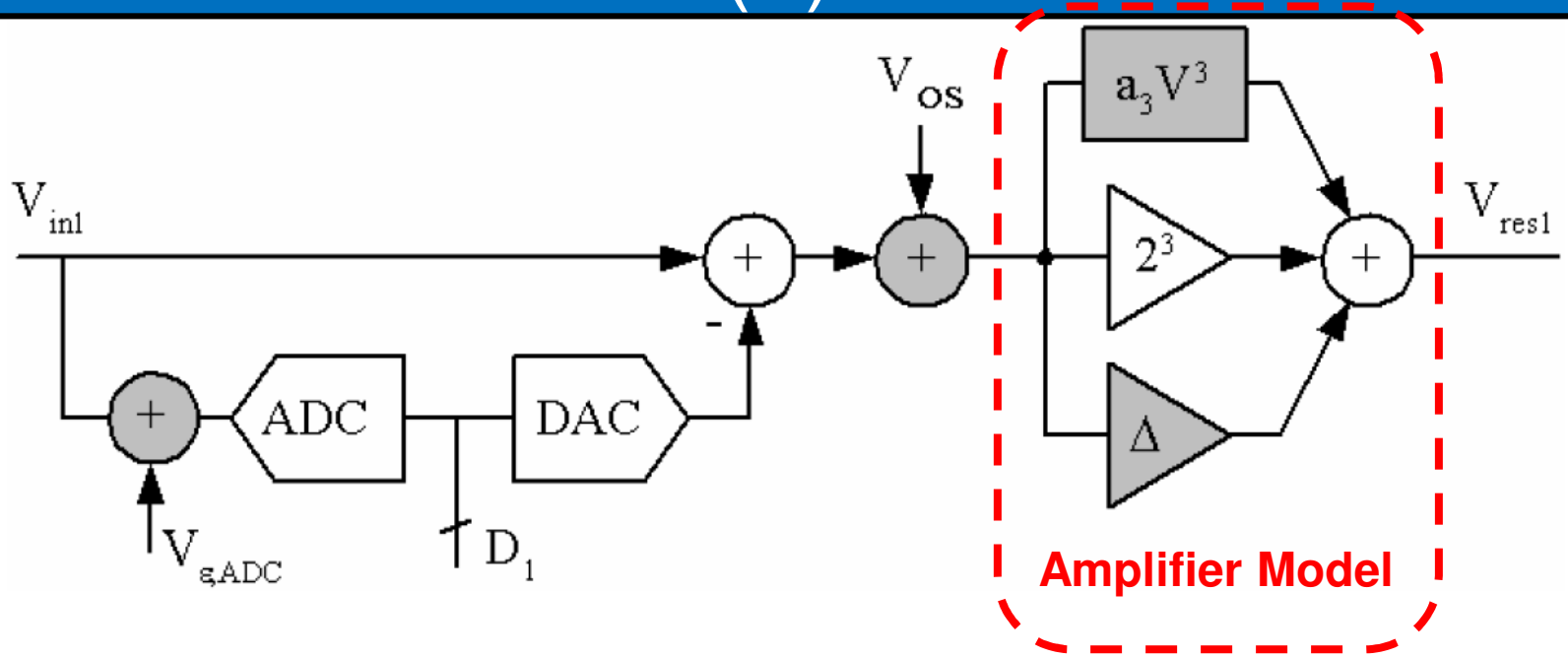
Open Loop Op amp Nonlinearity Calibration (1)



B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

- The 12-bit pipelined ADC incorporates:
  - 3-bit stage-1 realized using open-loop amplifier.
  - 1-bit stage-2 (with 1 redundant bit to incorporate the signal injection for calibration).
  - Seven 1.5-bit stages
  - 3-bit flash ADC.
- Although 14-bits of raw data the last two bits are used for calibration purpose.
- Only stage-1 is calibrated for linear gain error and non-linearity.
- All other stages form an ideal Back-end ADC.

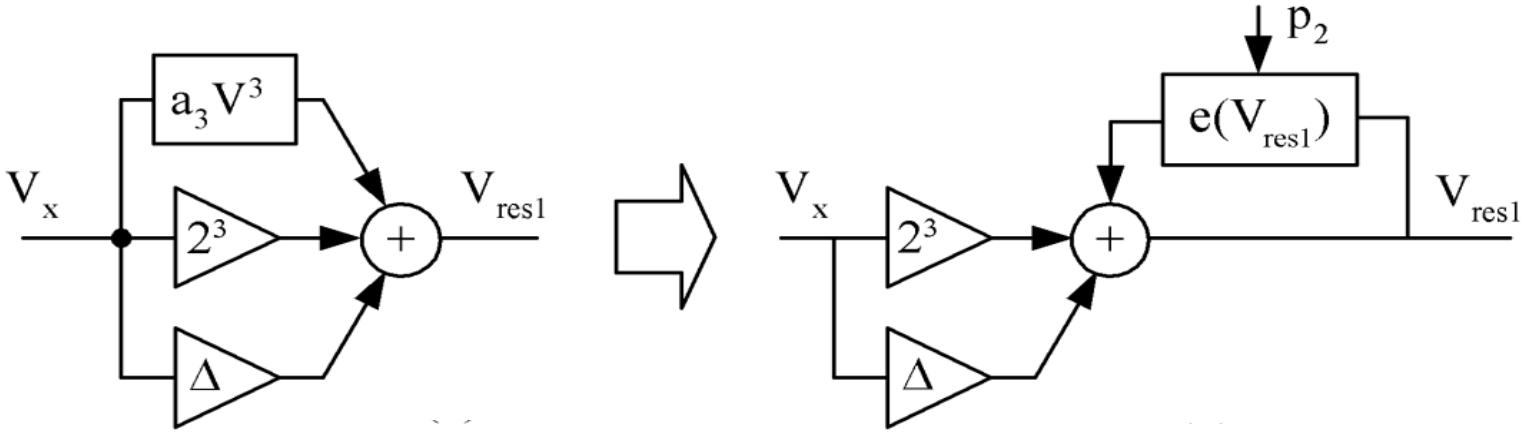
Open Loop Op amp Nonlinearity Calibration (2)



- **Stage-1 that incorporates an open-loop amplifier is modeled as per the above block diagram with various error sources:**
  - V_{OS} ➔ **op amp offset**
  - Δ ➔ **gain error ➔ modeled by calibration parameter p_1.**
  - a_3 ➔ **3rd order nonlinear term of the open-loop op amp.**

B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (3)



Amplifier model with input referred nonlinearity

Amplifier model with output referred nonlinearity

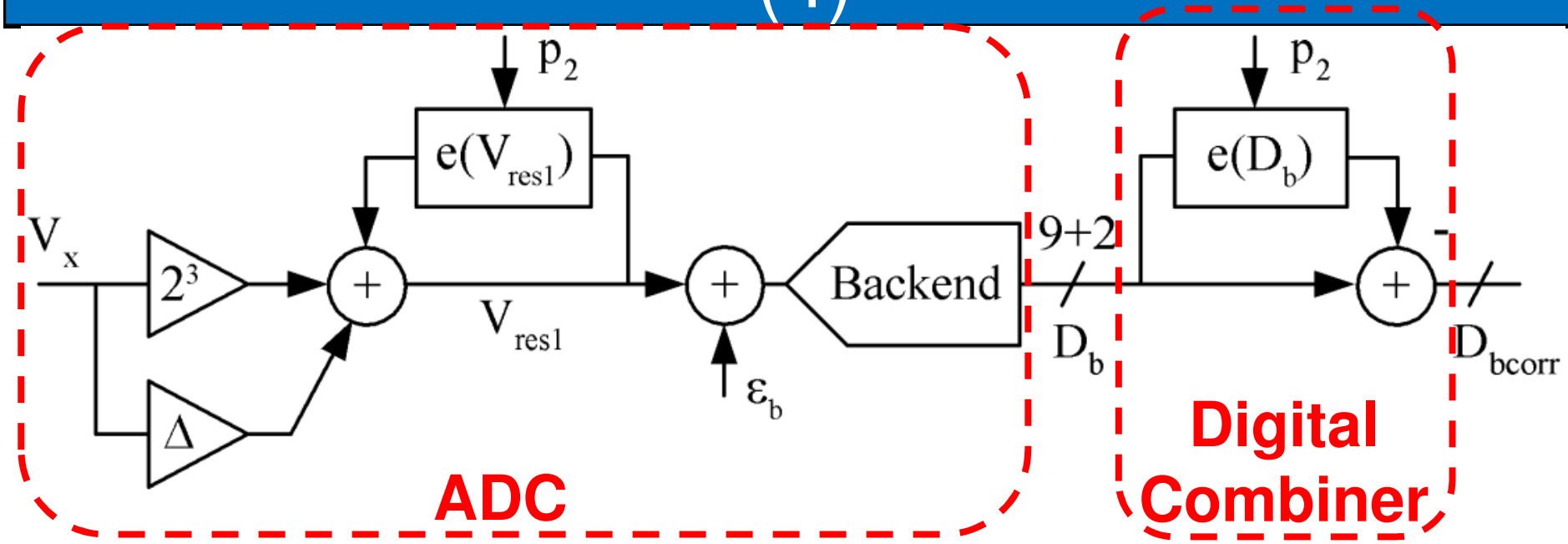
$$e(V_{res1}) = V_{res1} - 2\sqrt{-\frac{1}{3p_2}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{V_{res1}}{2\sqrt{-\frac{1}{27p_2}}}\right)\right]$$

where, V_{res1} is digitized by the back-end ADC and

$$p_2 = \frac{a_3}{(2^3 - \Delta)^3}$$

B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (4)

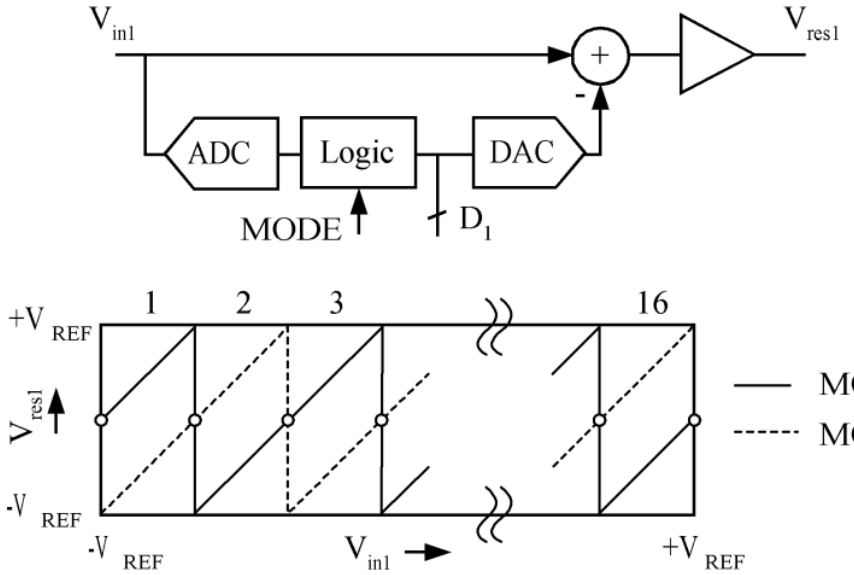


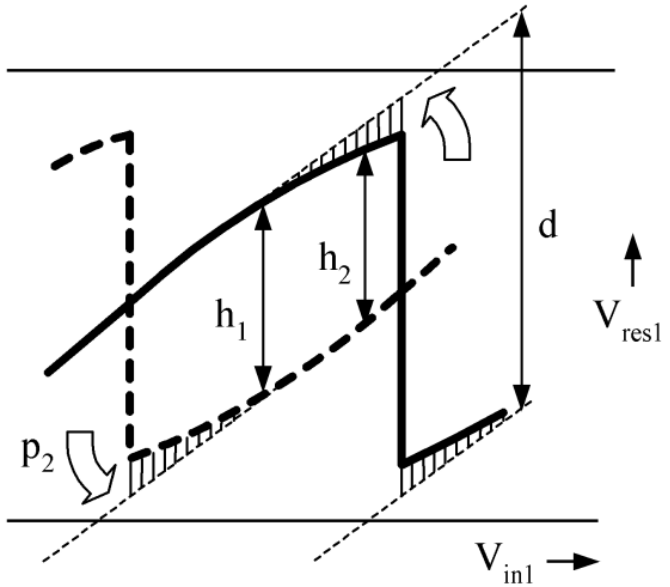
$$e(D_b) = D_b - 2\sqrt{-\frac{1}{3p_2}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_b}{2\sqrt{-\frac{1}{27p_2}}}\right)\right]$$

where, D_b is the back-end ADC output and the calibration engine estimates p_2.

B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (5)

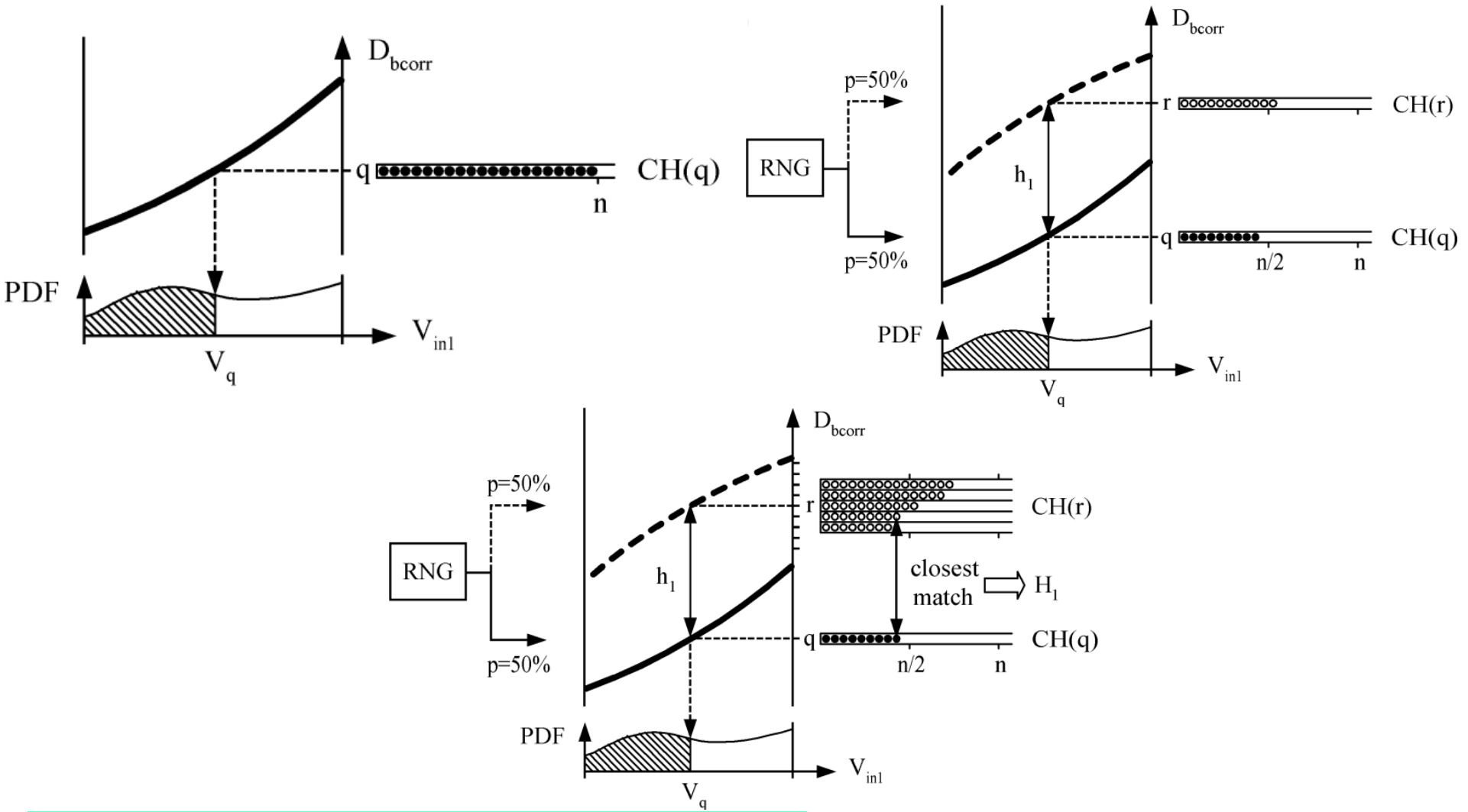




- V_{res1} can generate two curves based on the digital random-bit MODE.
- In order to accommodate the two transfer curves and not saturate the back-end ADC stage-2 has 1-bit of redundancy.
- The residue characteristic with nonlinearity shows compression.
- Nonlinearity is overcome if $h_1 = h_2$, i.e. the distance between the two residue characteristic is constant at all points.
- Its sufficient to estimate the distance at the center and at the extremes.

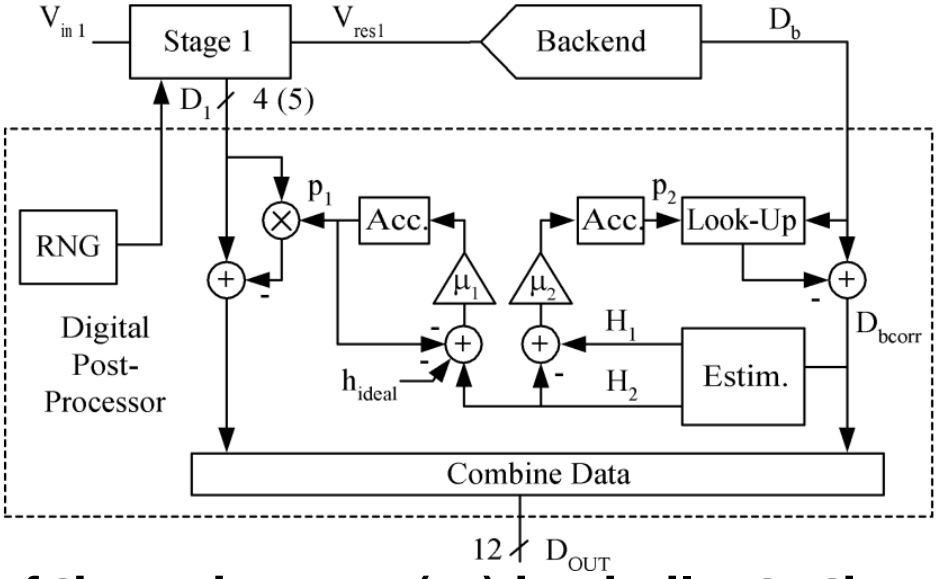
B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (6)



B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (7)



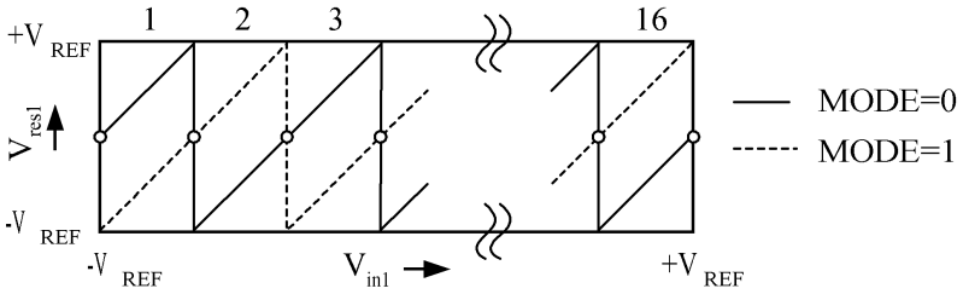
- Estimation of the gain error (p_1) is similar to the method in Li2003.
- Estimation of nonlinearity (p_2) is based on an LMS method which minimizes the MSE of $(H_1 - H_2)$.
- $(H_1 - H_2)$ is a function of p_2 as per

$$e(D_b) = D_b - 2\sqrt{-\frac{1}{3p_2}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_b}{2\sqrt{-\frac{1}{27p_2}}}\right)\right]$$

B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

Open Loop Op amp Nonlinearity Calibration (8)

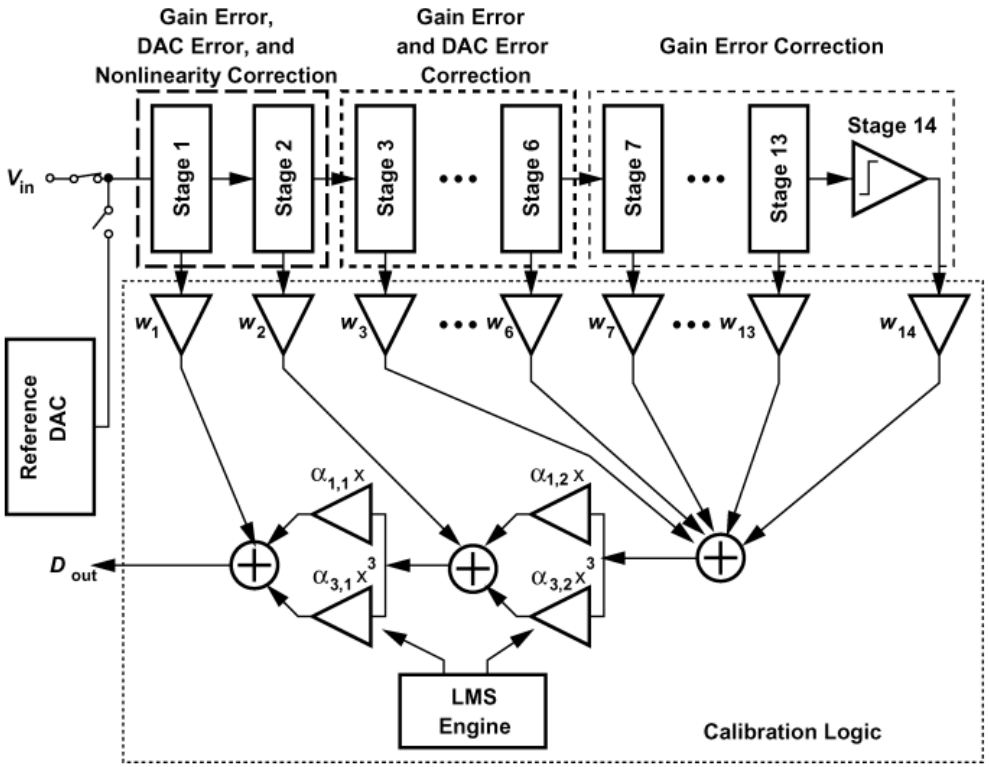
- Requires that the inputs be sufficiently busy, i.e., the analog input to the ADC be such that it exercises all the ADC levels. If the signal is not full scale then the calibration cannot estimate the nonlinearity.
- As shown below in the residue characteristic of stage-1, if the signal is within 1/16th of the full scale then also it exercises the full-scale of the back-end ADC and hence estimates the nonlinearity.



- The open-loop amplifier is very susceptible to gain variation due to temperature. If the LMS loop has a smaller time-constant as opposed to the gain variation then the calibration works.

B. Murmann and B. E. Boser, IEEE JSSC, vol. 38, pp. 2040-2050, Dec. 2003.

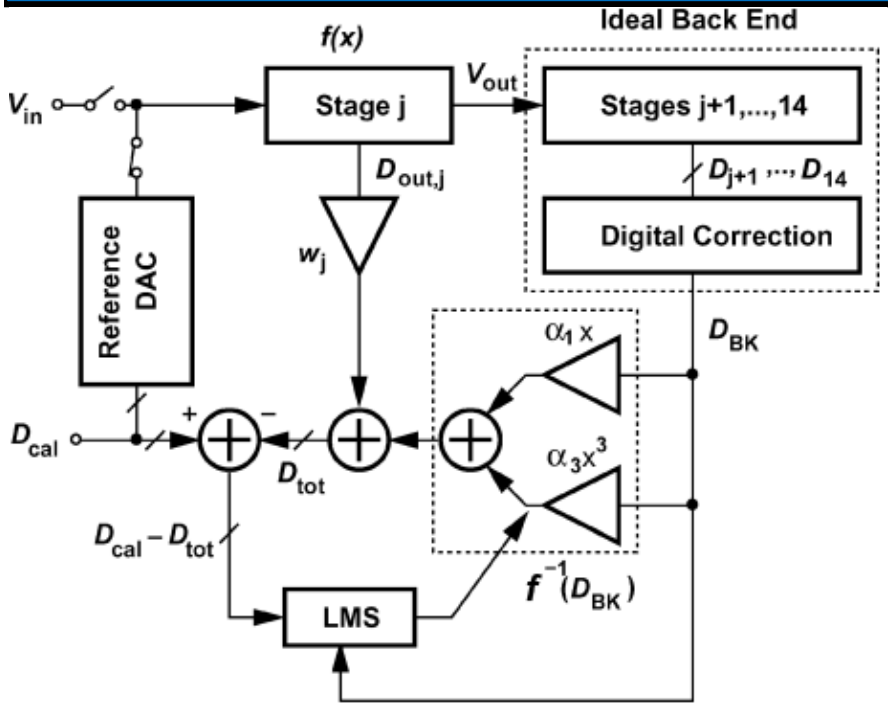
10-bit 500 MHz 55 mW CMOS ADC (1)



A. Verma and B. Razavi, IEEE JSSC, vol. 44, pp. 3039-3050, Nov. 2009.

- All stages use 1.5-bit flip-around topology.
- Gain error, capacitor mismatch, and op amp nonlinearity correction done in the 1st two stages.
- Gain error and capacitor mismatch calibration done in stage 3 to 6.
- No calibration for the remaining stages.
- LMS is used to do gain error and op amp nonlinearity calibration.

10-bit 500 MHz 55 mW CMOS ADC (2)



- Calibration requires a precision DAC.
  - For the 10-bit system here the reference DAC has to be 11-bit linear
- Calibration applies $\pm V_R/2$, $\pm V_R/4$, and 0 from the reference DAC to stage-*j* for calibration.
- Stage-*j* is configured in multiply-by-2 configuration.
- The digitized output of stage-*j* is given by

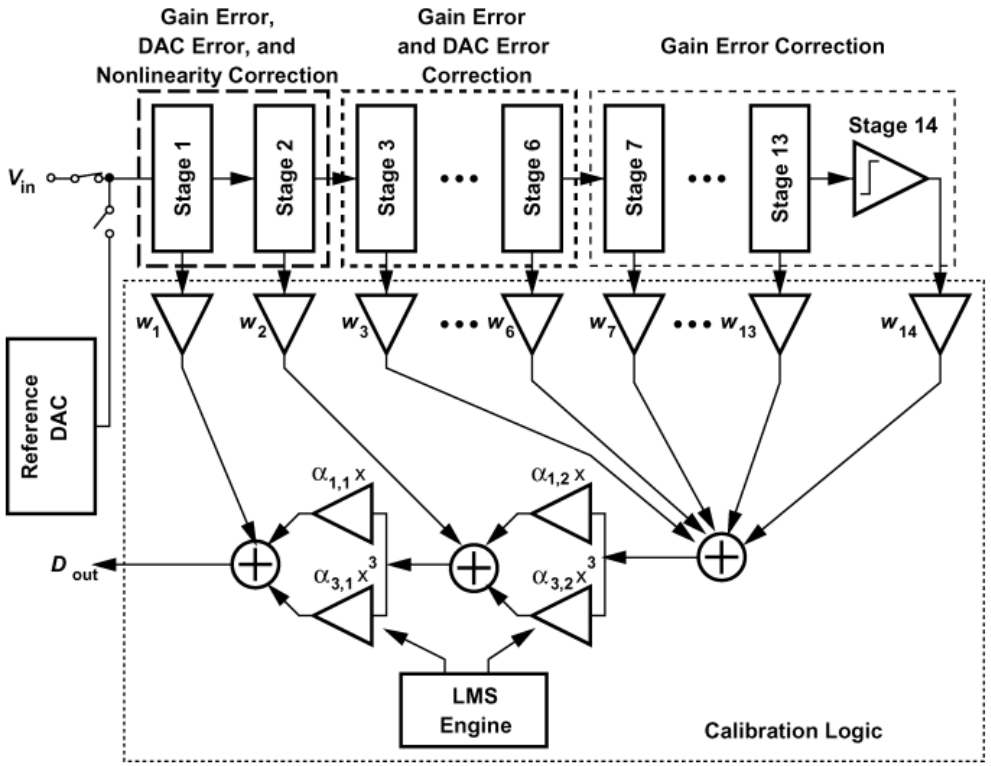
$$D_{tot} = \alpha_1 D_{BK} + \alpha_3 D_{BK}^3$$

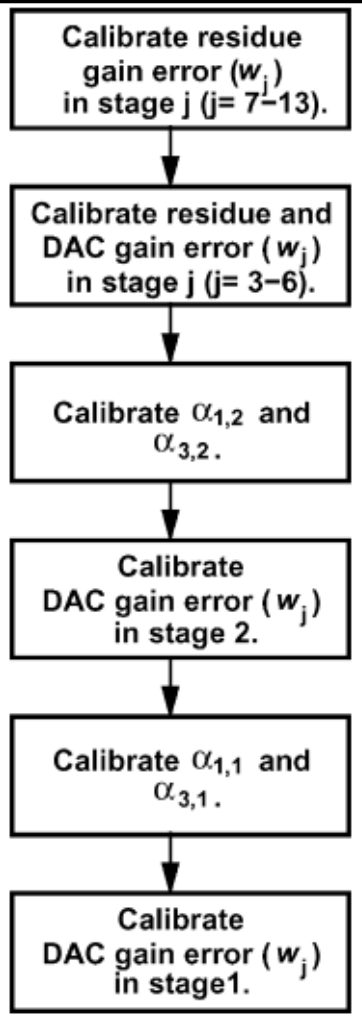
- α_1 and α_3 are updated using the following LMS equation:

$$\alpha_1(k+1) = \alpha_1(k) + \mu(D_{cal} - D_{tot})D_{BK}$$
$$\alpha_3(k+1) = \alpha_3(k) + \mu(D_{cal} - D_{tot})D_{BK}^3$$

A. Verma and B. Razavi, IEEE JSSC, vol. 44, pp. 3039-3050, Nov. 2009.

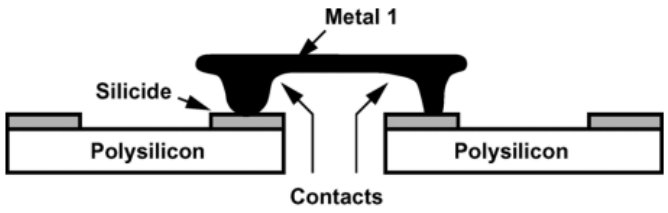
10-bit 500 MHz 55 mW CMOS ADC (3)

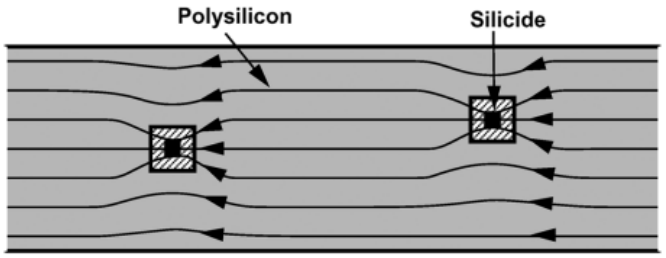


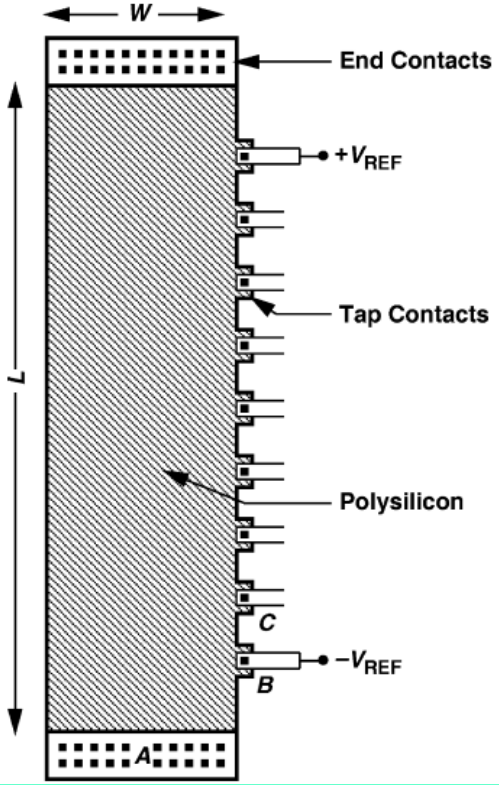


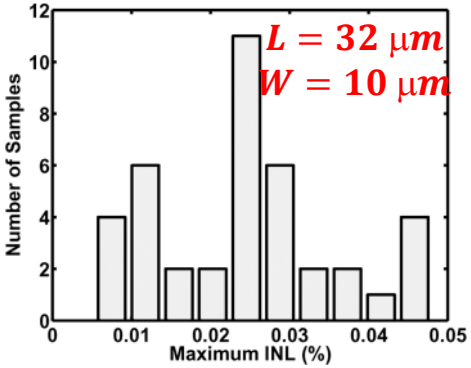
A. Verma and B. Razavi, IEEE JSSC, vol. 44, pp. 3039-3050, Nov. 2009.

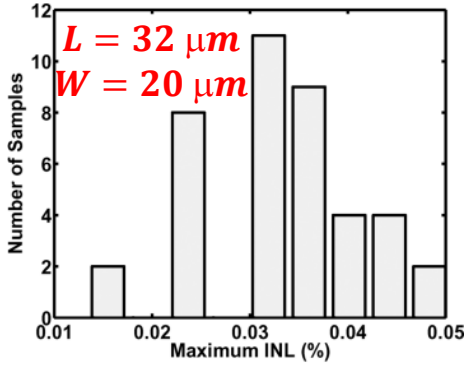
10-bit 500 MHz 55 mW CMOS ADC (4)

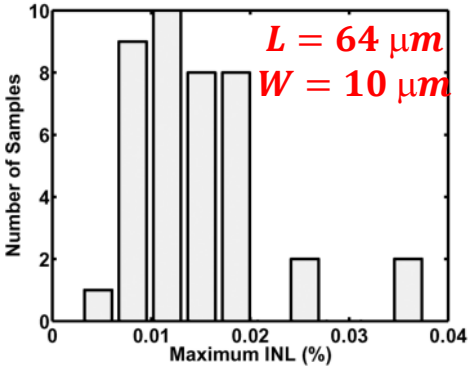


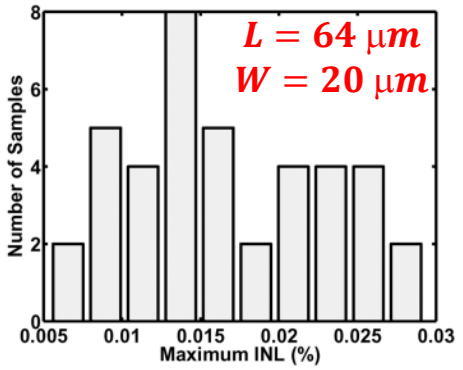












A. Verma and B. Razavi, IEEE JSSC, vol. 44, pp. 3039-3050, Nov. 2009.

10-bit 500 MHz 55 mW CMOS ADC (5)

- Calibration requires a precision DAC.
  - For a10-bit system the reference DAC has to be 11-bit linear
  - For a 12-bit system the reference DAC has to be 13-bit linear
  - Difficult to realize highly linear and precise DACs
  - The calibration technique cannot be used to calibrate more than 10-bit systems.
- Calibration applies signals from the resistor ladder ➔ calibration cannot be run at the full-speed of the ADC because of the RC-settling issue.
- High frequency settling behavior of the op amps is not captured.

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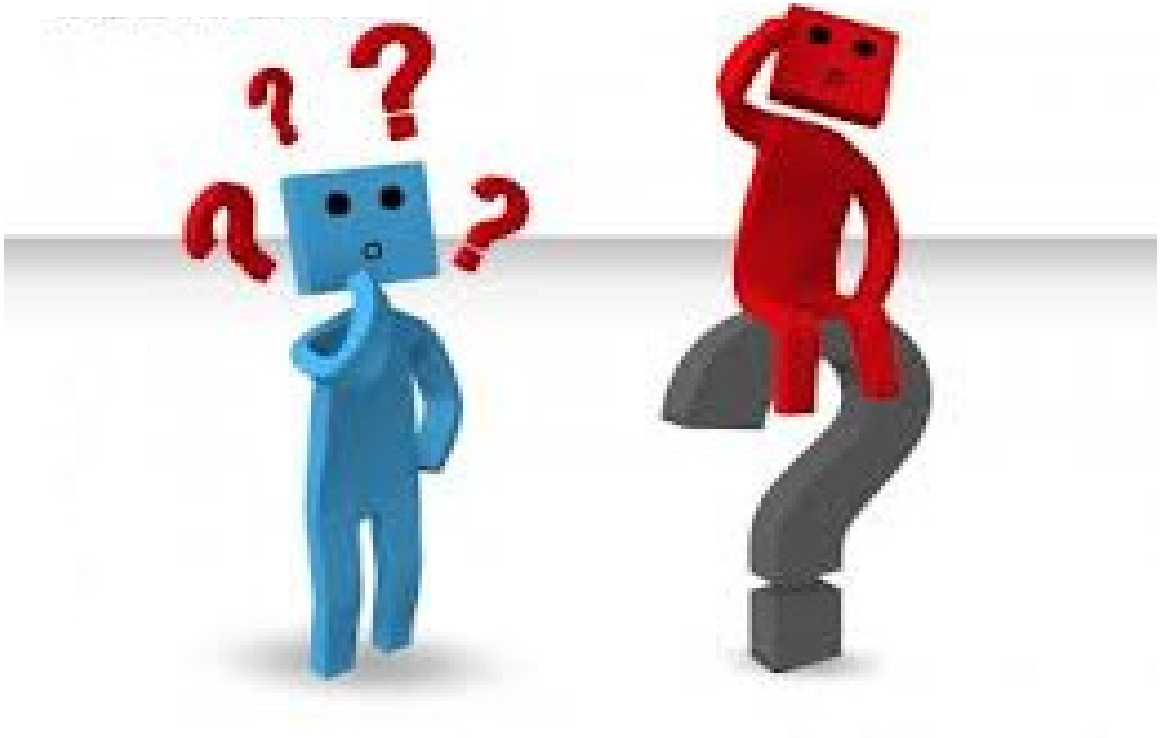
Thank You



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