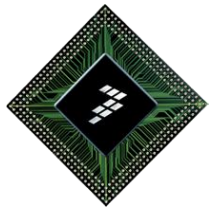
Analog-to-Digital Converters for Software Definable Radios



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freescale™ semiconductor

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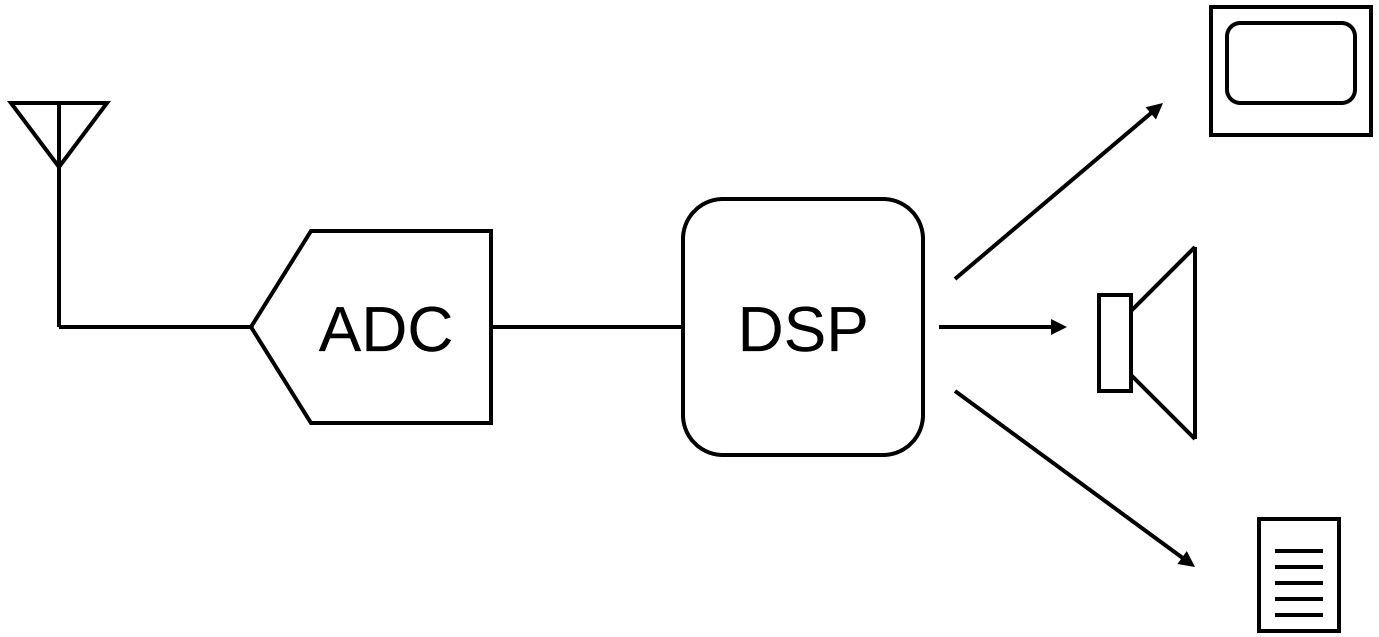
Analog-to-Digital Converters for Software-Definable Radios

- Intro
  - Radio architecture considerations
  - ADC limitations
- Case Study #1: Discrete-Time $\Sigma\Delta$ with Multi-bit Quantizer
  - Architecture
  - Circuit Design
  - Measurements
  - Alternate approaches
- Case Study #2: Pipelined Redundant-Signed-Digit (RSD) ADC
  - Architecture
  - Double-sampling
  - Issues
  - Measurements
- ADCs in other parts of the radio
- Conclusions

The Ideal Software-Definable Radio Receiver:



ADC at the Antenna
DSP performs all selectivity and BB processing
Maximum Flexibility

Initial thoughts on power dissipation:

$2 * Fs = 2 * P$

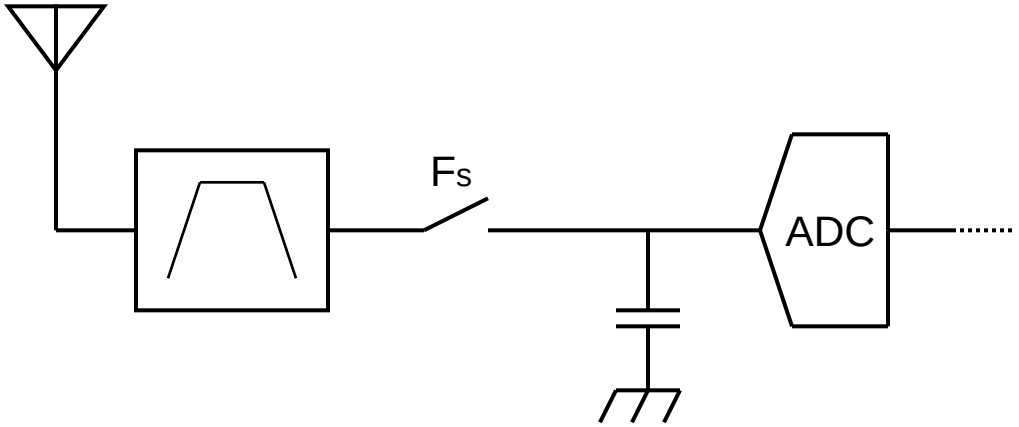
Adding one bit of resolution = $4 * P$

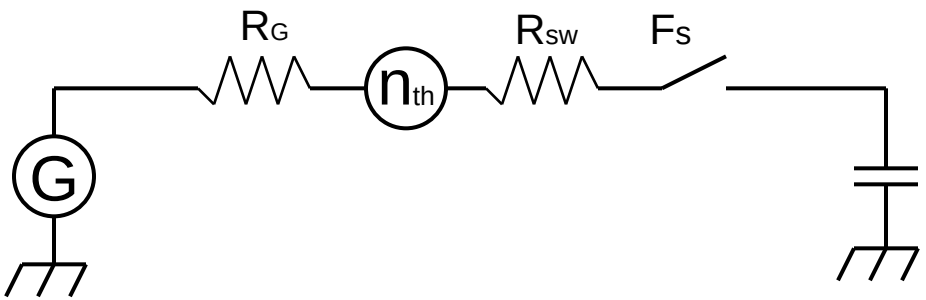
FILTERING IS KEY

One more bit of resolution only adds 6dB to the ability of the receiver to reject interferers. Filtering is much cheaper!!

Trend towards wider bandwidth modulations with stringent close in blocker specs places incredible demands on ADC design. Usually filtering is easier!!

Now, assume the filtering is sufficient to allow us to ignore aliasing issues.





$N = \frac{kT}{C}$ ← Thermal noise of switch

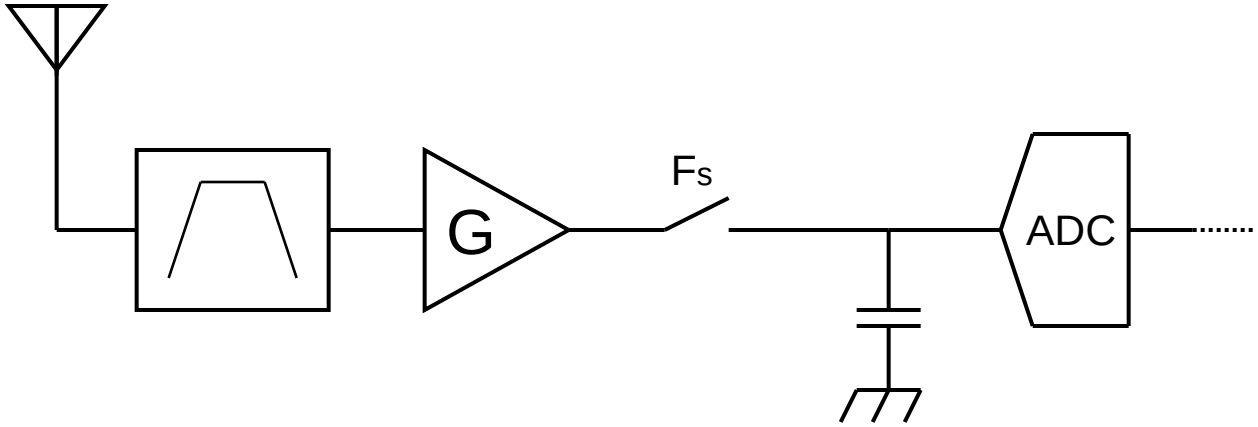
$F_S R_G = \frac{1}{C}$ ← Max power transfer condition

$N = kT\, F_S\, R_G$

Similar to purely resistive case → $SNR = \frac{P_{SIG}}{kT\, F_S}$

Conclusion : Need amplifier before the sampler!

Still assuming we have sufficient filtering, but now a fixed gain in the pre-amp, how much ADC dynamic range do we need?



Requirements vary, but 80 to 100dB of receiver dynamic range is not uncommon nor unreasonable to expect.

This means the ADC must be at least 13 bits.
What does that cost?

As stated previously:

$$P_{ADC} \propto F_s$$

$$P_{ADC} \propto 4^N$$

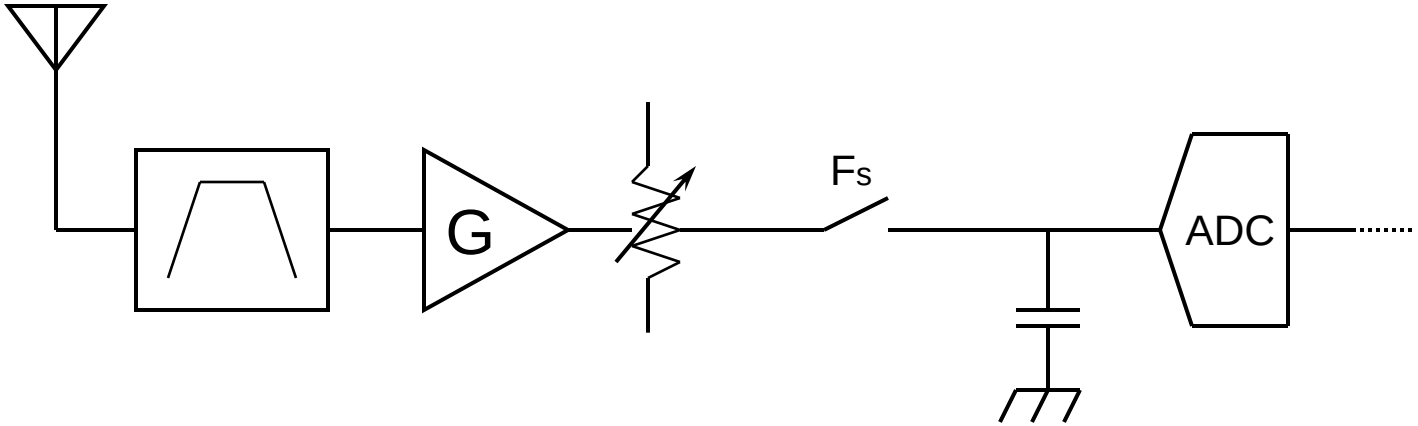
If an ADC is optimized for low power:

- Each doubling of Fs costs at least 2X power.
- Each additional bit of resolution costs at least 4X power.

An additional bit of ADC resolution buys only 6dB of dynamic range. It is usually more cost effective to provide 6dB of AGC.

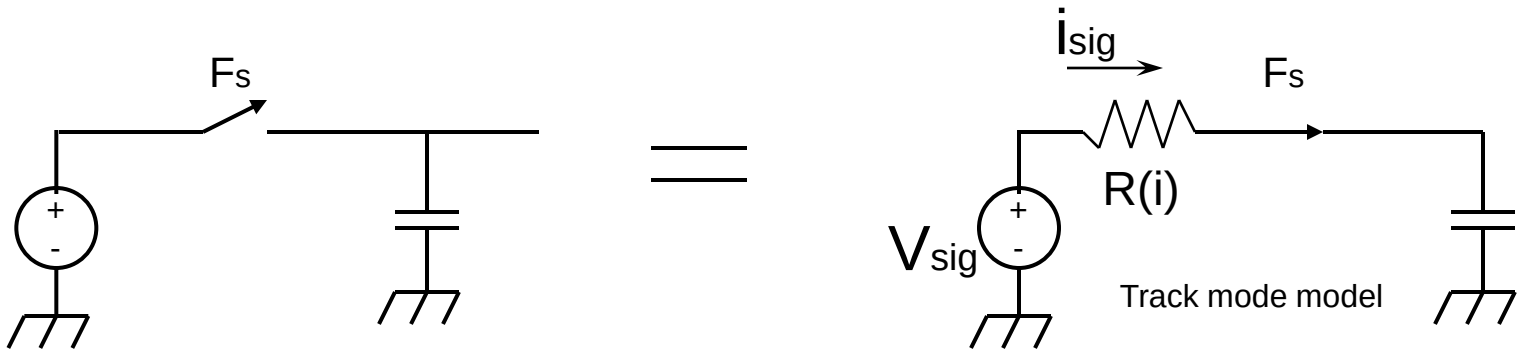
This will probably remain the case regardless of improvements in transistor technology, CCD samplers, or MEMS development.

So, now the RF sampling radio looks something like this.



Two more issues:
Switch Linearity
Sampling Jitter

Switch Linearity



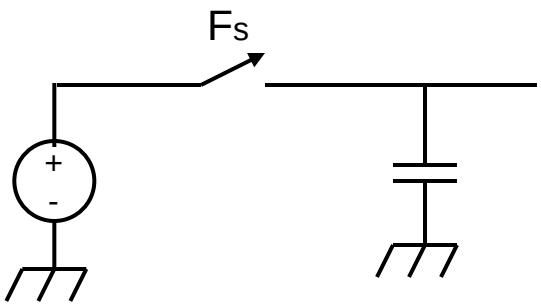
The switch is modeled as a non-linear resistance in series with an ideal switch.

The voltage sampled onto the cap deviates from the ideal in proportion to the signal current.

The signal current is directly proportional to the signal frequency and the cap size.

∴ You would like to sample low frequency signals onto small caps.

Sampling Jitter

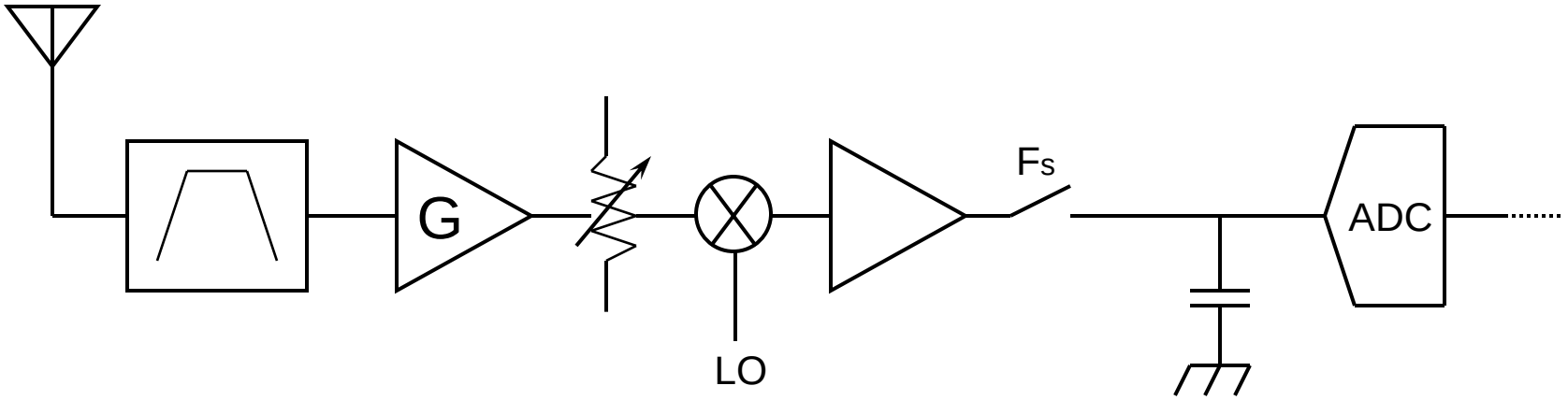


Phase noise in the sampling instant = increased noise floor.

$$SNR \propto \frac{1}{\omega_{sig}^{2}\sigma_{j}^{2}}$$

∴ Again, you want to sample low frequency signals.

A sampler can be thought of as a very non-linear mixer. Almost any imaginable improvement in sampler technology should be accompanied by a similar improvement in mixer technology. For high frequency signals, mixers are generally better behaved and more efficient to implement.



Look Familiar?

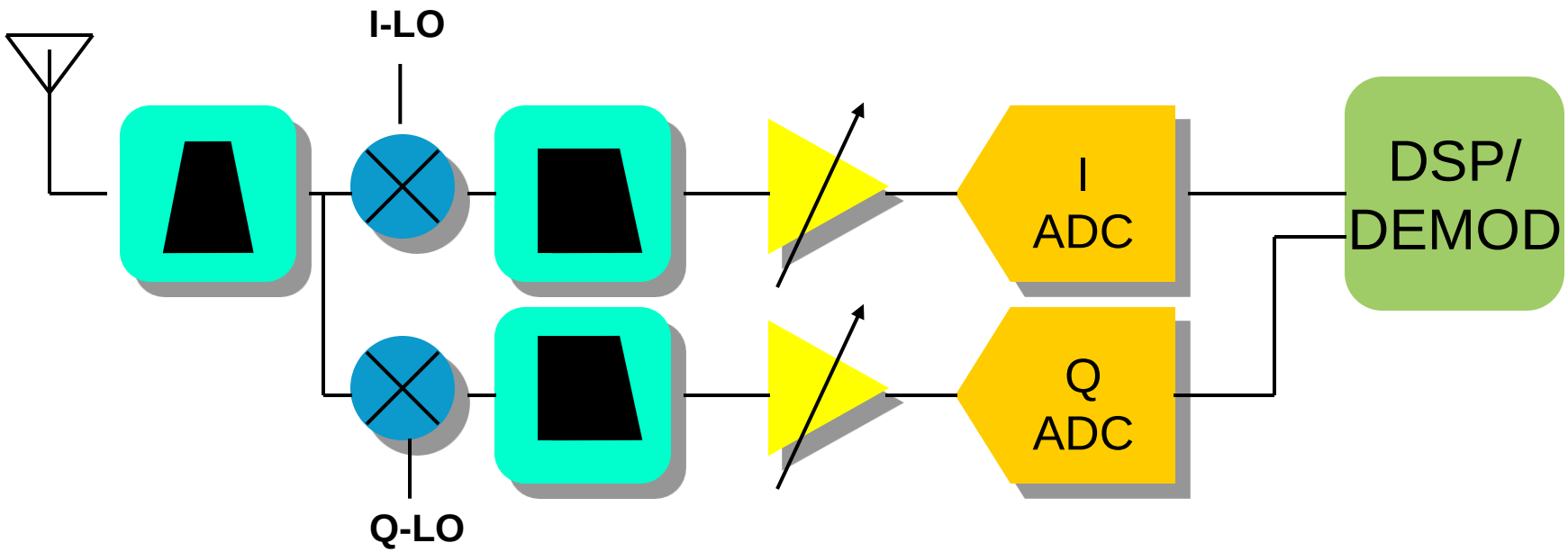
Initial Conclusions:

- **It is possible to make a very poor performing receiver with a simple sampling circuit at the antenna.**
- **The idea that an ADC can be put at the antenna and somehow rid a high performance radio of the LNA, BPF, AGC, and MIXER is a pipe dream. At the least, it's not the most efficient approach.**
- **The direct conversion approach is a good one for exploiting today's ADC technology and provides a good platform for migrating to future ADC architectures.**
- **Two new technologies that may improve ADC performance and thus relax requirements on the above mentioned blocks are:**

  MEMS - switches, resonators, filters, (resonant sampling switch?, mixer?) [C. T. C. Nuygen, "Vibrating RF MEMS for Next Generation Wireless Applications", proceedings 2004 CICC, pp. 257-264]

  Continuous time and/or multi-bit $\Sigma\Delta$

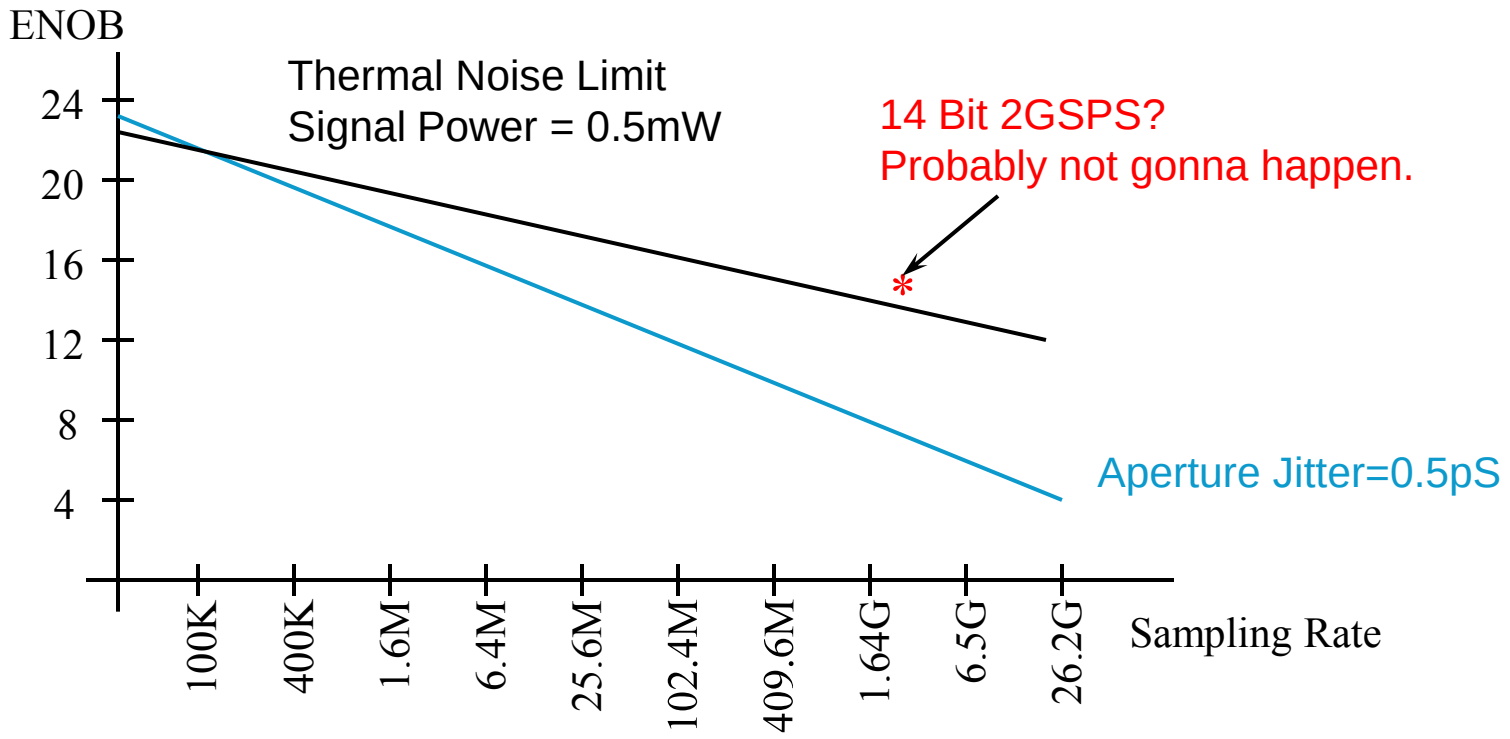
- **Tunable filters at the front end are key to multi-band receiver and will probably arrive first.**



Direct Conversion/Baseband Sampling

- Line-up includes pre-select filter, at least one mixer with the final mixer being quadrature and placing final IF at or near DC, LPF, AGC, and ADC followed by additional digital selectivity and demodulator.
- Moderate flexibility.
- Wide range of ADC requirements 4-15Bits 100KHz-10GHz.

ADC Type - Pipeline, Flash, Folding, and Sigma-delta.

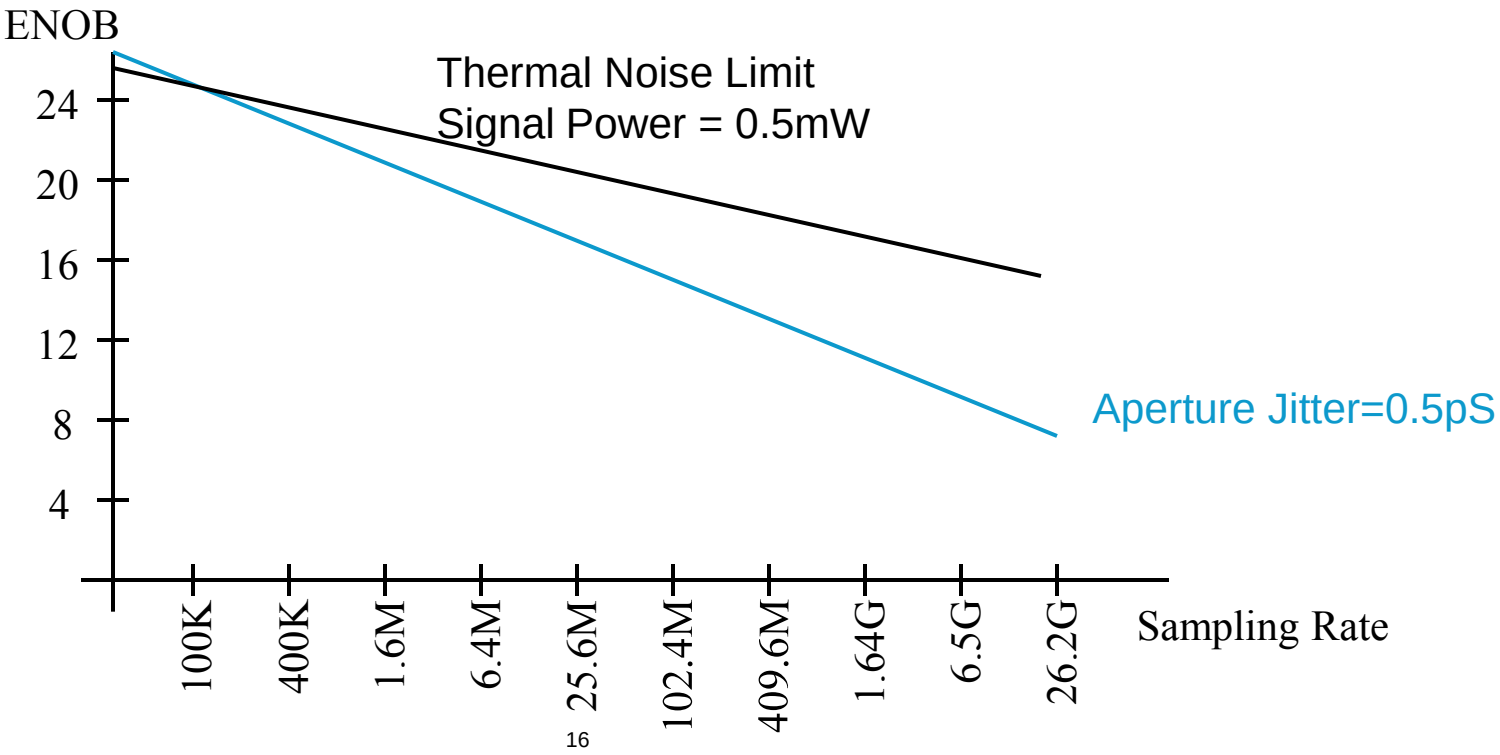


Fundamental limits of ADC resolution and speed.

Below 100kHz sampling rate, thermal noise limits ADC resolution for a given signal power.
At higher sampling rates sampling jitter limits resolution regardless of signal power.

Advances in ADC performance enable more flexible radio architectures.

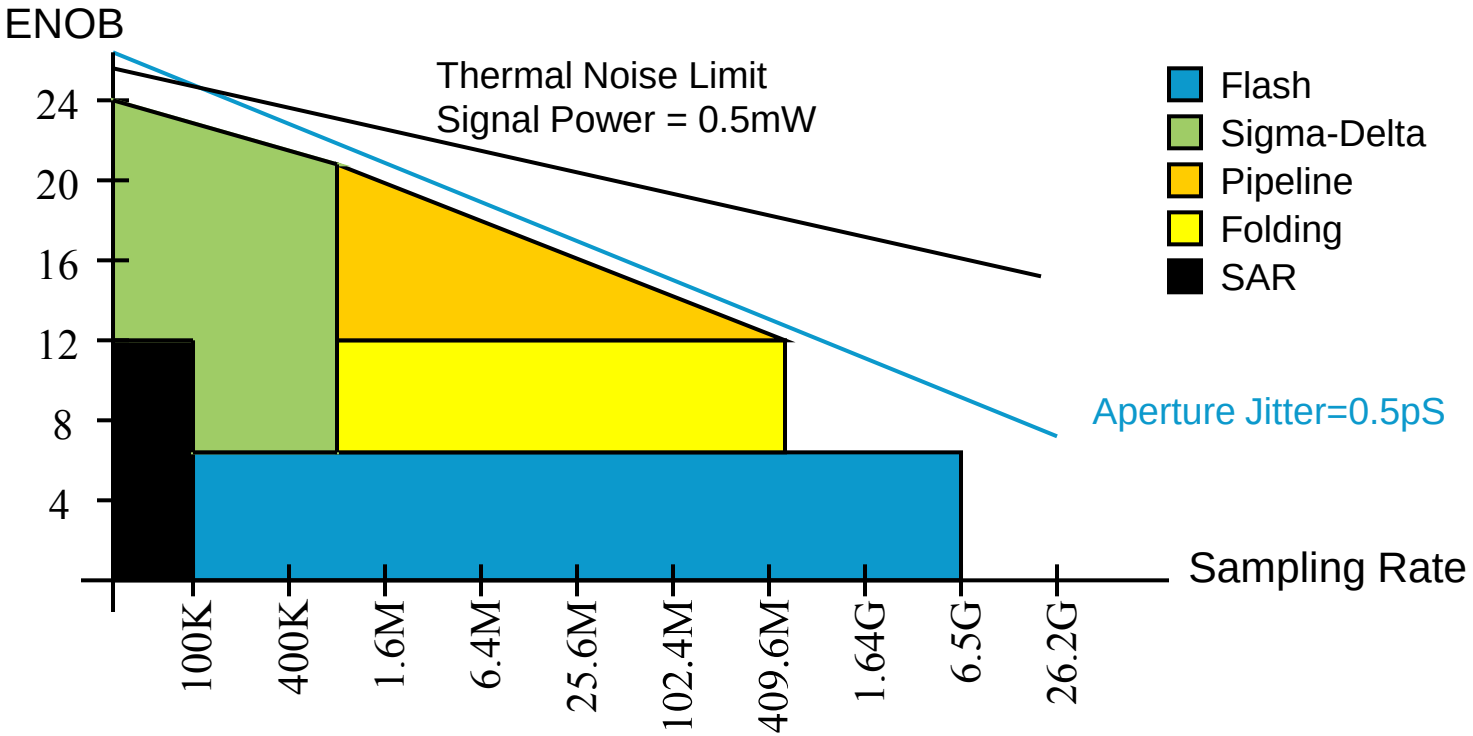
- **Below 1GHz sampling rates, state of the art ADC's available today are at or near the performance limit corresponding to 0.5pS sampling jitter.**
- **Improvement has been slow - about 1.5 bits at any given sampling rate over the last 8 years. [Walden, IEEE Comm. Magazine Feb. 1999]**



What type of ADC is best for DCRCV?

Well, it depends...

Different resolutions and bandwidths call for different ADC architectures.



Focus on ΣΔ and Pipeline ADCs.

- **Each architecture is starting to invade the territory of the other.**
- **Pipeline converters have acceptance for wide bandwidth (>10 or 20MHz) applications as long as latency is not an issue.**
- **Digital calibration techniques are making pipelines feasible for resolutions > 12 bits but the required digital circuitry consumes Si (best at <90nm process nodes).**
- **Matching issues tip the scale in favor ΣΔ over pipeline for resolutions > 10-12 bits and bandwidths up to a few MHz and process improvements are pushing up the sampling speeds.**
- **ΣΔ Bandwidth is inherently programmable at the expense of SNR.**

Case Study #1:

Switched-Capacitor Multi-Bit Sigma-Delta ADC

Application

System design

Dynamic Element Matching Technique

Circuit design

Test results

M.R. Miller, C. S. Petrie, "A Multibit Sigma-Delta ADC for Multimode Receivers," IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, pp. 475-482, March 2003.

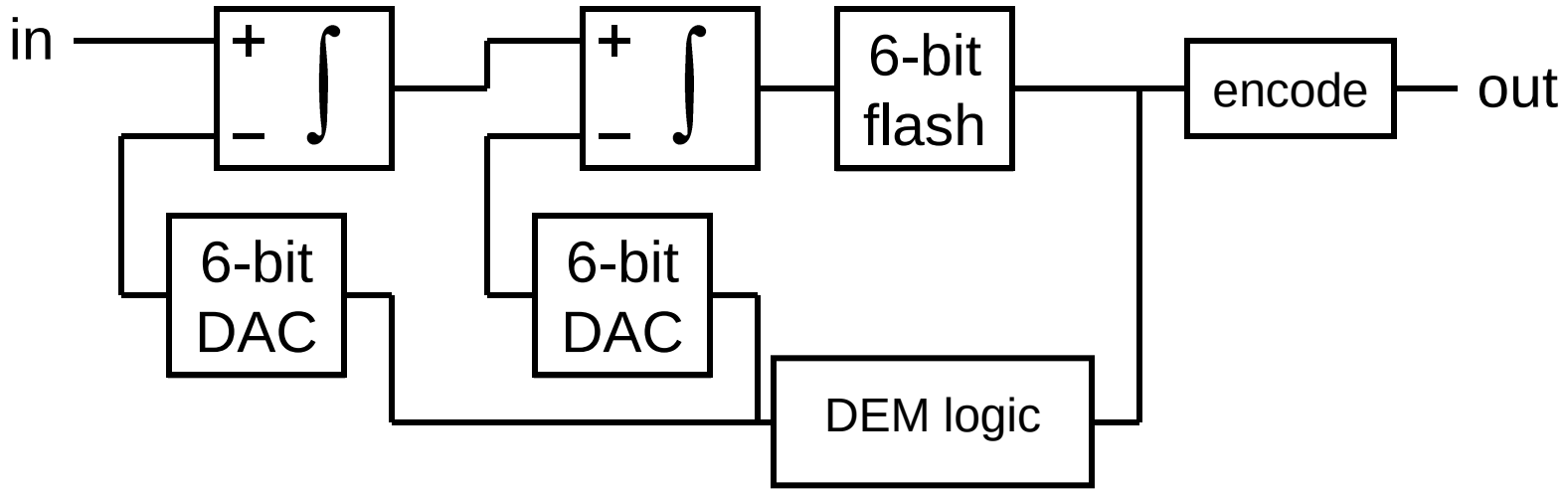
Motivation:

Single ADC to satisfy all cellular requirements:

- ✓ Handheld power dissipation (10's of mW)
- ✓ 0.18u CMOS part (Dual Gate Oxide process with MIM Cap)
- ✓ Variable and agile resolution

AMPS (15 kHz)	15 bits
GSM (180 kHz)	13 bits
CDMA (615 kHz)	12 bits
W-CDMA (1900 kHz)	11 bits

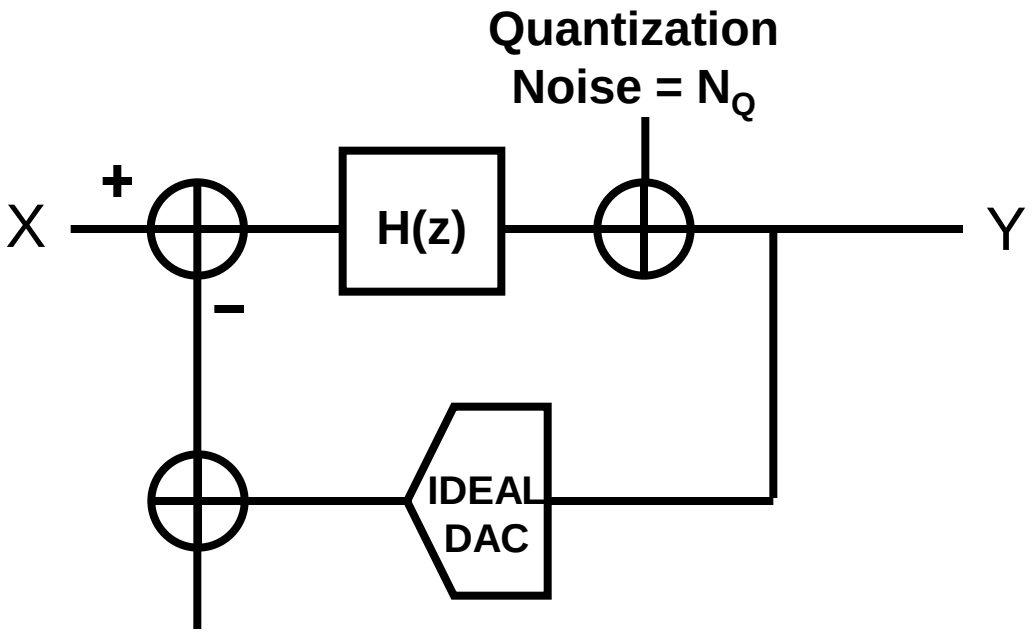
System Design - ΣΔ Architecture



Agility requirement points toward low order loop

High-resolution quantizer needed for W-CDMA

Make flash power ≈ integrator power ⇒ 6-bit flash ADC

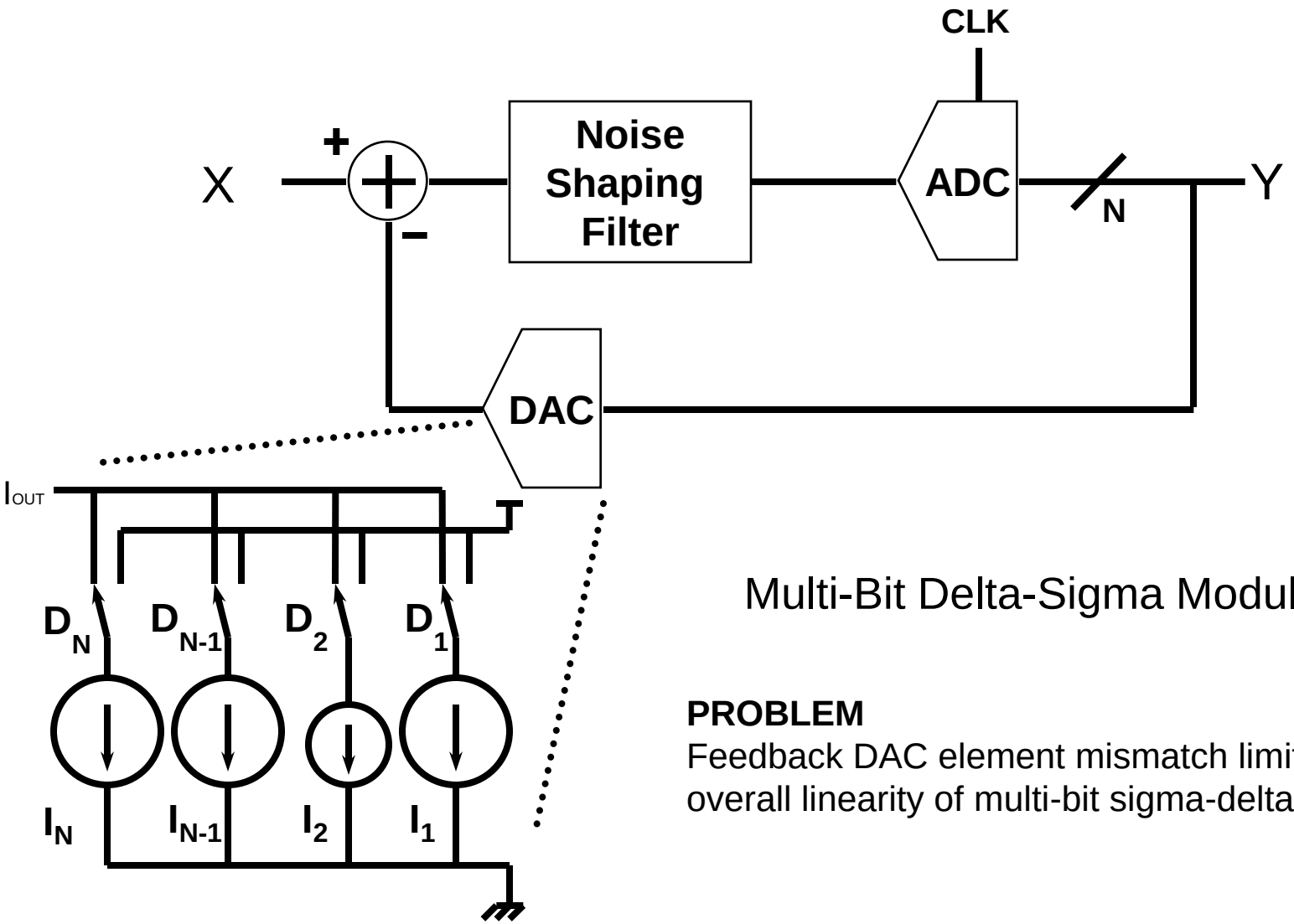


Multi-Bit Delta-Sigma Modulator - Linearized Model

$$Y = \frac{H(z)X}{1 + H(z)} + \frac{N_Q}{1 + H(z)} - \frac{H(z)N_D}{1 + H(z)}$$

Mismatch noise from DAC is unshaped.

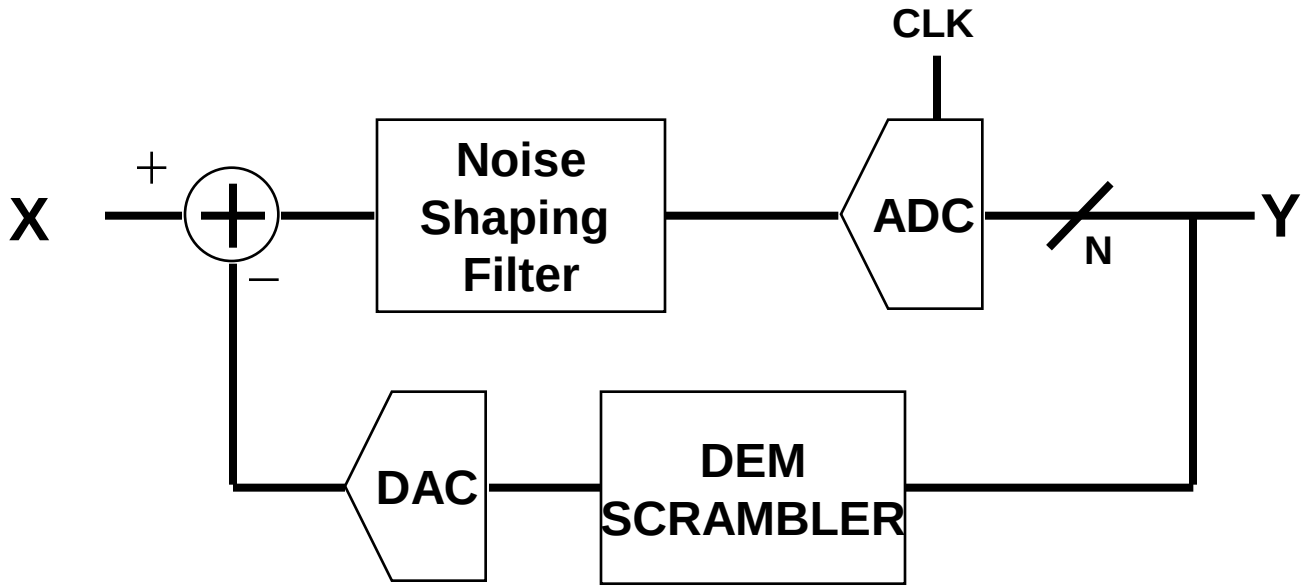
System Design - ΣΔ Architecture



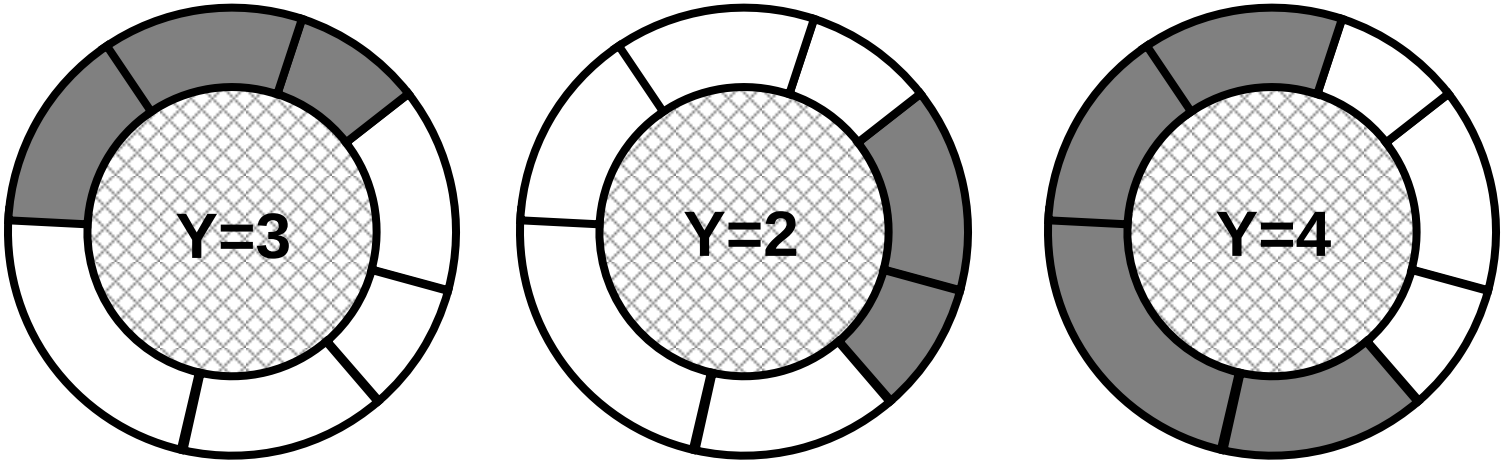
Multi-Bit Delta-Sigma Modulator

PROBLEM
Feedback DAC element mismatch limits overall linearity of multi-bit sigma-delta ADC.

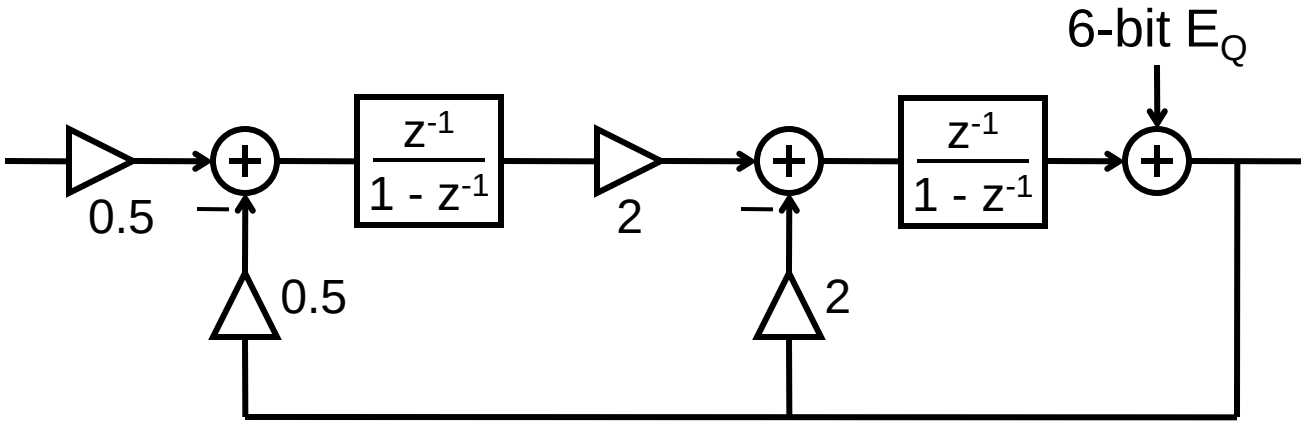
Noise-Shaped Dynamic Element Matching



EX: DAC states for code sequence 3, 2, 4

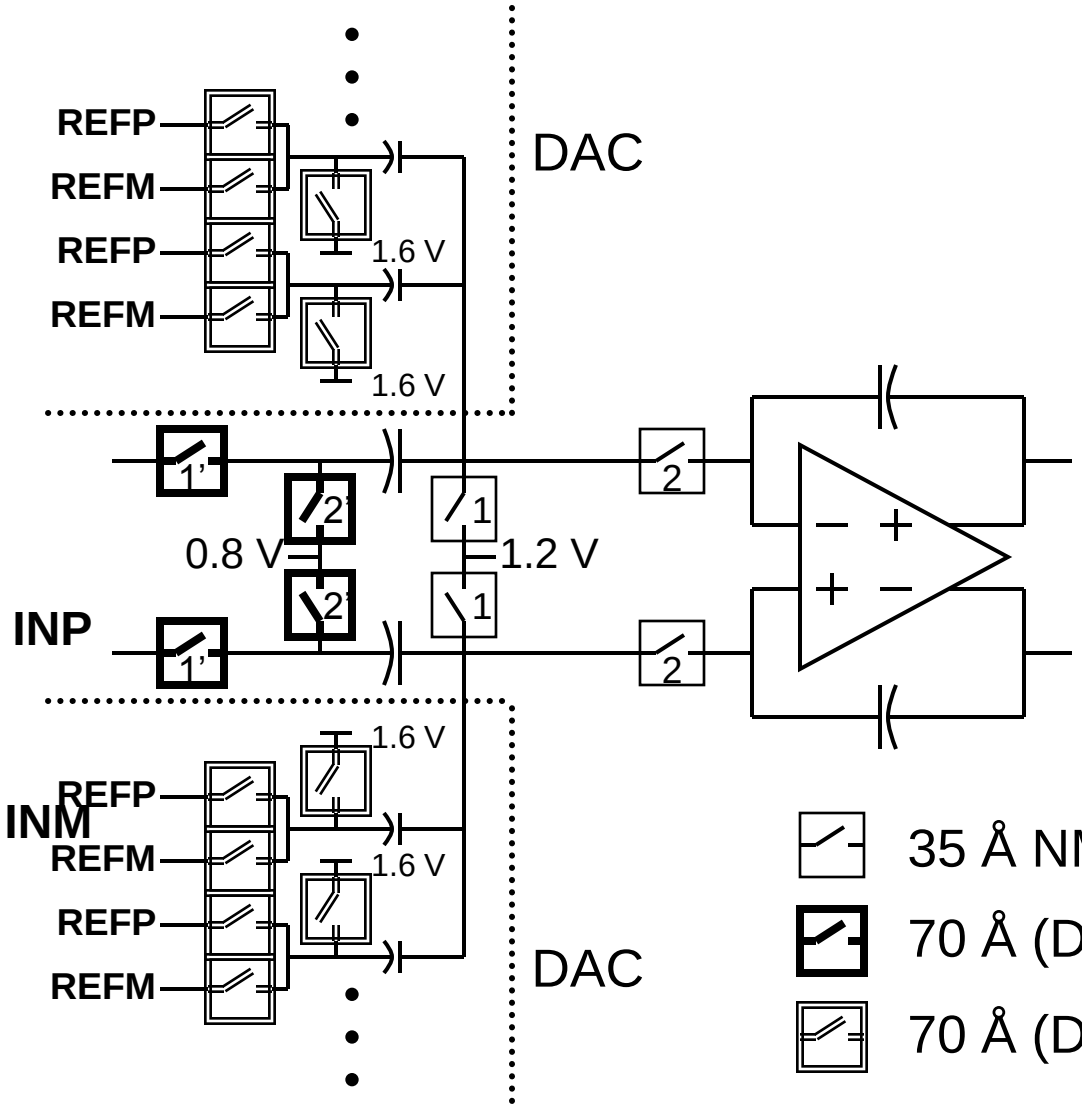


Circuit Design:



Gains chosen to keep integrator outputs within +/- 1.2 V differential

$$Y = X\, z^{-2} + N_Q(1-z^{-1})^2$$



Bottom-plate sampling

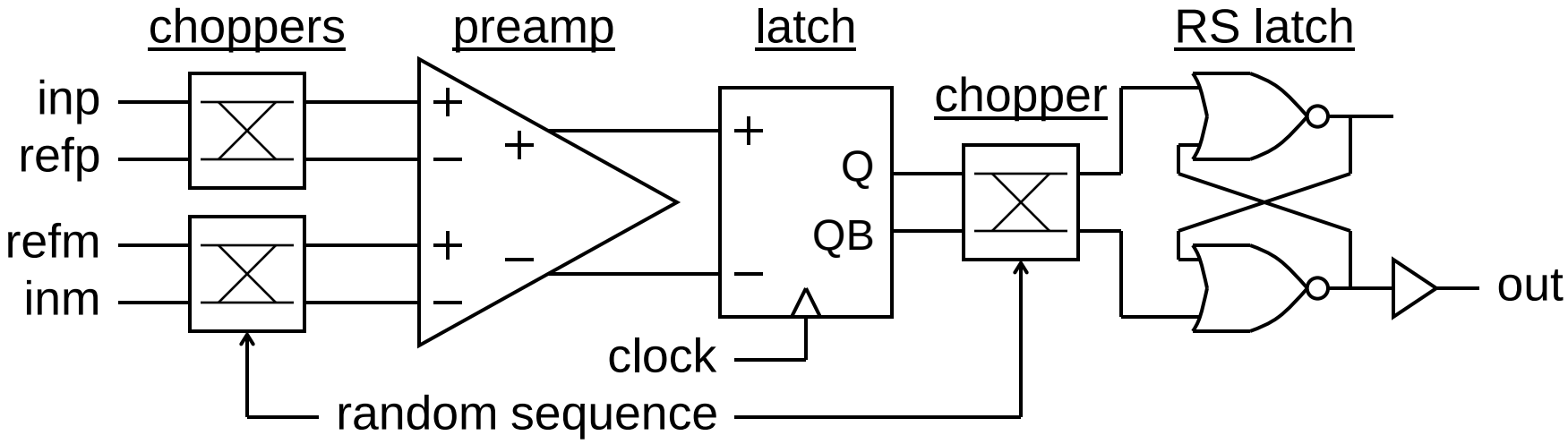
No correlated double-sampling

Judicious use of high voltage devices.

35 Å NMOS

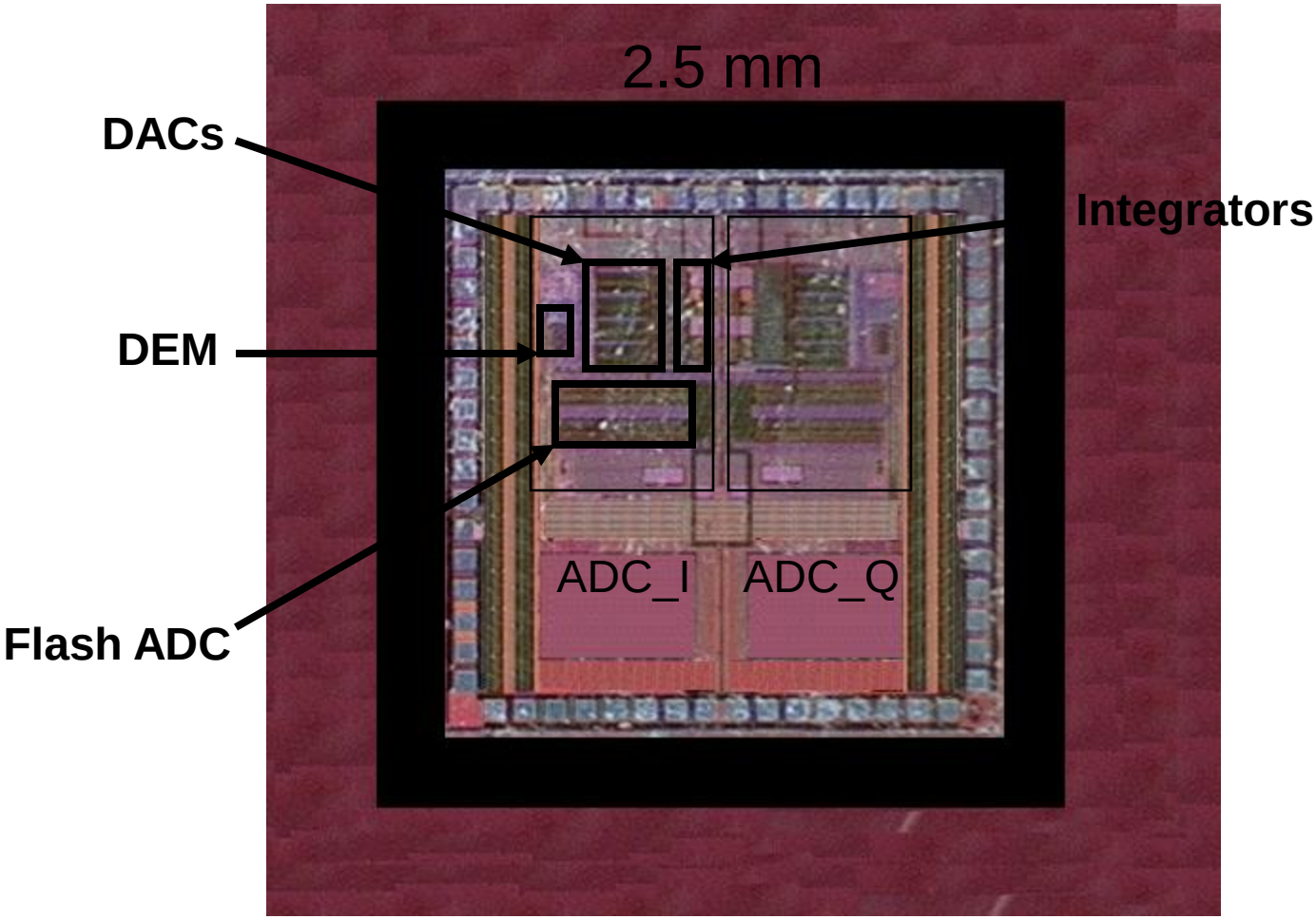
70 Å (DGO) NMOS (stage 1 only)

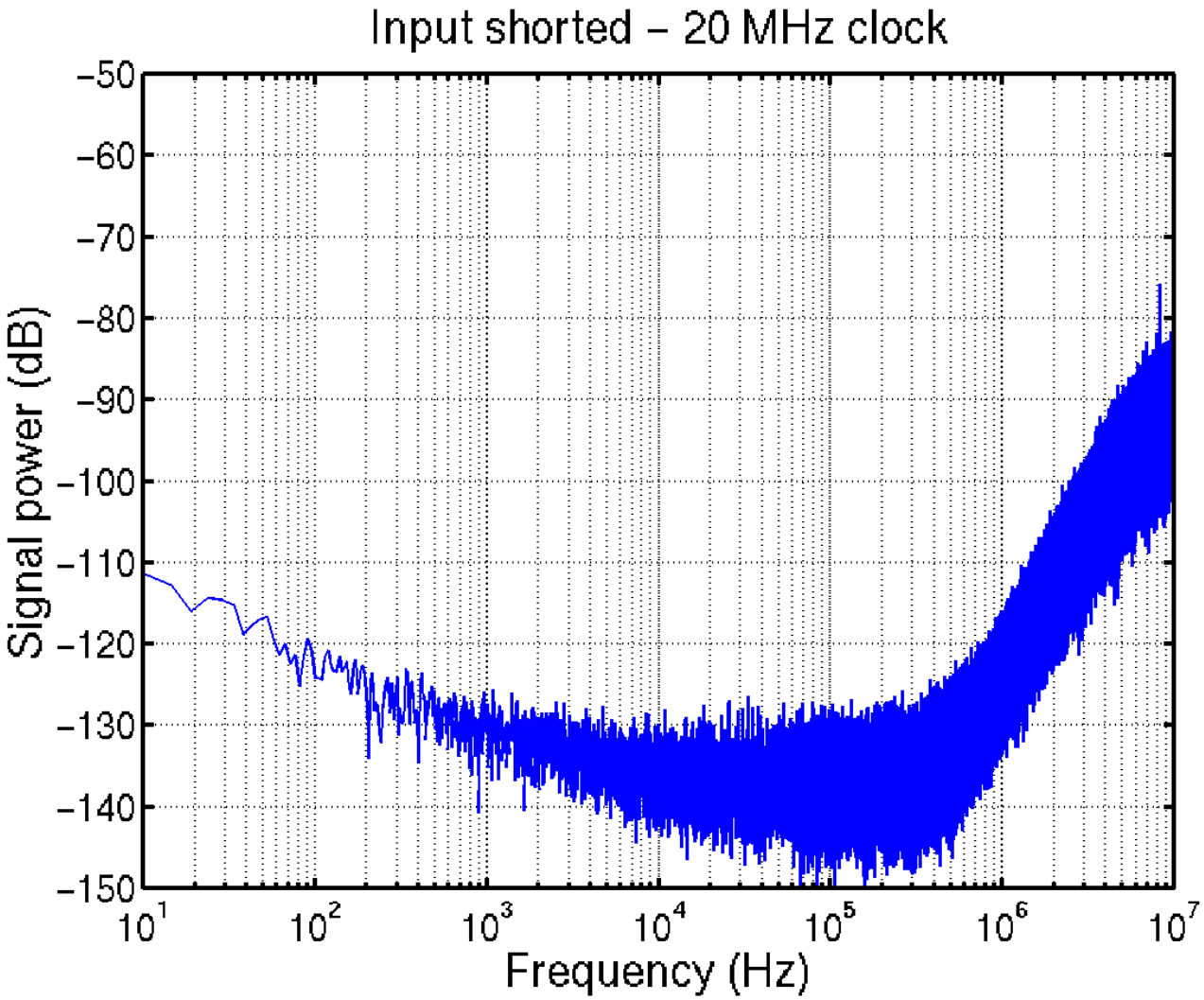
70 Å (DGO) TGATE

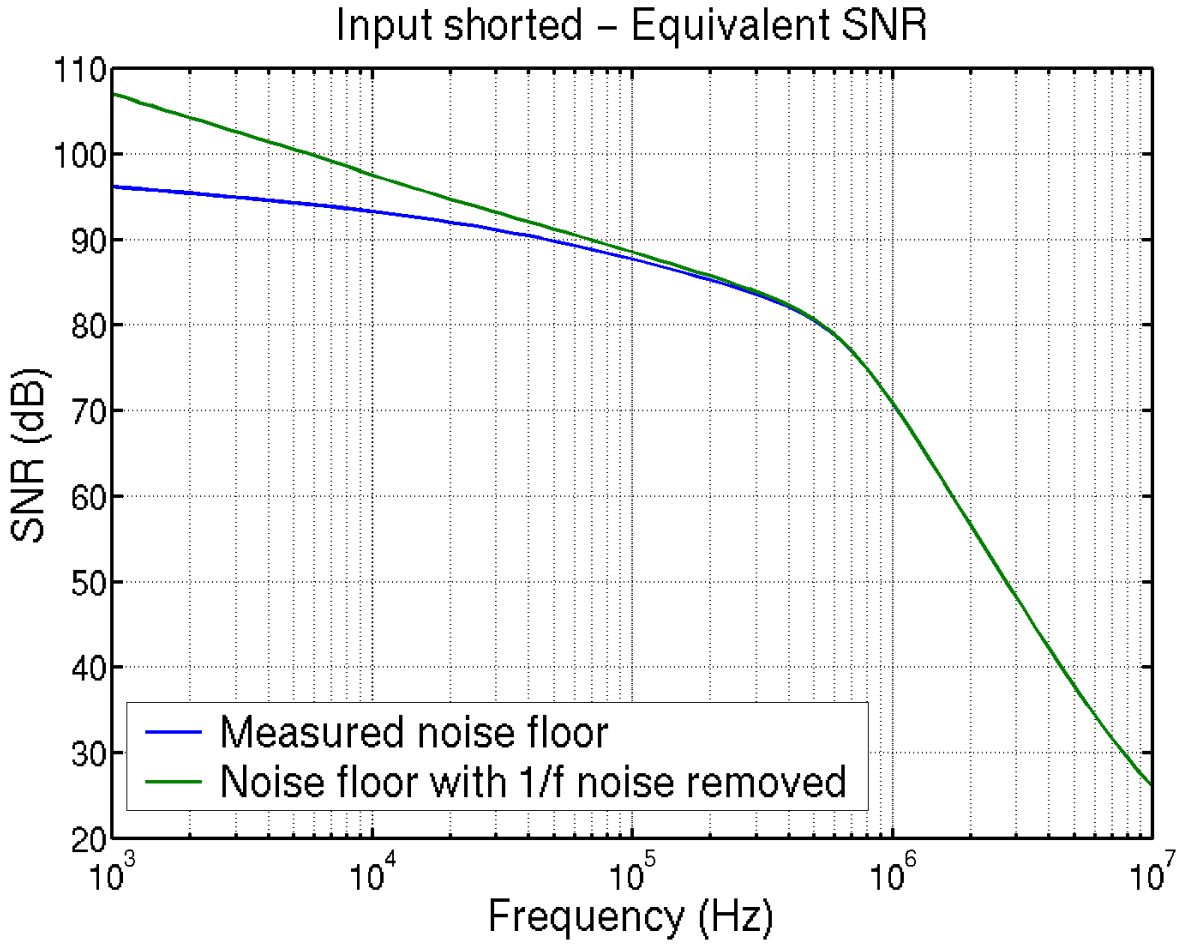


Offset chopping reduces high-frequency spurs by up to 20 dB (measured)

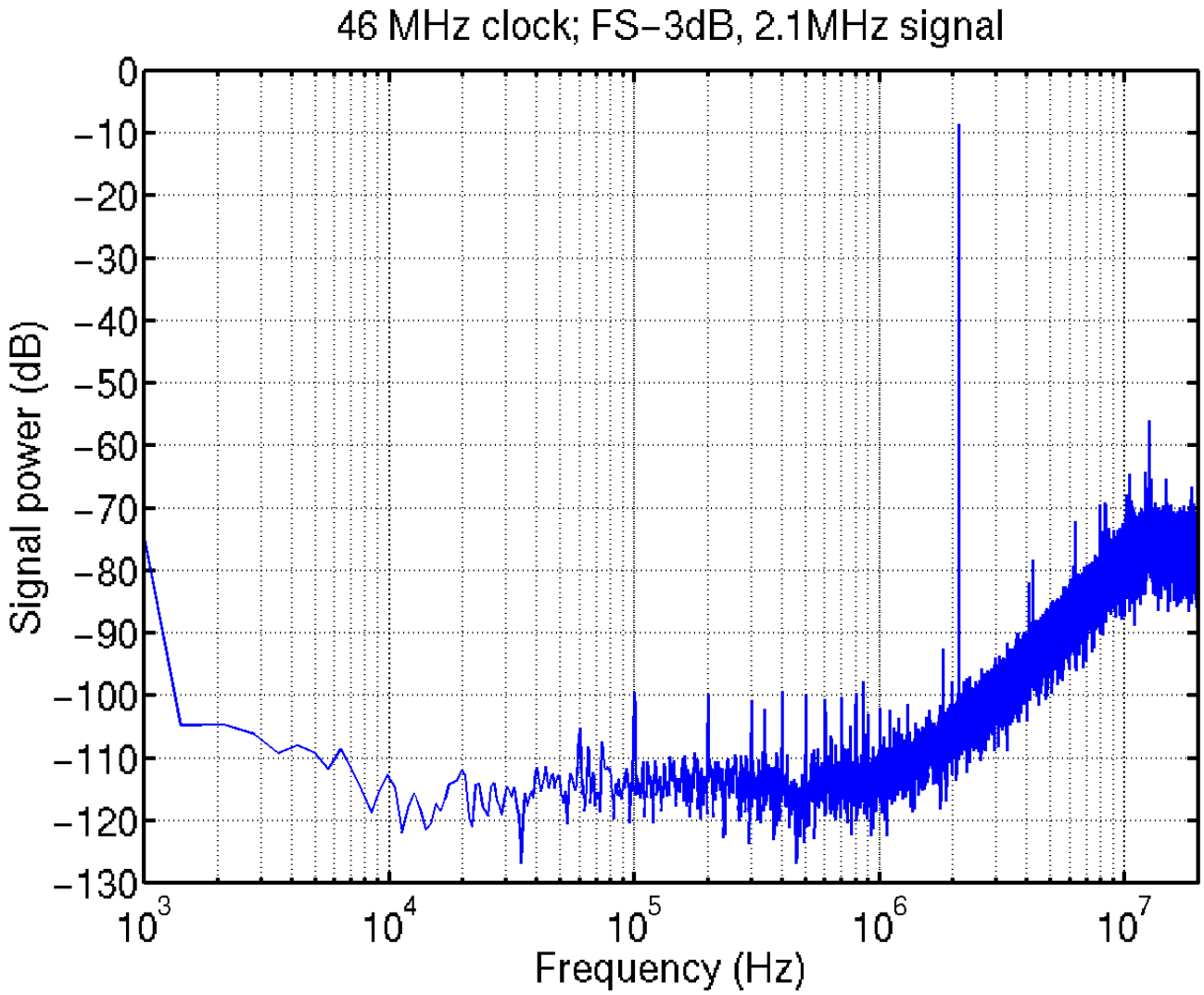
Chopping necessitates low impedance resistor string.

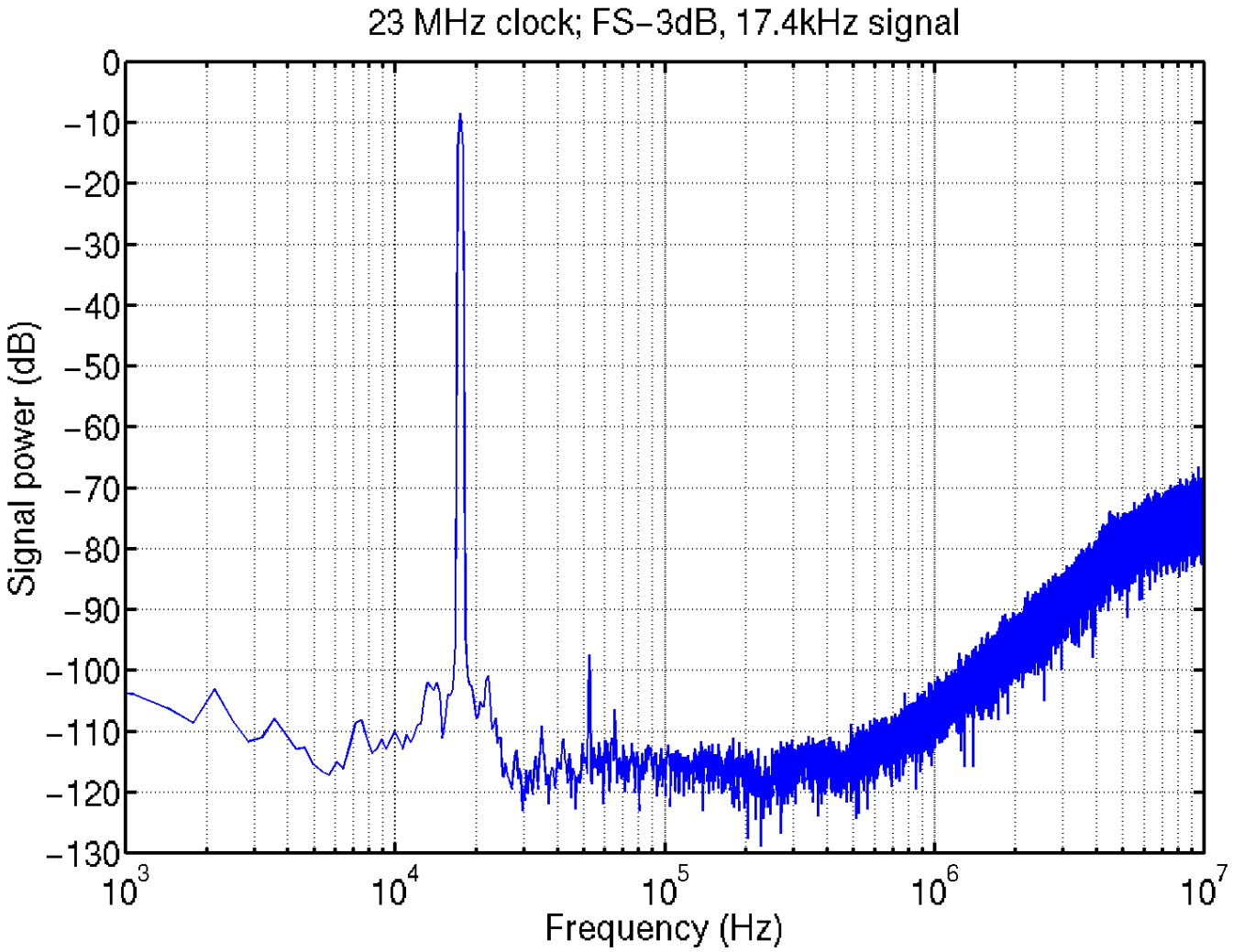

2.5 mm
DACs
Integrators
DEM
ADC_I
ADC_Q
Flash ADC

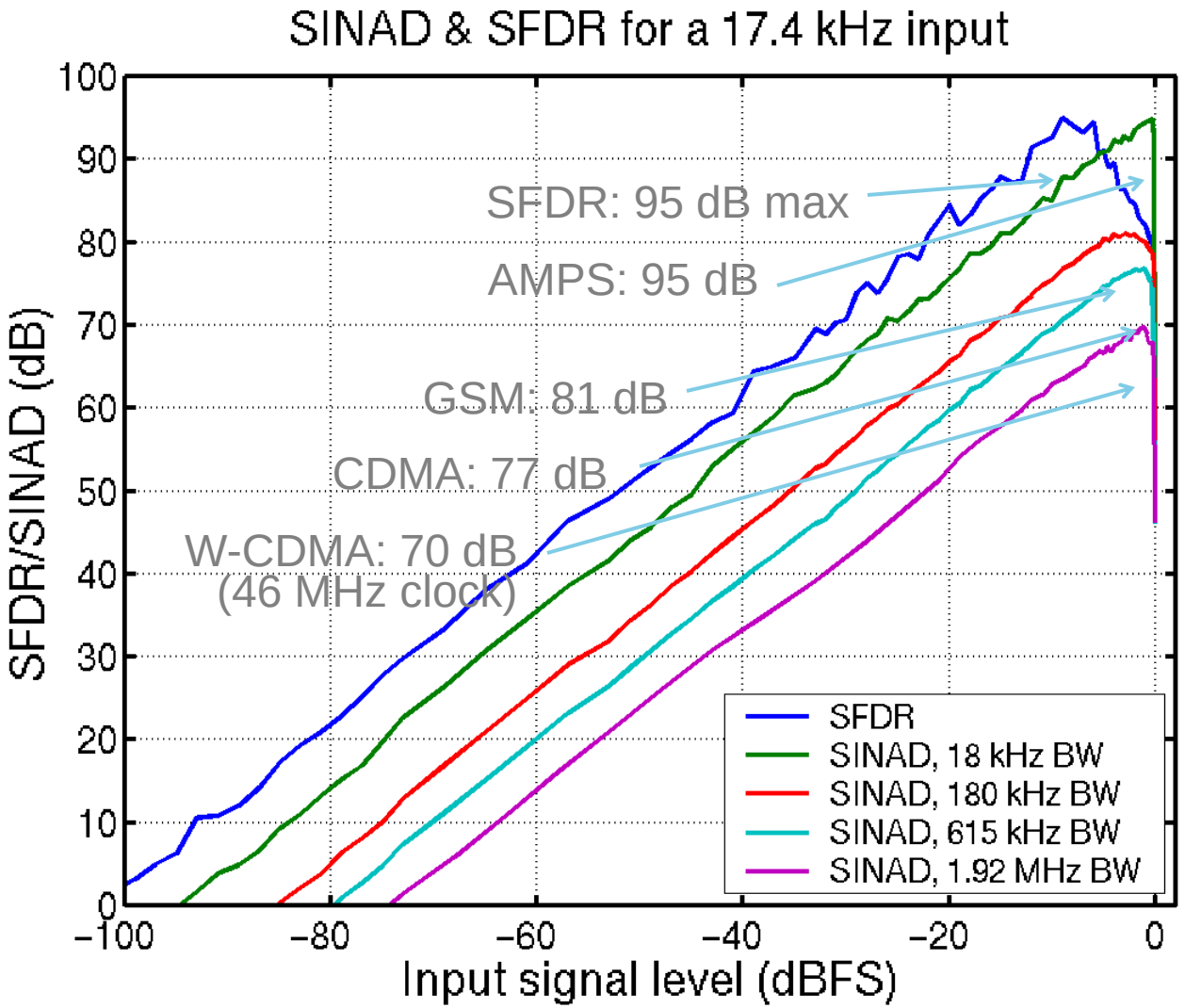

Input shorted – 20 MHz clock
Signal power (dB)
−50
−60
−70
−80
−90
−100
−110
−120
−130
−140
−150
10^1
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)



Small degradation from 1/f noise.


46 MHz clock; FS−3dB, 2.1MHz signal
Signal power (dB)
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
−110
−120
−130
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)


23 MHz clock; FS−3dB, 17.4kHz signal
Signal power (dB)
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
−110
−120
−130
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)


SINAD & SFDR for a 17.4 kHz input
SFDR/SINAD (dB)
Input signal level (dBFS)
100
90
80
70
60
50
40
30
20
10
0
−100
−80
−60
−40
−20
0
SFDR: 95 dB max
AMPS: 95 dB
GSM: 81 dB
CDMA: 77 dB
W-CDMA: 70 dB
(46 MHz clock)
SFDR
SINAD, 18 kHz BW
SINAD, 180 kHz BW
SINAD, 615 kHz BW
SINAD, 1.92 MHz BW

Test Results - Summary

Technology	0.18u CMOS, MIM CAP, 35/70 A DGO
Supply Voltage	2.7 V
Active Area	1.4 mm^2
Power Consumption	30 mW (20A/10D) at 23MHz Fsamp
Power Consumption	50 mW (30A/20D) at 46MHz Fsamp

Bandwidth →	W-CDMA	CDMA	GSM	AMPS
SINAD	70 dB	77dB	81 dB	92 dB
ENOB	11.3	12.5	13.2	15
SFDR	95 dB MAX			

Alternate Approaches:

T. Stockstad, D. Garrity, US patent #6,087,969

FIG. 1

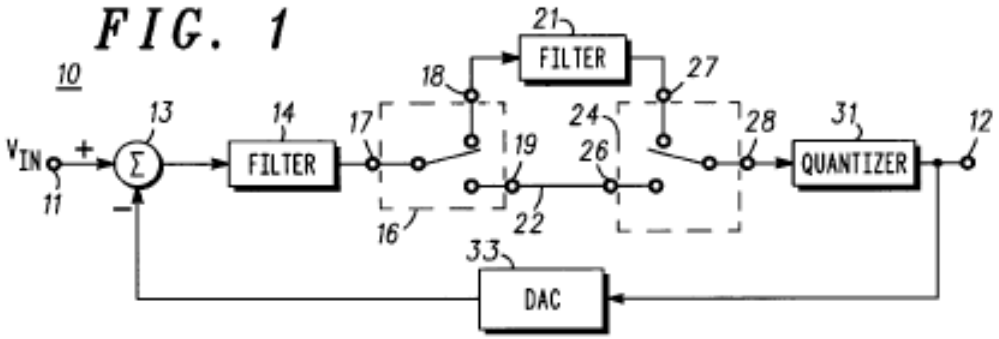
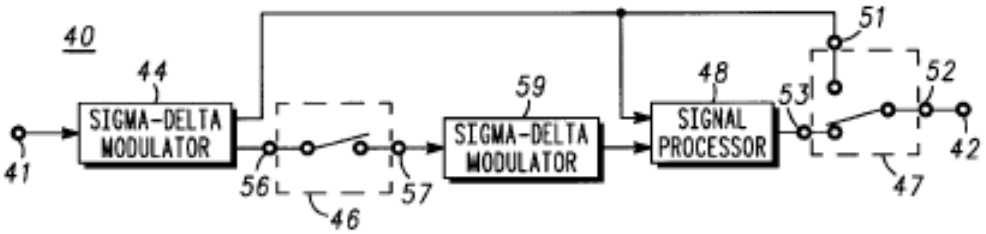


FIG. 2



If sufficient dynamic range cannot be achieved by adjusting the oversampling ratio alone, additional filtering can be added either within or after the first ΣΔ modulator.

Continuous-Time Sigma Delta ADCs:

R. H. M. van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator With Switched-Capacitor Feedback DAC for a GSM/EDGE/CDMA2000/UMTS Receiver," IEEE JSSC, Dec. 2003, pp. 2069-2076.

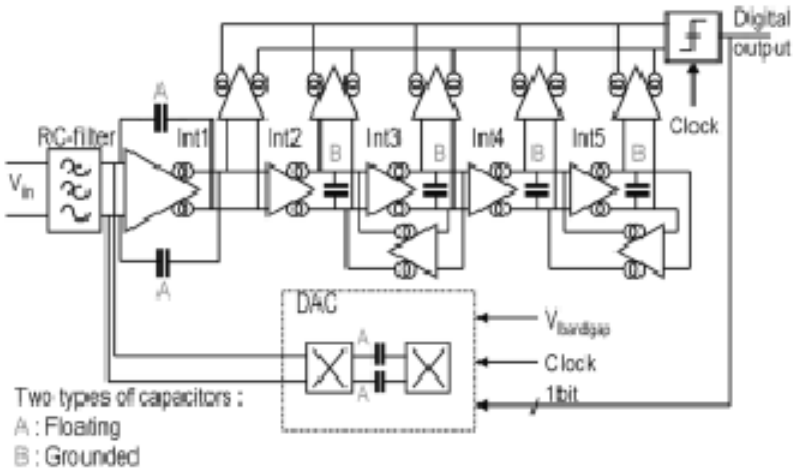
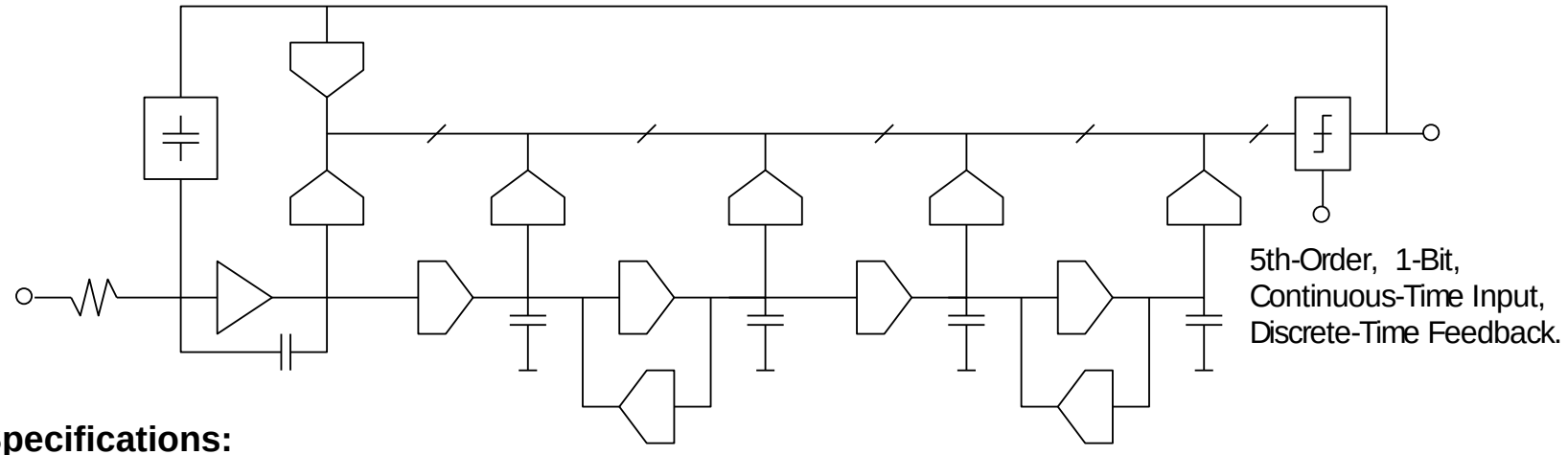


Fig. 7. Block diagram of the 1-bit fifth-order feedforward modulator.

- **discrete-time feedback DAC reduces clock jitter sensitivity**
- **a great deal of research both in academia and industry is currently focused in this area**

74dB/83dB/92dB in a 3.84MHz/1.228MHz/200kHz bandwidth with power dissipation of 4.5mW/4.1mW and 3.8mW respectively!!!

Continuous-Time ΣΔ RxADC



Specifications:

- **Input Clip Point:**
  1.8 Vpeak,differential.
- **SNDR:**
  65 dB over 4 MHz for DVB,
  80 dB over 2 MHz for WCDMA,
  90 dB over 200 kHz for GSM-EDGE.
- **Clock:**
  360 MHz for DVB,
  312 MHz for WCDMA,
  52 MHz for GSM-EDGE.

Continuous-Time Input:

- **Low Power: 10mW (4 mA) (dominated by WCDMA).**
- **Inherent Anti-Aliasing: 5th-Order.**

Clock Jitter Sensitivity:

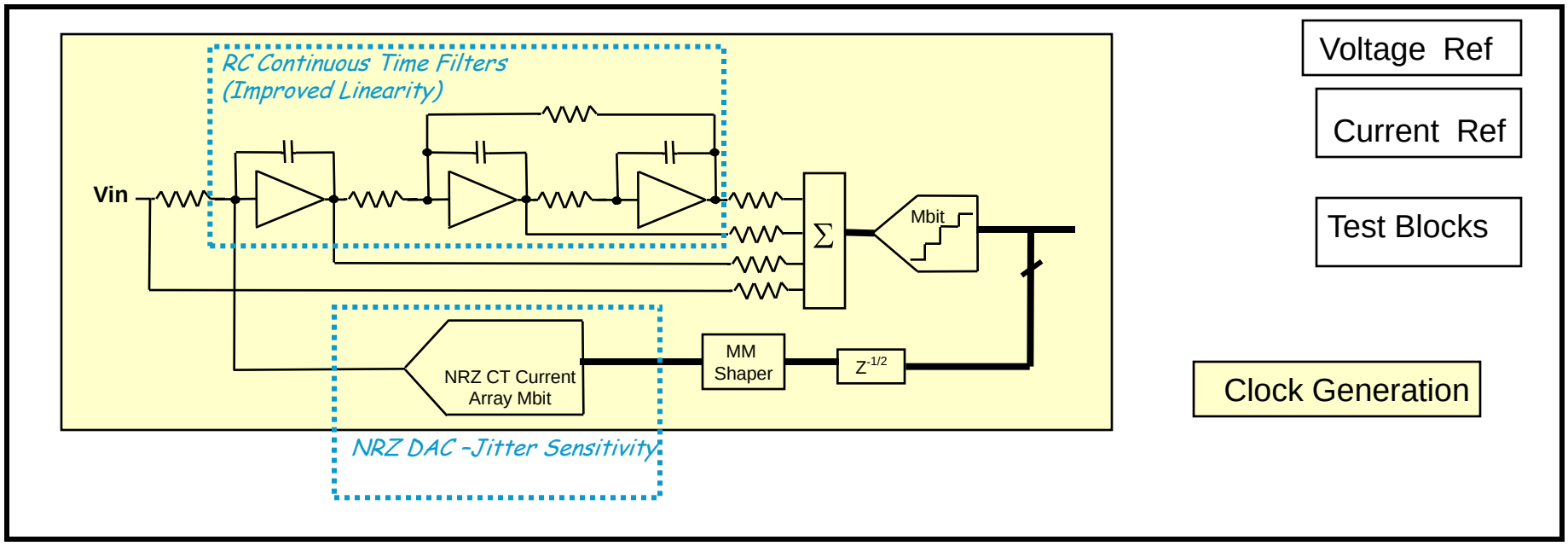
- **Reduced by discrete-time feedback.**
- **Reduced by OSR.**

Continuous-Time SD RxADC

Specs: BW = 10MHz

fs = 184Mhz

SNR = 70dB



Case Study #2:

Pipelined RSD (1.5 bit-per-stage) ADC

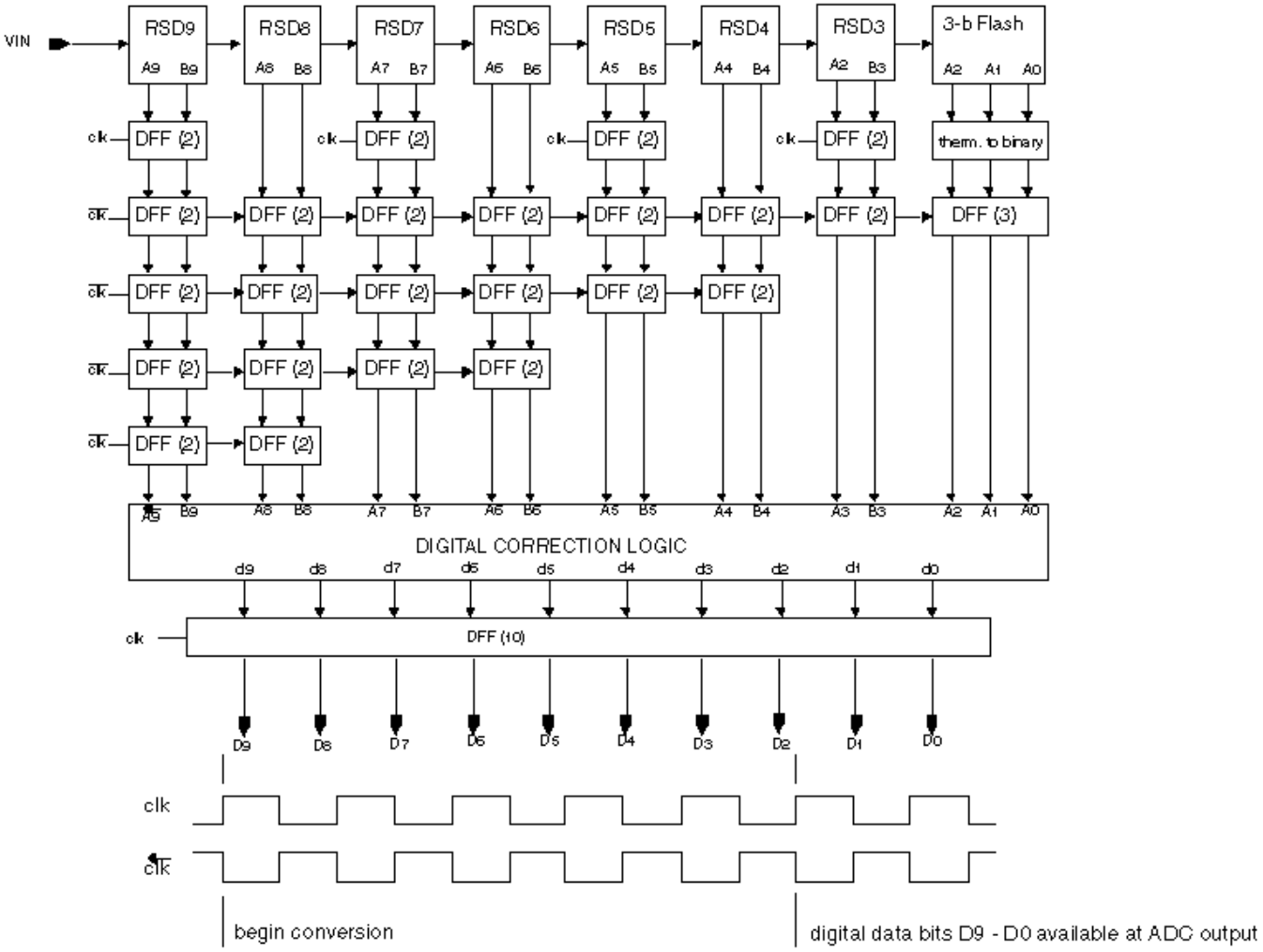
- Application
- System design
- Circuit design
- Test results

ADC for Wireless LAN radio receiver (and other broadband radio receivers):

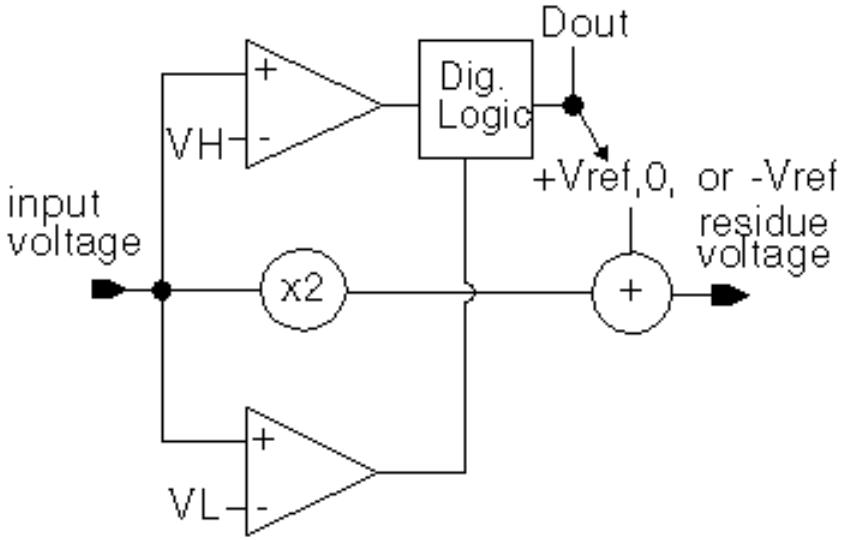
- ✓ two ADCs required (I and Q)
- ✓ low power dissipation (no separate track and hold)
- ✓ 0.13μm digital CMOS with isolated p-well option (for isolation)
- ✓ high performance with low cost
- ✓ specific requirements:

  no more than 0.6mm^2 per ADC
  sample rate > 20MHz
  10 bit resolution
  SINAD > 56dB
  power < 25mW per ADC
  SFDR > 65dB

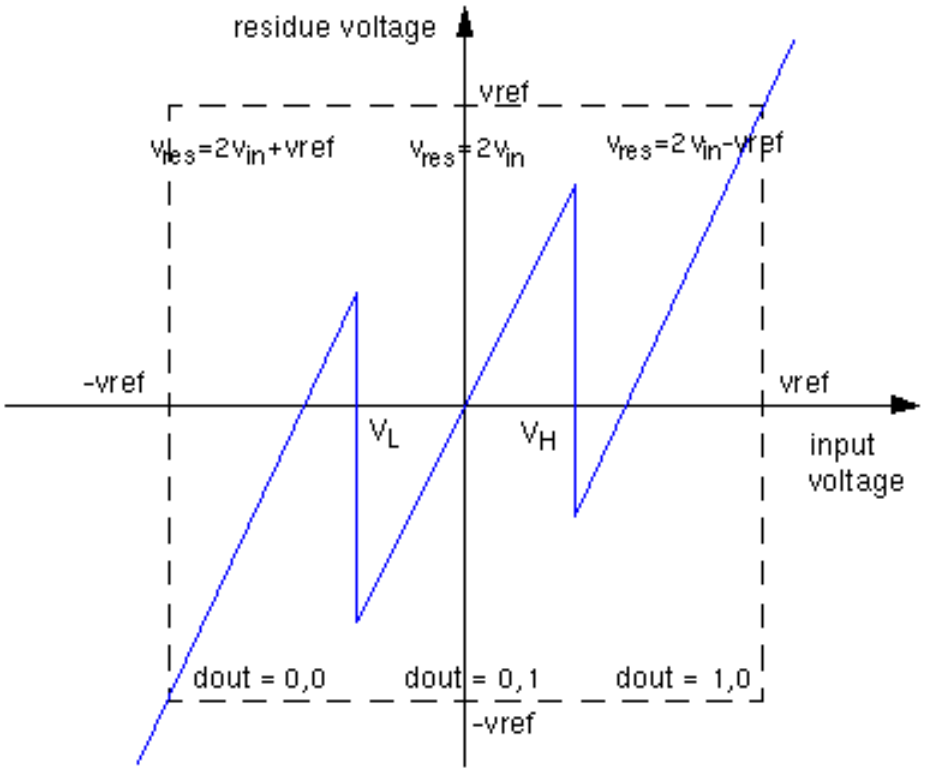
10 bit 20Ms/s Pipelined RSD ADC



RSD Stage Block Diagram and Transfer Function

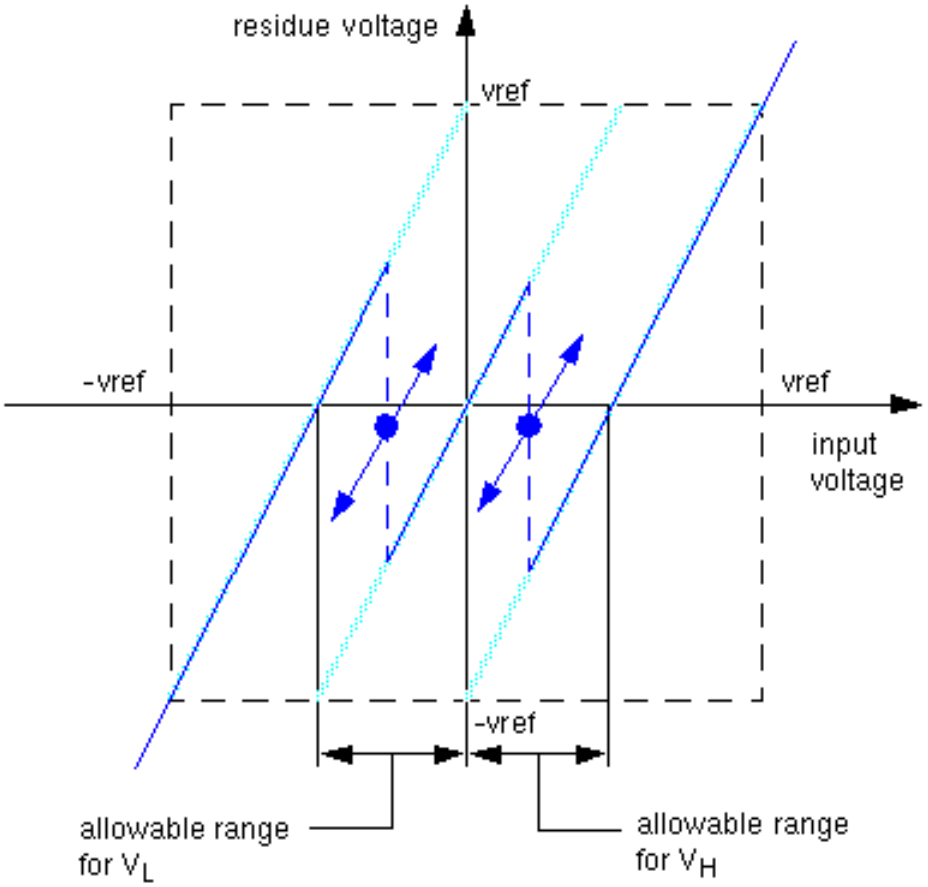


Block Diagram

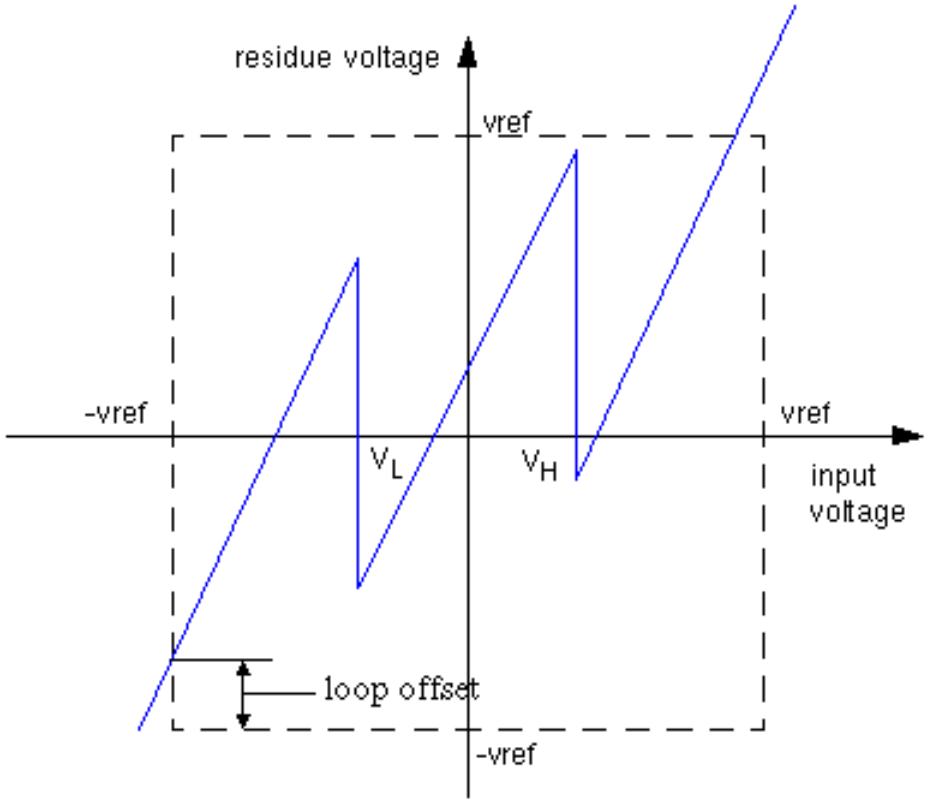


Robertson Diagram

RSD ADC: Offset Effects

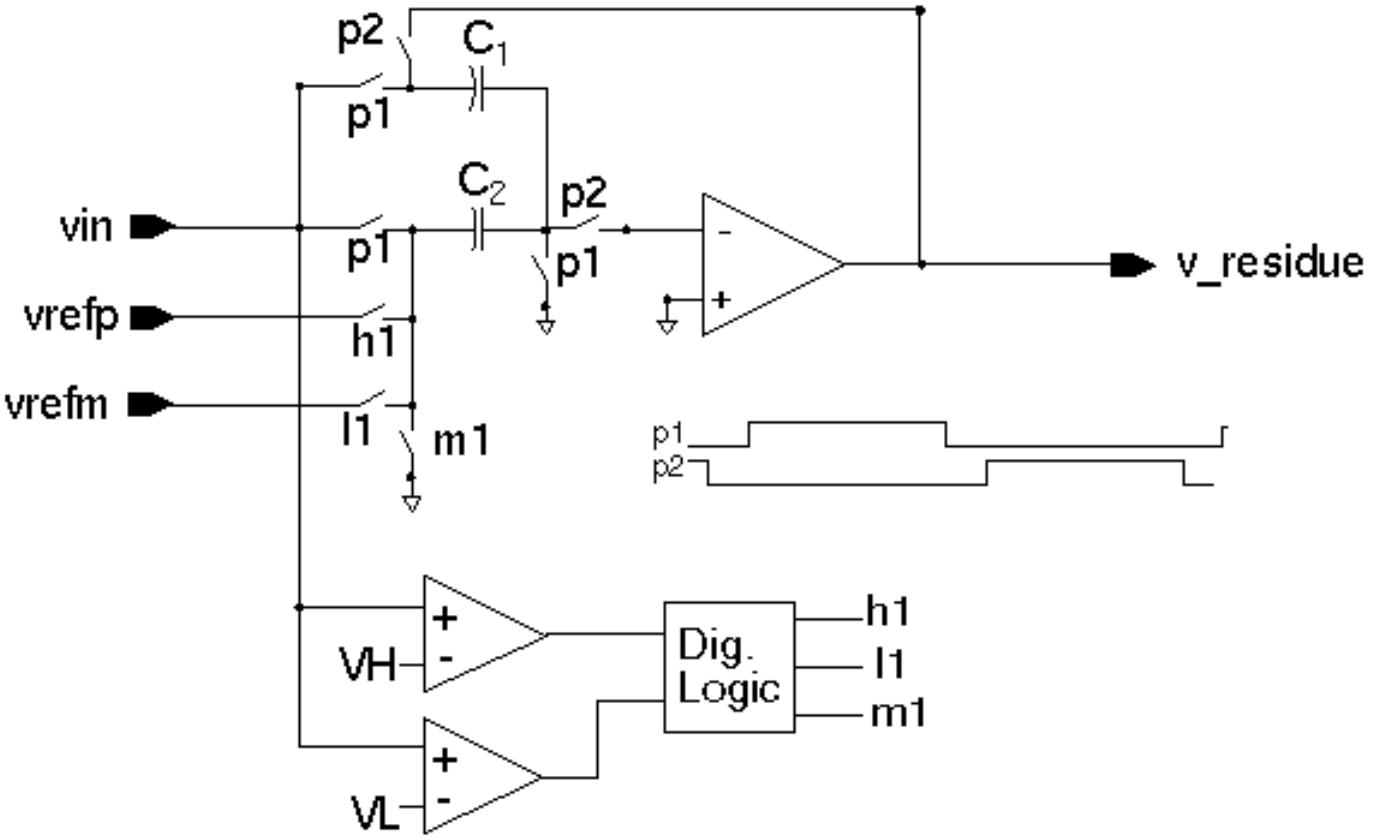


Comparator Offset



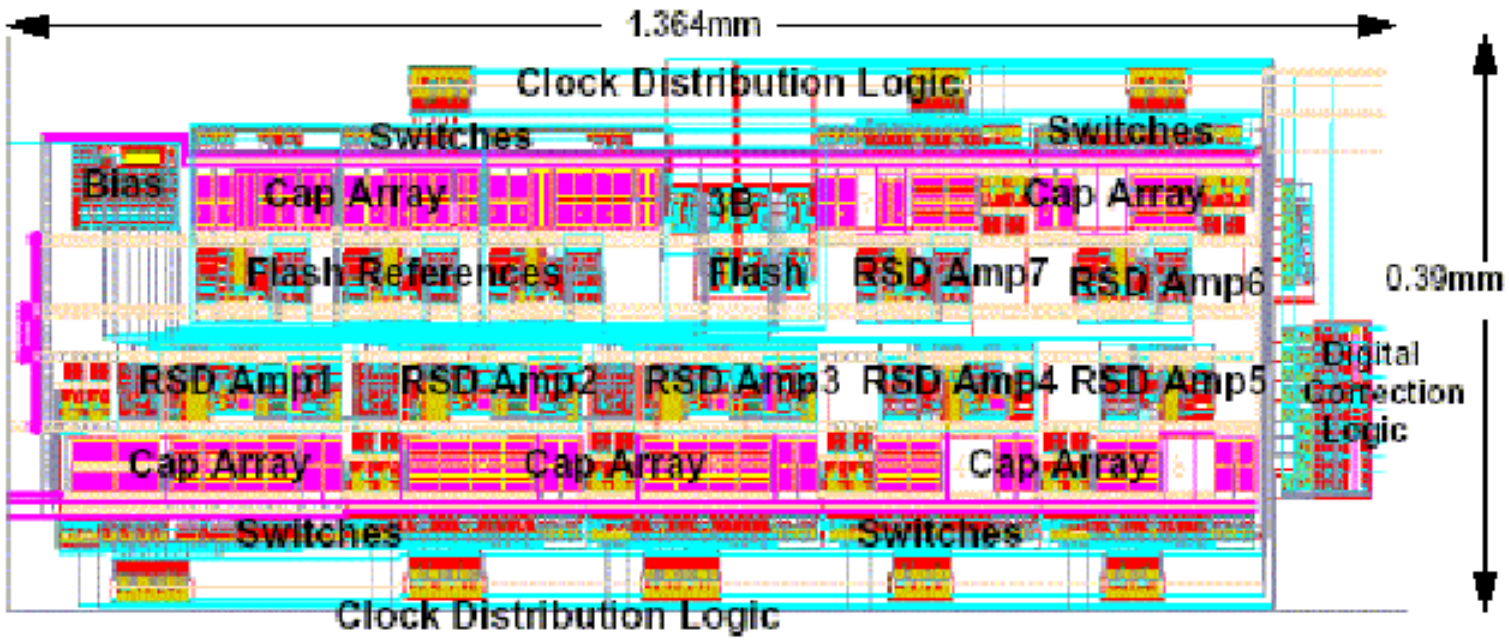
Loop Offset

RSD stage single-ended block Diagram:



Note that since RSD comparator accuracy requirements are significantly reduced, a separate track and hold is usually not required for resolutions up to 10 bits and input signal frequencies up to ~ 50MHz or so

Pipelined RSD ADC layout:

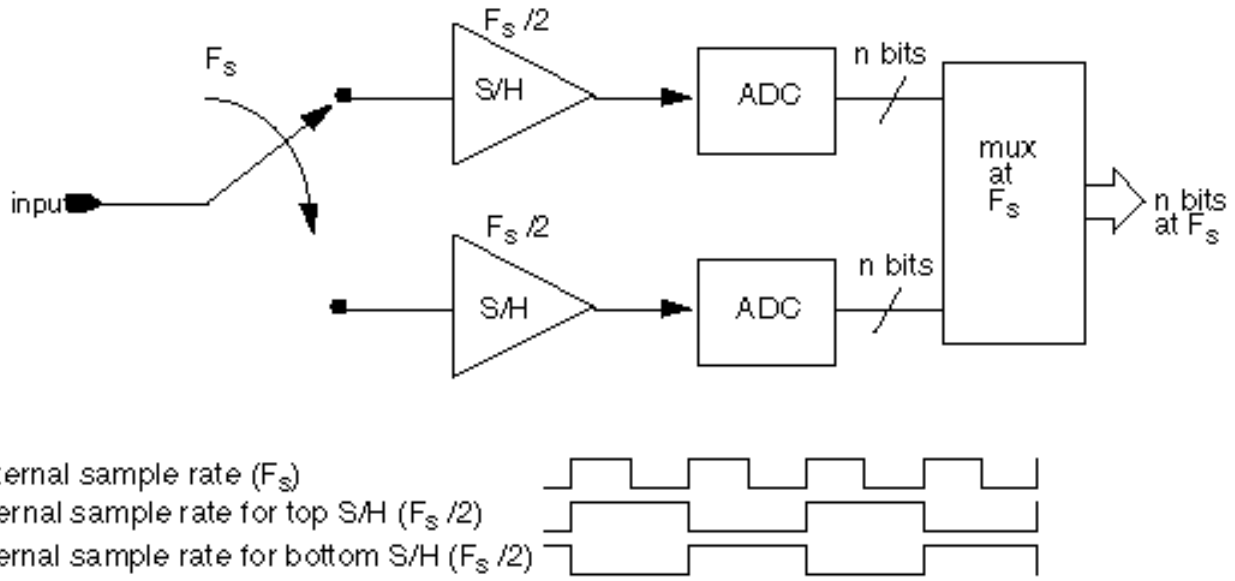


Expected Results (simulated):

Technology	**0.13μm CMOS, Fringe CAP, 70 A DGO**
Supply Voltage	**3.3 V**
Active Area	**0.53 mm^2**
Power Consumption	**24 mW at 20MHz Fsamp**

input bandwidth	**10MHz**
SINAD	**57dB**
ENOB	**9.2**
SFDR	**65 dB**

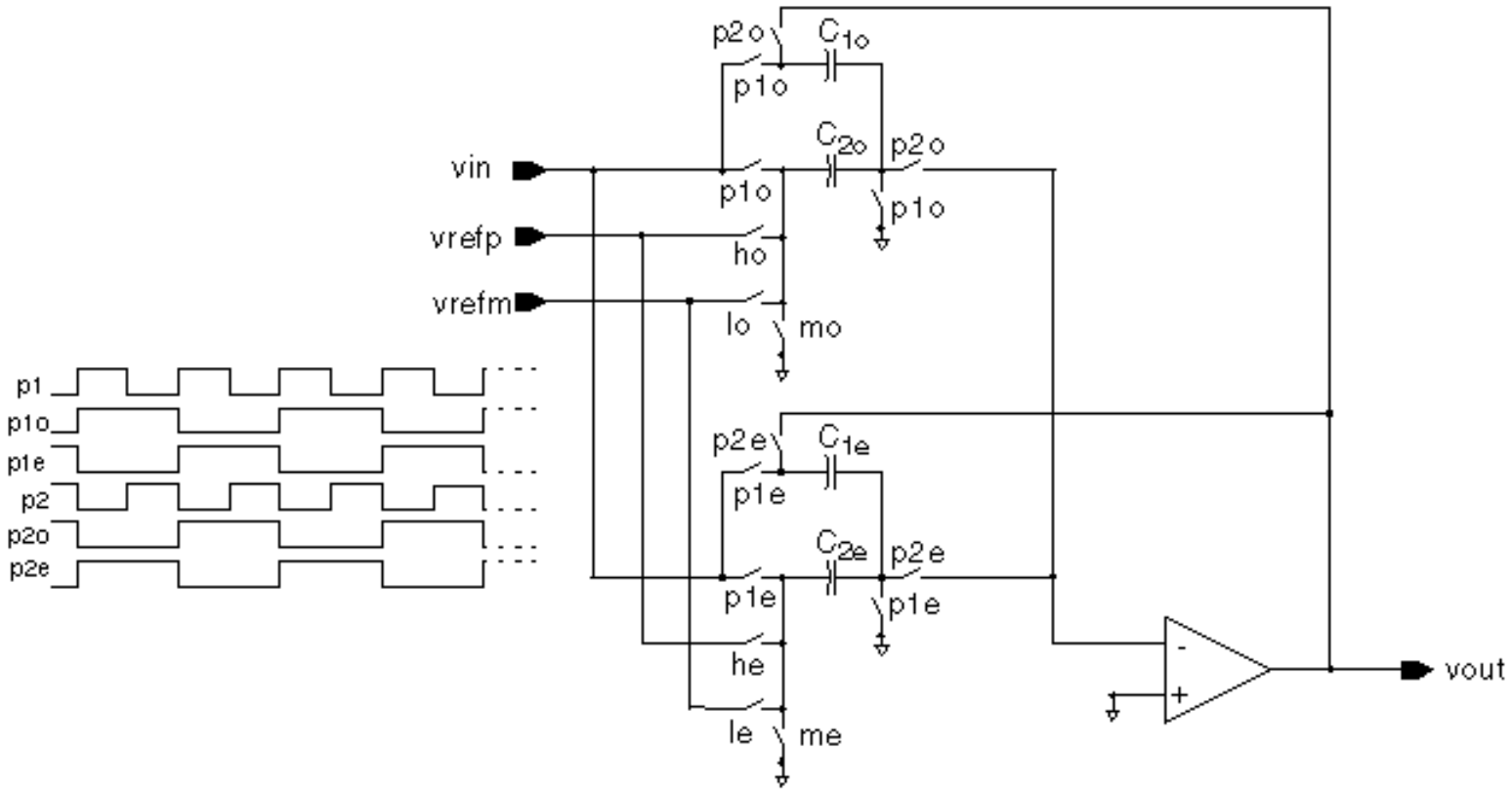
What if you need to go faster but you can't spend anymore power or area:



double-sampled pipeline ADC - theory of operation

D. Garrity and S. Aftab, "A 10 bit, 40Ms/s Pipelined A/D Converter," proceedings ASICON 1998, pp. 71-74

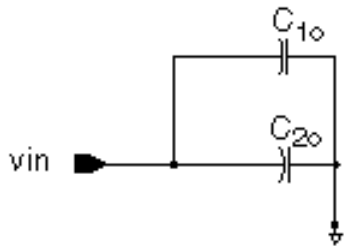
Simplified single-ended block diagram of a double-sampled RSD gain stage:



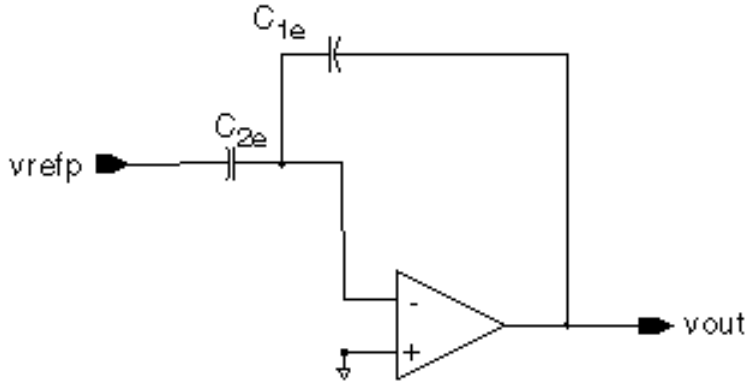
Single ended version of improved gain stage with associated timing diagram.

* Note that the input voltage is still sampled at the original system clock rate, while the internal circuitry is operating only half as fast. This allows a corresponding factor of 2 reduction in the supply current required for the gain stage opamp.

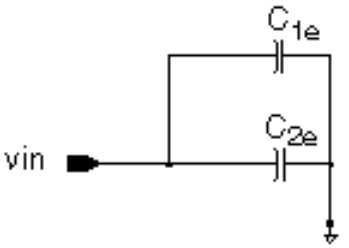
operation of single ended version of improved gain stage:



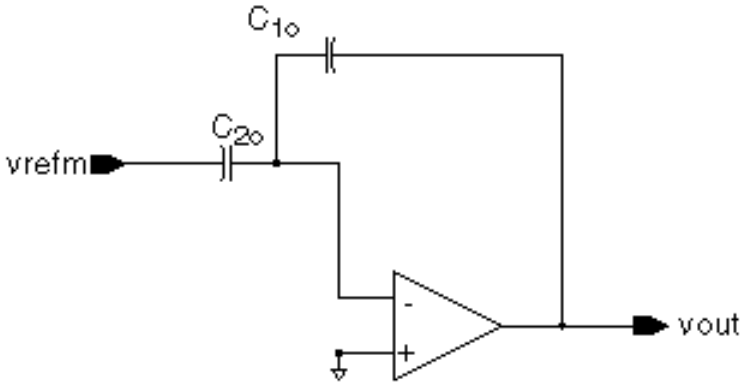
odd input during p1o



gain stage during p2e with signal he high

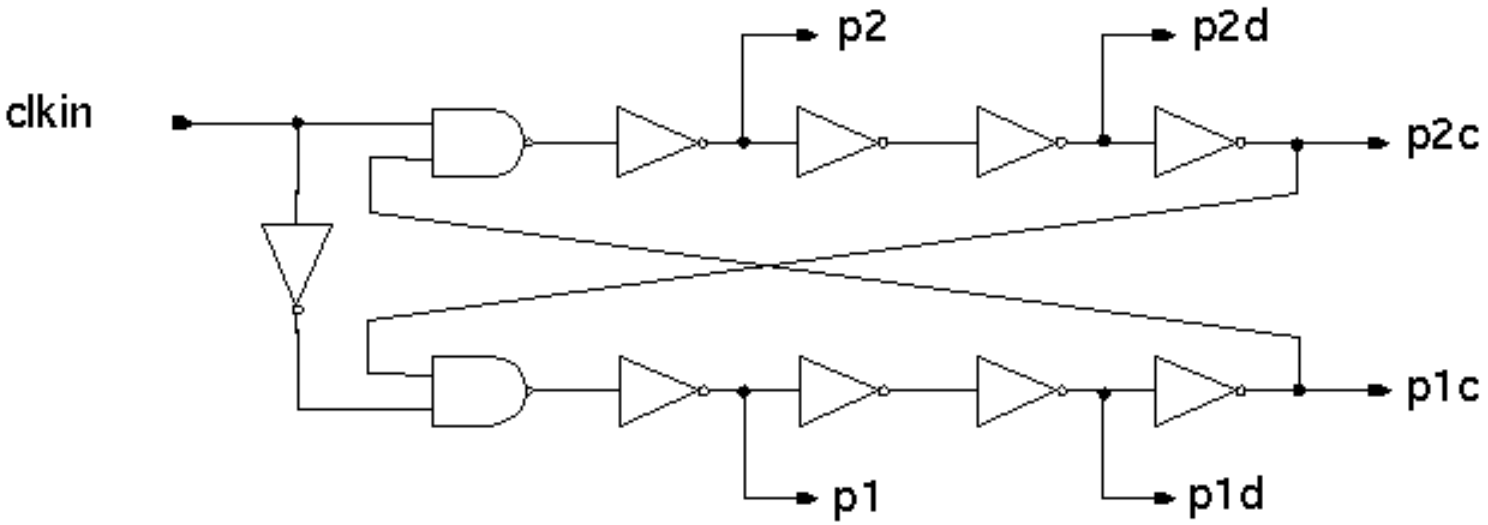


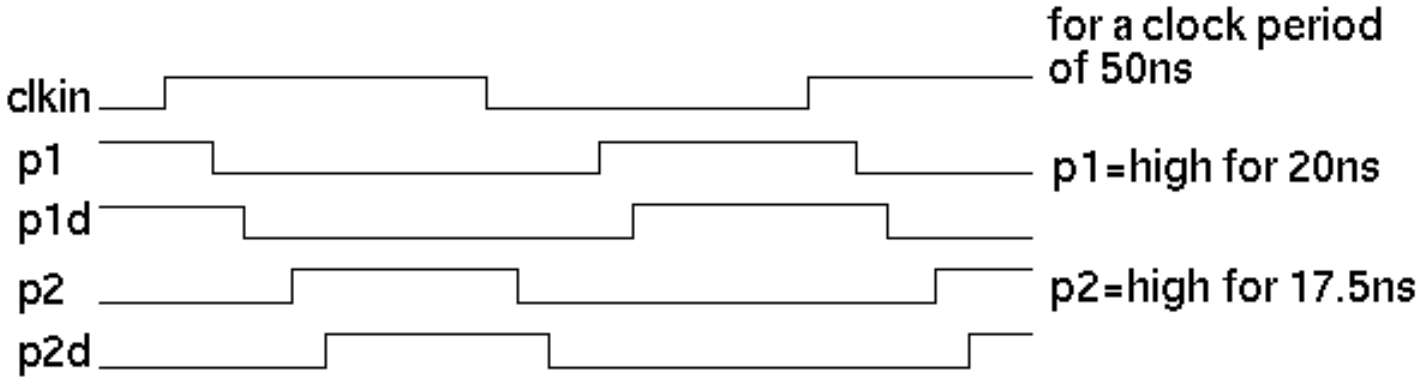
gain stage during p1e

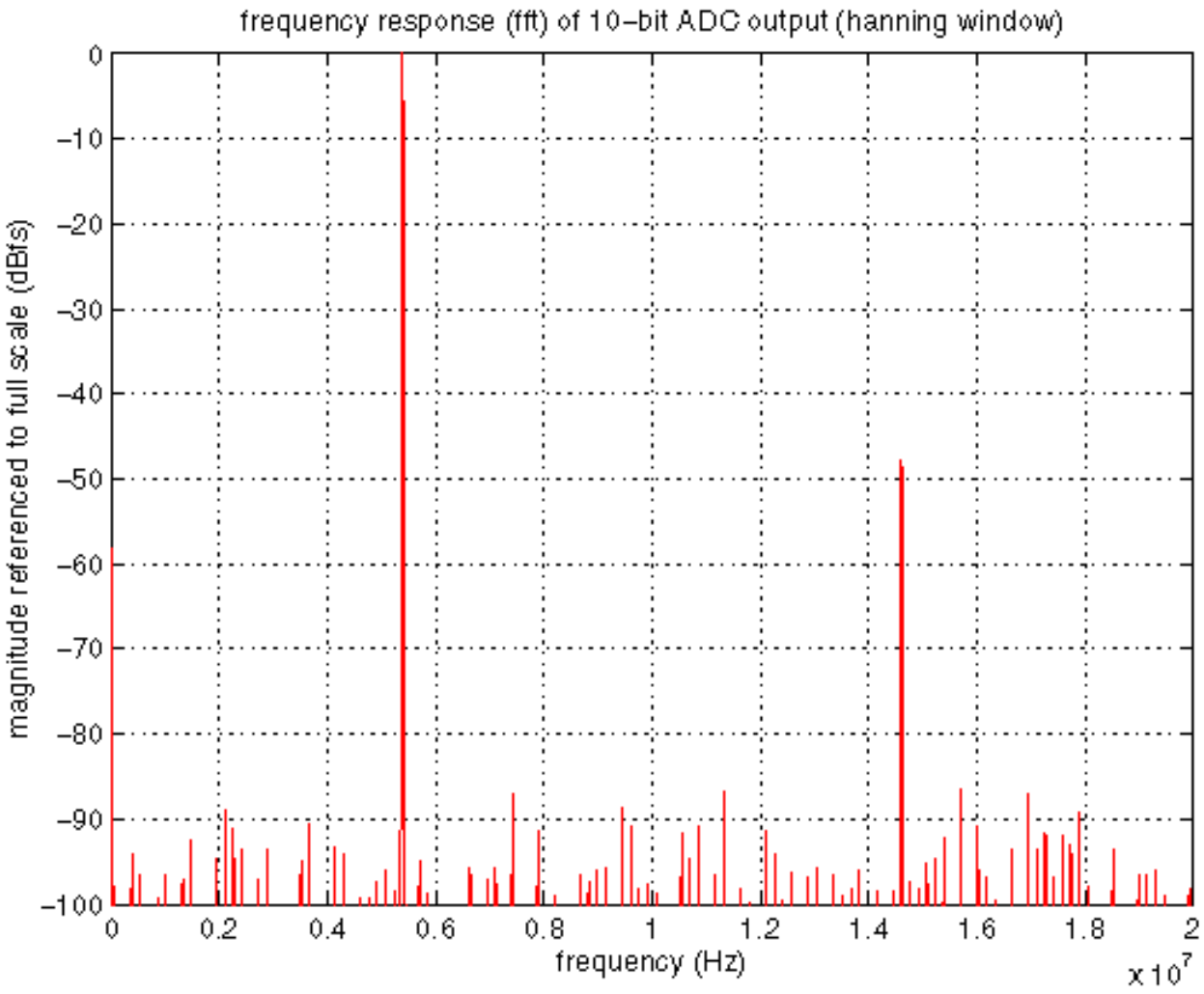


gain stage during p2o with signal lo high

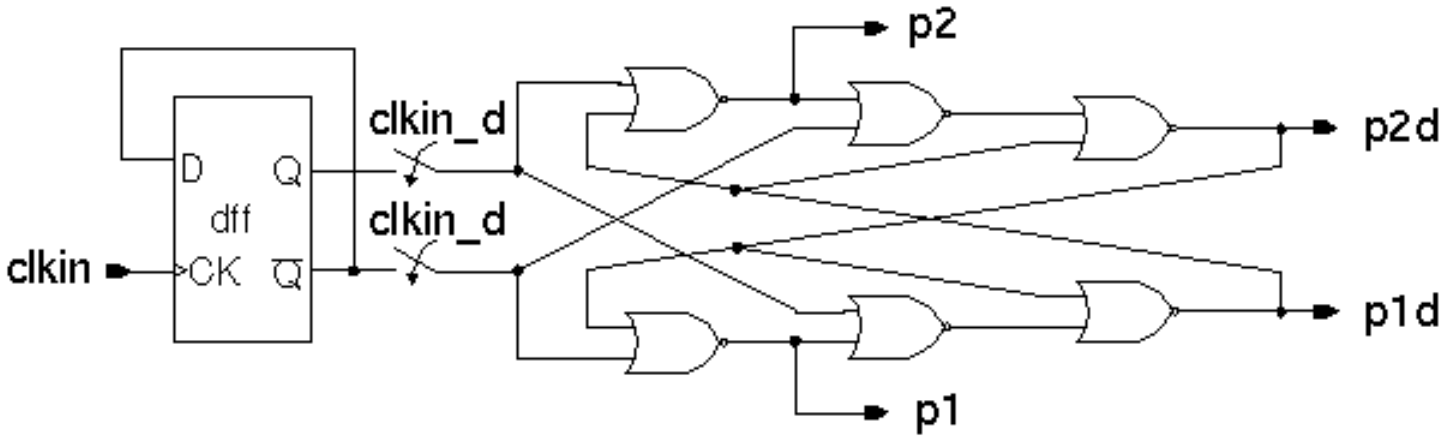
conventional non-overlapping clock generator for SC circuits

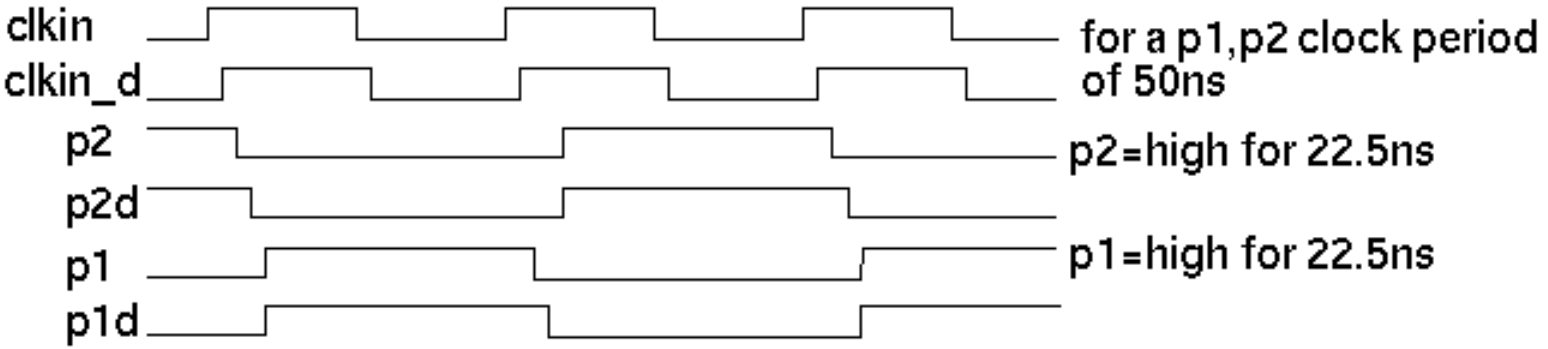




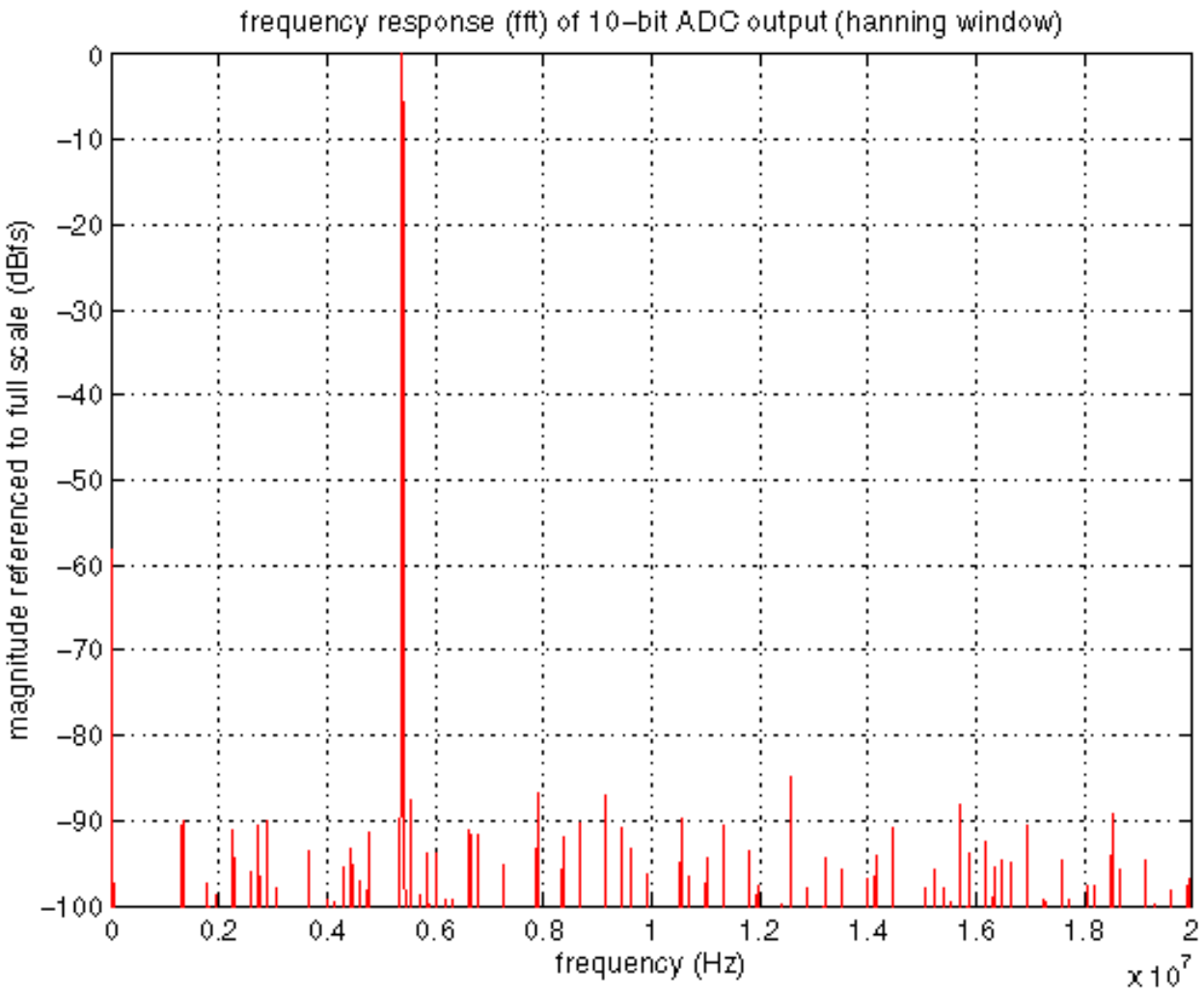

frequency response (fft) of 10−bit ADC output (hanning window)
magnitude referenced to full scale (dBfs)
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
frequency (Hz)
x 10^7

non-overlapping clock generator for time-interleaved SC circuits



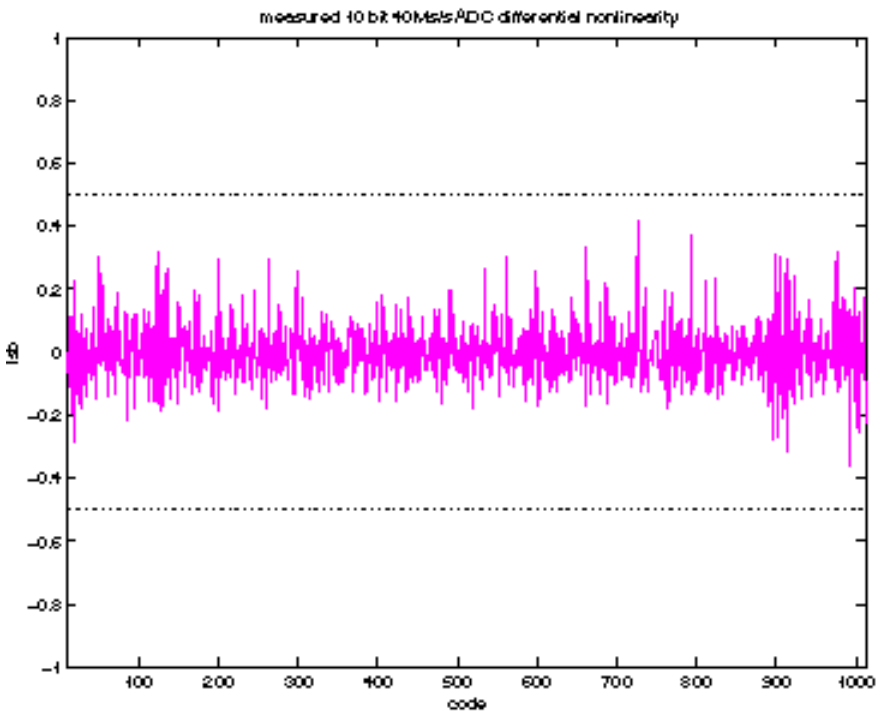


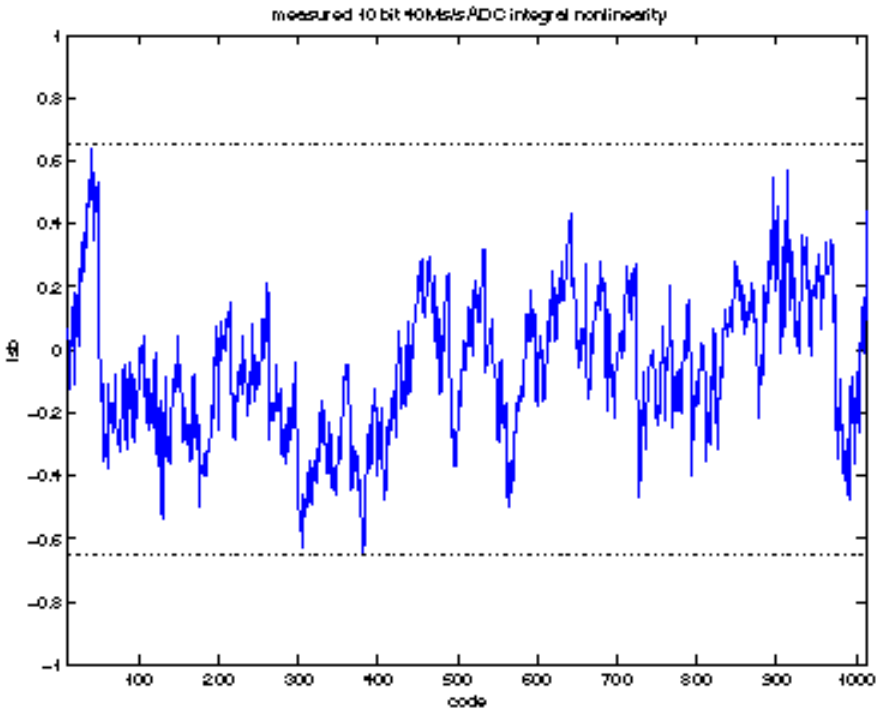
D. Garrity, D. Bersch, US patent 5,886,562

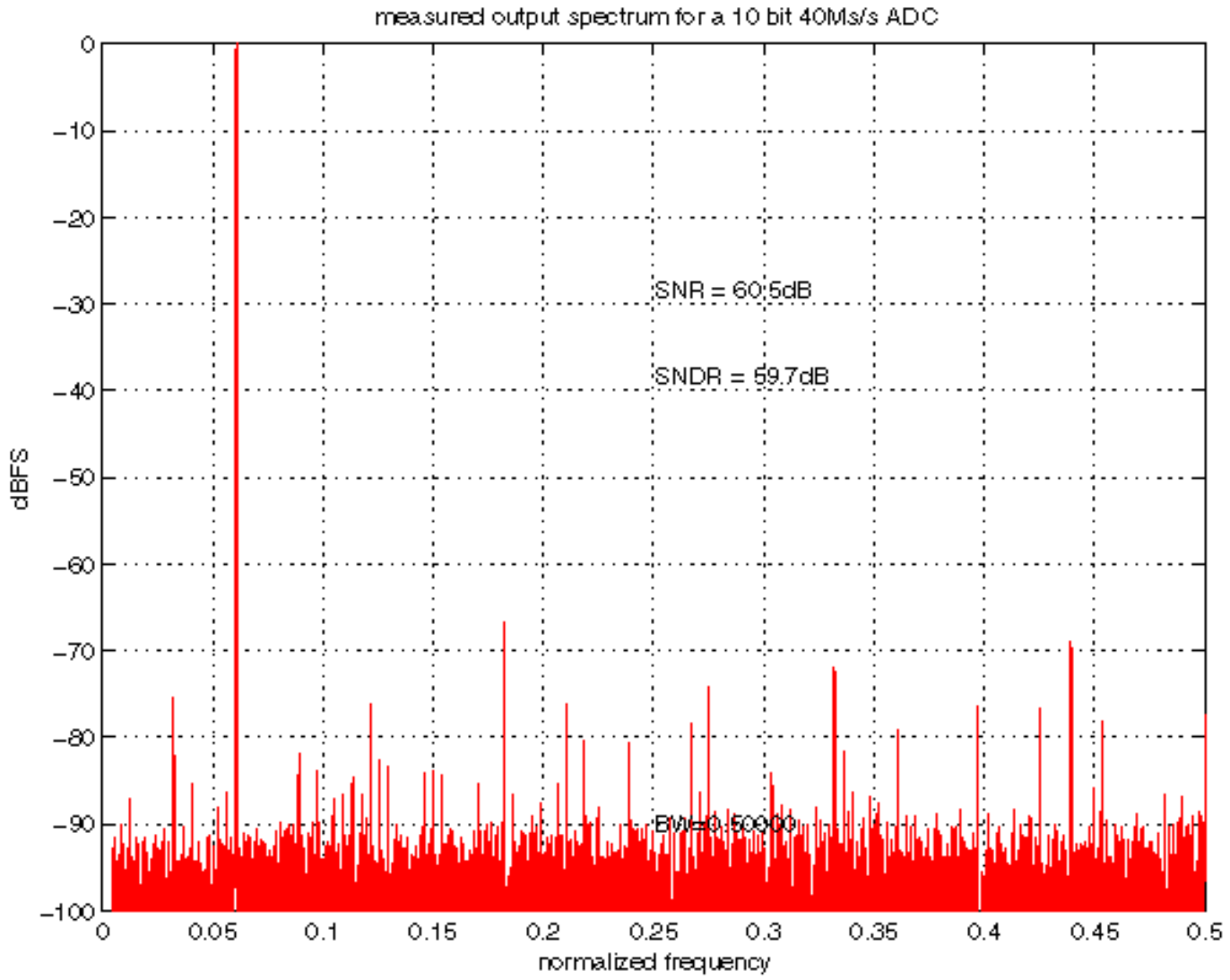

frequency response (fft) of 10−bit ADC output (hanning window)
magnitude referenced to full scale (dBfs)
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
frequency (Hz)
x 10^7

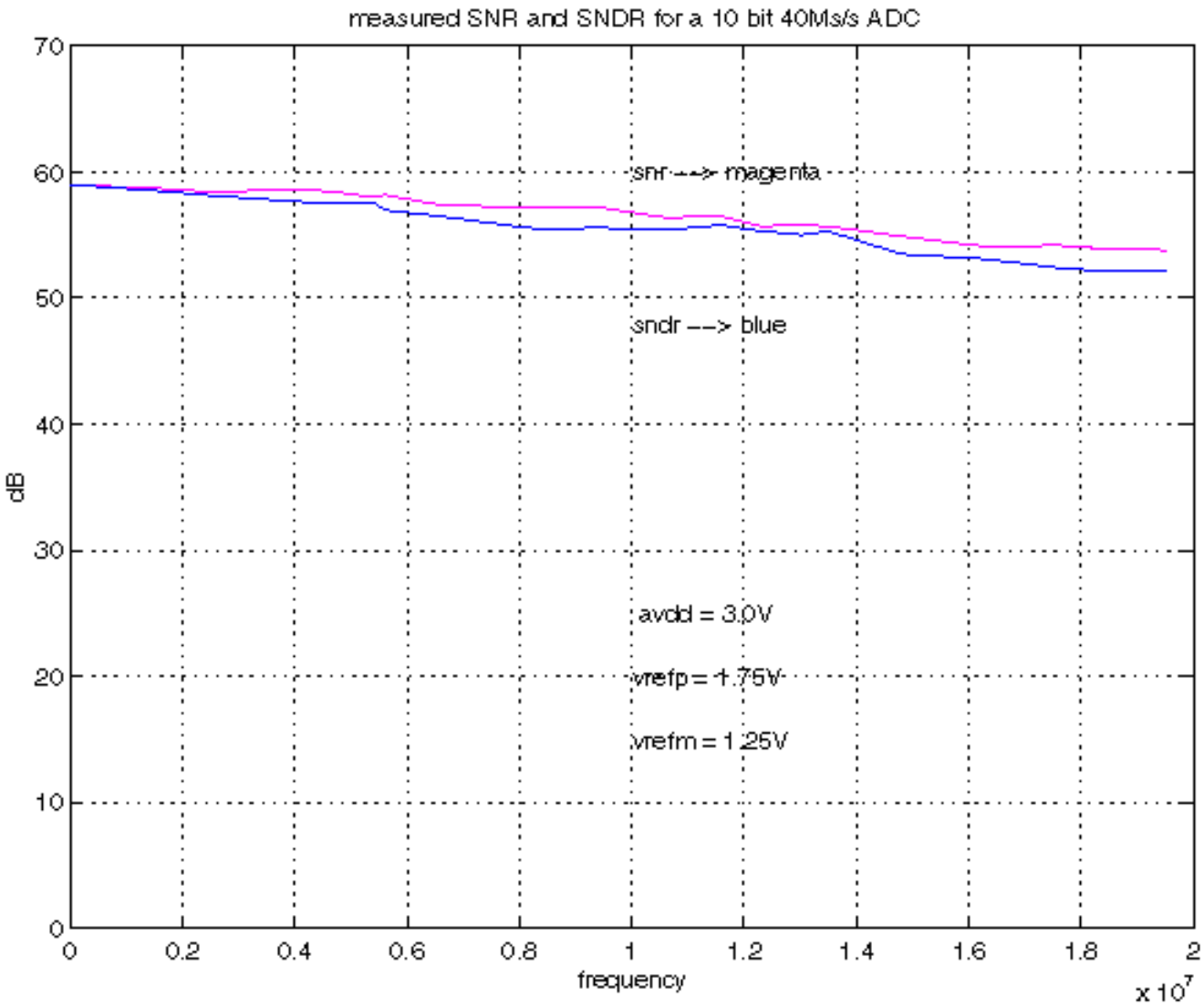
Experimental Results:

10 bit, 40Ms/s double-sampled pipelined ADC






measured output spectrum for a 10 bit 40Ms/s ADC
SNR = 60.5dB
SNDR = 59.7dB
BW=0.50000
dBFS
normalized frequency
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5

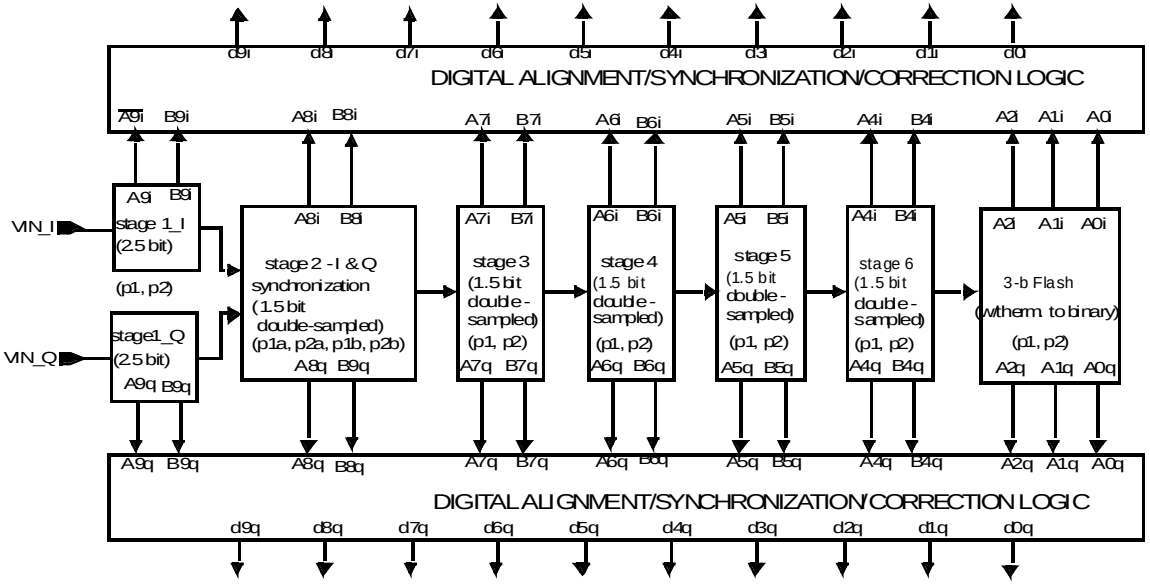

measured SNR and SNDR for a 10 bit 40Ms/s ADC
snr --> magenta
sndr --> blue
avdd = 3.0V
vrefp = 1.75V
vrefm = 1.25V
dB
frequency
x 10^7
0
10
20
30
40
50
60
70
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

Measured Results:

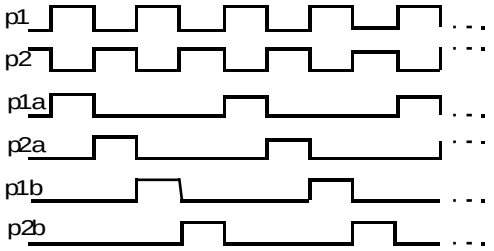
Technology	**0.5μm BiCMOS, Double-Poly Capacitor**
Supply Voltage	**3.0 V**
Active Area	**2.5 mm^2 (20% more than original ADC)**
Power Consumption	**100mW at 40MHz Fsamp (20% more)**

input bandwidth	**20MHz**
SINAD	**57dB**
ENOB	**9.34(at 2MHz), 8.5 (at 20MHz)**
SFDR	**60 dB**

Alternate approach: Single ADC that processes I and Q Channels (garrity et al. US patent #7,064,700)



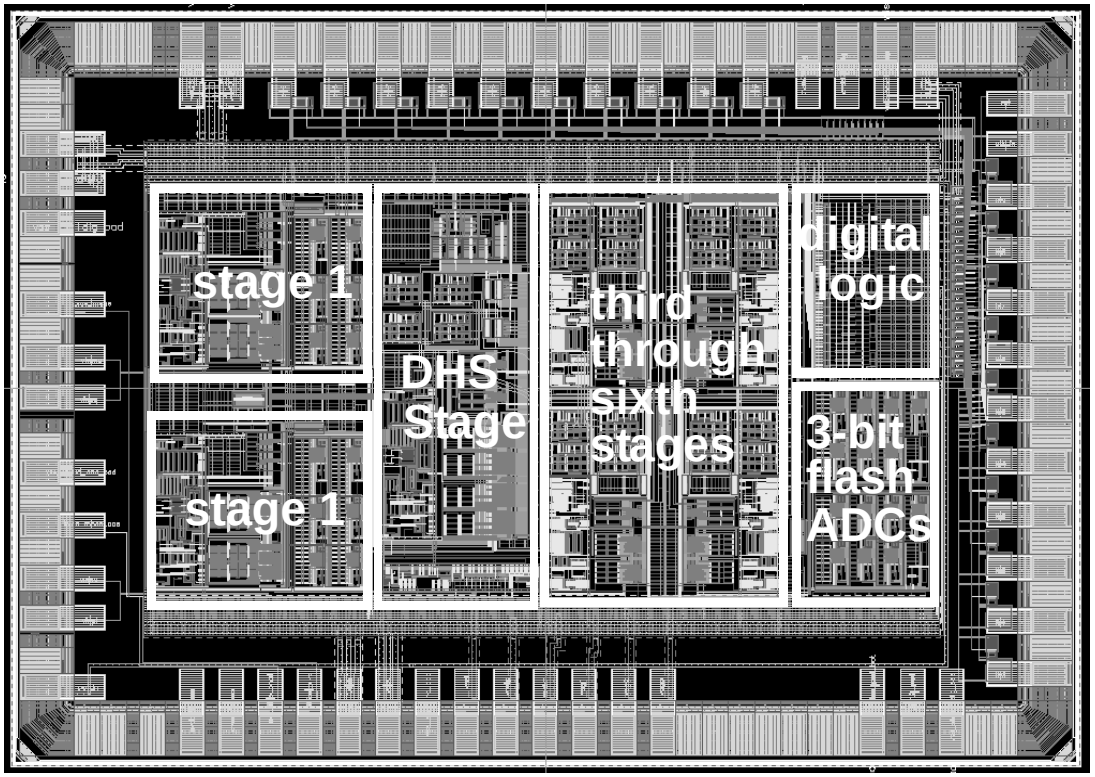
Simplified block diagram of prototype I/Q sampling ADC. The resolution and required clock phases for each stage are listed in parentheses.



Simplified timing diagram for I/Q sampling ADC

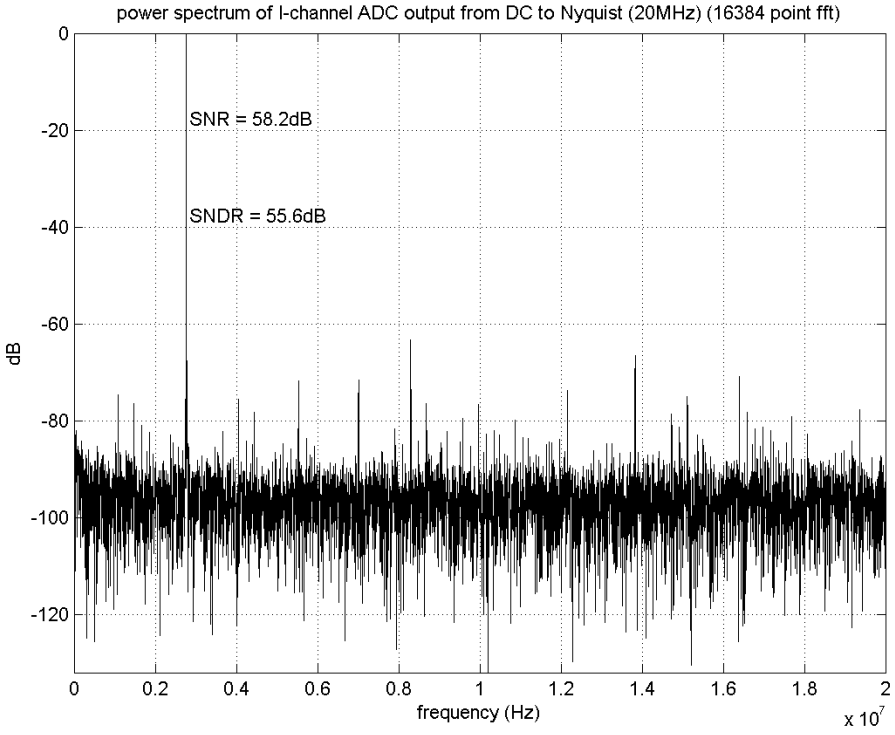
Measured Results:

plot of ADC layout (1.727mm^2 total area and per-ADC area of 0.864mm^2):



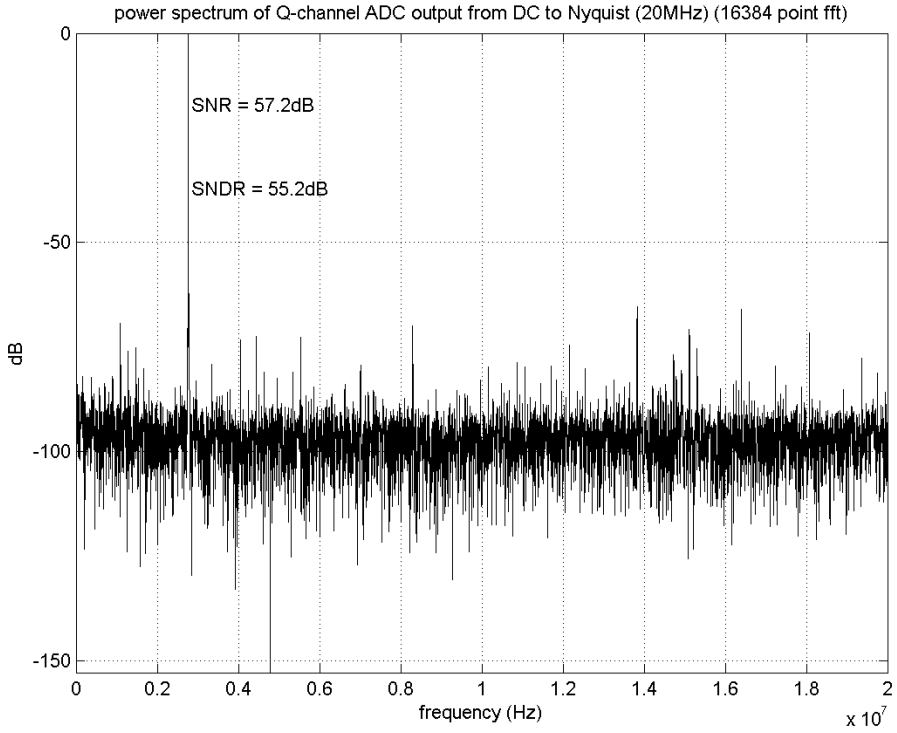
Measured Results:

I-Channel ADC Response to a 2.4MHz sine wave:



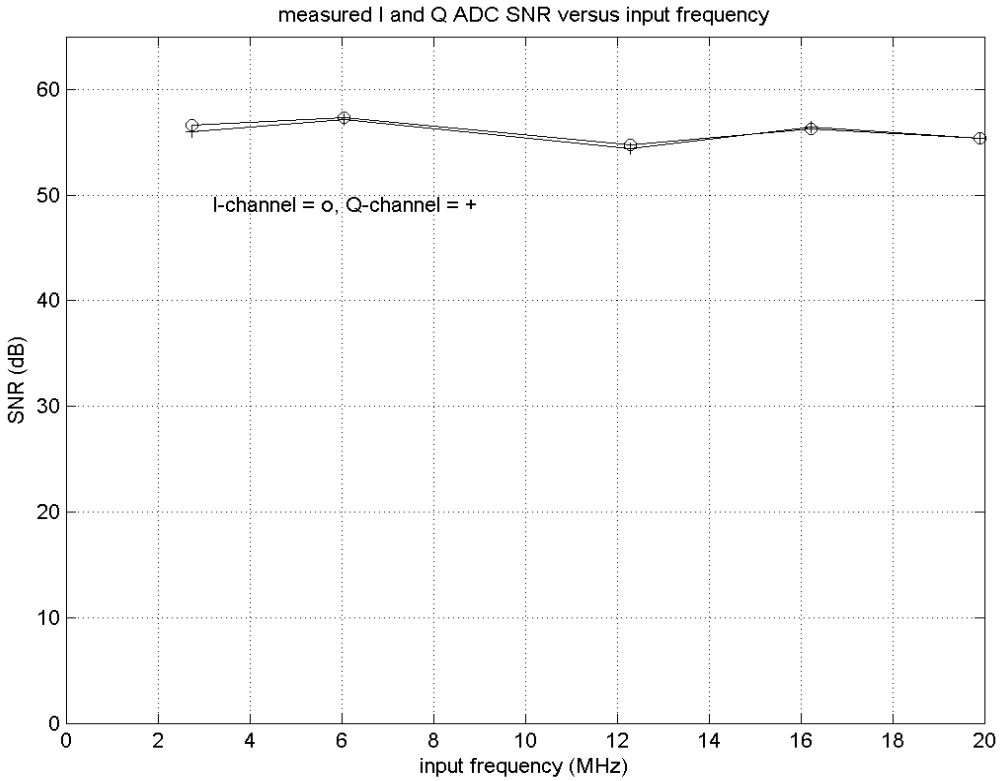
Measured Results:

Q-Channel ADC Response to a 2.4MHz sine wave:



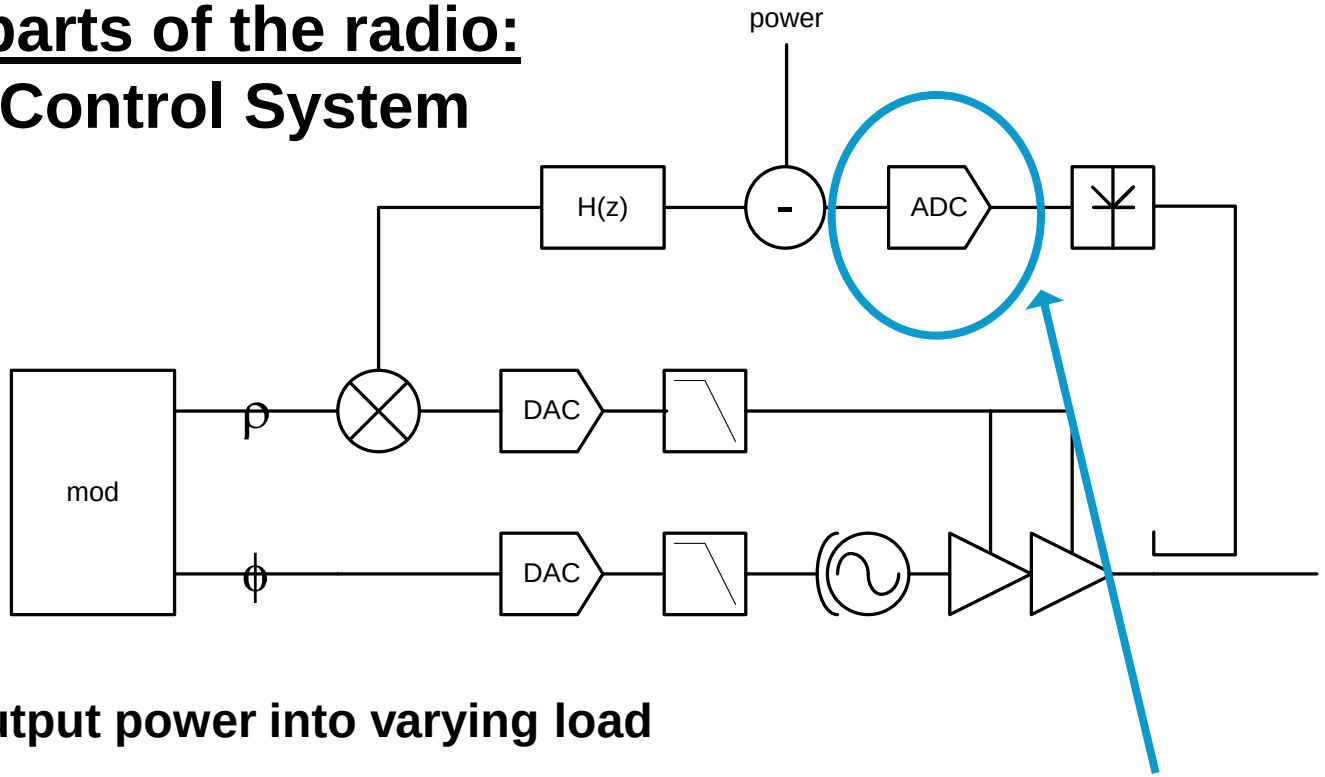
Measured Results:

I and Q channel ADC SNR Response vs Input Frequency:



	I-channel ADC	Q-channel ADC
resolution	10 bits	10 bits
sample rate	40MHz	40MHz
Input voltage range	1 Vpp differential	1 Vpp differential
peak SNR/SNDR	58.5/56.5 dB	58.5/56.5dB
DNL	-0.48/0.58 lsb	+/- 0.5 lsb
INL	+/- 1 lsb	+/- 1 lsb
power consumption	25mW	25mW
technology	90nm CMOS	90nm CMOS
area	0.864mm^2	0.864mm^2

Other parts of the radio:
Power Control System



Levels output power into varying load

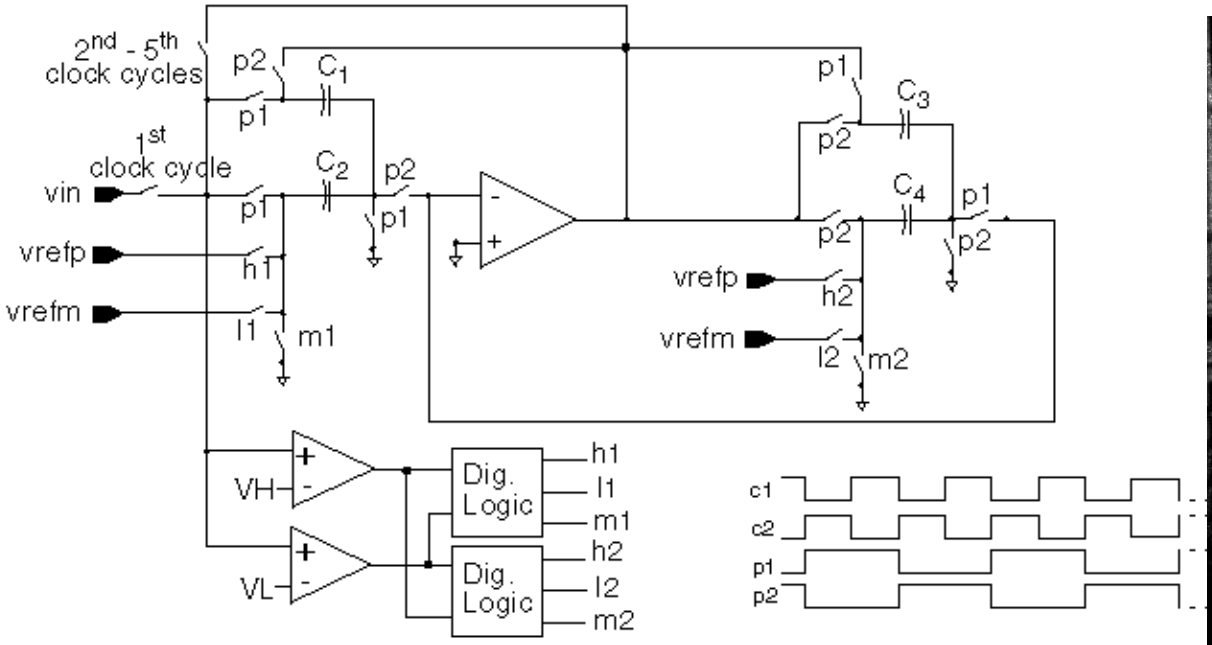
Polar architecture shown for reference

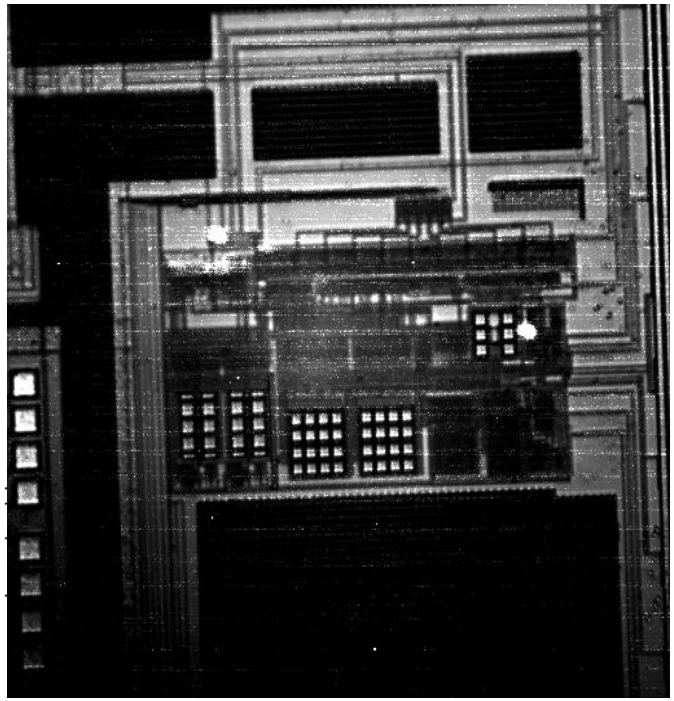
Digital implementation

- **Minimizes analog area**
- **Simplifies multi-mode support**
  - **Example**
    - **GSM + EDGE + WCDMA**

>10 bits resolution
> 1Ms/s
~ 1mW power
< 0.1mm² in 0.18μm CMOS

single-stage cyclic ADC architecture

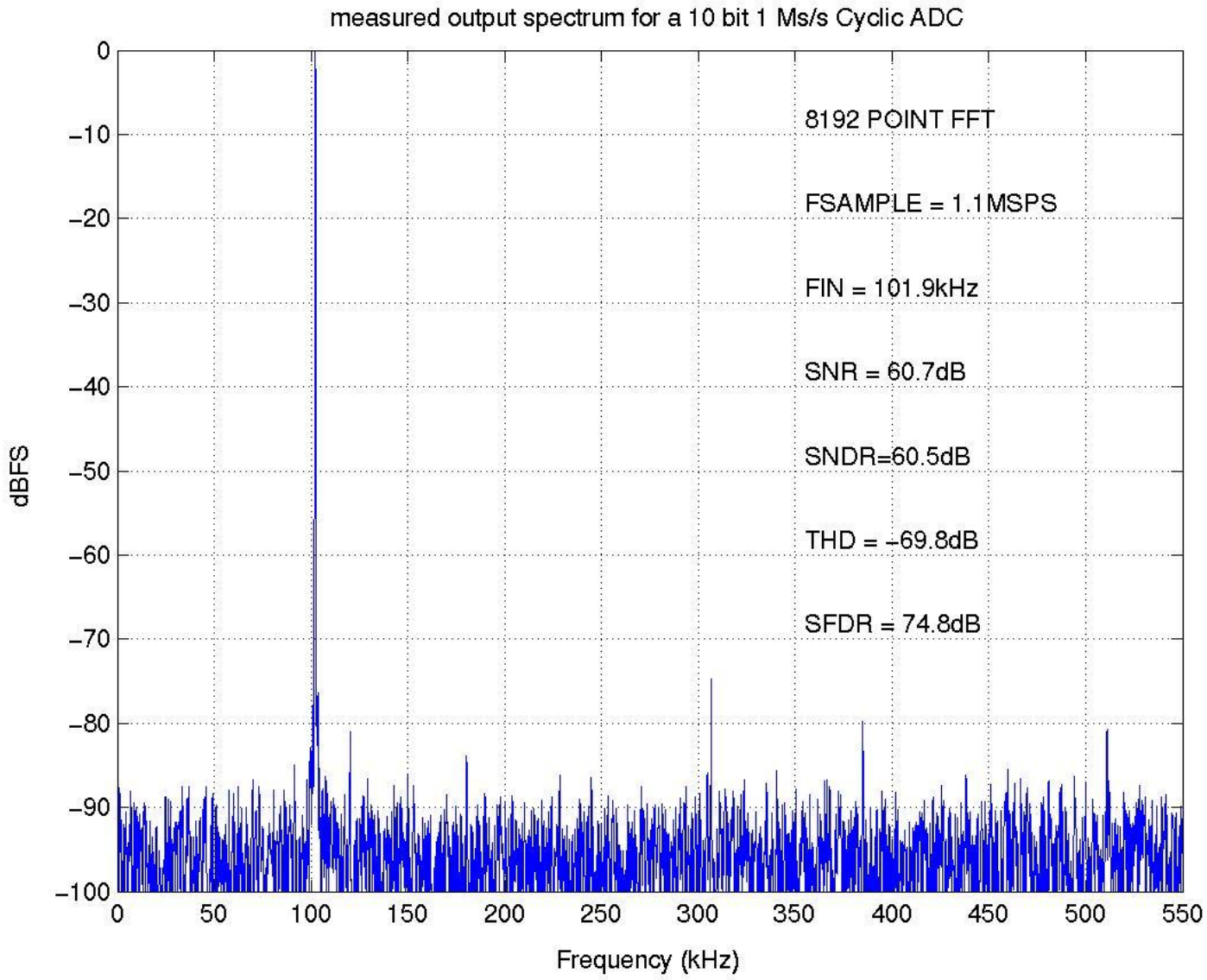


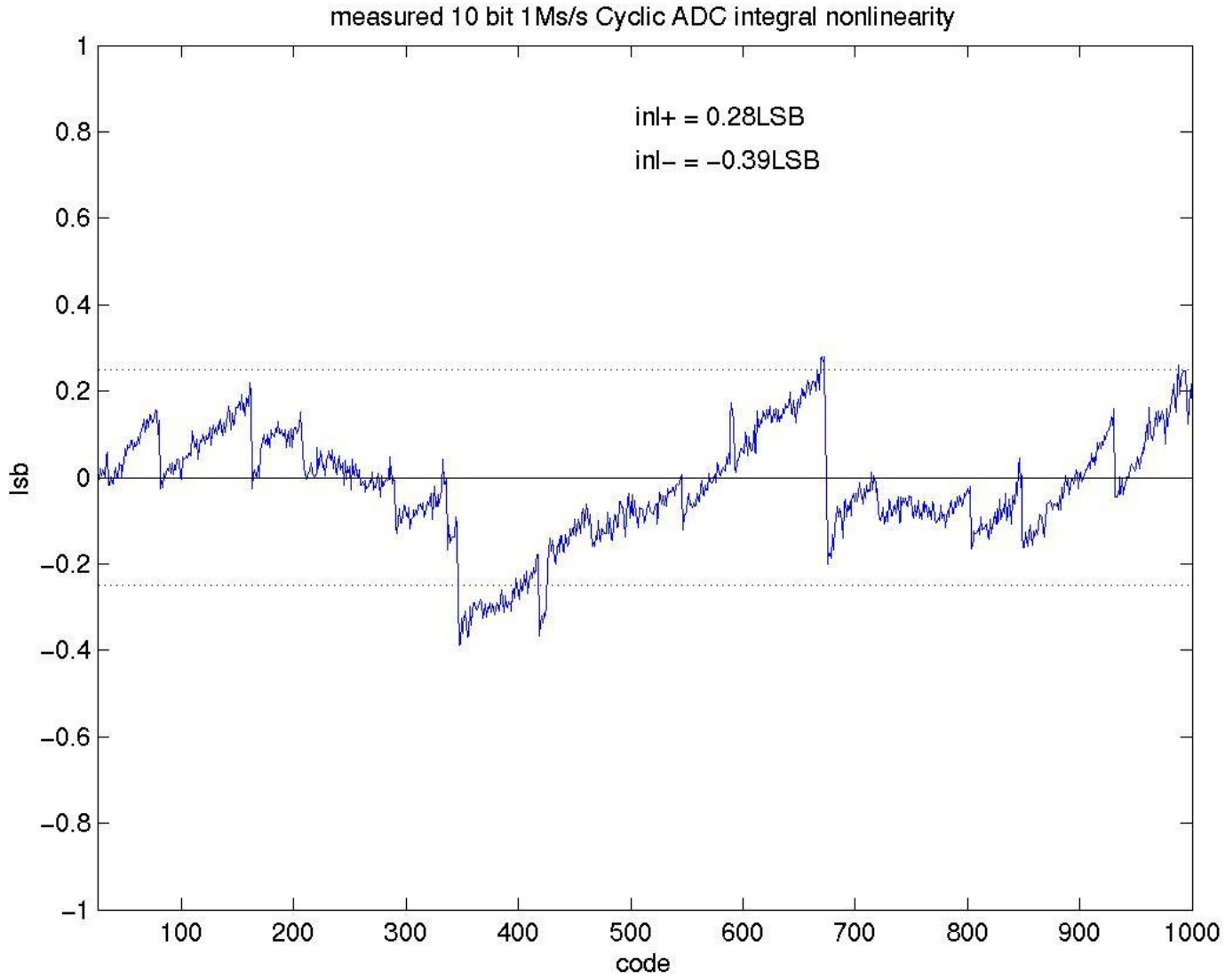


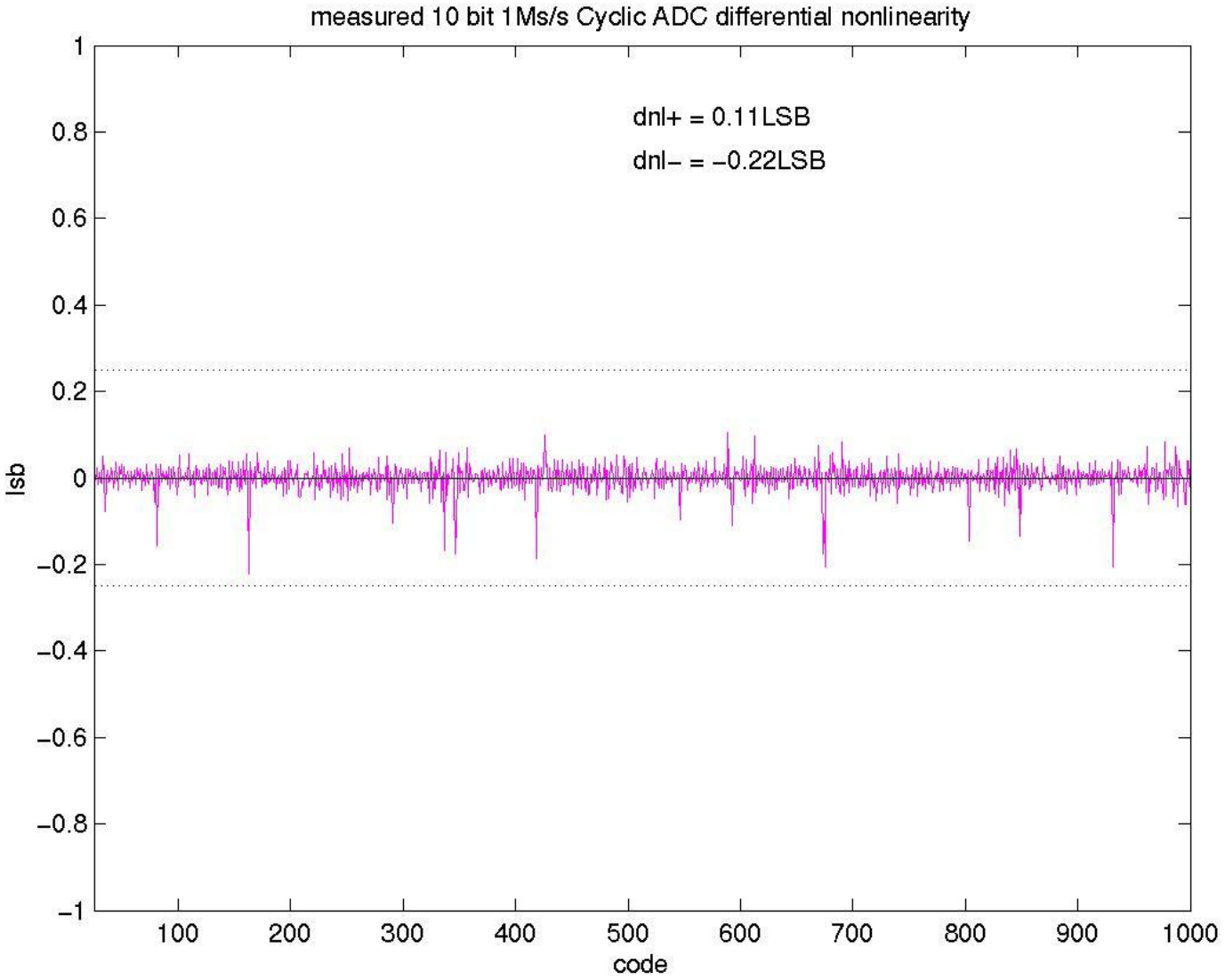
recent example:

- **10 bit, 1Ms/s, TSMC 0.18mm**
- **1.38mW from 3V, 0.085mm^2**
- **measured performance on upcoming slides**

D. Garrity, P. Rakers, US patent 6,535,157


measured output spectrum for a 10 bit 1 Ms/s Cyclic ADC
8192 POINT FFT
FSAMPLE = 1.1MSPS
FIN = 101.9kHz
SNR = 60.7dB
SNDR=60.5dB
THD = -69.8dB
SFDR = 74.8dB
dBFS
Frequency (kHz)
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
0
50
100
150
200
250
300
350
400
450
500
550


measured 10 bit 1Ms/s Cyclic ADC integral nonlinearity
inl+ = 0.28LSB
inl− = −0.39LSB
lsb
code
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
100
200
300
400
500
600
700
800
900
1000


measured 10 bit 1Ms/s Cyclic ADC differential nonlinearity
dnl+ = 0.11LSB
dnl− = −0.22LSB
lsb
code
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
100
200
300
400
500
600
700
800
900
1000

Measured Results:

Technology	**0.18μm (TSMC)CMOS, MiM CAP**
Supply Voltage	**2.7 V**
Active Area	**0.085 mm^2**
Power Consumption	**1.3 mW at 1MHz Fsamp**

input bandwidth	**500kHz**
SINAD	**60dB**
ENOB	**9.76**
INL/DNL	**+/- 0.39 lsb, +/- 0.22 lsb**

Conclusions:

- **For bandwidths up to 10MHz or 20MHz and dynamic ranges of greater than 70dB, ΣΔ based ADCs are the most promising**
- **Continuous-time ΣΔ ADCs are especially promising for the higher end of the ΣΔ bandwidth range.**
- **For bandwidths greater than several 10's of MHz and resolutions up to 12 bits or so, pipelined ADCs are a good choice for low power and low cost.**

- **Improvements in dynamic range/power/bandwidth come about mainly from ADC architectural breakthroughs and secondarily from IC process advances.**

Suggested Reading & Bibliography

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R. T. Baird, T.S. Fiez, “Improved $\Delta\Sigma$ DAC Linearity using Data Weighted Averaging,” Proceedings of the IEEE International Symposium on Circuits and Systems, May, 1995.

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R. W. Adams, T. W. Kwan, “Data-directed Scrambler for Multi-Bit Noise Shaping D/A Converters,” U.S. Patent No. 5,404,142, April 4, 1995.

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K. Vleugels, S. Rabii, and B. Wooley, “A 2.5V Sigma-Delta Modulator for Broadband Communications Applications,” IEEE Journal of Solid-State Circuits, vol. 36, No. 12, pp. 1887-1899, Dec. 2001.

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