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ANALYSIS OF VARIOUS PULSE WIDTH MODULATIONS (PWM) FOR MULTI-LEVEL INVERTER WITH REVERSING VOLTAGE TOPOLOGY

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ABSTRACT

Multi-level inverter technology is used to obtain a high output power from medium voltage sources like batteries and solar panel. Reduced harmonic distortion in the output voltage and lower EMI (Electro Magnetic Interference) are the main advantages of multi-level inverter. However, there are some disadvantages such as increased number of components as level is increased, complicated PWM control method and voltage balancing problem at neutral point. Reversing voltage topology overcomes the disadvantages of the conventional multi-level inverter. The new topology uses reduced quantity of total switches at higher levels which leads to the reduction in switching losses, lesser carrier signals for PWM control, improves power quality and reduces the harmonics at the output voltage. The new converter topology is implemented for 5-level and 9-level using Sinusoidal Pulse Width Modulation (SPWM) techniques. Phase disposition SPWM, Phase opposition disposition SPWM, Alternate phase opposition disposition SPWM and Variable frequency SPWM techniques are applied to generate the gate pulses for the switches in the 9-level inverter and the THD (%) is compared. The simulation results are presented and discussed.

Keywords: reversing voltage multilevel inverter, sinusoidal pulse width modulation (SPWM), phase disposition sinusoidal pulse width modulation (PDSPWM),Phase opposition disposition Sinusoidal pulse width modulation (PODSPWM), alternate phase disposition sinusoidal pulse width modulation (APDSPWM), variable frequency sinusoidal pulse width modulation (VFSPWM), total harmonic distortion (THD).

1. INTRODUCTION

The conventional voltage source inverter (VSI) generates a two level output voltage with levels +/ -V_{dc}/2 and zero, where V_{dc} is the dc link voltage. The various PWM strategies [1] are applied to high frequency switches to obtain the quality output voltage or current waveform with reduced ripple content. In high-power medium-voltage applications, the VSI have limitations such as switching losses at high frequency and voltage/power ratings.

The multilevel inverter consists of power semiconductors and capacitors voltage sources. The output voltage of the inverter will be stepped waveform which will be nearly equal to sinusoidal waveform. The higher voltage steps leads to reduced dv/dt stress on the load, lesser harmonic content and higher power quality waveforms [2]. The multilevel inverter requires large number of semiconductor switches which leads to complexity in the pulse generation, driver circuit and mechanical layout. The individual voltage sources or series capacitors produce a voltage balance problem. However, to solve the voltage balancing problem, another multilevel converter is required [3] [4].

The commonly used multilevel inverters are diode clamped, flying capacitor and cascaded H-bridge inverters [5]. In the diode clamped multilevel inverter, the diodes are switched to get the different voltage level. Therefore, it requires large number of diodes. In the flying capacitor multilevel inverter, the capacitors are charged and the capacitor voltages can be added or subtracted to obtain the required levels of the output voltage. Therefore, it requires more number of capacitors. In cascaded H-bridge inverters components like diodes and capacitors are not used. The H-bridge inverter requires minimal number of devices at the cost of higher number of dc-power supplies.

The Reversing Voltage topology uses less number of switches at higher levels as compared to available inverters. This topology requires less carrier signals and does not need balancing of the voltage [6] [7].

The new topology [6] [7] is implemented for 5-level and 9-level with PWM techniques. The first section describes the reversing voltage topology schematic. The pulses are generated by Phase disposition SPWM, Phase opposition disposition SPWM, Alternate phase opposition disposition SPWM and Variable frequency SPWM techniques for 9-level inverter. The final section shows the simulation results.

2. REVERSING VOLTAGE TOPOLOGY

The reversing voltage multilevel inverter has two parts i.e. level generator and polarity generator (Full bridge converter). The level generator produces the positive sign stepped waveform. The polarity of the generated stepped waveform can be altered using the polarity generator which is a full bridge converter. Thepolarity generator produces the positive and negative half stepped waveform. The level generator requires high frequency switches and polarity generator uses low frequency switches. The inverter uses both high and low frequency switches to reduce the voltage stress on the power devices.

A. Operation of five-level inverter using reversing voltage topology

The schematic of single-phase five level inverter is shown in the fig. The inverter consists of 2 DC sources and 8 switches. The switches S_1, S_2, S_3 and S_4 are level generator

switches. By switching the above switches in sequence the stepped waveform is generated. The full bridge switches S_6, S_7, S_8 and S_9 are used as a polarity generator. The positive and negative polarity of the output voltage is obtained by triggering these switches in sequence.

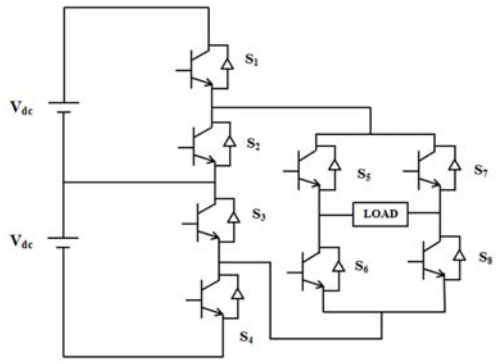

Figure-1. Schematic of single-phase five level inverter.

The switching modes to get the different voltage steps is

- When S_1 and S_4 is turned ON, the voltage level $2V_{dc}$ is generated at the output
- When S_1 and S_3 is turned ON, the voltage level V_{dc} is generated at the output
- When S_2 and S_3 is turned ON, the voltage level zero is generated at the output

The switching modes to get the positive and negative polarity is

- When S_5 and S_8 is turned ON, the positive half cycle of the output waveform is generated
- When S_7 and S_6 is turned ON, the negative half cycle of the output waveform is generated

Table-1. Switching states for reversing voltage nine level inverter.

Output voltage	S_1	S_2	S_3	S_4
0	0	1	1	0
V_{dc}	0	1	0	1
$2V_{dc}$	1	0	0	1

B. Operation of nine-level inverter using reversing voltage topology

The schematic of single-phase nine level inverter is shown in the fig. The nine-level inverter requires 12 switches and 4 DC sources to generate the output waveform. It is sufficient to produce pulses only for positive half cycles of the output voltage. The negative half cycle is automatically generated by switching the full bridge converter. It requires less high frequency switches. Therefore, the semiconductor switches are reduced when compared to the conventional multilevel inverter.

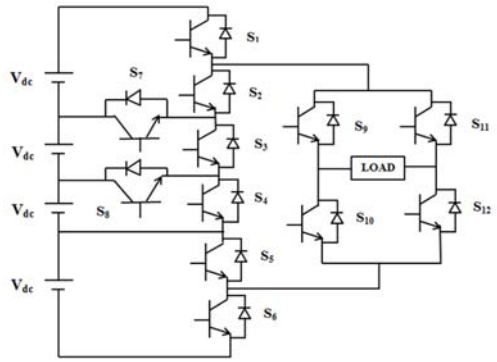

Figure-2. Schematic of single-phase nine level inverter.

The switching modes to get the different voltage steps are

- When S_1 and S_6 is turned ON, the voltage level $4V_{dc}$ is generated at the output
- When S_2, S_7 and S_6 is turned ON, the voltage level $3V_{dc}$ is generated at the output
- When S_2, S_3, S_8 and S_6 is turned ON, the voltage level $2V_{dc}$ is generated at the output
- When S_2, S_3, S_4 and S_6 is turned ON, the voltage level V_{dc} is generated at the output
- When S_2, S_3, S_4 and S_5 is turned ON, the voltage level zero is generated at the output

By switching S_1, S_2, S_3, S_4, S_5, S_6, S_7 and S_8 the nine-level stepped waveform is obtained. The Full bridge converter consists of four switches S_9, S_{10}, S_{11} and S_{12}.

- When S_9 and S_{12} is turned ON, the positive half cycle of the output waveform is generated
- When S_{10} and S_{11} is turned ON, the negative half cycle of the output waveform is generated

Table-2. Switching states for reversing voltage nine level inverter.

DC Voltage level	Switching operation
0	2, 3, 4, 5
V_{dc}	2, 3, 4, 6
$2V_{dc}$	2, 3, 6, 8
$3V_{dc}$	2, 7, 6
$4V_{dc}$	1, 6

3. SIMULATION RESULTS

In this section, the simulation results for nine-level inverter using Reversing Voltage topology are demonstrated by MATLAB R2009a software module. The design parameters for single phase nine-level inverter is:

- Each dc source voltage is 100 V and total voltage is 400 V
- Frequency of carrier signal is 5 KHz
- Full bridge converter switches are switched at 50 Hz
- Load R = 100 Ω

In conventional inverter, N-1 number of carriers is used, where N is the number of voltage levels. So, eight carrier waveforms are required to design a nine level. However, nine-level inverter using the new topology will require (N-1)/2 carriers, i.e. only fourcarriers. The four carrier waveforms are compared with the positive half cycle of the sinusoidal waveform to generate the required gate pulses. This topology requires only half the carriers when compared to the traditional multilevel inverter. It require simpler controller as the generation of the control signals are easy.

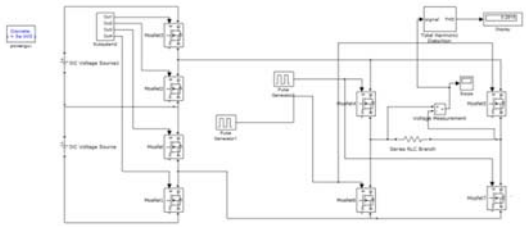

Figure-3. Circuit diagram of single-phase five level inverter.

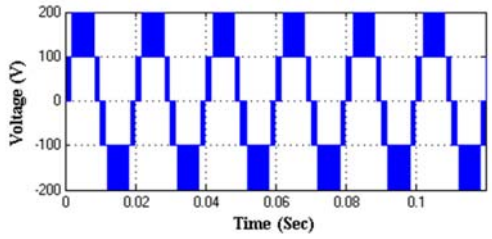

Figure-4. Output voltage waveform of single-phase five level inverter.

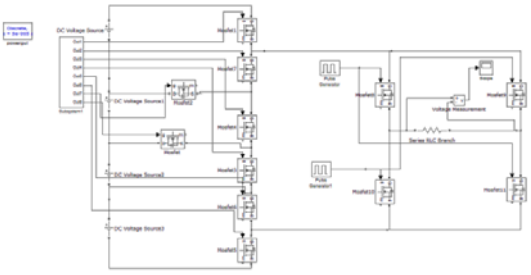

Figure-5. Circuit diagram of single-phase Nine level inverter.

A. Phase disposition SPWM

In this technique, each carrier waveform will be in phase with each other. The carrier waveforms are compared with the positive cycle of the sinusoidal waveform whenever the sinusoidal waveform intersects the carrier signal a pulse is generated. The four pulses are generated. The remaining pulses are produced by connecting NOT operator to the obtained four pulses. The eight gate pulses are given to the level generator switches

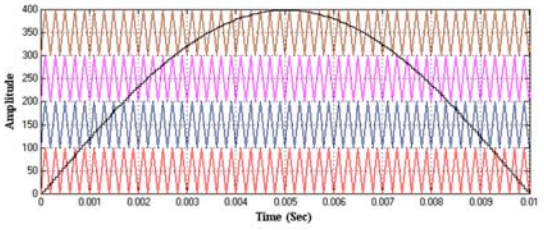

Figure-6. Phase disposition SPWM modulation waveform.

The pulses to the full generator switches are given from the pulse generator. The output voltage will have nine levels.

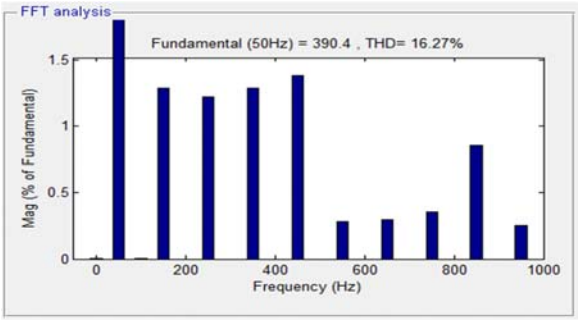

Figure-7. FFT Plot for output voltage PDSPWM.

The FFT plot is shown in Figure-7. The THD (%) of the output voltage is 16.27% when Phase disposition SPWM is implemented to the level generator switches.

B. Phase opposition disposition SPWM

In this technique, all carrier waveforms above reference will be in phase and 180 degree out of phase with those below reference. The FFT analysis for the output voltage is taken.

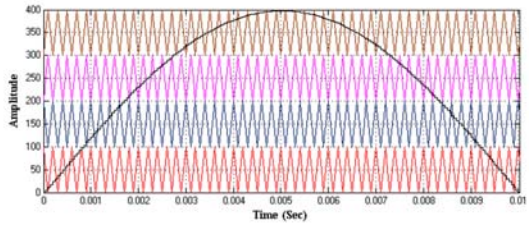

Figure-8. Phase opposition disposition SPWM modulation waveform.

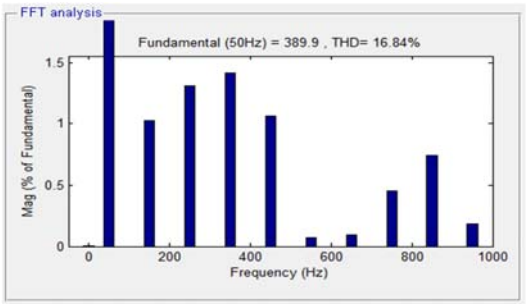

Figure-9. FFT Plot for output voltage PODSPWM.

The FFT plot is shown in fig. The THD (%) of the output voltage is 16.84% when Phase opposition disposition SPWM is implemented to the level generator switches.

A. Alternate phase opposition disposition SPWM

In this technique, each carrier waveform will be in out of phase with its neighbour carrier by 180 degree. The FFT analysis for the output voltage is taken.

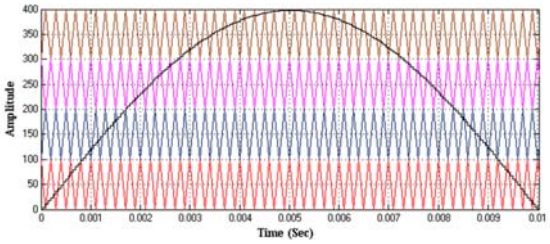

Figure-10. Alternate phase opposition disposition SPWM modulation waveform.

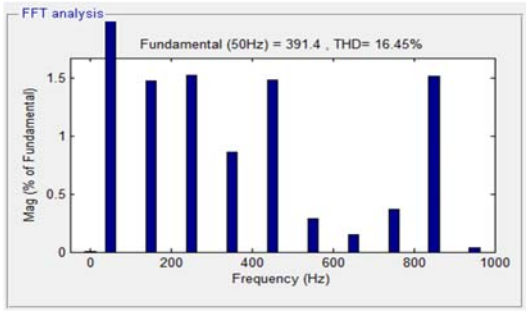

Figure-11. FFT Plot for output voltage APODSPWM.

The FFT plot is shown in fig. The THD (%) of the output voltage is 16.45% when Alternate phase opposition disposition SPWM is implemented to the level generator switches.

B. Variable frequency SPWM

in this technique, the time duration of the one or more waveforms will vary.

- Frequency of first carrier waveform is 2 KHz
- Frequency of second carrier waveform is 4 KHz
- Frequency of third and fourth carrier waveforms is 10 KHz

The frequency of the carrier signal will differ from each other. The pulses are generated when the positive sinusoidal waveform coincides with the carrier waveform. The obtained pulses and the pulses from the NOT operator are given to the level generator switches. The FFT analysis for the output voltage is taken.

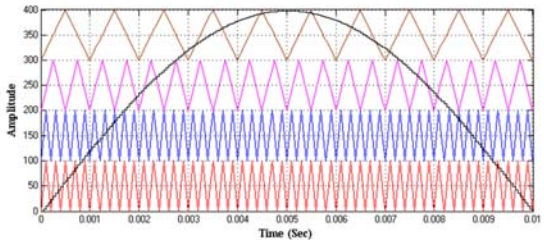

Figure-12. Variable frequency SPWM modulation waveform.

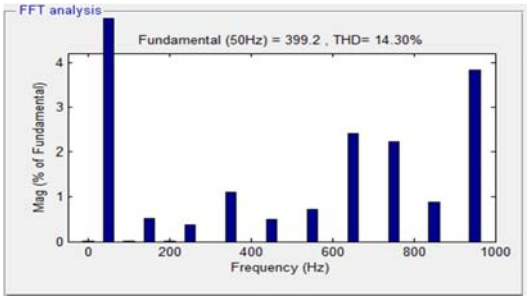

Figure-13. FFT Plot for output voltage VFSPWM.

The FFT plot is shown in fig. The THD (%) of the output voltage is 14.30% when Variable frequency SPWM is implemented to the level generator switches.

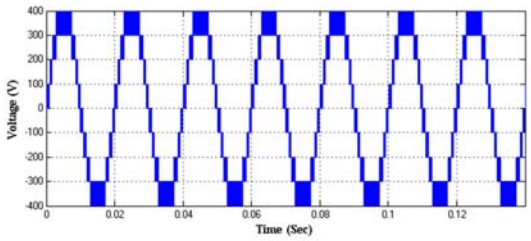

Figure-14. Output voltage waveform of single-phase five level inverter.

The output voltage waveform of the inverter for every PWM technique will be same. The THD in % is tabulated in the table. When compared to the other PWM techniques, the variable frequency PWM technique will give less THD (%) when compared to the other techniques.

Table-3. THD values for different PWM techniques.

Different types of PWM for 9-level inverter	THD (%)
Phase disposition PWM	16.27
Phase opposition disposition PWM	16.84
Alternate phase opposition disposition PWM	16.45
Variable Frequency PWM	14.30

CONCLUSIONS

In this project, Reversing Voltage is applied to improve multilevel performance with the aid of compensating the disadvantages in conventional multilevel inverters. This strategy improves output voltage, reduces utilizing a number of semiconductor switches and voltage imbalance. This project makes use of carrier based SPWM scheme using Phase Disposition, Phase opposition disposition, Alternate phase opposition disposition and variable frequency process and would manage output voltage and frequency and minimize the harmonic. A single phase 5-level and 9-level inverter with reversing voltage strategy is developed. The above mentioned SPWM techniques are applied to the 9-level inverter and observed the harmonic content. The variable frequency SPWM technique gives the less THD value 14.30% when compared to the other SPWM techniques.

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